
# PSMNR67-30YLE

## N-channel 30 V, 0.70 mOhm, ASFET for hotswap with enhanced SOA in LFPAK56E

10 November 2022 Product data sheet

## 1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LFPAK56E package optimized for low $R_{DSon}$ and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low $R_{DSon}$ / low $I^2R$ conduction losses
- LFPAK56E package for applications that demand the highest performance and reliability in a 30 $mm^2$ footprint
- Low leakage <1 µA at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C

## 3. Applications

- Hot swap in 12 V-20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

## 4. Quick reference data

**Table 1. Quick reference data**

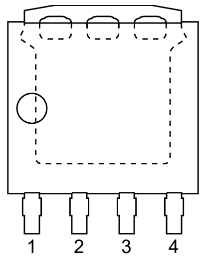
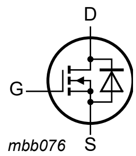
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 30 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 365 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 333 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.64 | 0.7 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.75 | 1 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 2 | 13 | 26 | nC |
| $Q_{G(tot)}$ | total gate charge | | | 23 | 52 | 86 | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | | |
| S | softness factor | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.94 | - | |

[1] 365 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

# 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |   **LFPAK56E; Power-SO8 (SOT1023)** |   |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMNR67-30YLE | LFPAK56E; Power-SO8 | plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch | SOT1023 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMNR67-30YLE | E67L30J |

# 8. Limiting values

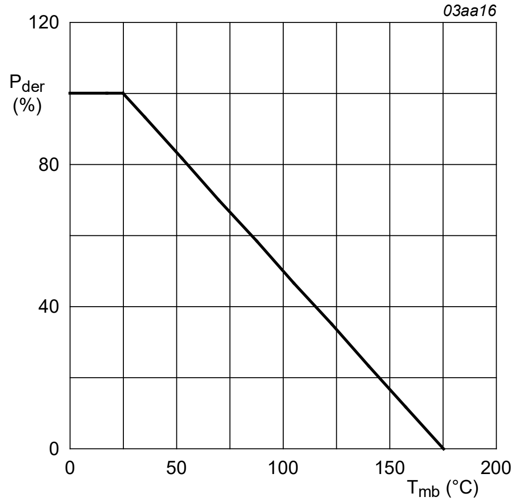
**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 333 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 365 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 361 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 2070 | A |

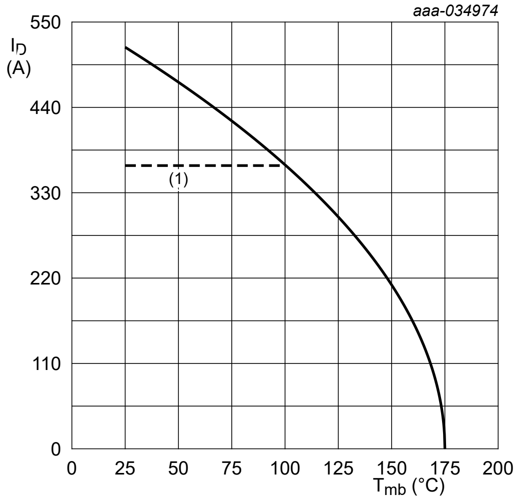
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 333 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 2070 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 25 A; $V_{sup}$ ≤ 30 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 10 ms | [2] | - | 4.9 | J |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ ≤ 30 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [2] | - | 190 | A |

[1] 365 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test.



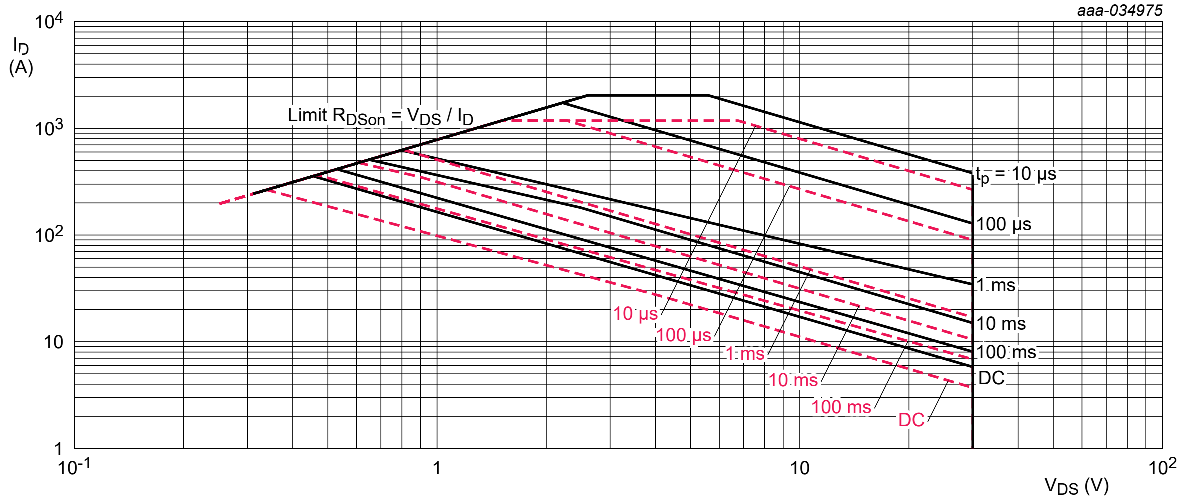

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




$V_{GS}$ ≥ 10 V
(1) 365 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C (solid black line); $T_{mb}$ = 125 °C (red dashed line); $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | | - | 0.34 | 0.45 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | | - | 42 | - | K/W |
| | | Fig. 6 | | - | 85 | - | K/W |

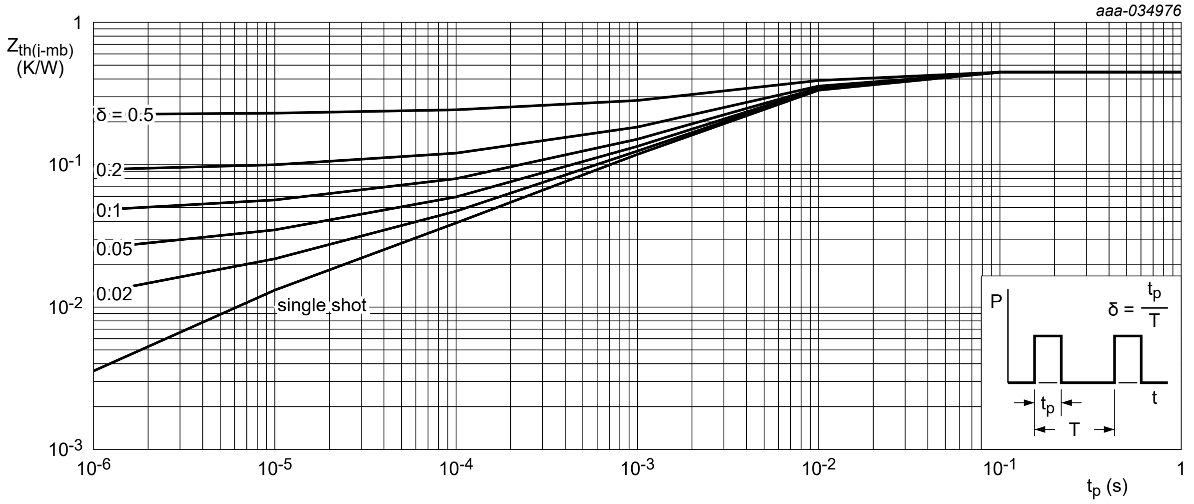
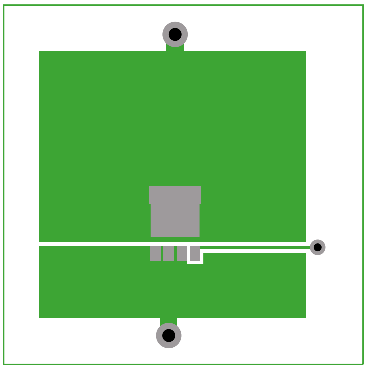


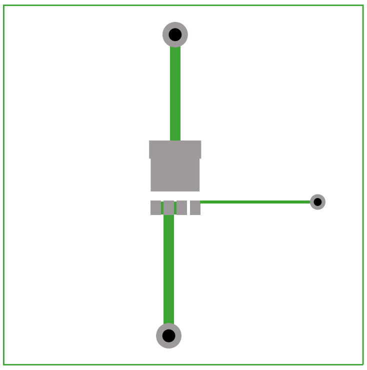

**Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**



aaa-027933

Copper area 25.4 mm square; 70 µm thick on FR4 board

**Fig. 5. PCB layout for thermal resistance from junction to ambient**



aaa-027935

70 µm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

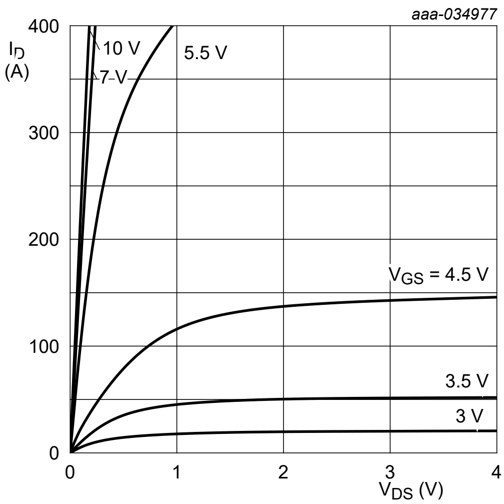
## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 30 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 2 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C | | 1.2 | 1.79 | 2.2 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -3.9 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 24 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 24 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 10 | - | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.64 | 0.7 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 1.3 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 10 | | - | 0.75 | 1 | mΩ |
| | | $V_{GS}$ = 7 V; $I_D$ = 25 A; $T_j$ = 150 °C; Fig. 11 | | - | - | 1.9 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | 1.4 | 3.6 | 9 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 23 | 52 | 86 | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 50 | 112 | 185 | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C | | - | 60 | - | nC |

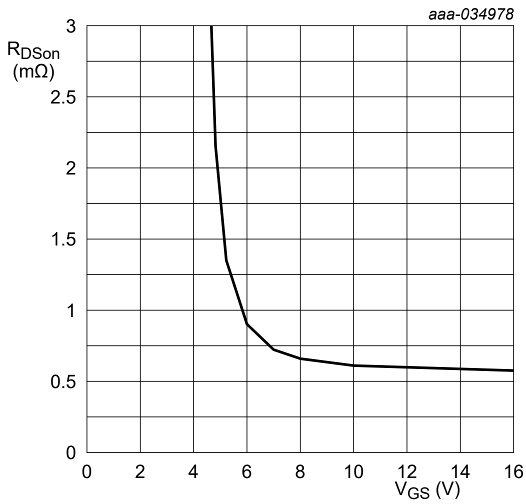
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 6.5 | 24 | 46 | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | 3.5 | 13 | 25 | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | 3 | 11 | 21 | nC |
| $Q_{GD}$ | gate-drain charge | | | 2 | 13 | 26 | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | - | 3.1 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 15 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 14 | | 4967 | 8278 | 12417 | pF |
| $C_{oss}$ | output capacitance | | | 1542 | 2570 | 3855 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | 117 | 435 | 1044 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 15 V; $R_L$ = 0.6 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 64 | - | ns |
| $t_r$ | rise time | | | - | 124 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 52 | - | ns |
| $t_f$ | fall time | | | - | 59 | - | ns |
| $Q_{oss}$ | output charge | $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; f = 1 MHz; $T_j$ = 25 °C | | - | 62 | - | nC |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 15 | | - | 0.77 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 15 V; $T_j$ = 25 °C; Fig. 16 | | - | 42 | - | ns |
| $Q_r$ | recovered charge | | [1] | - | 42 | - | nC |
| $t_a$ | reverse recovery rise time | | | - | 21.5 | - | ns |
| $t_b$ | reverse recovery fall time | | | - | 20.3 | - | ns |
| S | softness factor | | | - | 0.94 | - | |

[1] includes capacitive recovery




$T_j$ = 25 °C

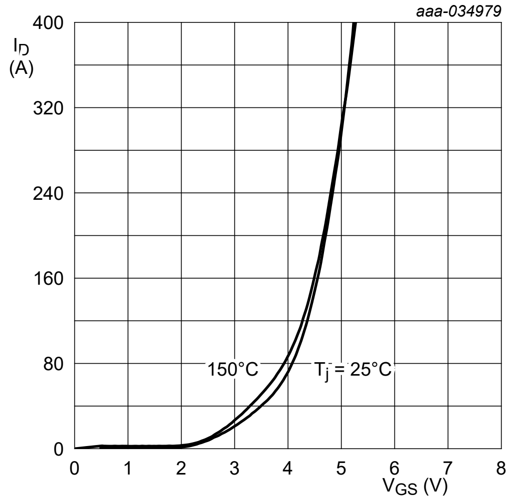
**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**




$T_j$ = 25 °C; $I_D$ = 25 A

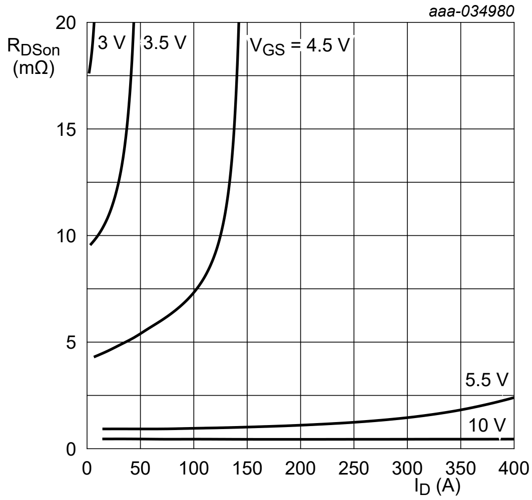
**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**



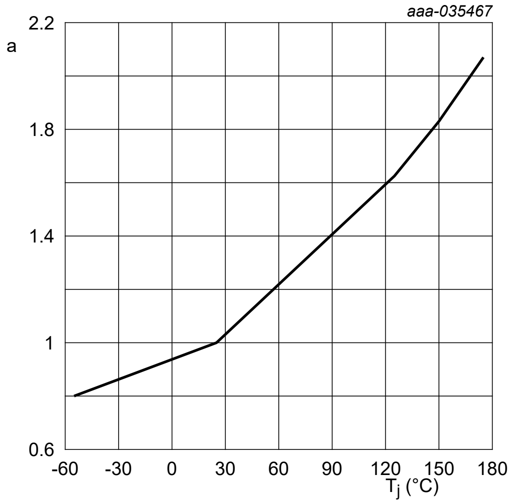

$V_{DS}$ = 8 V

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



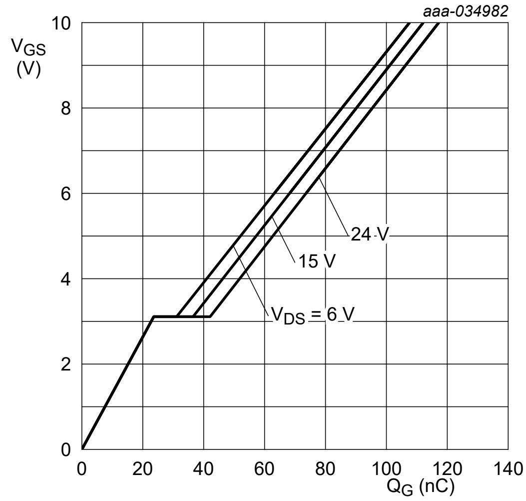

$T_j$ = 25 °C

**Fig. 10. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 12. Gate-source voltage as a function of gate charge; typical values**

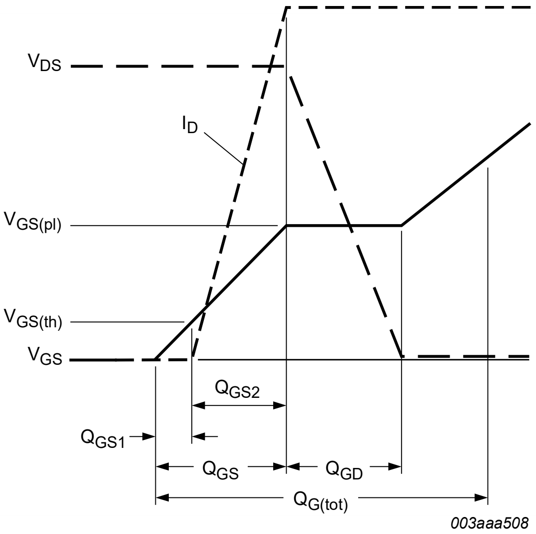
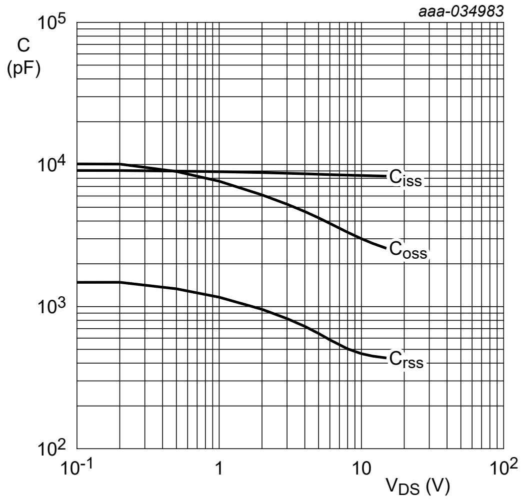
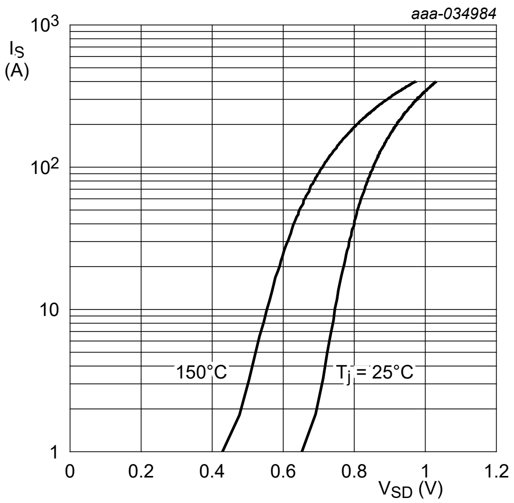



Fig. 13. Gate charge waveform definitions




$V_{GS}$ = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values




$V_{GS}$ = 0 V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

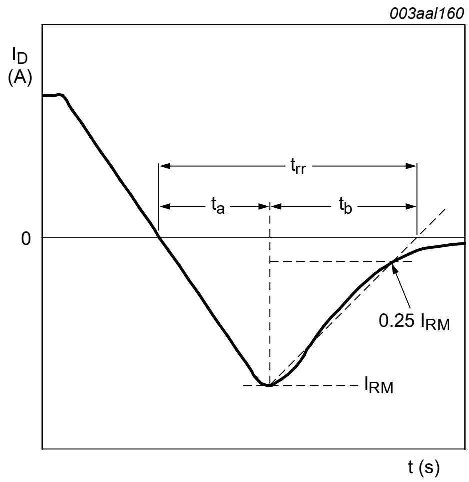
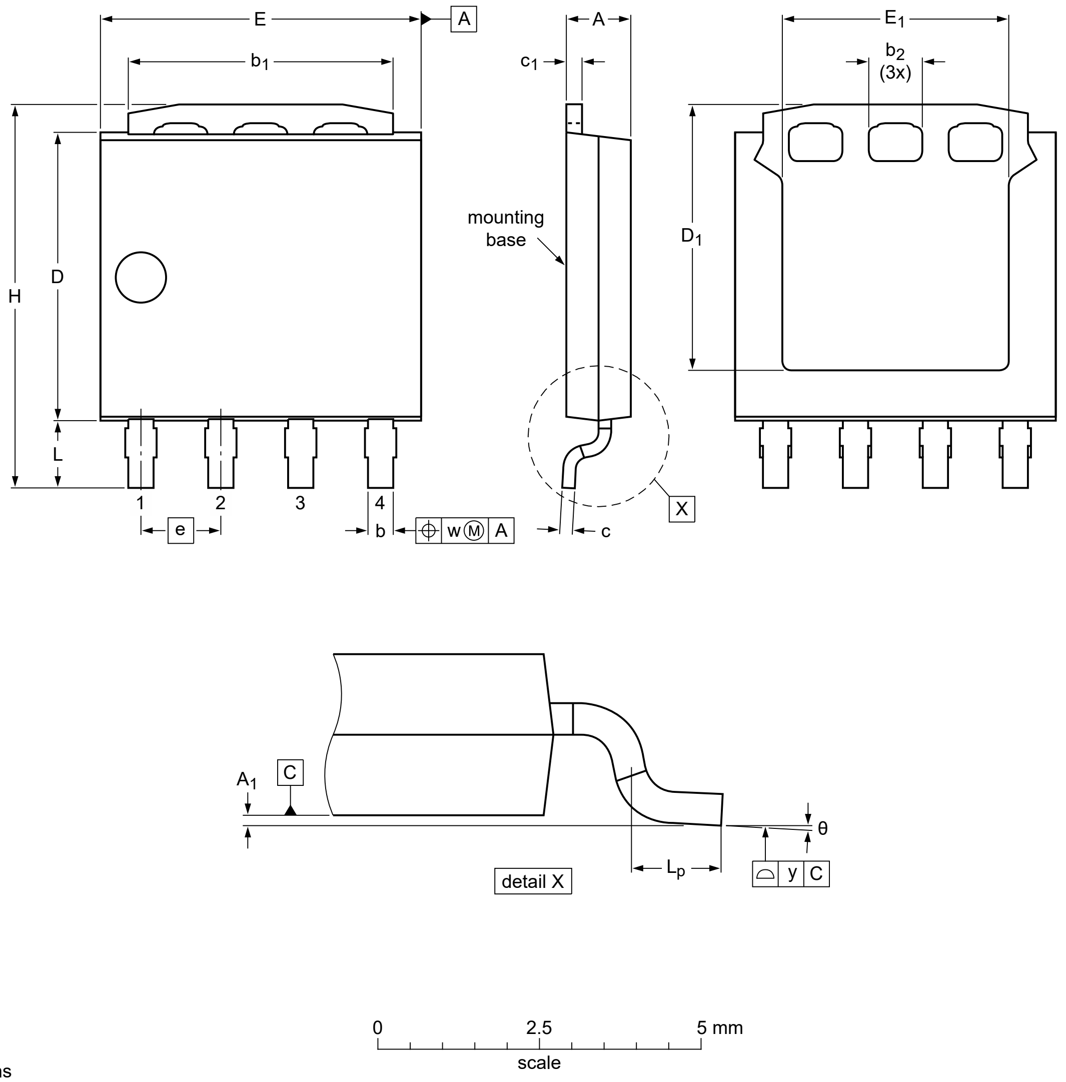



Fig. 16. Reverse recovery timing definition

## 11. Package outline

**Plastic single-ended surface-mounted package (LFPAK56E); 4 leads** **SOT1023**




Dimensions

| Unit | | A | A1 | b | b1 | b2 | c | c1 | D(1) | D1(1) | E(1) | E1(1) | e | H | L | Lp | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.10 | 0.15 | 0.50 | 4.41 | | 0.25 | 0.30 | 4.70 | 4.45 | 5.30 | 3.7 | | 6.2 | 1.3 | 0.85 | | | 8° |
| | nom | | | | | 0.85 | | | | | | | 1.27 | | | | 0.25 | 0.1 | |
| | min | 0.95 | 0.00 | 0.35 | 3.62 | | 0.19 | 0.24 | 4.45 | | 4.95 | 3.5 | | 5.9 | 0.8 | 0.40 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

*sot1023_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1023 | | | | | | ~~13-03-05~~ 17-07-31 |

**Fig. 17. Package outline LFPAK56E; Power-SO8 (SOT1023)**

## 12. Soldering

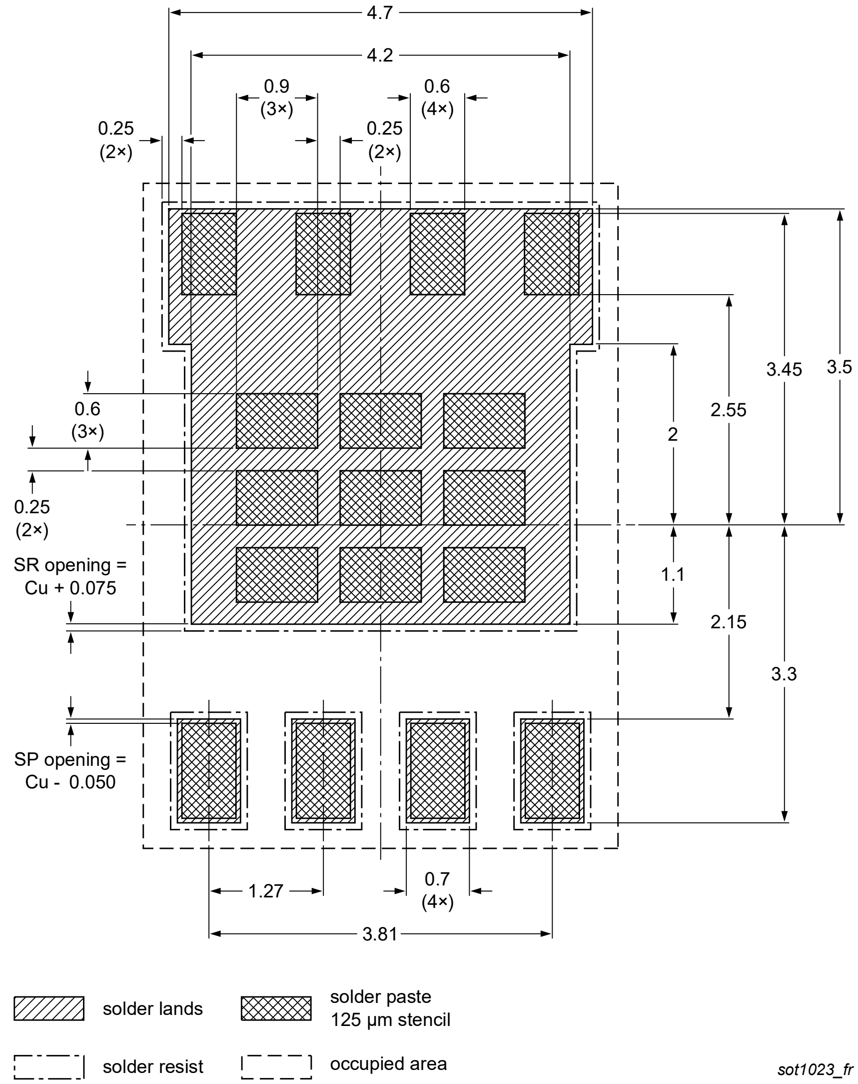



**Fig. 18. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)**

# 13. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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