

MOSFET – P-Channel, POWER TRENCH® -150 V, -13 A, 107 mΩ

FDMC86259P

General Description

This P-Channel MOSFET is produced using onsemi's advanced POWER TRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

- Max $r_{DS(on)}$ = 107 mΩ at $V_{GS} = -10$ V, $I_D = -3$ A
- Max $r_{DS(on)}$ = 137 mΩ at $V_{GS} = -6$ V, $I_D = -2.7$ A
- Very Low RDS-on Mid Voltage P Channel Silicon Technology Optimized for Low Qg
- This Product is Optimised for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant

Applications

- Active Clamp Switch
- Load Switch

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

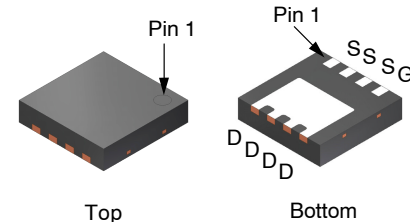
Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			-150	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	-13	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	-3.2	
		Pulsed		-20	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			181	mJ
P_D	Power Dissipation		$T_C = 25^\circ\text{C}$	62	W
	Power Dissipation (Note 1a)		$T_A = 25^\circ\text{C}$	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-150 V	107 mΩ @ -10 V	-13 A
	137 mΩ @ -6 V	



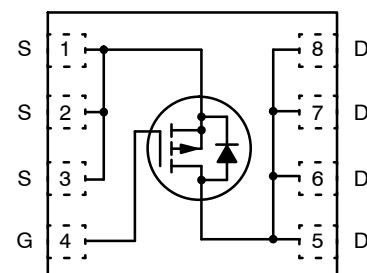
PQFN8 3.3x3.3, 0.65P
CASE 483AW
Power 33

MARKING DIAGRAM

\$Y&Z&3&K
FDMC
86259P

\$Y = Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot Code
FDMC86259P = Specific Device Code

PIN ASSIGNMENT



P-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C	-	-88	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -120\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	-2	-2.8	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C	-	6	-	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}$, $I_D = -3\ \text{A}$	-	87	107	m Ω
		$V_{GS} = -6\ \text{V}$, $I_D = -2.7\ \text{A}$	-	99	137	
		$V_{GS} = -10\ \text{V}$, $I_D = -3\ \text{A}$, $T_J = 125^\circ\text{C}$	-	145	178	
g_{FS}	Forward Transconductance	$V_{DS} = -10\ \text{V}$, $I_D = -3\ \text{A}$	-	12	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -75\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	-	1535	2045	pF
C_{oss}	Output Capacitance		-	125	170	pF
C_{rss}	Reverse Transfer Capacitance		-	6	10	pF
R_g	Gate Resistance		0.1	1.4	3	Ω

SWITCHING CHARACTERISTICS

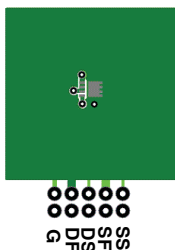
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\ \text{V}$, $I_D = -3\ \text{A}$, $V_{GS} = -10\ \text{V}$, $R_{GEN} = 6\ \Omega$	-	12	23	ns
t_r	Rise Time		-	3.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22	36	ns
t_f	Fall Time		-	9.6	20	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-10\ \text{V}$, $V_{DD} = -75\ \text{V}$, $I_D = -3\ \text{A}$	-	22	32	nC
		$V_{GS} = 0\ \text{V}$ to $-6\ \text{V}$, $V_{DD} = -75\ \text{V}$, $I_D = -3\ \text{A}$	-	14	20	
Q_{gs}	Total Gate Charge	$V_{DD} = -75\ \text{V}$, $I_D = -3\ \text{A}$	-	5.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	4.3	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = -3\ \text{A}$ (Note 2)	-	-0.80	-1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = -1.9\ \text{A}$ (Note 2)	-	-0.78	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -3\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	-	77	123	ns
Q_{rr}	Reverse Recovery Charge		-	208	333	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Starting $T_J = 25^\circ\text{C}$; P-ch: $L = 3\ \text{mH}$, $I_{AS} = -11\ \text{A}$, $V_{DD} = -150\ \text{V}$, $V_{GS} = -10\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = -34\ \text{A}$.

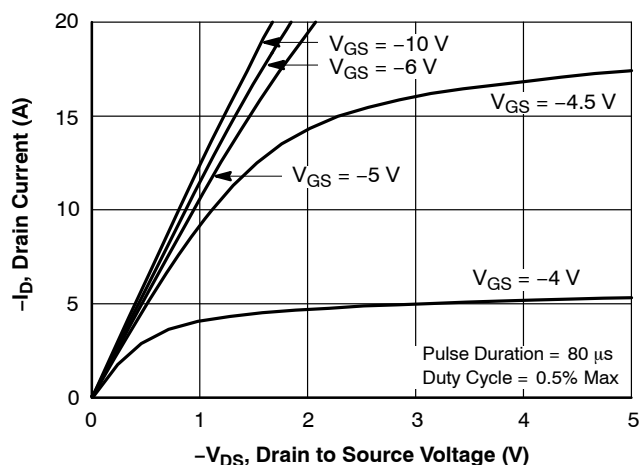
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Figure 1. On Region Characteristics

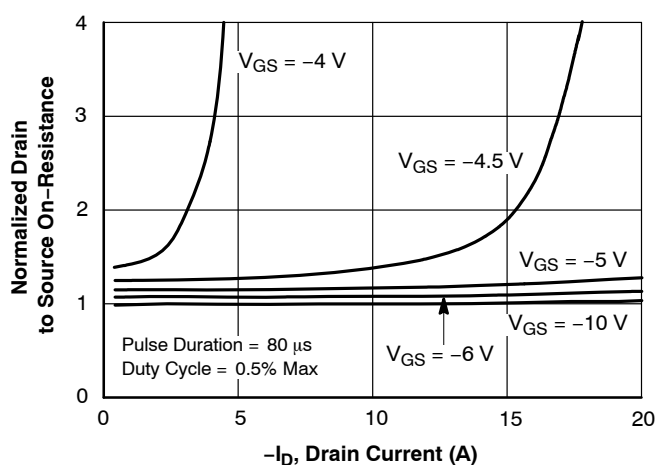


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

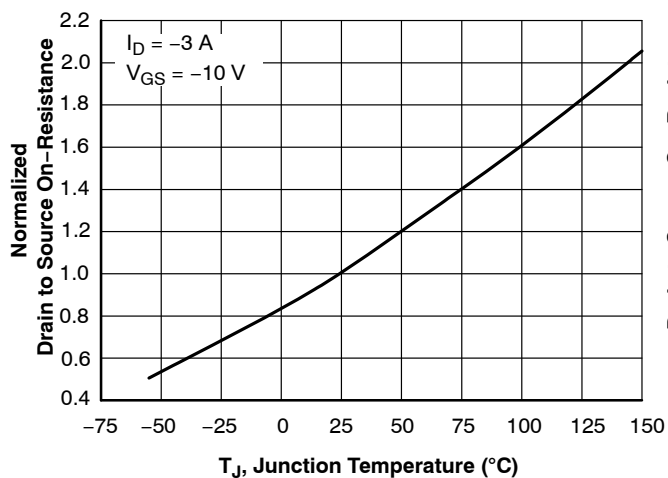


Figure 3. Normalized On Resistance vs. Junction Temperature

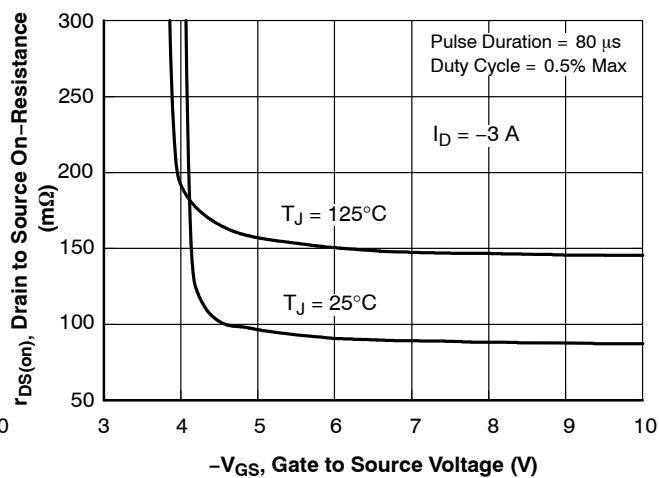


Figure 4. On-Resistance vs. Gate to Source Voltage

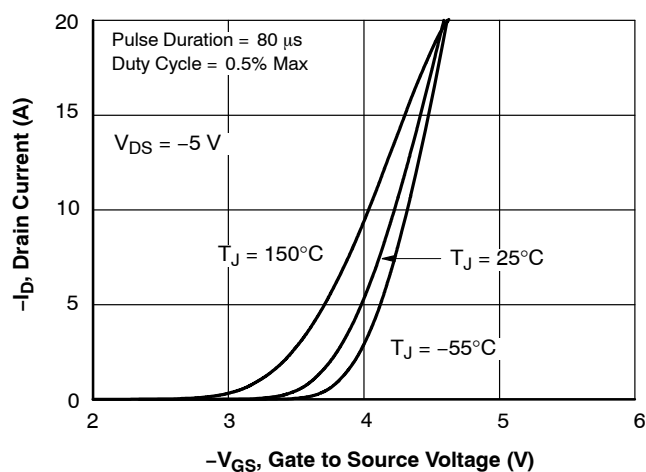


Figure 5. Transfer Characteristics

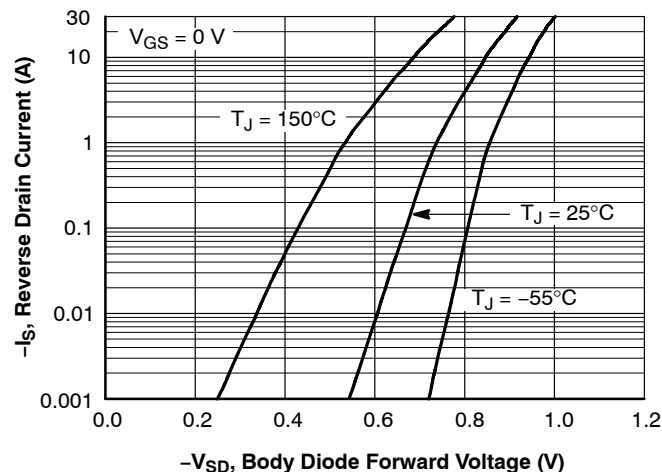


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

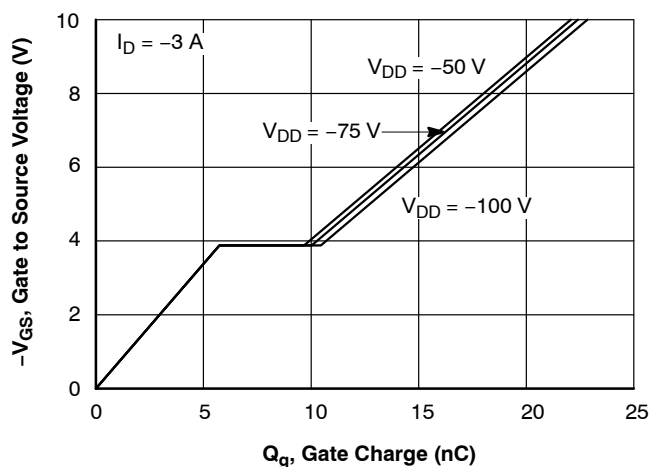
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Figure 7. Gate Charge Characteristics

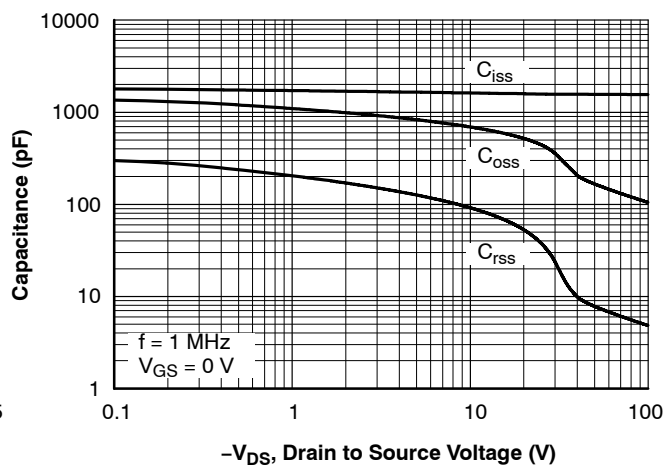


Figure 8. Capacitance vs. Drain to Source Voltage

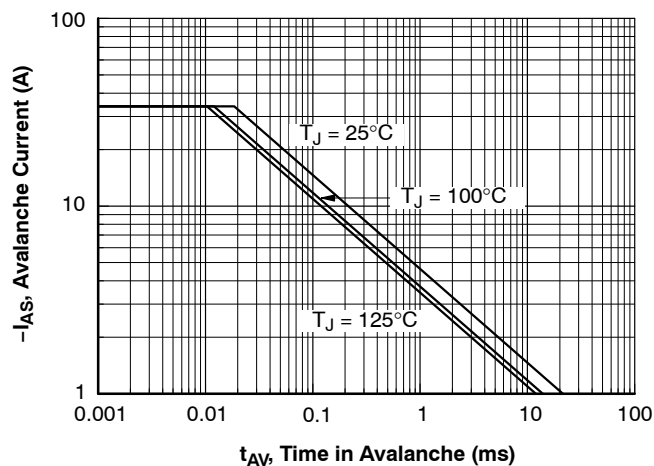


Figure 9. Unclamped Inductive Switching Capability

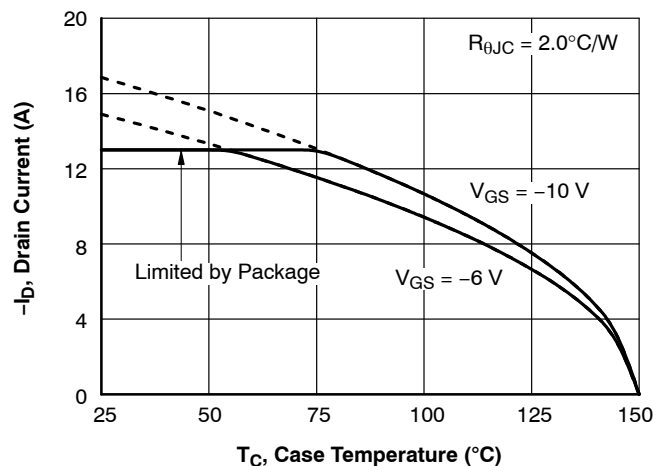


Figure 10. Maximum Continuous Drain Current vs Case Temperature

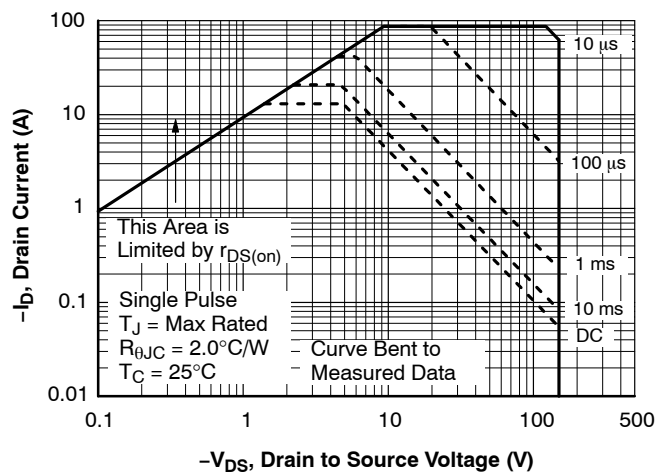


Figure 11. Forward Bias Safe Operating Area

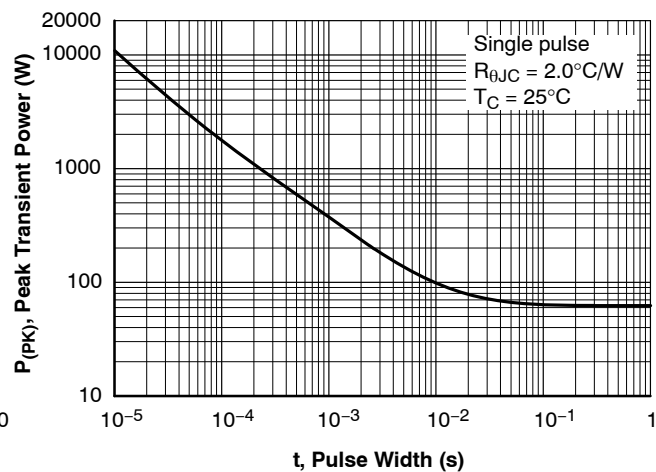


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

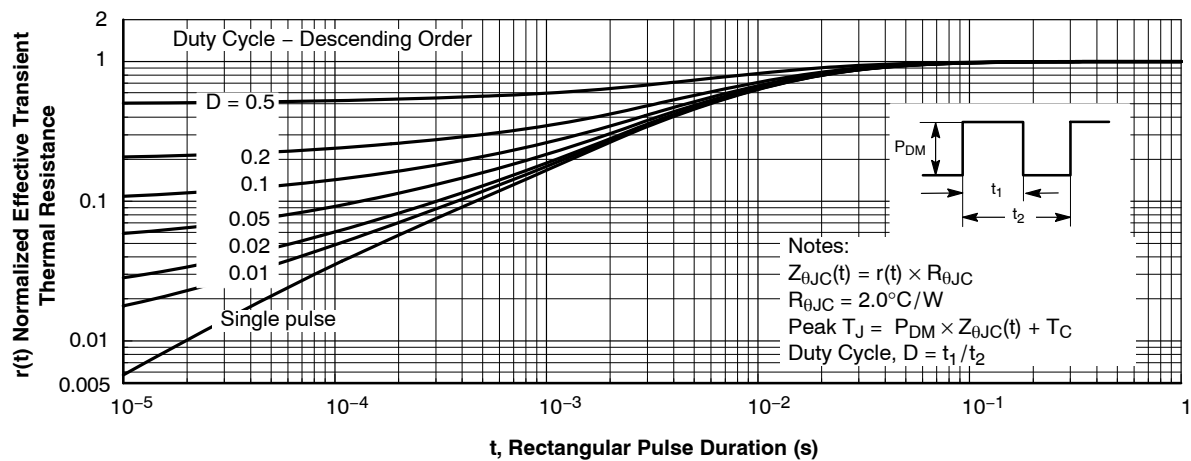
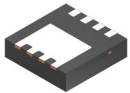


Figure 13. Junction-to-Case Transient Thermal Response Curve

ORDERING INFORMATION

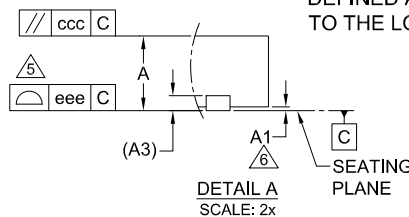
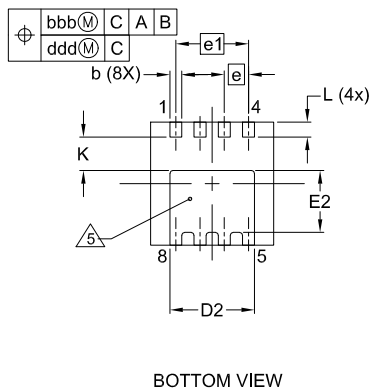
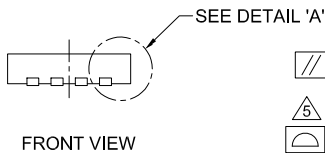
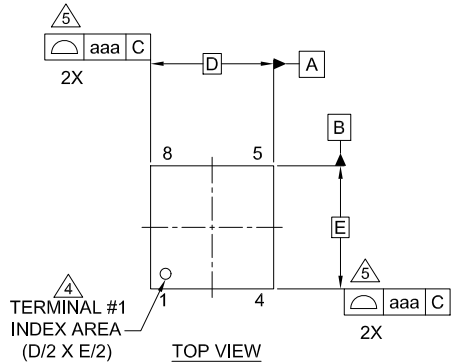
Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC86259P	FDMC86259P	PQFN8 3.3x3.3, 0.65P Power 33 (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

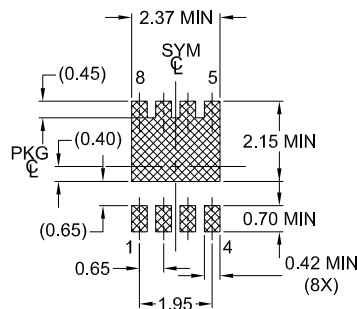


WDFN8 3.30x3.30x0.75, 0.65P
CASE 483AW
ISSUE B

DATE 22 MAR 2024



LAND PATTERN
RECOMMENDATION



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3.30x3.30x0.75, 0.65P	PAGE 1 OF 1

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