

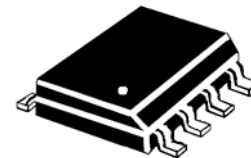
DESCRIPTION

This TRANSIENT VOLTAGE SUPPRESSOR (TVS) array is packaged in an SO-8 configuration giving protection to 2 Bidirectional data or interface lines. It is designed for use in applications where protection is required at the board level from voltage transients caused by electrostatic discharge (ESD) as defined in IEC 61000-4-2, electrical fast transients (EFT) per IEC 61000-4-4 and effects of secondary lightning. The bidirectional feature is obtained by tying pins 1 and 2 together to the protected line as well as pins 7 and 8 together to ground (or visa versa) where each of two TVS legs are in antiparallel as shown in the schematic on the second page for these pins. The same is achieved when tying pins 3 and 4 together and pins 5 and 6 together in a similar antiparallel manner for the second protected line to ground.

These TVS arrays have a peak power rating of 500 watts for an 8/20 μ sec pulse. This array is suitable for protection of sensitive circuitry consisting of TTL, CMOS DRAM's, SRAM's, HCMOS, HSIC microprocessors, **UNIVERSAL SERIAL BUS (USB)** and I/O transceivers. The USB08XXC product provides board level protection from static electricity and other induced voltage surges that can damage or upset sensitive circuitry.

IMPORTANT: For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

APPEARANCE



SO-8

FEATURES

- Protects up to 2 bidirectional lines
- Surge protection per IEC 61000-4-2, IEC 61000-4-4
- Provides electrically isolated protection
- UL 94V-0 Flamability Classification
- LOW CAPACITANCE 5 pF per line pair**
- LOW LEAKAGE**

APPLICATIONS / BENEFITS

- EIA-RS485 data rates:
5 Mbs
- 10 Base T Ethernet
- USB data rate: 900 Mbs
- Tape & Reel per EIA Standard 481
- 13 inch reel; 2,500 pieces (OPTIONAL)
- Carrier tubes; 95 pcs (STANDARD)

MAXIMUM RATINGS

- Operating Temperature: -55°C to +150°C
- Storage Temperature: -55°C to +150°C
- Peak Pulse Power: 500 watts (8/20 μ s, Figure 1)
- Pulse Repetition Rate: < .01%

MECHANICAL AND PACKAGING

- Molded SO-8 Surface Mount
- Weight 0.066 grams (approximate)
- Marking: Logo, device marking code, date code
- Pin #1 defined by dot on top of package

ELECTRICAL CHARACTERISTICS

PART NUMBER	DEVICE MARKING	STAND OFF VOLTAGE V_{WM}	BREAKDOWN VOLTAGE V_{BR} @1 mA	CLAMPING VOLTAGE V_C @ 1 Amp (Figure 2)	CLAMPING VOLTAGE V_C @ 5 Amp (Figure 2)	STANDBY CURRENT I_D @ V_{WM}	CAPACITANCE (f=1 MHz) C @0V	TEMPERATURE COEFFICIENT OF V_{BR} α_{VBR}
		VOLTS	VOLTS	VOLTS	VOLTS	μ A	pF	mV/°C
		MAX	MIN	MAX	MAX	MAX	MAX	MAX
USB0803C	3C	3.3	4	8	11	200	5	-5
USB0805C	5C	5.0	6.0	10.8	13	40	5	1
USB0812C	12C	12.0	13.3	19	26	1	5	8
USB0815C	15C	15.0	16.7	24	32	1	5	11
USB0824C	24C	24.0	26.7	43	57	1	5	28

Note: Transient Voltage Suppressor (TVS) product is normally selected based on its stand off voltage V_{WM} . Product selected voltage should be equal to or greater than the continuous peak operating voltage of the circuit to be protected.

SYMBOLS & DEFINITIONS

Symbol	Definition
V_{WM}	Stand Off Voltage: Maximum dc voltage that can be applied over the operating temperature range. V_{WM} must be selected to be equal or be greater than the operating voltage of the line to be protected.
V_{BR}	Minimum Breakdown Voltage: The minimum voltage the device will exhibit at a specified current
V_C	Clamping Voltage: Maximum clamping voltage across the TVS device when subjected to a given current at a pulse time of 20 μs .
I_D	Standby Current: Leakage current at V_{WM} .
C	Capacitance: Capacitance of the TVS as defined @ 0 volts at a frequency of 1 MHz and stated in picofarads.

GRAPHS

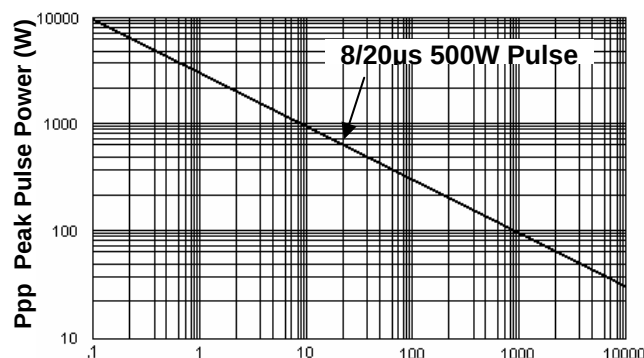


Figure 1
Peak Pulse Power Vs Pulse Time $t = \mu sec$

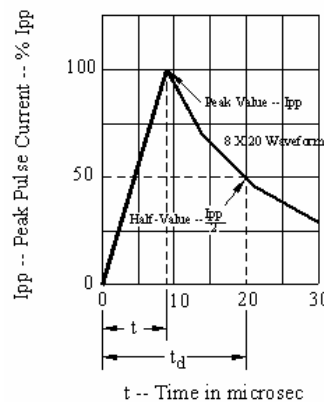
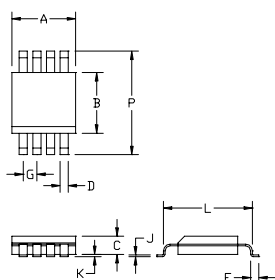


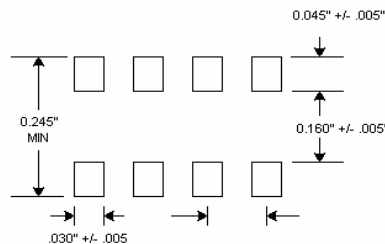
Figure 2
Pulse Wave Form

OUTLINE AND SCHEMATIC

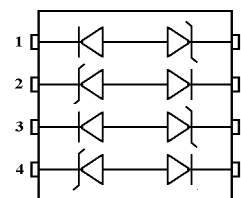


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.188	0.197	4.77	5.00
B	0.150	0.158	3.81	4.01
C	0.053	0.069	1.35	1.75
D	0.011	0.021	0.28	0.53
F	0.0160	0.050	0.41	1.27
G	0.050 BSC		1.27 BSC	
J	0.006	0.010	0.15	0.25
K	0.004	0.008	0.10	0.20
L	0.189	0.206	4.80	5.23
P	0.228	0.244	5.79	6.19

OUTLINE



PAD LAYOUT



SCHEMATIC