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Evaluating the AD4696 16-Channel, 16-Bit, 1 MSPS Multiplexed SAR ADC

FEATURES

- Full featured evaluation board for the AD4696
- 2 channels customizable for external connections and 14 channels for on-board dc voltages
- On-board reference circuitry
- ACE plugin available for device configuration and performance evaluation
- FMC compatible
- System demonstration platform (SDP-H1) compatible

EVALUATION KIT CONTENTS

- EVAL-AD4696FMCZ evaluation board

EQUIPMENT NEEDED

- System demonstration platform (EVAL-SDP-CH1Z)
- Precision analog signal source(s)
- 12 V switched mode power supply (included with EVAL-SDP-CH1Z)
- USB cable (included with EVAL-SDP-CH1Z)
- PC running Windows 7 or higher with USB 2.0 port

ONLINE RESOURCES

- AD4696 data sheet
- EVAL-AD4696FMCZ user guide
- AD4696 ACE plugin evaluation software

GENERAL DESCRIPTION

The EVAL-AD4696FMCZ is designed to demonstrate AD4696 performance and provide access to its many configuration options via an easy to use ACE plugin graphical interface. The AD4696 is a 16-channel, 16-bit, 1 MSPS, multiplexed successive approximation register (SAR) analog-to-digital converter (ADC) that enables high performance data acquisition of multiple signals in a small form factor. The AD4696 employs easy drive features and on-chip channel sequencing that simplify hardware and software designs and allow it to fit into a variety of space constrained precision multichannel applications.

The EVAL-AD4696FMCZ allows users to quickly evaluate the performance of the AD4696 with no or minimal hardware modifications. The hardware includes two externally driven analog input channels for evaluating ac performance and 14 channels with dc levels generated on board for evaluating dc and settling performance. The externally driven channels have configurable drive circuitry and interface with precision signal generators via SMA connectors.

The AD4696 ACE plugin communicates with the EVAL-AD4696FMCZ hardware through the EVAL-SDP-CH1Z controller board. The software allows AD4696 device configuration via a register map view and easy to use GUIs. The software also enables performing analog-to-digital conversions and provides time and frequency domain analysis tools for quick evaluation of the AD4696.

More detailed feature descriptions and device specifications are provided in the AD4696 data sheet and must be consulted in conjunction with this user guide when using the EVAL-AD4696FMCZ. Full details on the EVAL-SDP-CH1Z are available on the SDP-H1 product page.

TABLE OF CONTENTS

REVISION HISTORY

12/2020—Revision 0: Initial Version

EVAL-AD4696FMCZ PHOTOGRAPH

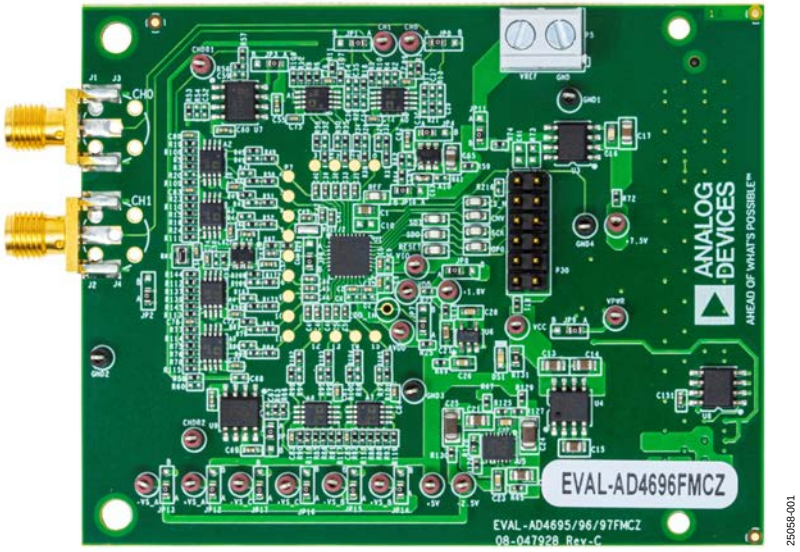

Figure 1.

EVALUATION BOARD HARDWARE GUIDE

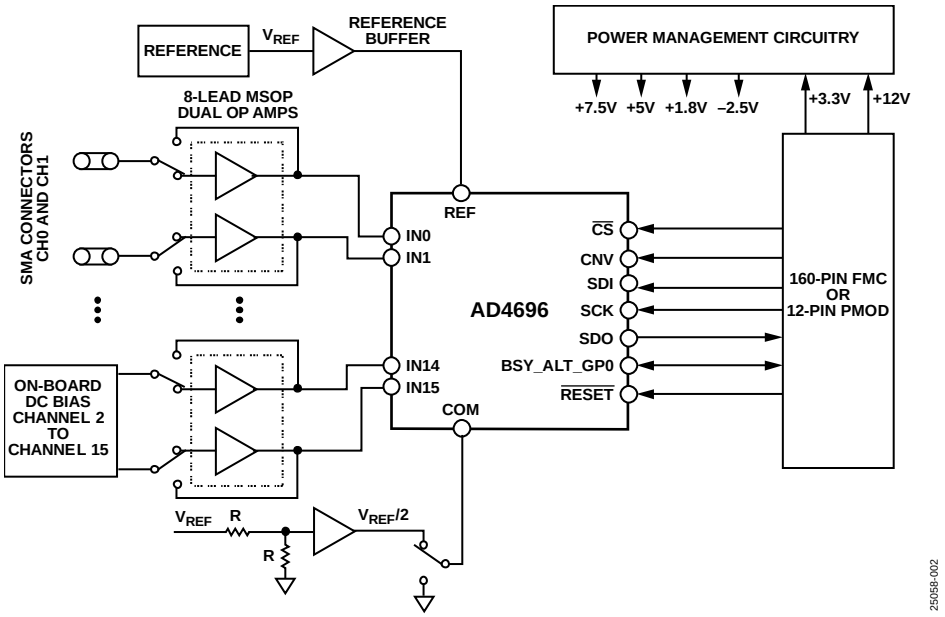

Figure 2. EVAL-AD4696FMCZ Simplified Block Diagram

HARDWARE OVERVIEW

Figure 2 shows a simplified block diagram of the EVAL-AD4696FMCZ hardware. This evaluation board features the AD4696 and peripheral circuitry required for evaluating the device.

The EVAL-AD4696FMCZ is a quick start evaluation platform that showcases the performance of the AD4696 with no or minimal modifications required. Figure 24 to Figure 30 contain the EVAL-AD4696FMCZ schematics. The evaluation board includes an on-board 5 V reference, an ADC driver amplifier for all 16 AD4696 channels, the ability to configure driver amplifiers on Channel IN0 and Channel IN1 in many common configurations, and configurable dc voltage levels for the IN2 through the IN15 channels. By default, the EVAL-AD4696FMCZ is powered entirely from the FMC connector supplies. The Analog Front-End section, the Reference section, the Power Supplies section, and the Digital Interface section describe the design of each of these circuit blocks, how they are used to evaluate the AD4696, and common hardware modifications for each.

ANALOG FRONT-END

The EVAL-AD4696FMCZ evaluation hardware includes an ADC driver amplifier for each of the 16 analog inputs (IN0 to IN15). The driver amplifiers (ADA4805-2 to drive IN0 and IN1, and seven LT6237 devices to drive IN2 and IN15) come in a common dual-amplifier, 8-lead MSOP package, which allows multiple ADC driver options to be evaluated with the AD4696 on the EVAL-AD4696FMCZ.

Channel IN0 and Channel IN1 have been configured to demonstrate ac performance of the AD4696, whereas Channel IN2 through Channel IN15 have been configured to demonstrate simple noise measurements and signal settling measurements with dc voltages generated on board. The amplifiers driving Channel IN0 and Channel IN1 can be configured to perform common signal conditioning functions by adding specific passive components (see the Evaluating AD4696 AC Performance section). The amplifiers driving Channel IN2 to Channel IN15 are driven to dc voltages by on-board amplifiers and user configurable resistor dividers (see the Configuring DC Channels (IN2 Through IN15) section).

Evaluating AD4696 AC Performance (IN0 and IN1)

The EVAL-AD4696FMCZ hardware includes two channels for evaluating the ac performance of the AD4696 using a precision ac signal generator.

Component A0 includes two amplifiers that function as the ADC drivers for the AD4696 IN0 and IN1 inputs. By default, A0 is populated with the ADA4805-2 due to its low noise and low distortion that makes it suitable for ac performance evaluation. The Subminiature Version A (SMA) connectors, J1 through J4, are routed to the inputs of A0 via the signals labeled CH0 and CH1 in Figure 24 and Figure 26.

The J1 through J4 SMA connectors are shown in Figure 24. To apply an ac signal to the IN0 channel, connect the ac signal generator output to J1 or J3. Likewise, to apply an ac signal to the IN1 channel, connect the ac signal generator output to J2 or J4. The ac signal generator must have similar or lower noise and distortion specifications to the AD4696 to properly evaluate AD4696 ac performance (see the AD4696 data sheet for AD4696 device specifications).

The IN0 and IN1 channel amplifiers in A0 can be configured to implement common feedback topologies including a unity-gain buffer, non inverting or inverting amplifier, and active filters, by populating the surrounding passive components appropriately

(see Figure 26). This flexibility allows prototyping of many potential driver configurations. Both A0 amplifiers are configured as unity-gain buffers by default.

The CH0 and CH1 signals from the SMA connectors can be routed to either the non inverting or inverting inputs of the A0 amplifiers to support non inverting and inverting amplifier configurations. Table 1 lists the hardware modifications required to route the CH0 and CH1 signals appropriately for unity gain, non inverting gain, and inverting amplifier configurations for both IN0 and IN1 channels. DNI means do not insert.

Table 1. Hardware Settings for Routing to A0 Inputs

Configuration	IN0	IN1
Unity Gain Buffer	R1 = 0 Ω (default) R13 = DNI (default)	R3 = 0 Ω (default) R14 = DNI (default)
Non Inverting with Gain	R1 = 0 Ω (default) JP0 = Position B	R3 = 0 Ω (default) JP1 = Position B
Inverting	R1 = DNI JP0 = Position A (default)	R3 = DNI JP1 = Position A (default)

Resistor dividers are provided on the non inverting inputs of the CH0 and CH1 channels of A0 to provide a dc bias generated on board via CHDR1 (see R2, R9, R4, and R10 in Figure 26). These resistor dividers are not populated by default. Populate these resistor dividers to drive the non inverting pins of A0 to a constant dc voltage. When populating these resistor dividers while routing an external signal to the non inverting inputs of A0, take care to select the resistor sizes appropriately to achieve the desired attenuation of the dc and ac voltage components.

When modifying the A0 amplifier (currently populated with ADA4805-2) configurations to non default settings, it is recommended to consult the ADA4805-2 data sheet for the selected amplifiers, and consider amplifier stability, noise, distortion, power consumption, and output current when selecting amplifiers and passive component values. When evaluating ac performance, it is also recommended to use NP0 or C0G capacitors in the signal path to avoid distortion degradation associated with the voltage coefficient specifications of other capacitor material types (this applies to all capacitors surrounding the A0 amplifiers in Figure 26).

Configuring DC Channels (IN2 Through IN15)

The analog inputs of the AD4696 are unipolar and accept inputs in the range from 0 V to V_{REF}. For this reason, additional amplifiers are provided on the EVAL-AD4696FMCZ hardware, which generate low noise dc voltages from the reference source that can be used to drive the IN2 through IN15 channels on the AD4696 to fixed dc voltages. Channel IN2 through Channel IN15 are therefore considered dc channels and are provided to evaluate noise performance and settling accuracy performance when sequencing the multiplexer between channels or channel configurations.

There are two dc signals labeled CHDR1 and CHDR2 in Figure 26, Figure 27, and Figure 28. CHDR1 and CHDR2 are generated by two ADA4841-1 devices configured as unity-gain buffers (U7 and U9 in Figure 28). The inputs of U7 and U9 are connected to the output of the voltage reference (U3) by default. Therefore, CHDR1 and CHDR2 are equal to VREF by default. CHDR1 (the output of U7) is routed to the amplifiers in A1 through A3, and CHDR2 (the output of U9) is routed to the amplifiers in A4 through A7 to drive the IN8 through IN15 channels on the AD4696.

Component A1 through Component A7 are dual precision amplifiers that function as the ADC drivers for the AD4696 IN2 through IN15 inputs (see Figure 26 and Figure 27). By default, A1 through A7 are populated with the LT6237 and are fixed as unity-gain buffers. LT6237 is a low noise amplifier suitable for driving SAR ADCs in applications that involve switching.

The dc voltages for IN2 through IN15 channels can be modified via resistor dividers at the inputs of U7 and U9 (see Table 2 and Figure 28) or via resistor dividers at the inputs of A1 through A7 (see Table 3, Figure 26, and Figure 27). Modifying the resistor dividers in Table 2 changes the voltages of CHDR1 and CHDR2, and therefore changes the dc voltages on all downstream ADC driver channels. To configure the voltages for each channel independently from each other, it is recommended to use the default configuration for the resistor dividers in Table 2 and only modify the resistor dividers in Table 3.

When making any modifications to the resistor dividers in front of the ADC drivers, A0 to A7, ensure that the total current load demands for U7 and U9 do not violate the output current limit specification of the ADA4841-1. The output current source limitations of the ADA4841-1 is 30 mA (see the ADA4841-1 data sheet for more information). Ensure the total load of each resistor divider is at least 10 kΩ. By default, each resistor divider on each channel is populated with two 10 kΩ resistors. Thus, the resistor dividers of each channel is equivalent to a 20 kΩ load, and draws 0.5 mA each (when CHDR1 and CHDR2 are the default 5 V). To limit resistor thermal noise coupling into the AD4696 input channels, 0.1 µF capacitors are populated on the non inverting inputs of A1 through A7 (see Figure 26 and Figure 27).

As described in the Evaluating AD4696 AC Performance (IN0 and IN1) section, CHDR1 is also routed to the amplifiers in A0 to supply a dc bias to the IN0 and IN1 ADC drivers. CHDR1 is not connected to the inputs of A0 by default.

Table 2. Resistor Dividers for Setting CHDR1 and CHDR2

Signal	Reference Designators	Default Values
CHDR1	R53	0 Ω
	R54	Do not insert
CHDR2	R58	0 Ω
	R60	Do not insert

Table 3. Resistor Dividers for Setting A0 through A7 DC Input Voltages

Channel	Default Voltage	Series Resistor	Shunt Resistor
IN0	CH0[1]	R2	R9
IN1	CH1[1]	R4	R10
IN2	2.5 V	R6	R11
IN3	2.5 V	R8	R12
IN4	2.5 V	R5	R19
IN5	2.5 V	R7	R20
IN6	2.5 V	R15	R23
IN7	2.5 V	R16	R24
IN8	2.5 V	R137	R144
IN9	2.5 V	R139	R145
IN10	2.5 V	R75	R77
IN11	2.5 V	R76	R78
IN12	2.5 V	R85	R90
IN13	2.5 V	R86	R91
IN14	2.5 V	R88	R92
IN15	2.5 V	R89	R93

[1] CH0 and CH1 are voltages that are supplied externally through J1 or J3, and J2 or J4.

Hardware Configurations for Supporting AD4696 Polarity Modes

As described in the AD4696 data sheet, the AD4696 analog inputs (IN0 through IN15) include channel pairing and polarity mode features to support both single-ended and pseudo differential input types. Each of these options can be evaluated by making simple hardware modifications and associated configuration changes to the register settings of the AD4696 within the AD4696 evaluation software (see the Memory Map View section for instructions on how to modify the contents of the registers of the AD4696).

To ensure correct operation of the AD4696, the EVAL-AD4696FMCZ hardware must be configured with the correct voltages on each analog input, dictated by the operating input voltage specification in the AD4696 data sheet. To ensure correct operation of the AD4696, the EVAL-AD4696FMCZ hardware must be configured with the correct voltages on each of the following analog inputs:

- When COM pairing is selected
  - Unipolar mode enabled = COM must be driven to 0 V
  - Pseudo bipolar mode enabled = COM must be driven to $V_{REF}/2$ V
- When even or odd numbered input pairing is selected
  - Unipolar mode enabled = odd numbered must be driven to 0 V
  - Pseudo bipolar mode enabled = odd numbered input must be driven to $V_{REF}/2$ V

The device does not function as described in the AD4696 data sheet if the hardware configuration does not match the software settings as described in the previous list.

The COM voltage can be tied to ground or $V_{REF}/2$ using the JP6 solder link (see Figure 24 and Table 4). Amplifier A8 produces a dedicated $V_{REF}/2$ V dc voltage utilizing a matched resistor network from the selected VREF source. JP6 selects whether the COM pin is connected directly to the EVAL-AD4696FMCZ ground (for example, 0 V) or the $V_{REF}/2$ V output of A8. Ensure that JP6 is configured appropriately for the channel configuration settings selected via the AD4696 evaluation software. By default, the COM pin is connected to AGND through JP6.

When pairing even and odd numbered inputs, modify the resistor divider components on the input of the ADC driver connected to the relevant odd numbered channel to achieve the required voltage (see the Configuring DC Channels (IN2 Through IN15) section). By default, the odd numbered inputs from IN3 through IN15 are driven to $V_{REF}/2$ V via the resistor dividers listed in Table 3. To drive any given odd numbered input to 0 V instead, it is recommended to populate the corresponding shunt resistor with a 0 Ω resistor and to not populate the corresponding series resistor.

Table 4. JP6 Settings and COM Voltage

JP6 Setting	COM Voltage
A	$V_{REF}/2$ V
B (Default)	0 V

Recommended ADC Drivers

As described in the Evaluating AD4696 AC Performance (IN0 and IN1) section and the Configuring DC Channels (IN2 Through IN15) section, the EVAL-AD4696FMCZ is populated by default with an ADA4805-2 (A0) functioning as the ADC driver for the IN0 and IN1 AD4696 inputs and seven LT6237 devices functioning as the ADC drivers for the remaining 14 AD4696 inputs (IN2 to IN15). These ADC drivers (A0 to A7) can be replaced with other amplifiers, provided they are available in a pin-compatible dual-amplifier, 8-lead MSOP package. Several recommendations include the following:

- ADA4807-2
- ADA4610-2
- ADA4077-2

The AD4696 is compatible with a wider variety of ADC drivers than many multichannel SAR ADCs. Traditionally, SAR ADCs require ADC drivers with high bandwidth to settle voltage steps that occur at its inputs during the conversion process. The inputs of the AD4696 are designed to reduce these voltage steps, which reduces the drive requirements of the amplifiers acting as the ADC drivers. See the AD4696 data sheet for more information.

When using the ADA4610-2 and the ADA4077-2 or using larger resistors between the amplifier and AD4696 input, it is recommended to enable the analog input high-Z mode on the corresponding channels setting the AINHIZ_EN bit in the relevant per channel configuration registers (CONFIG_IN0 through CONFIG_IN15). See the Memory Map View section for instructions on how to configure these register settings.

REFERENCE

The EVAL-AD4696FMCZ includes an on-board precision voltage reference and a reference buffer that supplies the REF pin on the AD4696. The 5 V reference is provided by the ADR4550 (U3), which is an ultralow noise, high accuracy reference source. The ADA4807-1 (A10) functions as a reference buffer. C1 functions as the REF decoupling capacitor (see Figure 24).

The EVAL-AD4696FMCZ provides several options for driving the AD4696 REF input. Jumper JP11 (see Figure 28 and Table 5) selects between the on-board voltage reference (U3, see Figure 25) and an external, user supplied reference source (via the P5 terminal block, see Figure 28).

The selected reference source (on board or external) is also used to generate a dedicated $V_{REF}/2$ voltage and drive the dc bias amplifiers, U7 and U9. The dedicated $V_{REF}/2$ voltage is reserved for setting the COM pin for the COM referenced pseudobipolar mode. See the Configuring DC Channels (IN2 Through IN15) section and the Hardware Configurations for Supporting AD4696 Polarity Modes section for a description of how these voltages are used in evaluating AD4696 performance.

The AD4696 reference input high-Z mode feature effectively lowers the current consumption of the REF pin when performing conversions (see the AD4696 data sheet for more information). The reference input high-Z mode is enabled by default, but can be disabled via the REFHIZ_EN bit (see the Memory Map View section).

Table 5. JP11 Positions for Selecting Reference Source

Position	Reference Source
A	External reference via P5
B (Default)	On-board reference via U3

POWER SUPPLIES

The EVAL-AD4696FMCZ is designed to operate from a 12 V supply (labeled VPWR_12V) and a 3.3 V supply (labeled VCC_HOST) provided from the host controller board via the FMC connector (P1). Alternatively, VPWR_12V can be provided from an external source via the VPWR test point. If the controller board in use does not provide the 12 V supply, the user can provide it through VPWR test point. The on-board power circuitry converts the 12 V VPWR_12V supply into voltage rails to power the AD4696, the A0 to A8 amplifiers, the 5 V on-board reference, and other support circuitry.

The ADP7142 (U2) converts VPWR_12V (12 V) to approximately 7.5 V. ADM660 (U4) converts VCC_HOST (3.3 V) to −V_SUP (−3.3 V). Using 7.5 V and −3.3 V (V_SUP), LT3032 (U5) generates +5 V and −2.5 V. LT1761 (U6) generates a 1.8 V rail from the 5 V rail.

Setting Amplifier Supply Voltages

The positive and negative voltage supply rails of the on-board amplifiers (A0 to A8, A10, U7, and U9) can optionally be set to +7.5 V or +5 V, and −2.5 V or ground, respectively. The on-board amplifiers are connected to one of a set of three positive and three negative supply banks, and the voltage of the banks can be selected via solder links (shown in Figure 29 and Table 6). These banks provide users a way of configuring the on-board amplifiers with different power supply voltages. For example, tying the amplifier negative supplies to ground, the user can evaluate the performance of the AD4696 in unipolar supply systems. Table 6 shows the name and default settings of each bank, the solder link that connects them to the voltage rails, and the amplifiers powered by each bank.

Note that the symbols for A0 through A7 (ADC drivers) are split throughout the schematic, such that the amplifier pins are shown in Figure 26 and Figure 27, whereas the supply pins and the supply bank solder links are shown in Figure 29.

Table 6. Voltage Supply Banks Amplifier Assignments

Supply Bank Name	Default Voltage	Solder Link	Amplifiers
+VS Bank A	7.5 V	JP12	A0, A1, A2, A3
−VS Bank A	−2.5 V	JP13	A0, A1, A2, A3
+VS Bank B	7.5 V	JP14	A4, A5, A6, A7
−VS Bank B	−2.5 V	JP15	A4, A5, A6, A7
+VS Bank C	7.5 V	JP16	A8, A10, U7, U9
−VS Bank C	AGND	JP17	A8, A10, U7, U9

+VS Bank A and −VS Bank A are used to set the supply voltages of the ADC driver amplifiers for Channel IN0 through Channel IN7 of the AD4696 (A0 through A3). +VS Bank B and −VS Bank B are used to set the supply voltages of the ADC driver amplifiers for Channel IN8 through Channel IN15 of the AD4696 (A4 through A7). +VS Bank C and −VS Bank C are used to set the supply voltages of the $V_{REF}/2$ amplifier (A8), the reference buffer (A10) and supply voltages of the dc bias amplifiers (U7 and U9). The grouping of the power supplies into different voltage supply banks allows the user to implement different supplies for different sets of amplifiers, as shown in Table 6.

Power Options for the AD4696

The AD4696 requires an analog supply (AVDD), an ADC core supply (VDD), and I/O logic supply (VIO). Refer to the AD4696 data sheet for voltage range requirements for each of these supplies.

By default, the AVDD pin is powered by the on-board dual low dropout (LDO) linear regulator, LT3032 (U5), and the VIO pin is powered by the on-board 1.8 V LDO regulator, LT1761 (U6).

The VDD (1.8 V) pin of the AD4696 can be powered either with the AD4696 internal LDO regulator, or alternatively from the on-board LT1761 (U6). The hardware can be configured for either of these options via connections between the on-board supply rails and LDO_IN and VDD inputs.

To power VDD with the AD4696 internal LDO regulator, the LDO_IN pin must be powered either by an on-board or externally generated supply, and the VDD pin must be disconnected from any other device (for example, left floating). The EVAL-AD4696FMCZ is configured in the factory accordingly, with the LT1761 disconnected from the VDD pin and the LDO_IN pin driven by LT3032 (U5). In this configuration, the AD4696 internal LDO

regulator is enabled and supplies VDD with 1.8 V automatically on power-up.

To configure the hardware to utilize the on-board regulator instead of the AD4696 internal LDO regulator, the R27 resistor can be populated with 0 Ω, connecting the (1.8 V) output of the LT1761 to VDD. The internal LDO regulator of the AD4696 can then be disabled in the AD4696 ACE plugin by setting the LDO_EN bit to 0. It is worth noting that because the internal LDO regulator of the AD4696 is enabled by default, when the EVAL-AD4696FMCZ is powered up in this configuration, the VDD pin of the AD4696 is simultaneously driven by its internal LDO regulator and the on-board 1.8 V supply. For this reason, the internal LDO regulator of the AD4696 is designed to withstand being driven by an external 1.8 V supply while enabled, but it is recommended to ground the LDO_IN input by changing the position of JP7 to ensure the internal LDO regulator output is not driven at power-up.

See the AD4696 data sheet for more information on the operation of the internal LDO.

Powering EVAL-AD4696FMCZ Externally

All of the active devices can be disconnected from the on-board power circuitry on the EVAL-AD4696FMCZ to enable external power options (for example, a bench top supply). The voltage rails (for example, +7.5 V, +5 V, +1.8 V, and −2.5 V) can be powered externally by removing the 0 Ω resistors at the outputs of the power management ICs that generate them (see Table 7 for the list). The supply pins of the on-board reference, the AD4696, and the amplifier supply banks, can also be disconnected from the on-board supplies in the same way. See the schematic in Figure 25 to locate the relevant components for powering each voltage rail and component supplies.

Table 7. Resistors to Disconnect Voltage Rails from On-Board Supplies

Supply Rail (V)	Resistor
7.5	R123
5	R129
1.8	R135
−2.5	R130

Powering the EVAL-AD4696FMCZ with Other FMC- or PMOD-Compatible Controller Boards

The EVAL-SDP-CH1Z provides the 3.3 V (VCC_HOST) and 12 V supply (VPWR_12V) to the EVAL-AD4696FMCZ through the FMC connector (P1). The EVAL-AD4696FMCZ can also be powered by 3.3 V supplies from other FMC-compatible or PMOD-compatible controller boards (via P1 and P30, respectively) and by 12 V supplies through the VPWR test point (remove R31) or via P1. Before connecting other controller boards to the EVAL-AD4696FMCZ, ensure that their supplies are the correct voltages and have adequate current sourcing capabilities.

The current required by the EVAL-AD4696FMCZ hardware depends on the configuration of on-board circuitry (for example, populated ADC driver amplifiers and number of on-board vs. external power supplies).

DIGITAL INTERFACE

The EVAL-AD4696FMCZ provides access to the AD4696 digital interface pins via a 160-pin field programmable gate array (FPGA) mezzanine card (FMC) connector (P1) and alternatively via a 12-pin extended SPI PMOD-compatible connector (P30).

The AD4696 ACE plugin communicates to the EVAL-AD4696FMCZ hardware via the SDP-H1 board through a 160-pin FMC connector (P1). The software and hardware are designed to quickly and easily connect and enable evaluation of the AD4696.

Alternatively, the user can use a PMOD-compatible device to communicate with the AD4696 through P30. If the user chooses to use a PMOD-compatible device, ensure that the pin assignments match those on the P30 connector.

Setting the AD4696 Logic Voltage (VIO)

The output logic levels of the AD4696 are set by the voltage applied to its VIO pin, which can range from 1.2 V to 1.8 V (see the AD4696 data sheet for detailed VIO specifications). The EVAL-AD4696FMCZ provides several means to drive VIO.

By default, VIO is driven by the on-board, 1.8 V LDO regulator (U6, LT1761). Changing the position of Solder Link JP8 (see Figure 24) allows the VADJ pin on the FMC connector (Pin G39) to drive VIO instead. Both options are compatible with the SDP-H1 that is used in conjunction with the AD4696 evaluation software. Using VADJ also allows the EVAL-AD4696FMCZ to interface with third party FMC-compatible controller boards, provided VADJ can be set within the acceptable range of the VIO pin (see the Using Third Party Controller Boards section).

4-Wire SPI Operation

The AD4696 can be operated using only four SPI signals, if desired, by driving CNV and $\overline{CS}$ with the same signal. The EVAL-AD4696FMCZ enables this mode by changing the default position of JP31. Note that the AD4696 evaluation software does not support this option, and it is intended for use only with third party controller boards with a 4-wire SPI peripheral (see the Using Third Party Controller Boards section).

Using Third Party Controller Boards

The EVAL-AD4696FMCZ hardware largely follows VMEbus International Trade Association (VITA) standards with the FMC pin-to-signal assignments and with the board width on the side with the FMC connector (P1). The pinout on the PMOD connector (P30) follows the PMOD extended SPI standard. By following these standards as much as possible, the EVAL-AD4696FMCZ allows mating of the AD4696 with other common controller boards. If using an FMC-compatible controller board other than the SDP-H1, ensure that its logic levels and VADJ pin (Pin G39) can be set to between 1.2 V and 1.8 V. It is also recommended to use a cable to interface PMOD-compatible controller boards to the PMOD header on the evaluation board.

Note that when using PMOD-compatible boards, it is necessary to supply the 12 V VPWR supply externally through the VPWR test point.

LINK CONFIGURATION OPTIONS

Take care before applying power and signals to the EVAL-AD4696FMCZ to ensure all solder link positions are set as required by the operating mode. Table 8 lists the solder link functions on the EVAL-AD4696FMCZ hardware, and indicates the default positions in which the links are set as manufactured.

Table 8. Links, Factory Default Settings

Link	Default	Function	Comment
JP0, JP1	A	Connects the inverting inputs of the IN0 and IN1 channel ADC drivers (A0) to SMA inputs (J1 or J3, and J2 or J4) or board ground. Default state is SMA input.	Change to B to tie the inverting input to ground (populate R13 = R14 = 0 Ω as well).
JP2	A	Used to enable or disable the on-board VREF/2 divider (A8, ADA4807-1). The VREF/2 divider must be enabled when configuring an AD4696 channel in pseudobipolar mode and paired with COM. Default state is enabled.	Change to B to disable the VREF/2 divider.
JP3	A	Used to enable or disable the dc bias generator for Channel 0 to Channel 7 (U7, ADA4841-1). Default state is enabled.	Change to B to disable the dc bias generator for IN0 to IN7.
JP4	A	Used to enable or disable the on-board reference buffer (A10, ADA4807-1). Default state is enabled.	Change to B to disable the on-board reference buffer.
JP5	A	Used to enable or disable the dc bias generator for Channel 8 to Channel 15 (U9, ADA4841-1). Default state is enabled.	Change to B to disable the dc bias generator for IN8 to IN15.
JP6	B	Connects the COM pin of the ADC to ground or the output of the VREF/2 buffer (A8). See the Hardware Configurations for Supporting AD4696 Polarity Modes section for instructions on selecting the appropriate position of JP6.	Change to A to connect the COM pin to VREF/2 V.
JP7	A	Connects LDO_IN to AVDD or AGND. By default, the internal LDO is enabled because LDO_IN is connected to AVDD and VDD is floating. To disable the internal LDO regulator, connect LDO_IN to AGND.	Change to B to connect LDO_IN to AGND
JP8	A	Connects VIO to 1.8 V on board (U6, LT1761) or VADJ. By default, VIO is connected to 1.8 V on board.	Change to B to connect VIO to VADJ.
JP9	A	Used to enable or disable ADP7142 (U2) LDO regulator on board. By default, this LDO is enabled. If powering the 7.5 V test point using an external source, this LDO can be disabled.	Change to B to disable the LDO.
JP11	B	Used to select between on-board reference (U3, ADR4550) and external reference (P5). By default, the on-board reference is connected.	Change to A to use external reference.
JP12	A	Selects between the on-board 7.5 V and 5 V voltage rails for +VS Bank A. Default state is 7.5 V.	+VS Bank A connects to the positive supply pins of A0 to A3. Change JP12 to Position B to select 5 V. See the Setting Amplifier Supply Voltages section for more information.
JP13	A	Selects between the on-board −2.5 V voltage rail and ground for −VS Bank A. Default state is −2.5 V.	−VS Bank A connects to the negative supply pins of A0 to A3. Change JP13 to Position B to select ground. See the Setting Amplifier Supply Voltages section for more information.
JP14	A	Selects between the on-board 7.5 V and 5 V voltage rails for +VS Bank B. Default state is 7.5 V.	+VS Bank B connects to the positive supply pins of A4 to A7. Change JP14 to Position B to select 5 V. See the Setting Amplifier Supply Voltages section for more information.
JP15	A	Selects between the on-board −2.5 V voltage rail and ground for −VS Bank B. Default state is −2.5 V.	−VS Bank B connects to the negative supply pins of A4 to A7. Change JP15 to Position B to select ground. See the Setting Amplifier Supply Voltages section for more information.
JP16	A	Selects between the on-board 7.5 V and 5 V voltage rails for +VS Bank C. Default state is 7.5 V.	+VS Bank C connects to the positive supply pins of A8, A10, U7, and U9. Change JP16 to Position B to select 5 V. See the Setting Amplifier Supply Voltages section for more information.
JP17	A	Selects between the on-board −2.5 V voltage rail and ground for −VS Bank C. Default state is −2.5 V.	−VS Bank C connects to the negative supply pins of A8, A10, U7, and U9. Change JP17 to Position B to select ground. See the Setting Amplifier Supply Voltages section for more information.
JP31	B	Connects CNV and CS_N signals for 4-wire SPI operation (see the 4-Wire SPI Operation section). By default, the CNV and CS_N signals are not connected to each other.	Change to Position A to connect the CS_N and CNV signals.

GETTING STARTED

SOFTWARE INSTALLATION

Download the ACE evaluation software from the EVAL-AD4696FMCZ product page. Both the EVAL-AD4696CFMCZ software and the EVAL-SDP-CH1Z (SDP-H1) board drivers must be installed.

Warning

The ACE evaluation software and drivers must be installed before connecting the EVAL-AD4696FMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the ACE Evaluation Software

To install the ACE evaluation software, take the following steps:

1. Download the ACE evaluation software to a Windows®-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the software is saved to **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box appears asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. Click **Next >** to continue the installation, as shown in Figure 3.

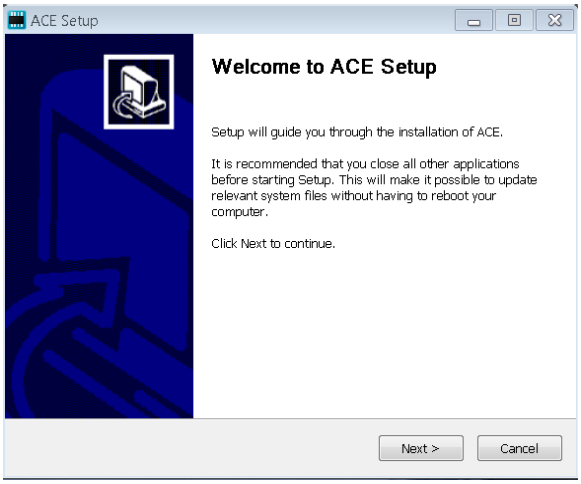

Figure 3. Evaluation Software Install Confirmation

5. Read the license agreement and click **I Agree.**

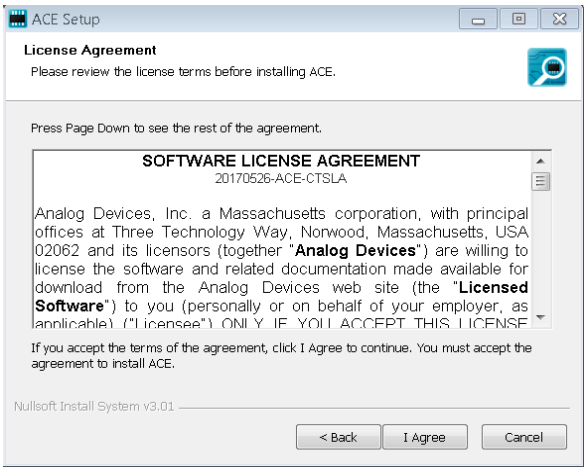

*Figure 4. **License Agreement***

6. Choose the install location and click **Next >**.

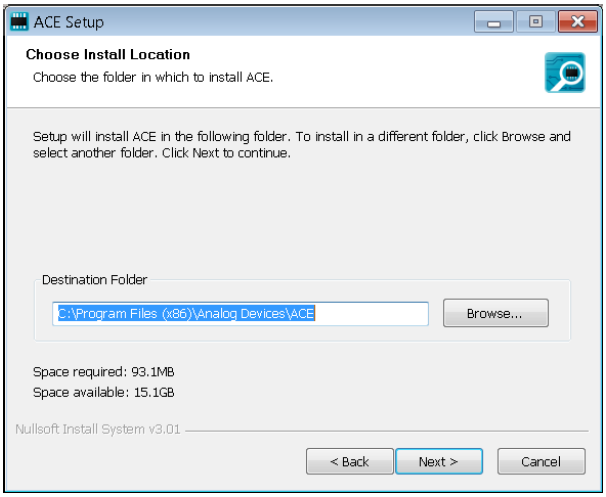

*Figure 5. **Choose Install Location** Window*

7. The components to install are preselected. Click **Install.**

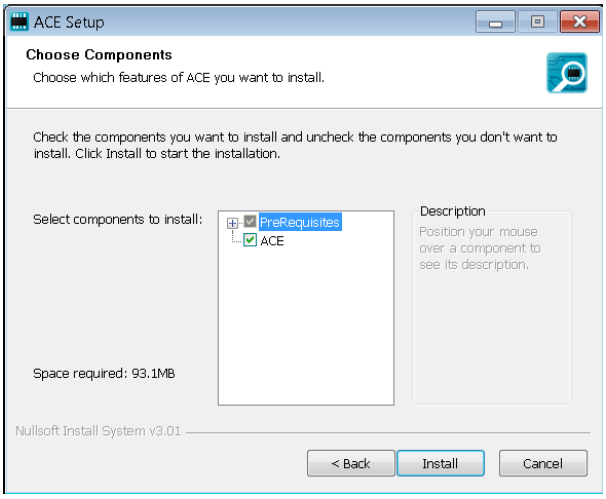

*Figure 6. **Choose Components***

8. A display bar showing the installation progress appears, as shown in Figure 7.

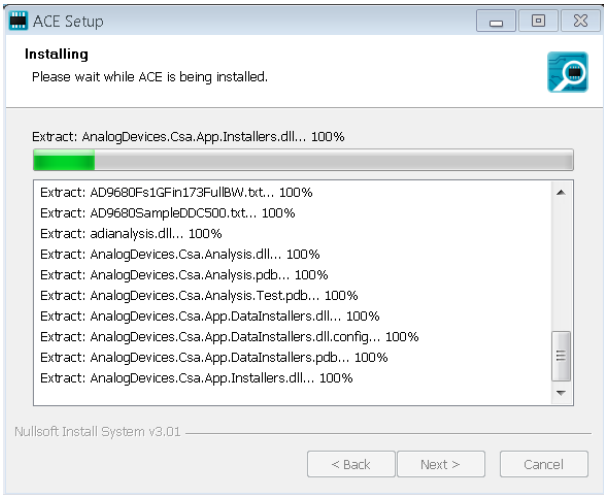

Figure 7. Installation in Progress

9. When the installation is complete, click **Next >**, and then click **Finish** to complete.

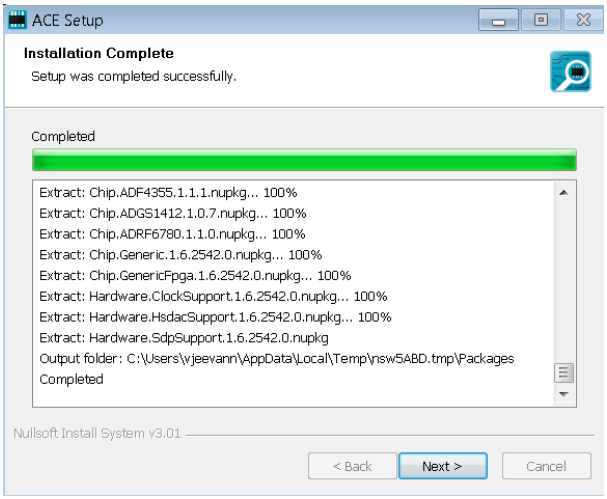

*Figure 8. **Installation Complete***

When first plugging in the SDP-H1 via the USB cable provided, allow the **Found Hardware Wizard** to run. After the drivers are installed, ensure that the SDP-H1 is connected properly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer** > **Manage** > **Device Manager** from the list of **System Tools**.

The **Analog Devices SDP-H1** appears under **ADI Development Tools**, as shown in Figure 9.

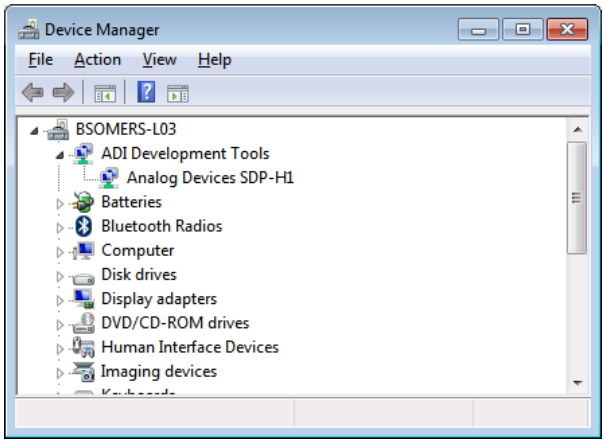

*Figure 9. **Device Manager** Window*

Installing and Updating the AD4696 ACE Plugin

After the EVAL-AD4696FMCZ and SDP-H1 boards are properly connected to the PC as described in the Evaluation Hardware Setup Procedure section, launch the ACE evaluation software. To install and update the AD4696 ACE plugin, perform the following steps:

1. From the **Start** menu, select **All Programs > Analog Devices > ACE > ACE.exe**, which brings up the window shown in Figure 13.
2. To install the AD4696 ACE plugin, click **Plug-in Manager** on the left of the ACE main window, as shown in Figure 10.
3. Select the **Available Packages** drop down menu on the left and search for AD4696 using the search text box on the right, as shown in Figure 11 (the AD4696 plugin is not shown as an option in Figure 11 because that plugin is not released yet).
4. Select the AD4696 plugin and click **Install Selected** at the bottom of the plugin manager window to install the AD4696 plugin.

ACE automatically checks for updates to all installed plugins when launched, and displays a prompt to install updates when available. To manually check for updates to the AD4696 plugin, perform the following steps:

1. Click the **Plug-in Manager** on the left of the ACE main window, as shown in Figure 10.
2. Select the **Available Updates** drop down menu on the left and search for AD4696 using the search text box on the right. If an update is available, it is shown in the list.
3. Select the AD4696 plugin and click **Update Selected** at the bottom of the plugin manager window to update the AD4696 plugin, as shown in Figure 12 (the AD4696 plugin is not shown as an option in Figure 12 because that plugin is not released yet).

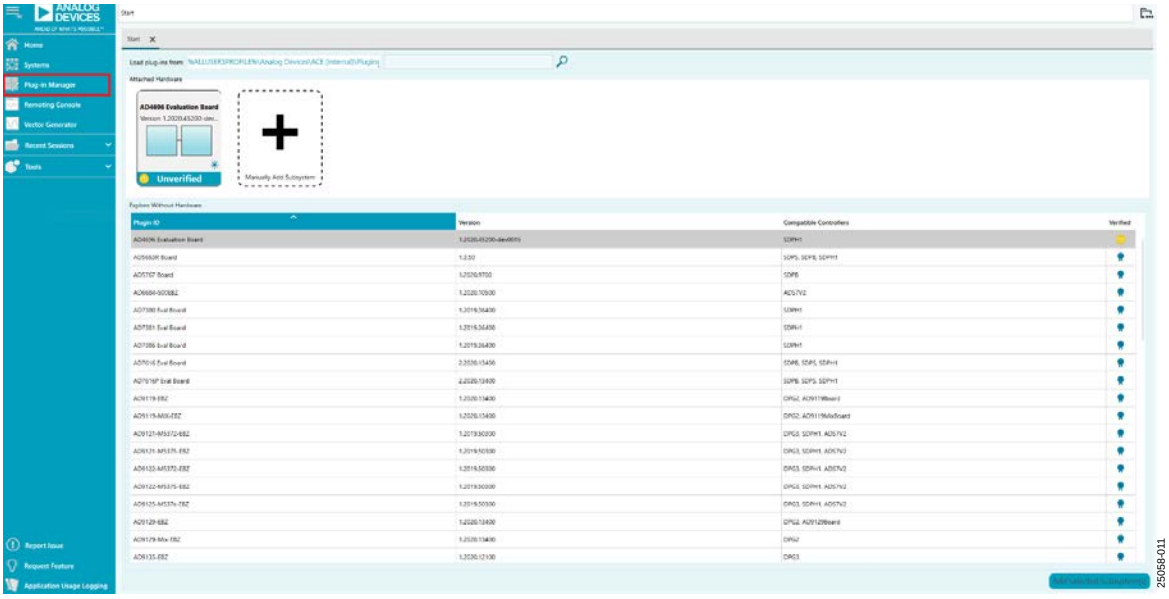

*Figure 10. Selecting **Plug-in Manager***

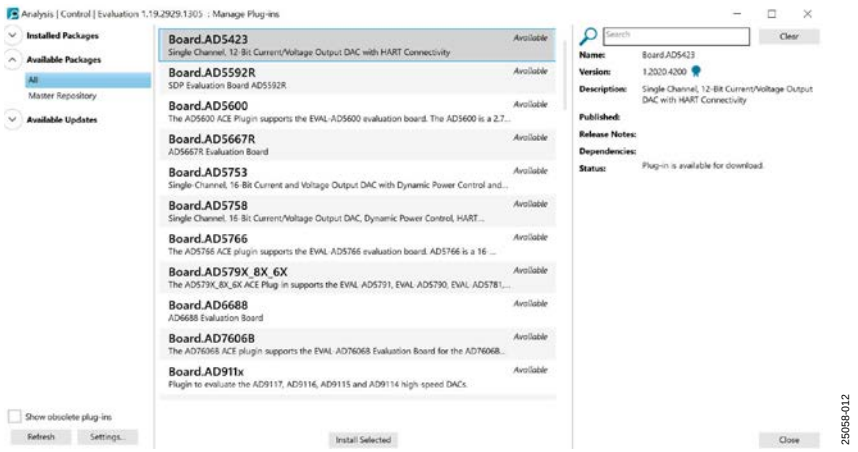

Figure 11. Installing AD4696 ACE Plugin

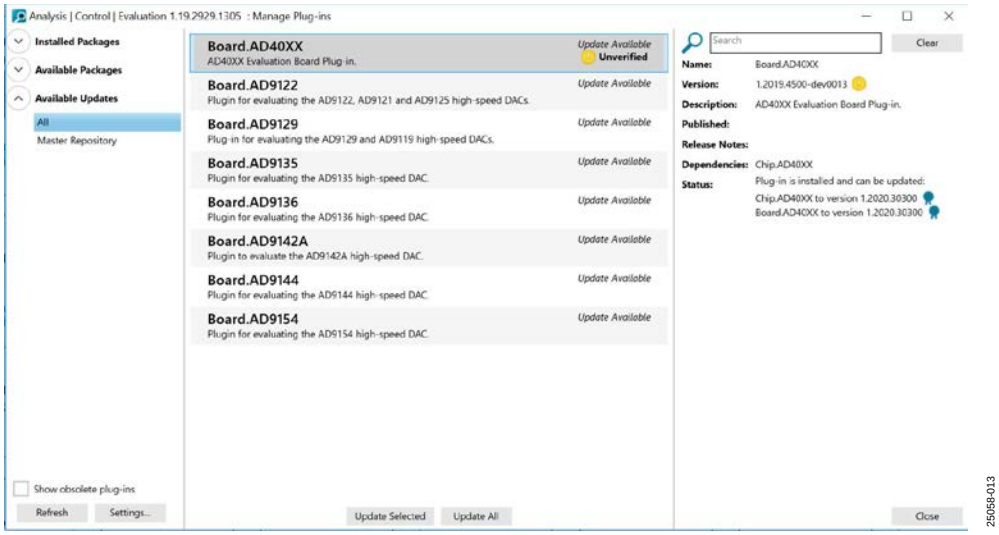

Figure 12. Updating AD4696 ACE Plugin

EVALUATION HARDWARE SETUP PROCEDURE

When using the AD4696 ACE plugin, the SDP-H1 is required to interface between the EVAL-AD4696FMCZ hardware and the PC. The EVAL-AD4696FMCZ connects to the SDP-H1 via the FMC connector (P1).

Connecting the Evaluation Hardware to a PC

To connect the EVAL-AD4696FMCZ and SDP-H1 to a PC, perform the following steps:

1. Before connecting power, connect the FMC connector of the EVAL-AD4696FMCZ (P1) to the FMC connector on the SDP-H1 (J4).
2. Power the SDP-H1 with the included 12 V dc adapter as described in the Power Supplies section.
3. Connect the SDP-H1 to the PC with the USB cable.
4. If generating any of the supply rails externally, turn on the external supplies before launching the AD4696 ACE plugin.

Verifying Hardware Connection

To verify the EVAL-AD4696FMCZ is properly connected to the PC, take the following steps:

1. Allow the **Found New Hardware Wizard** to finish running after the SDP-H1 is connected to the PC via the USB cable. Choose the **Automatically Search for the Appropriate Drivers** option for the SDP drivers if prompted.
2. Verify the hardware to PC connection by navigating to the **Device Manager** via the **Control Panel**. If the hardware is properly connected, **Analog Devices SDP-H1** appears under **ADI Development Tools**.

Disconnecting the Evaluation Hardware from the PC

The recommended steps for disconnecting and powering down the EVAL-AD4696FMCZ are as follows:

1. Power down and disconnect any external sources connected to the SMA inputs.
2. Press the reset switch on the SDP-H1.
3. If using external supplies for any of the supply rails, disconnect them.
4. Disconnect the USB cable from the SDP-H1.
5. Disconnect the 12 V supply from the SDP-H1.

EVALUATION SOFTWARE OPERATION

LAUNCHING THE AD4696 ACE PLUGIN

After the EVAL-AD4696FMCZ and SDP-H1 are correctly connected to the PC as described in the Evaluation Hardware Setup Procedure section, launch the ACE evaluation software as described in the following steps.

1. From the **Start** menu, select **All Programs > Analog Devices > ACE > ACE.exe**, which opens the window shown in Figure 13.
2. Double click the **AD4696 Evaluation Board** icon in the **Attached Hardware** section in the ACE **Start** window to display the AD4696 evaluation board view (see Figure 13).
3. Double click the **AD4696** chip icon to display the AD4696 chip view (see Figure 14).

DESCRIPTION OF CHIP VIEW

After completing the steps in the Software Installation section and the Launching the AD4696 ACE Plugin section, the AD4696 chip view is displayed. The AD4696 chip view allows the user to configure the most commonly used AD4696 device features and for navigating to the other plugin views described throughout the Evaluation Software Operation section.

Block Diagram Configuration Menus

The AD4696 chip view includes a block diagram representation of the AD4696 with controls for configuring the connected device on the EVAL-AD4696FMCZ. Block icons that are dark blue are programmable blocks. Clicking a dark blue block icon opens a pop up window with controls for configuring several AD4696 device features and settings.

Modifying the controls in any block icon automatically updates the relevant registers and bit fields in the memory map view. The controls in each block icon also update if their corresponding registers and bit fields are modified directly in the memory map view.

After selecting the desired device configuration settings in the block icons in the chip view, click the **Apply Changes** button to apply the new settings to the connected hardware.

Plugin View Navigation Buttons

On the chip view are the following view navigation buttons (see Figure 15):

- **Configure Sequence**
- **Configure Channels**
- **Proceed to Analysis**
- **Proceed to Memory Map**

The **Configure Sequence** button opens either the **Standard Sequencer** view or the **Advanced Sequencer** view, depending on which sequencer mode is selected in the software memory map (see the Description of the Standard Sequencer View section and the Description of the Advanced Sequencer View section).

The **Configure Channels** button opens the **Channel Configuration** view (see the Channel Configuration View section).

The **Proceed to Analysis** button opens the **AD4696 Analysis** view (see the Analysis View section).

The **Proceed to Memory Map** button opens the **AD4696 Memory Map** view (see the Memory Map View section).

Memory Map Side-by-Side View

Clicking the **Memory Map Side-By-Side** button displays the memory map view in a window beside the chip view. Displaying the chip view and memory map view side-by-side allows the user to observe which bit field and register settings in the AD4696 memory map correspond with GUI controls in the chip view.

SEQUENCER CONFIGURATION VIEWS

The AD4696 ACE plugin includes two sequencer configuration views that streamline the setup of channel sequences for the AD4696 standard sequencer and advanced sequencer. The sequencer configuration views are a GUI representation of the multiplexer channel sequence settings programmed into the AD4696 via the device memory map. See the AD4696 data sheet for a detailed description of the standard sequencer and advanced sequencer.

The sequencer configuration views include the following:

- Standard sequencer view
- Advanced sequencer view

Accessing the Sequencer Configuration Views

The standard sequencer view and the advanced sequencer view can be accessed from either the chip view or the analysis view.

In the chip view, press the **Configure Sequence** button to display either the standard sequencer view or the advanced sequencer view (see the Plugin View Navigation Buttons section).

In the analysis view, select either the standard sequencer or advanced sequencer using the **Sequencer Mode** dropdown box and click the **Go To Sequencer** button to display the selected sequencer configuration view (see the Analysis View section).

Description of the Standard Sequencer View

The standard sequencer view appears as shown in Figure 16. Select the list of channels that are to be a part of the sequence using the **Channel Enable** checkboxes, and click **Apply Changes** to configure the connected device accordingly.

The **Channel Sample Rates** indicators display the effective sample rates computed for each channel enabled in the standard sequencer via the **Channel Enable** checkboxes, where FSR refers to the sample rate setting stored in the **Throughput (kSPS)** control in the analysis view (see Figure 20).

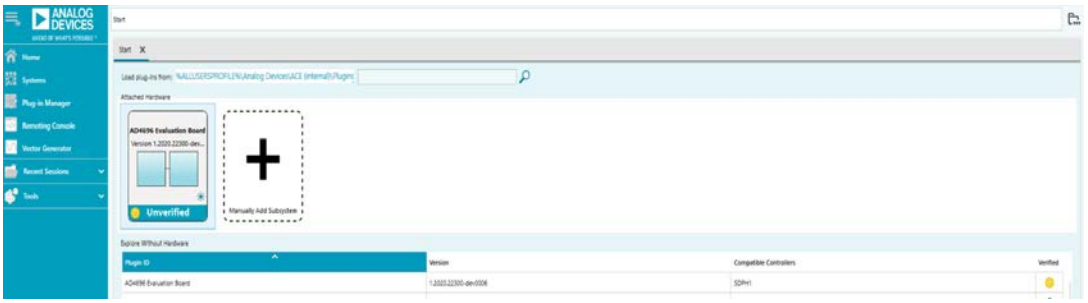

*Figure 13. ACE Software **Start** Window*

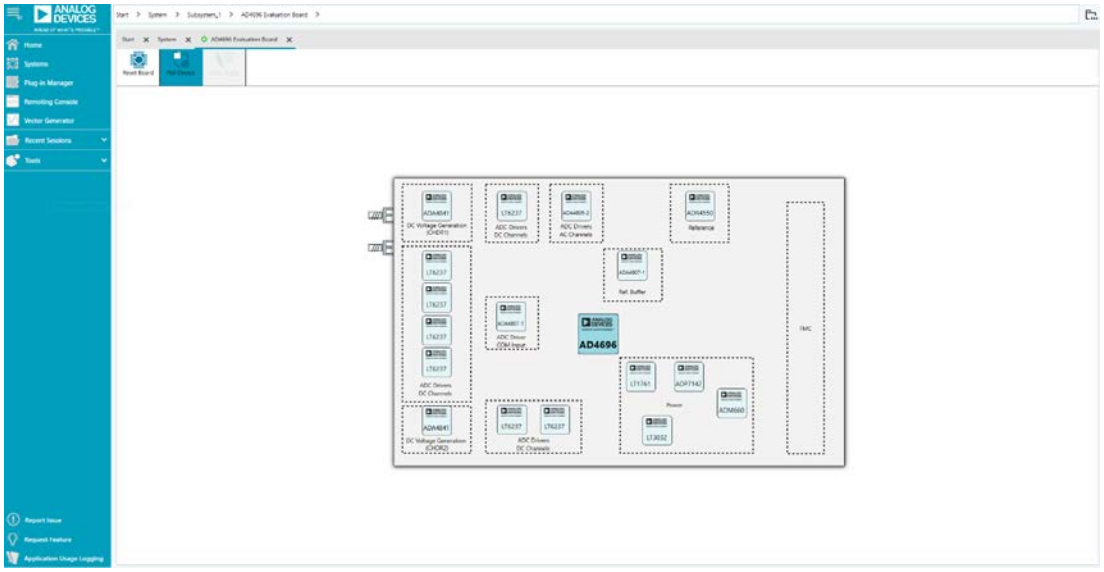

Figure 14. Evaluation Board View

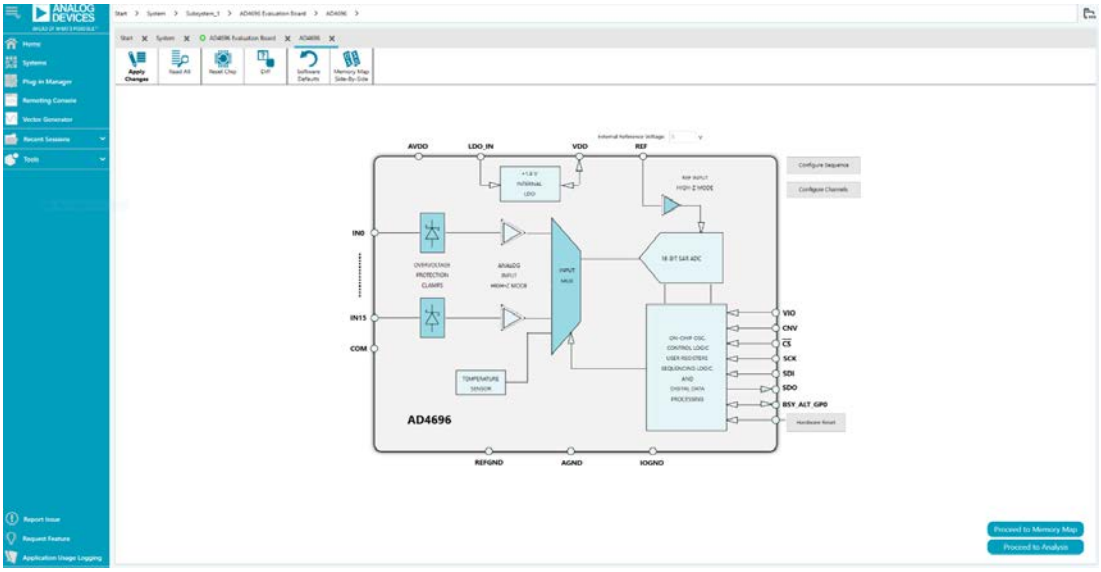

Figure 15. Chip View

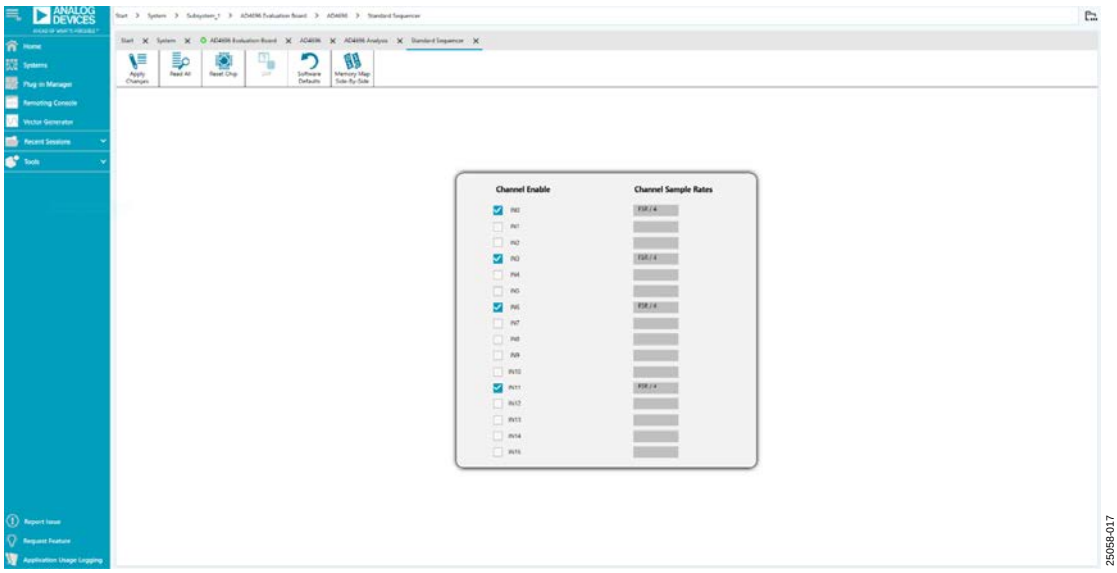

*Figure 16. **Standard Sequencer** View*

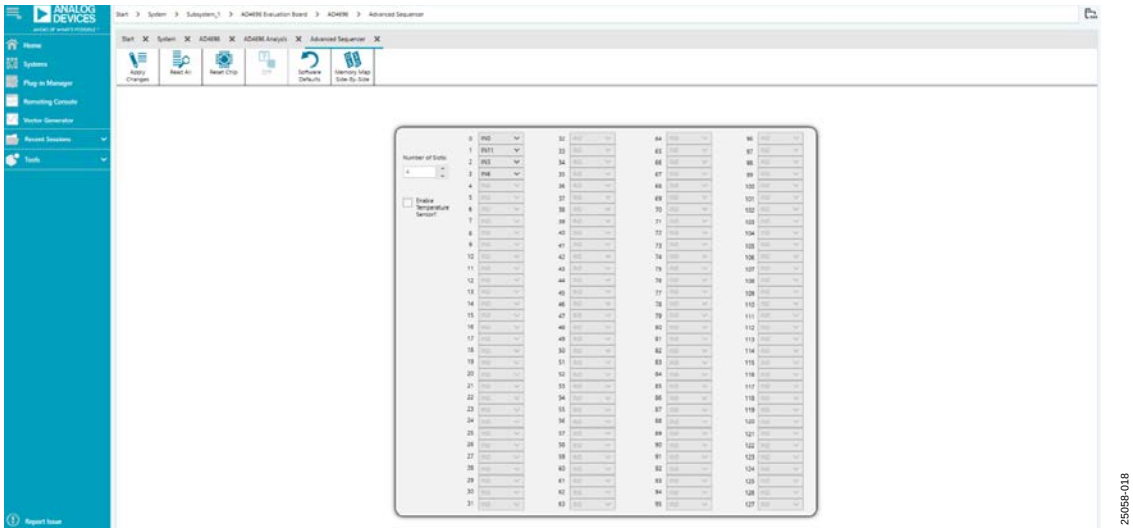

*Figure 17. **Advanced Sequencer** View*

For example, in Figure 16, each enabled channel has an effective sample rate of FSR/4 because there are four channels enabled in the sequence. Therefore, each channel is polled once per four conversion periods in this sequence.

The standard sequencer configuration can also be manually configured via the memory map view. Modifying the state of the **Channel Enable** checkboxes in the standard sequencer view updates the corresponding bit fields in the memory map view, and vice versa. See the AD4696 data sheet for a detailed description of the configuration register settings required to configure the AD4696 standard sequencer.

Description of the Advanced Sequencer View

The advanced sequencer view appears as shown in Figure 17. Use the **Number of Slots** text box to enter the number of desired slots in the sequence. Select the desired channel for each slot using the slot assignment dropdown menus. Click **Apply Changes** to configure the connected device accordingly.

The number of slot assignment dropdown boxes that are enabled or disabled is determined by the value in the **Number of Slots** text box. All slot assignment controls are disabled (in gray) if they are not included in the sequence. For example, in Figure 17, the **Number of Slots** control is set to 4. Therefore, four slot assignment controls are active while the remaining 124 are disabled.

The advanced sequencer configuration can also be manually configured via the memory map view. Modifying the state of the **Number of Slots** and slot assignment controls updates the corresponding bit fields in the memory map view, and vice versa. See the AD4696 data sheet for a detailed description of the configuration register settings required to configure the AD4696 advanced sequencer.

CHANNEL CONFIGURATION VIEW

The AD4696 ACE plugin includes a channel configuration view that streamlines the configuration of the AD4696 analog input channels. The channel configuration view is a GUI representation of the channel settings for each of the 16 AD4696 channels controlled via the device memory map.

Click the **Configure Channels** button in the chip view to open the **Channel Configuration** view (see Figure 18).

The **Channel Configuration** view divides the various channel configuration settings into different tabs based on which AD4696 channel they correspond to. Settings that are common to all AD4696 channels are displayed in the **All Channel Controls** section (see Figure 18 and Figure 19). Settings that are independent for each individual channel (IN0 through IN15) are shown in the **Controls for Channel** section (see Figure 18 and Figure 19).

The controls that are visible in the **All Channel Controls** tab vs. the controls visible in the **Controls for Channel** tab depends on the active sequencer mode (standard sequencer vs. advanced sequencer) to reflect how these settings are applied differently based on the channel sequencer mode. See the AD4696 data sheet for a detailed description on how the channel sequencing mode affects how channel configuration settings are applied to the 16 AD4696 channels.

The channel configuration settings for the connected device can also be manually configured via the memory map view. Modifying the state of the controls in the channel configuration view updates the corresponding bit fields in the memory map view, and vice versa. See the AD4696 data sheet for a detailed description of the features accessible via the **Channel Configuration** view and the corresponding register configuration settings.

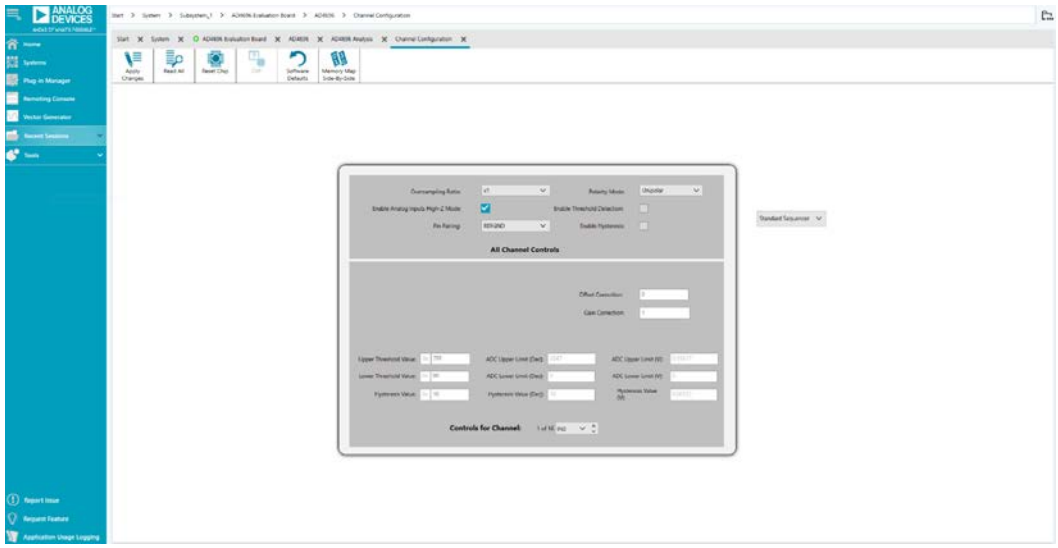

*Figure 18. **Channel Configuration** View when Standard Sequencer Is Enabled*

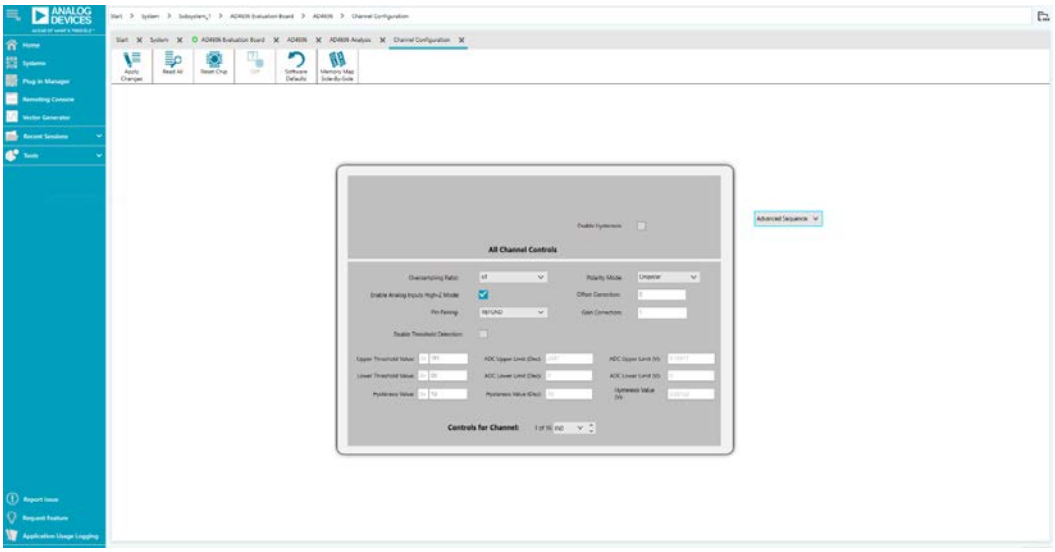

*Figure 19. **Channel Configuration** View when Advanced Sequencer Is Enabled*

All Channel Controls

The **All Channel Controls** tab appears at the top of the **Channel Configuration** view as shown in Figure 18 and Figure 19. After the desired selections are made, click **Apply Changes** to configure the connected device accordingly.

Controls for Channel

Settings that are applicable for each channel separately can be applied through the **Controls for Channel** tab at the bottom of the **Channel Configuration** view, as shown in Figure 18 and Figure 19.

The **Offset Correction** text box accepts signed integer values in decimal format. The value typed into this control has units of codes and is the decimal representation of the binary, twos complement value that is stored into the offset bit field in the corresponding OFFSET_INn register.

The **Gain Correction** text box accepts double data type values between 0 and 1.99997. The value written to the gain bit field in the corresponding GAIN_INn register is determined by the following expression: gain = M × (2^{15}), where M is the value entered in the **Gain Correction** text box.

The **Upper Threshold Value** text box accepts 12-bit hexadecimal values between 0x000 and 0xFFF. The value entered in this text box is written to the upper bit field in the corresponding UPPER_INn register.

The **Lower Threshold Value** text box accepts 12-bit hexadecimal values between 0x000 and 0xFFF. The value entered in this text box is written to the lower bit field in the corresponding LOWER_INn register.

The **Hysteresis Value** text box accepts 12-bit hexadecimal values between 0x000 and 0xFFF. The value entered in this text box is written to the hysteresis bit field in the corresponding HYST_INn register.

When the required selections have been made, click **Apply Changes** to confirm the changes.

ANALYSIS VIEW

The analysis view includes controls to configure and perform ADC data capture as well as to display the captured data and analysis summary of the performance of connected hardware. Click the **Proceed to Analysis** button in the chip view to open the analysis view, as shown in Figure 15.

The analysis view contains the **Waveform** tab, **Histogram** tab, and **FFT** tab, each described in the Waveform Tab section, Histogram Tab section, and FFT Tab section, respectively. These tabs display data and analyzed performance of the data captured from the connected hardware.

The **Waveform**, **Histogram**, and **FFT** tabs each display the **CAPTURE** pane and the **ANALYSIS SETTINGS** pane. The **CAPTURE** pane includes controls for configuring the ADC data capture (see the Capture Pane section). The **ANALYSIS SETTINGS** pane includes settings and parameters for frequency domain analysis, including FFT calculation and ac performance calculations (see the Analysis Settings section).

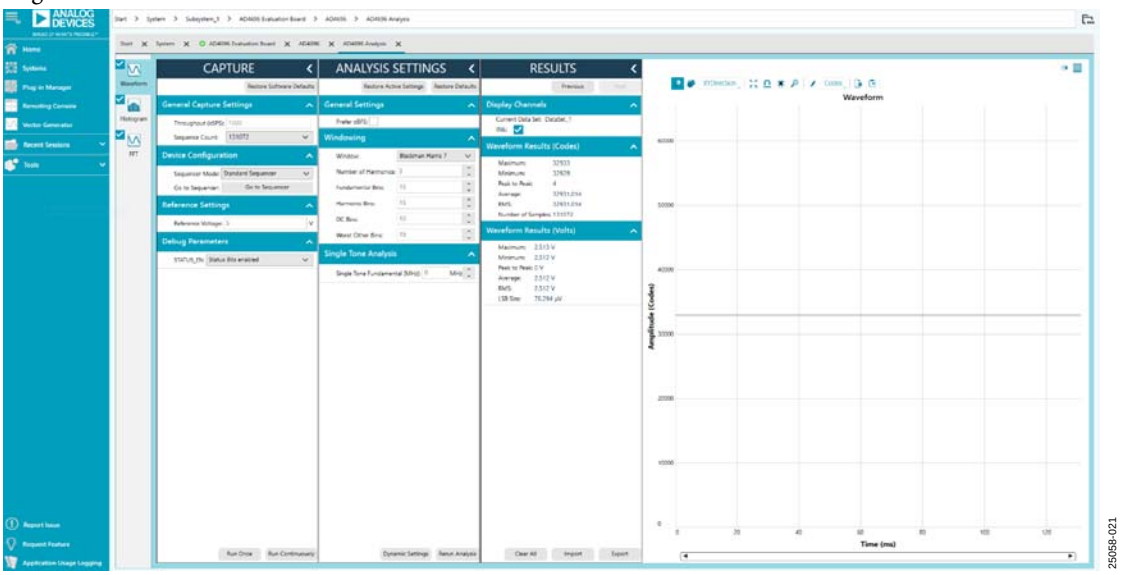

*Figure 20. Analysis View with **Waveform** Tab Selected*

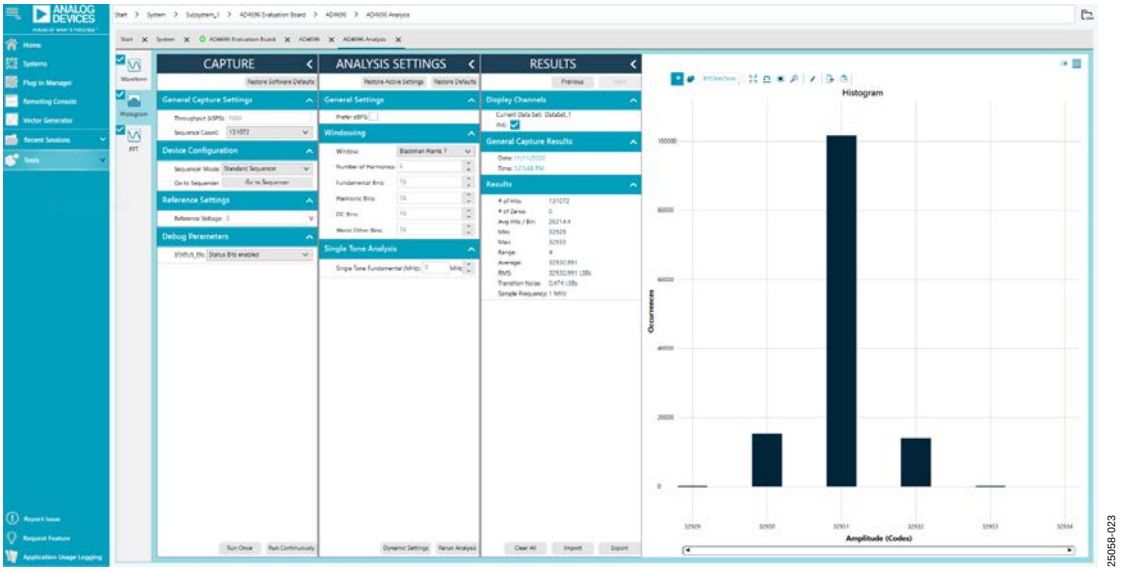

*Figure 21. **Histogram** Tab*

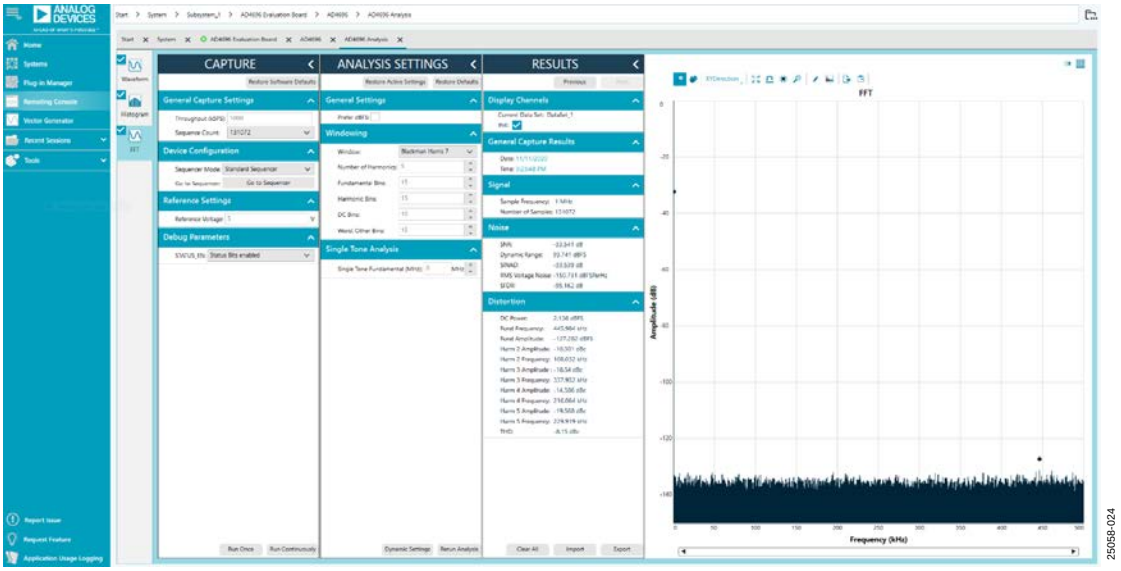

*Figure 22. **FFT** Tab*

Capture Pane

General Capture Settings

The **Sequence Count** list box allows the user to select the number of times to execute the configured channel sequence per capture.

The user can enter the sample rate in kilosamples per second (kSPS) in the **Throughput (kSPS)** box. Note that this box sets the sample rate of the AD4696 ADC core (for example, CNV signal frequency), whereas the effective sample rate for each AD4696 channel depends on the sequencer configuration.

Device Configuration

The **Sequencer Mode** dropdown box allows the user to select the desired sequencer mode.

Clicking the **Go to Sequencer** button opens either the standard sequencer view or the advanced sequencer view based on the value selected in the **Sequencer Mode** dropdown menu.

Reference Settings

Use the **Reference Voltage** text box to enter the value of the reference voltage on the connected hardware. The **Reference Voltage** box is used by the analysis math to convert between ADC codes and equivalent input voltage. Changing the **Reference Voltage** value does not modify any hardware or memory map settings on the connected hardware. If the value in the **Reference Voltage** box does not match the reference voltage used on the connected hardware, the data in the **Waveform** graph is incorrect when displayed in volts.

Run Once

Click **Run Once** to start a data capture at the sample rate specified in the **Throughput (kSPS)** box for the number of channel sequence iterations specified in **Sequence Count** list box. The total number of samples per capture is equal to the number of sequences in the **Sequence Count** list box multiplied by the length of the sequence.

Clicking **Run Once** instructs the software to put the connected AD4696 in conversion mode, capture the requested number of samples, then put the connected AD4696 back into register configuration mode and plot the data in the **Waveform**, **Histogram**, and **FFT** tabs.

Run Continuously

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time. When **Run Continuously** is active, the software repeatedly executes the capture routine specified by the **Run Once** button. To terminate the repeated captures, click the **Run Continuously** button again to put it in the inactive state.

Analysis Settings

General Settings

Select the **Prefer dBFS** checkbox to display the results of the FFT analysis in dBFS.

Windowing

The **Windowing** pane allows the user to select the windowing type used in the FFT analysis, the number of harmonic bins, and the number of fundamental bins that must be included.

WAVEFORM TAB

Click the **Waveform** tab icon on the left side of the analysis view to display the **Waveform** tab (see Figure 20). The **Waveform** graph shows the time domain representation of the most recently read conversion results from the connected AD4696 hardware, and the **RESULTS** pane displays several common time domain analysis items.

Results Pane

Display Channels

The **Display Channels** section lists the active channels in the current sequence. Select the check box in the display channels tab to display the results for the corresponding channel. To remove a particular channel from display, clear the box for the corresponding channel.

Results

The **Waveform Results (Codes)** section and the **Waveform Results (Volts)** section display amplitude, sample frequency, and noise analysis information for the selected channel(s).

Export

Click the **Export** button to export captured data to a file. The waveform, histogram, and FFT data are stored in .xml files along with the values of parameters at capture.

Waveform Graph

The data waveform graph shows each successive sample of the ADC output. The user can zoom and pan the waveform using the embedded waveform tools. The channels to display can be selected in **Display Channels.**

Display Units and Axis Controls

Click the display units dropdown list to select whether the data graph displays in units of Hex, volts, or codes (decimal) (see Figure 20).

HISTOGRAM TAB

Click the **Histogram** tab icon on the left side of the analysis view to display the **Histogram** tab (see Figure 21). The **Histogram** graph shows the number of occurrences for each ADC code result in the data shown in the waveform graph, and the **RESULTS** pane displays several common statistical analysis items.

FFT TAB

Click the **FFT** tab icon on the left side of the analysis view to display the **FFT** tab (see Figure 22). The **FFT** graph shows the FFT calculated from the data displayed in the waveform graph, and the **RESULTS** pane displays several frequency domain analysis items and performance metrics, including SNR, THD, and SINAD.

MEMORY MAP VIEW

Click the **Proceed to Memory Map** button in the chip view (see Figure 15) to open the memory map view shown in Figure 23. The memory map view shows the names, locations, and current states of all configuration registers and bit fields of the connected AD4696 device.

Bit fields displayed as gray boxes in the memory map view are categorized as read only bit fields and cannot be changed through the memory map view. Read only bit fields in the memory map view are all either read only bits of the AD4696 itself, or else control features of the AD4696 that are not supported by the AD4696 ACE plugin.

The bit field states shown in the memory map view are only written to the connected device when the **Apply Changes** button is clicked. When modifying a bit field in the memory map view or through a GUI control in the chip view, the memory map view of the affected bit field is displayed in bold typeface to signify the contents have been updated but that those contents have not been written to the connected device.

The tabs on the left side of the memory map view provide navigation tools of the AD4696 memory map, including bit field search tools and sorting by functional groups.

The function of the buttons that appear at the top of the memory map view are described in this section. Some of these controls are included in the other views in the plugin as well.

Apply Changes

All registers contain the default values when powered up. Click **Apply Changes** to write to all registers.

Apply Selected

Click **Apply Selected** to write data only to selected registers. To select a register, click the desired register in the memory map view**.**

Read All

Click **Read All** to read all the registers on the connected AD4696.

All bit fields in the memory map view and all corresponding GUI controls in the plugin views are updated to reflect the current state of the connected AD4696.

Read Selected

Click **Read Selected** to read data only from selected registers on the connected AD4696. To select a register, click the desired register in the memory map view**.**

Only bit fields in the selected registers and their corresponding GUI controls in the plugin views are updated to reflect the state of the connected AD4696.

Reset Chip

Clicking **Reset Chip** causes the software to reset the AD4696 with a hardware reset (see the AD4696 data sheet for a description of hardware resets and other reset modalities of the AD4696).

Following the device reset, all bit fields in the memory map view and all corresponding GUI controls in the other plugin views are restored to their default states.

Diff

Click **Diff** to check for difference in register values between software and the connected AD4696. Clicking **Diff** performs a read of the full register map of the connected device and compares the bit field states to those reported in the memory map view.

Software Defaults

Click **Software Defaults** to update the bit fields in the memory map view to their default states.

Clicking **Software Defaults** only updates the bit field states in the AD4696 ACE plugin and does not apply any settings to the connected AD4696 device. To apply the software default memory map settings to the connected device, click **Software Defaults** and then click **Apply Changes** to write to the registers on the connected AD4696. Alternatively, click the **Reset Chip** button to reset the device and memory map view bit fields to their hardware default states defined in the AD4696 data sheet.

Export

Click the **Export** button to export the memory map view bit field contents to a comma delimited text file (.csv).

Chip View Side-By-Side

Clicking the **Chip View Side-By-Side** button displays the chip view in a window beside the memory map view. Displaying the chip view and memory map view side by side allows the user to observe which bit field and register settings in the AD4696 memory map correspond with the GUI controls in the chip view.

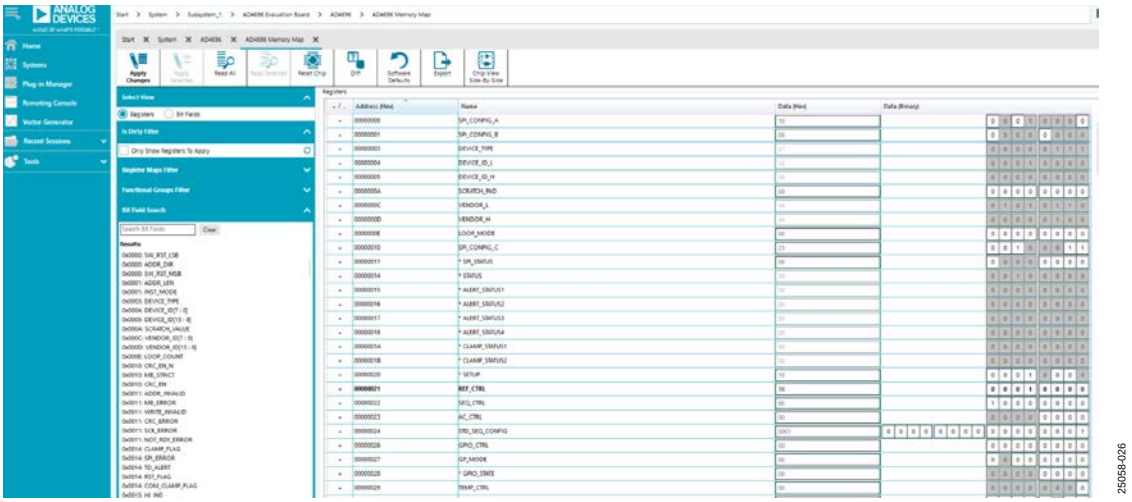

Figure 23. Memory Map View

EVALUATION BOARD SCHEMATICS AND ARTWORK

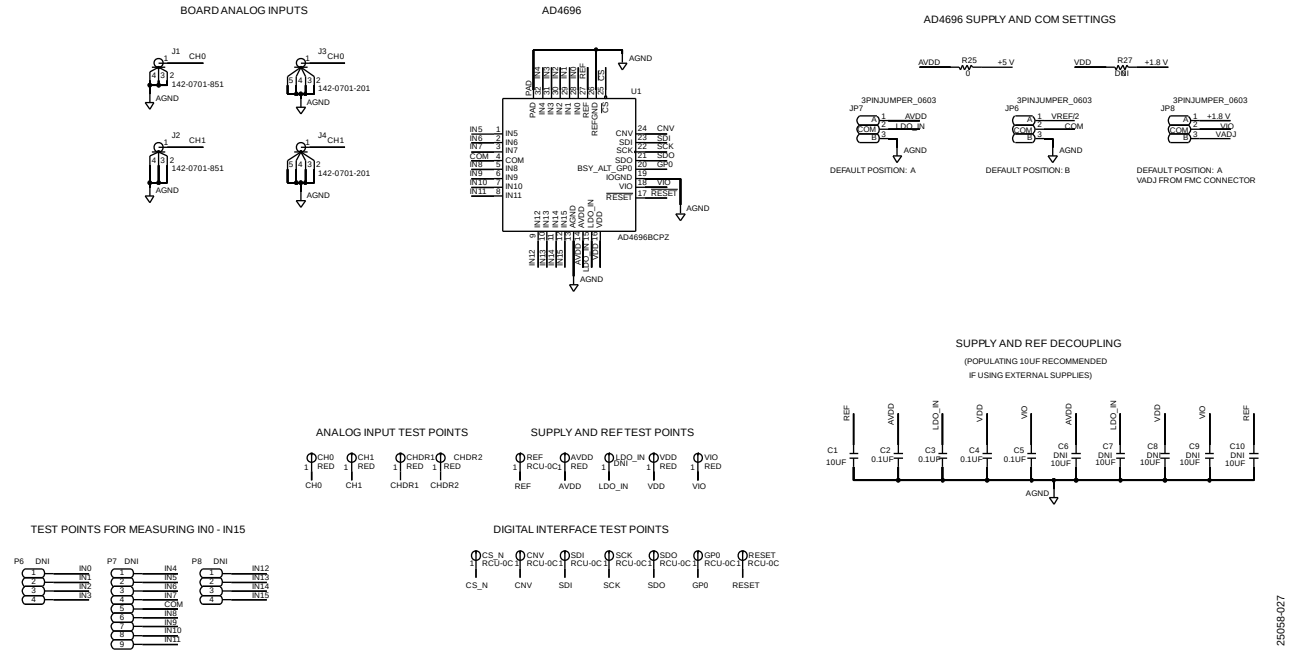

Figure 24. EVAL-AD4696FMCZ Top Level Schematic

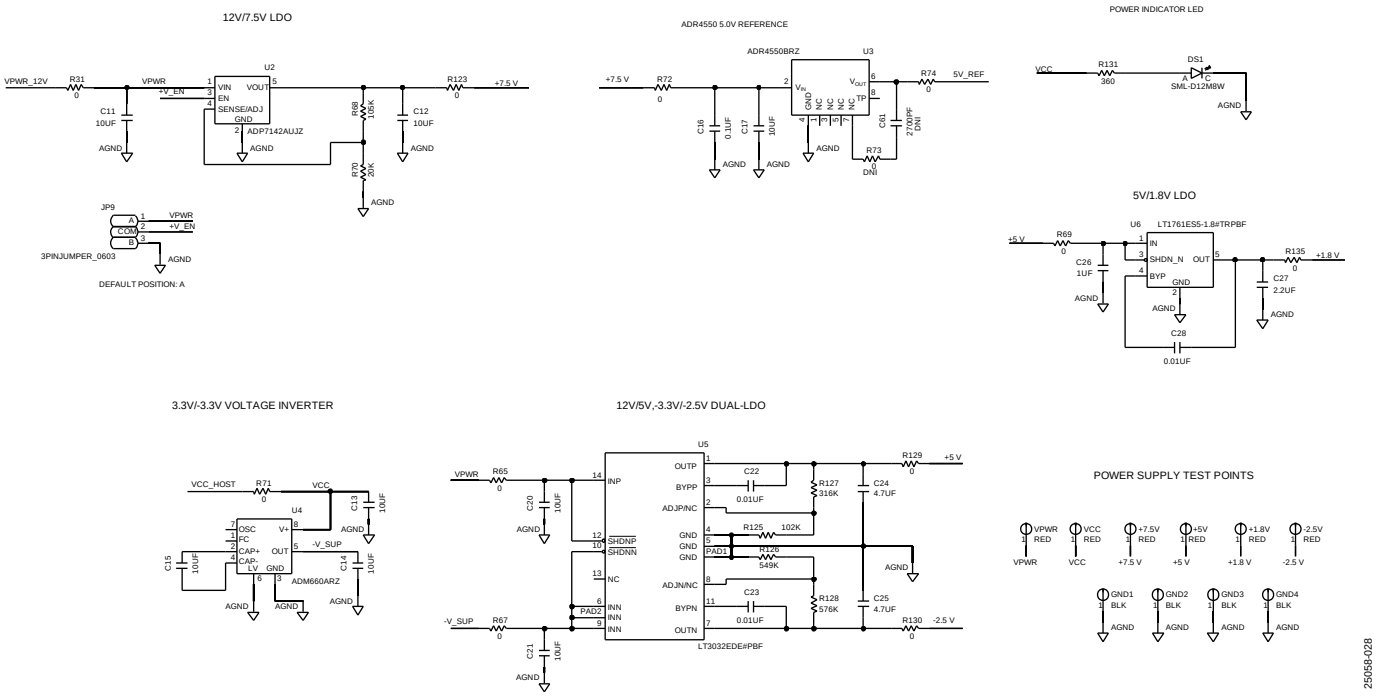

Figure 25. EVAL-AD4696FMCZ Power Management Schematic

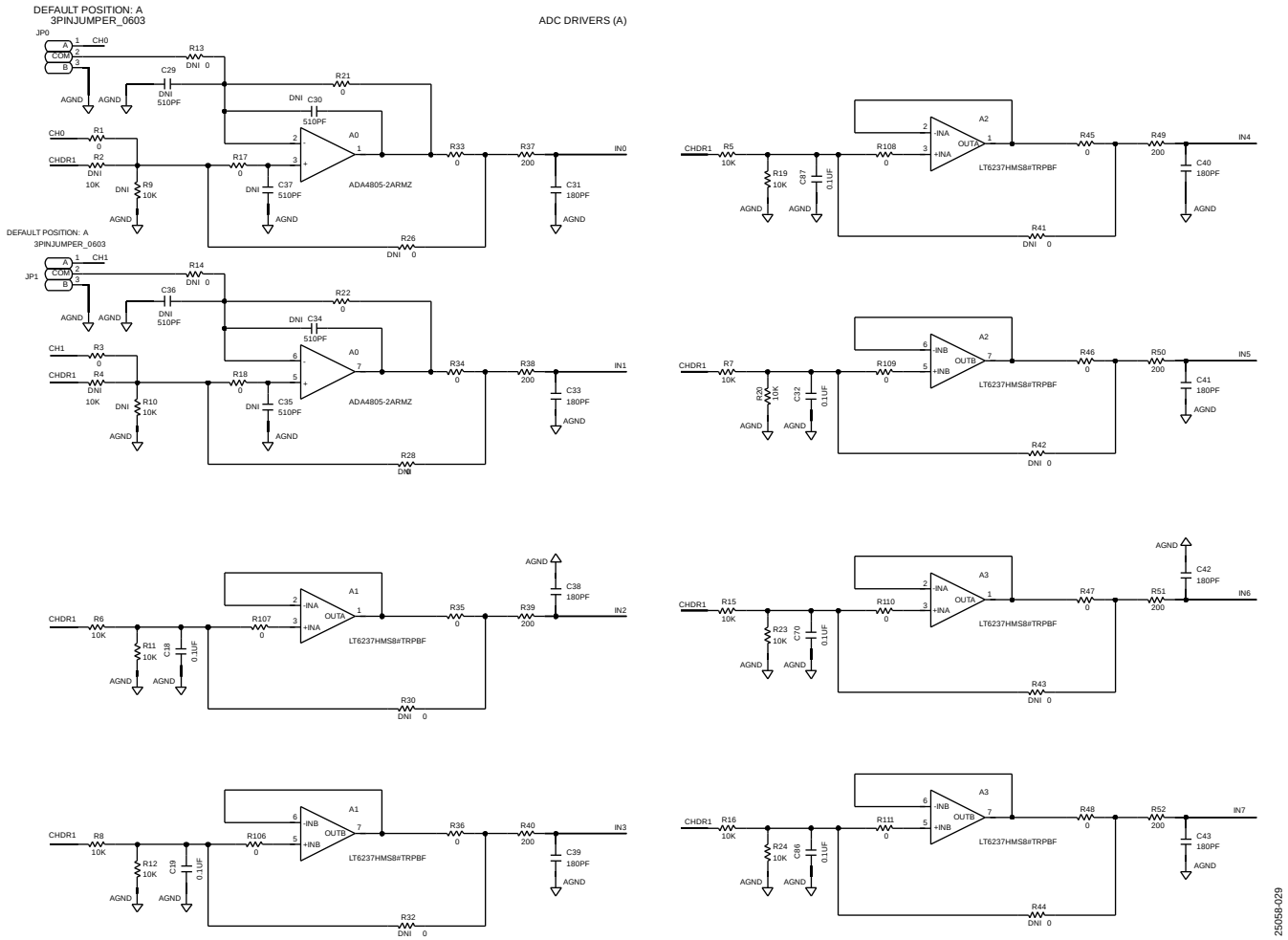

Figure 26. EVAL-AD4696FMCZ Driver Amplifier Schematic, IN0 to IN7

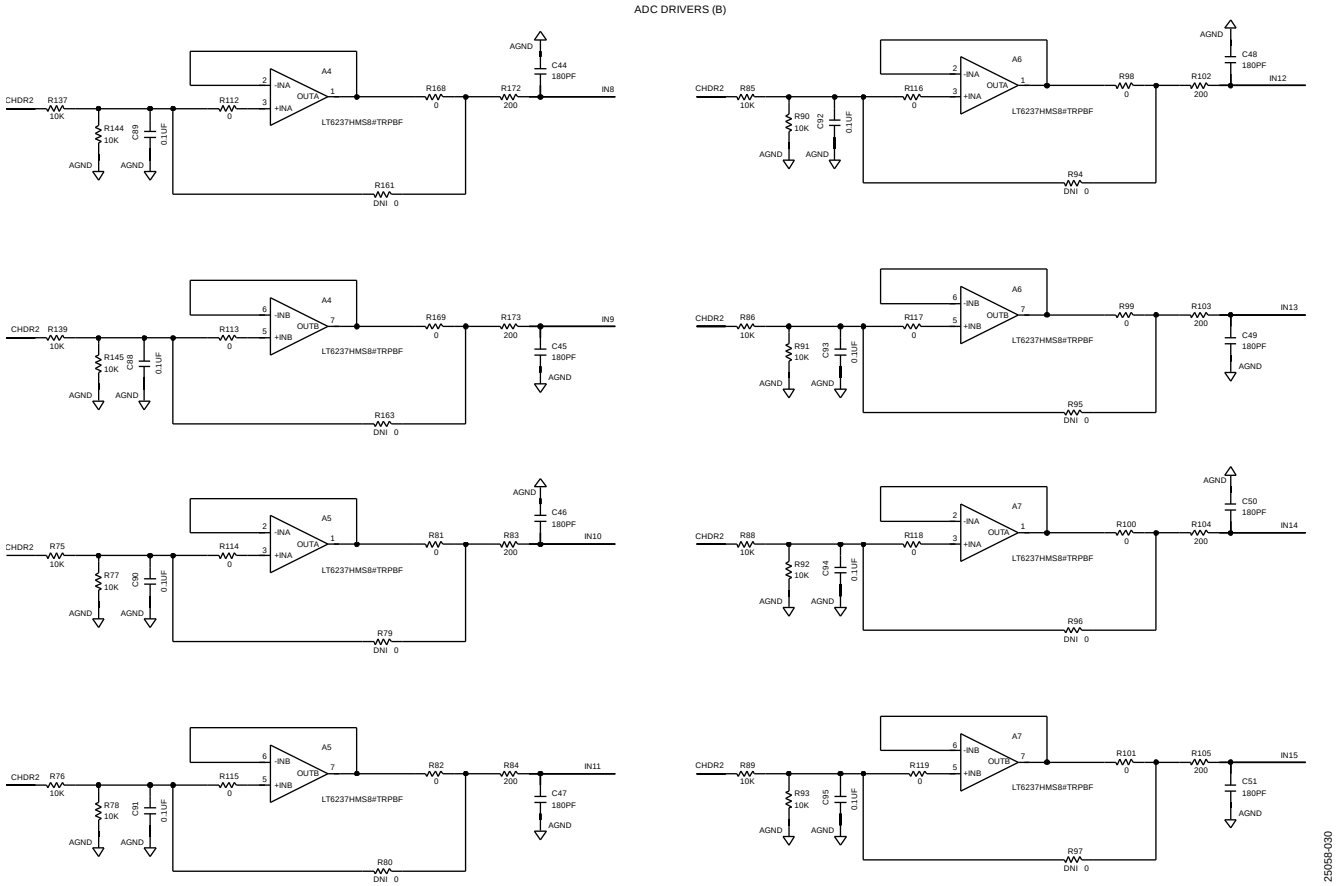

Figure 27. EVAL-AD4696FMCZ Driver Amplifier Schematic, IN8 to IN15

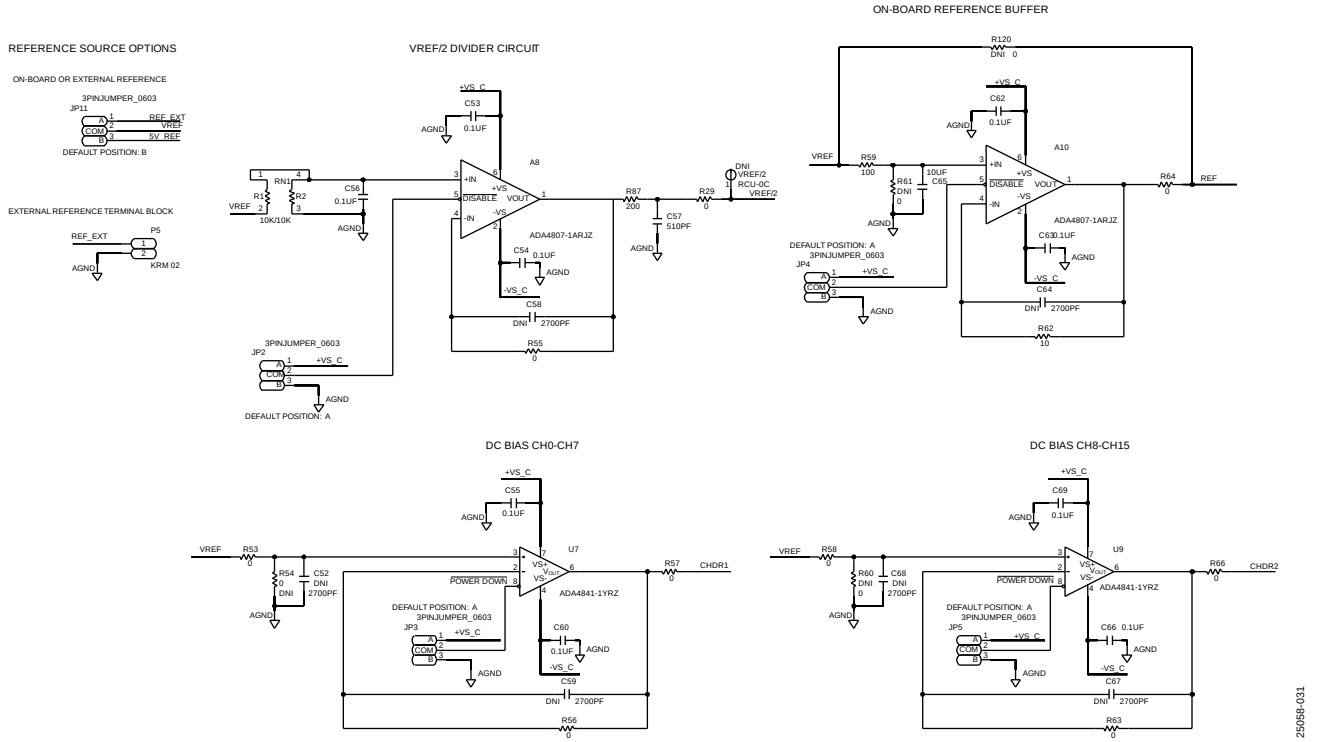

Figure 28. EVAL-AD4696FMCZ Buffer Schematic

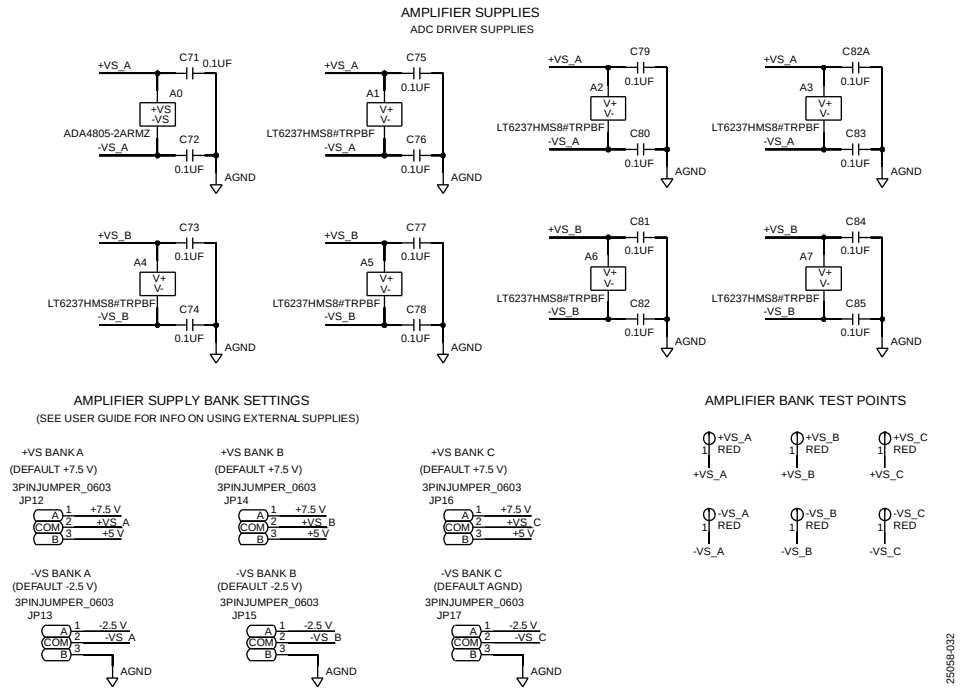

Figure 29. EVAL-AD4696FMCZ Amplifier Power Supply Jumper Selection Schematic

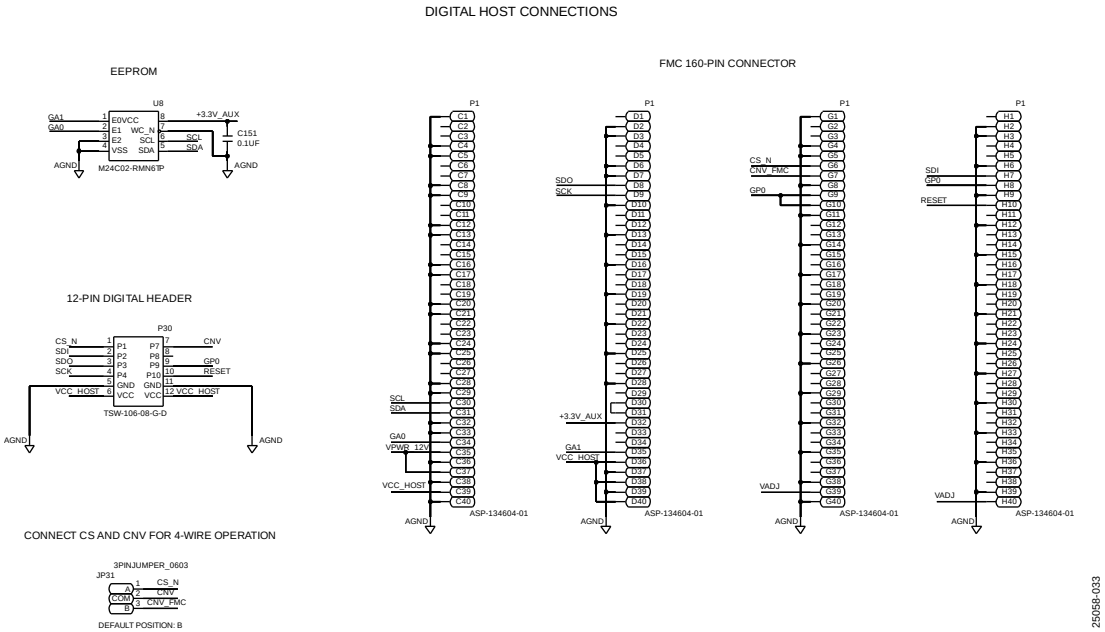

Figure 30. EVAL-AD4696FMCZ FMC Connector Schematic

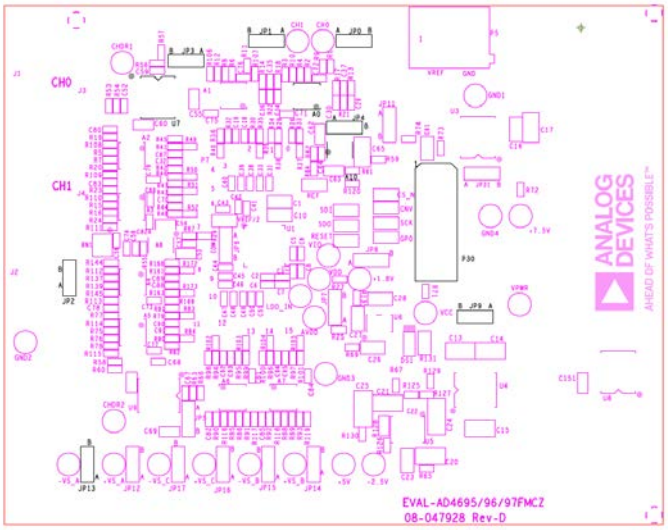

Figure 31. EVAL-AD4696FMCZ Silkscreen, Top Assembly

Figure 32. EVAL-AD4696FMCZ, Top Layer

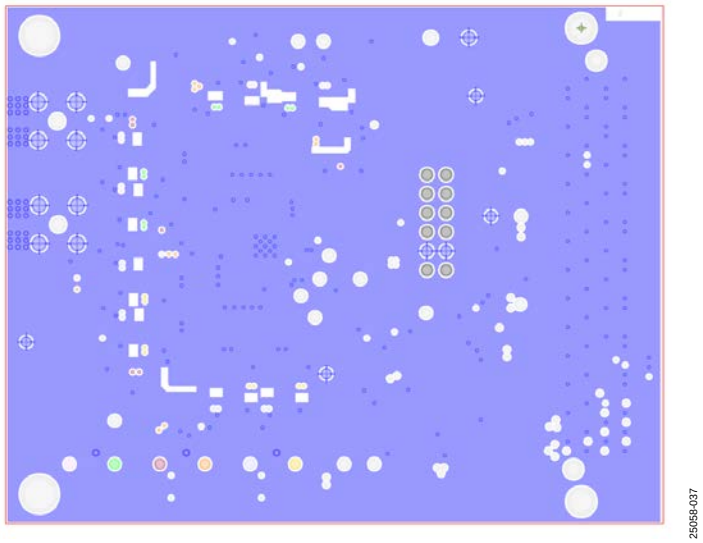

Figure 33. EVAL-AD4696FMCZ Layer 2, Ground

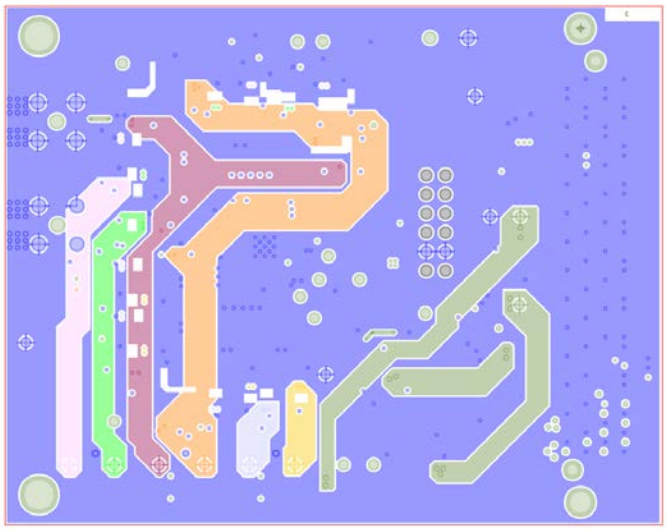

Figure 34. EVAL-AD4696FMCZ Layer 3, Power

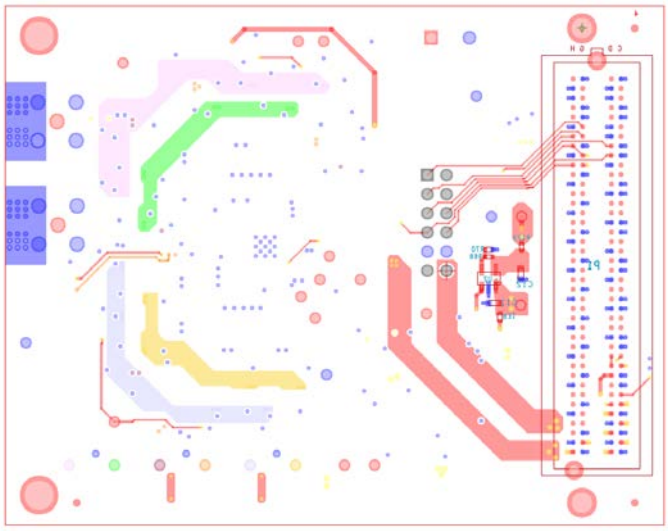

Figure 35. EVAL-AD4696FMCZ Bottom Layer

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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