

Power MOSFET

30 V, 3.2 A, Single N-Channel, SC-88

Features

- Offers an Low $R_{DS(on)}$ Solution in the SC-88 Package
- Low Profile (< 1.1 mm) Allows it to fit Easily into Extremely Thin Environments such as Portable Electronics
- Operates at Standard Logic Level Gate Drive
- Low Gate Charge
- This is a Pb-Free Device

Applications

- DC-DC Converters (Buck and Boost Circuit)
- Optimized for Battery Powered Portable Equipment such as, Cell Phones, PDAs, Media Players, etc.
- Load Management
- Battery Charging and OV IC Protection Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	I_D	2.6	A	
			1.9		
	$t \leq 1 \text{ s}$		3.2		
Power Dissipation (Note 1)	Steady State	P_D	0.62	W	
	$t \leq 1 \text{ s}$		0.95		
Continuous Drain Current (Note 2)	Steady State	I_D	1.8	A	
			1.3		
Power Dissipation (Note 2)		P_D	0.3		
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	10	A	
Operating Junction and Storage Temperature		$T_{J, STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	1.3	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in $[2 \text{ oz}]$ including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size.

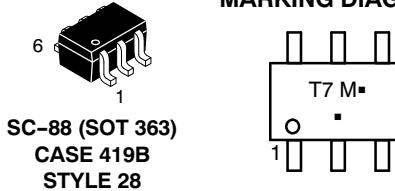


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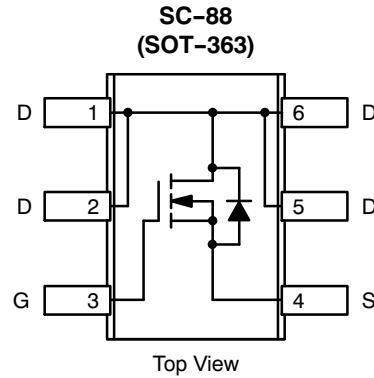
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
30 V	45 m Ω @ 10 V	
	65 m Ω @ 4.5 V	3.2 A

MARKING DIAGRAM



T7 = Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)



ORDERING INFORMATION

Device	Package	Shipping [†]
NTJS4160NT1G	SC-88 (Pb-Free)	3000 Units/Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	200	$^{\circ}\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 1 \text{ s}$ (Note 3)	$R_{\theta JA}$	132	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	420	

3. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}/T_J}$	$I_D = 250 \mu\text{A}$, ref to 25°C		20		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 24 \text{ V}$	$T_J = 25^{\circ}\text{C}$		1.0	μA
			$T_J = 125^{\circ}\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = +20 \text{ V}$			100	nA
		$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = -20 \text{ V}$			-200	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}$, $I_D = 250 \mu\text{A}$	0.8		2.4	V
Gate Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})/T_J}$			-5.0		$\text{mV}/^{\circ}\text{C}$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 2.6 \text{ A}$		45	60	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}$, $I_D = 2.2 \text{ A}$		65	85	
Forward Transconductance	g_{FS}	$V_{\text{GS}} = 5.0 \text{ V}$, $I_D = 3.0 \text{ A}$		4.2		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$, $V_{\text{DS}} = 10 \text{ V}$		230		pF
Output Capacitance	C_{OSS}			62		
Reverse Transfer Capacitance	C_{RSS}			39		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 4.5 \text{ V}$, $V_{\text{DS}} = 15 \text{ V}$, $I_D = 2.6 \text{ A}$		2.75		nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			0.37		
Gate-to-Source Charge	Q_{GS}			0.87		
Gate-to-Drain Charge	Q_{GD}			1.1		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	$V_{\text{GS}} = 4.5 \text{ V}$, $V_{\text{DD}} = 15 \text{ V}$, $I_D = 1.0 \text{ A}$, $R_G = 6.0 \Omega$		8.7	15	ns
Rise Time	t_r			7.2	13	
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$			10.9	19	
Fall Time	t_f			1.9	4.0	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 1.3 \text{ A}$	$T_J = 25^{\circ}\text{C}$		0.79	1.2	V
			$T_J = 125^{\circ}\text{C}$		0.67		
Reverse Recovery Time	t_{RR}	$V_{\text{GS}} = 0 \text{ V}$, $dI_S/dt = 100 \text{ A}/\mu\text{s}$, $I_S = 1.3 \text{ A}$			10.3		ns
Charge Time	T_a				7.2		
Discharge Time	T_b				3.1		
Reverse Recovery Charge	Q_{RR}				4.0		

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

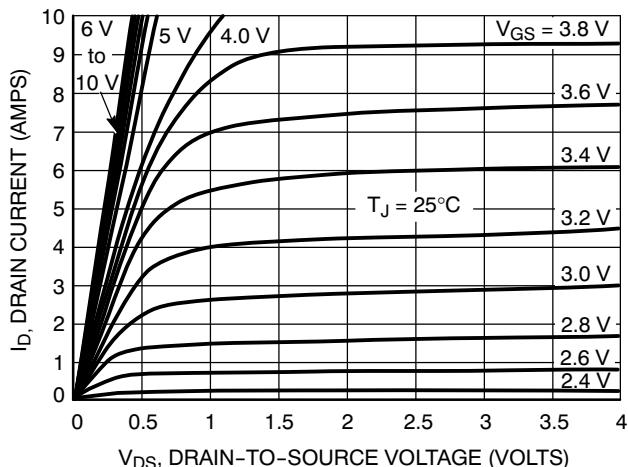


Figure 1. On-Region Characteristics

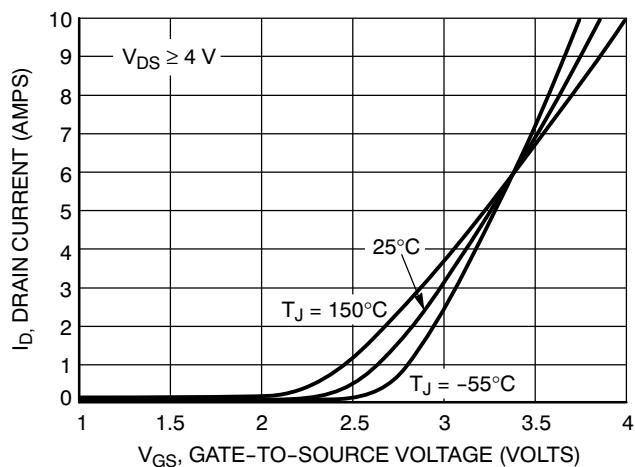


Figure 2. Transfer Characteristics

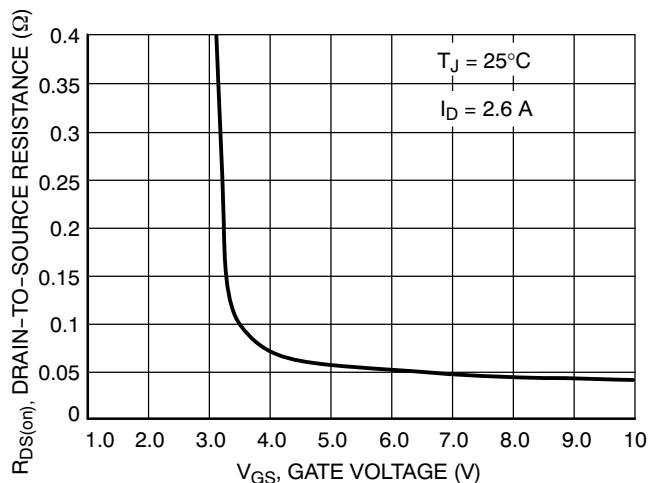


Figure 3. On-Resistance vs. Gate Voltage

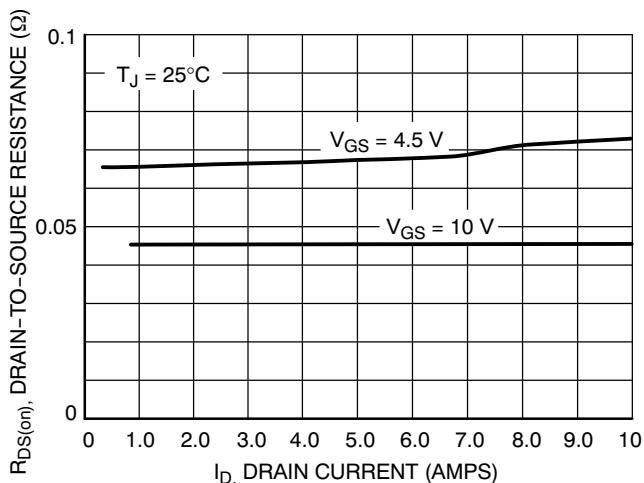


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

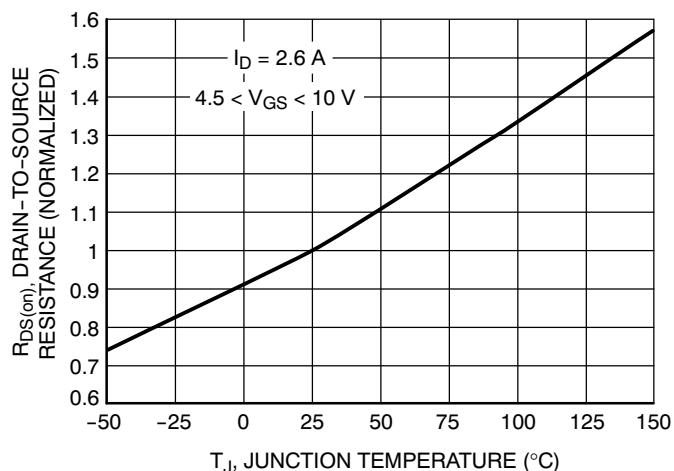


Figure 5. On-Resistance Variation with Temperature

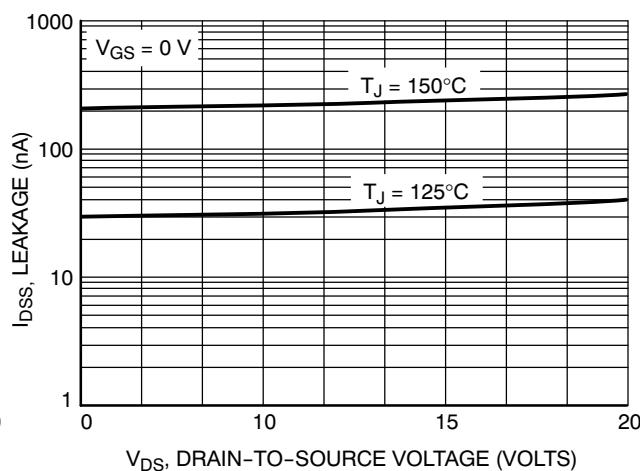


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTJS4160N

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

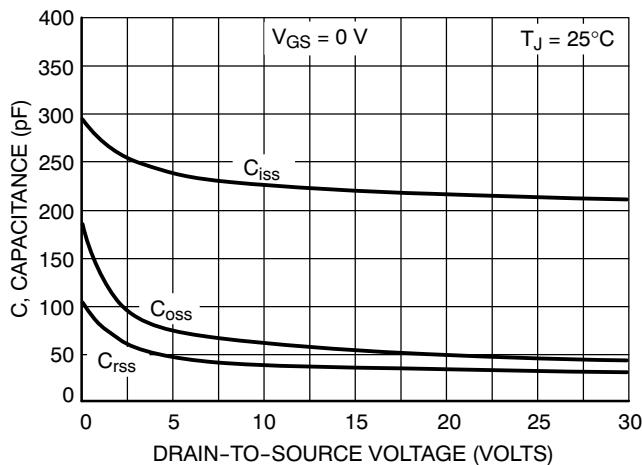


Figure 7. Capacitance Variation

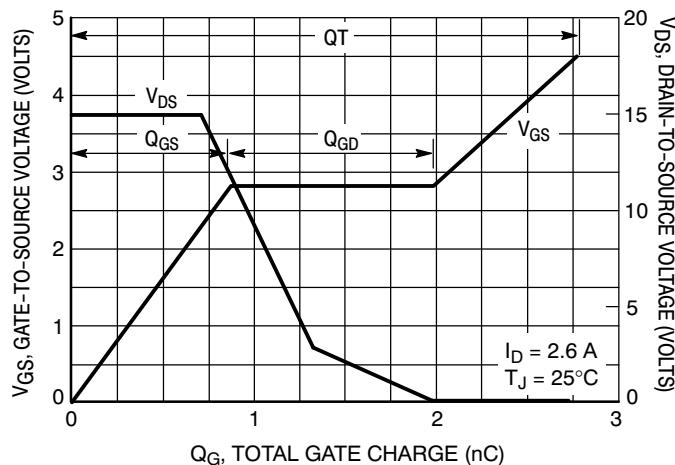


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

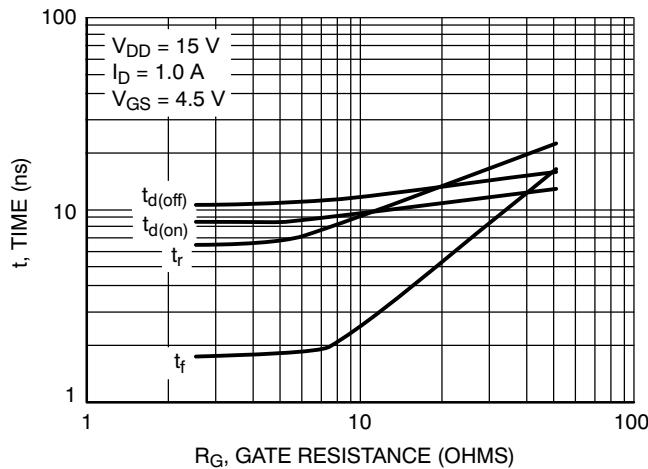


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

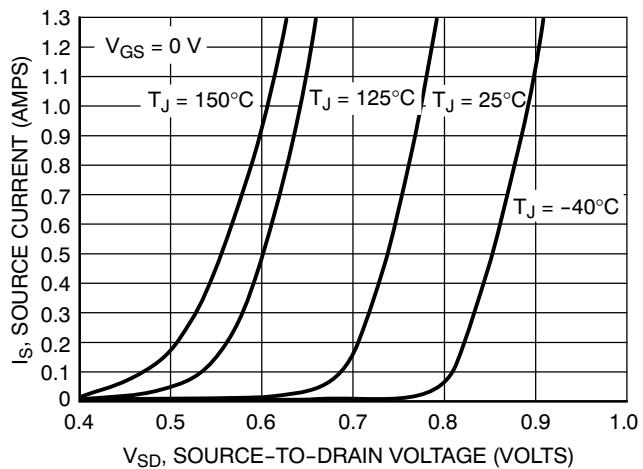


Figure 10. Diode Forward Voltage vs. Current

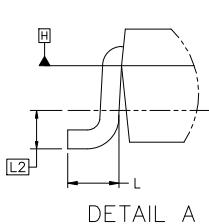
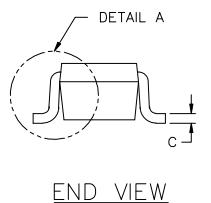
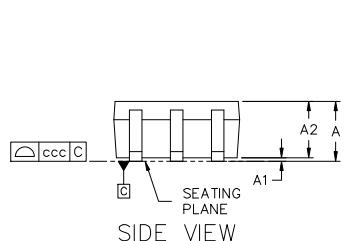
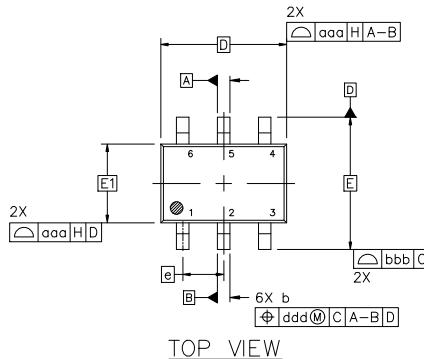


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

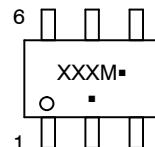
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUM A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00	BSC	
E	2.10	BSC	
E1	1.25	BSC	
e	0.65	BSC	
L	0.26	0.36	0.46
L2	0.15	BSC	
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code*

- = Date Code
- = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOI DFRM D.

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SC-88 2.00x1.25x0.90, 0.65P
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DATE 18 APR 2024

STYLE 1: PIN 1. Emitter 2 2. Base 2 3. Collector 1 4. Emitter 1 5. Base 1 6. Collector 2	STYLE 2: Cancelled	STYLE 3: Cancelled	STYLE 4: PIN 1. Cathode 2. Cathode 3. Collector 4. Emitter 5. Base 6. Anode	STYLE 5: PIN 1. Anode 2. Anode 3. Collector 4. Emitter 5. Base 6. Cathode	STYLE 6: PIN 1. Anode 2 2. N/C 3. Cathode 1 4. Anode 1 5. N/C 6. Cathode 2
STYLE 7: PIN 1. Source 2 2. Drain 2 3. Gate 1 4. Source 1 5. Drain 1 6. Gate 2	STYLE 8: Cancelled	STYLE 9: PIN 1. Emitter 2 2. Emitter 1 3. Collector 1 4. Base 1 5. Base 2 6. Collector 2	STYLE 10: PIN 1. Source 2 2. Source 1 3. Collector 1 4. Drain 1 5. Drain 2 6. Gate 2	STYLE 11: PIN 1. Cathode 2 2. Cathode 2 3. Anode 1 4. Cathode 1 5. Cathode 1 6. Anode 2	STYLE 12: PIN 1. Anode 2 2. Anode 2 3. Cathode 1 4. Anode 1 5. Anode 1 6. Cathode 2
STYLE 13: PIN 1. Anode 2. N/C 3. Collector 4. Emitter 5. Base 6. Cathode	STYLE 14: PIN 1. Vref 2. GND 3. GND 4. Iout 5. Ven 6. Vcc	STYLE 15: PIN 1. Anode 1 2. Anode 2 3. Anode 3 4. Cathode 3 5. Cathode 2 6. Cathode 1	STYLE 16: PIN 1. Base 1 2. Emitter 2 3. Collector 2 4. Base 2 5. Emitter 1 6. Collector 1	STYLE 17: PIN 1. Base 1 2. Emitter 1 3. Collector 2 4. Base 2 5. Emitter 2 6. Collector 1	STYLE 18: PIN 1. Vin1 2. Vcc 3. Vout2 4. Vin2 5. Gnd 6. Vout1
STYLE 19: PIN 1. Iout 2. Gnd 3. Gnd 4. Vcc 5. Ven 6. Vref	STYLE 20: PIN 1. Collector 2. Collector 3. Base 4. Emitter 5. Collector 6. Collector	STYLE 21: PIN 1. Anode 1 2. N/C 3. Anode 2 4. Cathode 2 5. N/C 6. Cathode 1	STYLE 22: PIN 1. D1 (l) 2. Gnd 3. D2 (l) 4. D2 (c) 5. Vbus 6. D1 (c)	STYLE 23: PIN 1. Vn 2. Ch1 3. Vp 4. N/C 5. Ch2 6. N/C	STYLE 24: PIN 1. Cathode 2. Anode 3. Cathode 4. Cathode 5. Cathode 6. Cathode
STYLE 25: PIN 1. Base 1 2. Cathode 3. Collector 2 4. Base 2 5. Emitter 6. Collector 1	STYLE 26: PIN 1. Source 1 2. Gate 1 3. Drain 2 4. Source 2 5. Gate 2 6. Drain 1	STYLE 27: PIN 1. Base 2 2. Base 1 3. Collector 1 4. Emitter 1 5. Emitter 2 6. Collector 2	STYLE 28: PIN 1. Drain 2. Drain 3. Gate 4. Source 5. Drain 6. Drain	STYLE 29: PIN 1. Anode 2. Anode 3. Collector 4. Emitter 5. Base/Anode 6. Cathode	STYLE 30: PIN 1. Source 1 2. Drain 2 3. Drain 2 4. Source 2 5. Gate 1 6. Drain 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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