NTJS4160N

Power MOSFET
30 V, 3.2 A, Single N–Channel, SC–88

Features

- Offers an Low $R_{DS(on)}$ Solution in the SC–88 Package
- Low Profile (< 1.1 mm) Allows it to fit Easily into Extremely Thin Environments such as Portable Electronics
- Operates at Standard Logic Level Gate Drive
- Low Gate Charge
- This is a Pb–Free Device

Applications

- DC–DC Converters (Buck and Boost Circuit)
- Optimized for Battery Powered Portable Equipment such as, Cell Phones, PDAs, Media Players, etc.
- Load Management
- Battery Charging and OV IC Protection Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25 °C	I_D	2.6	A
		T_A = 85 °C		1.9	
	t ≤ 1 s	T_A = 25 °C		3.2	
Power Dissipation (Note 1)	Steady State	T_A = 25 °C	P_D	0.62	W
	t ≤ 1 s			0.95	
Continuous Drain Current (Note 2)	Steady State	T_A = 25 °C	I_D	1.8	A
		T_A = 85 °C		1.3	
Power Dissipation (Note 2)		T_A = 25 °C	P_D	0.3	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	10	A
Operating Junction and Storage Temperature			T_J, T_{STG}	–55 to 150	°C
Source Current (Body Diode)			I_S	1.3	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
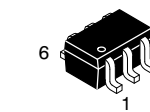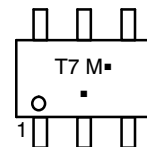2. Surface mounted on FR4 board using the minimum recommended pad size.

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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
30 V	45 mΩ @ 10 V	3.2 A
	65 mΩ @ 4.5 V	

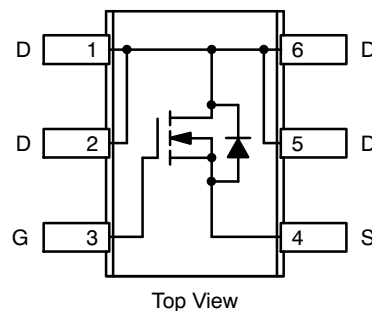**MARKING DIAGRAM**

SC–88 (SOT 363)
CASE 419B
STYLE 28

T7 M▪

T7 = Device Code
M = Date Code
▪ = Pb–Free Package
(Note: Microdot may be in either location)

SC–88 (SOT–363)

D	1		6	D
D	2		5	D
G	3		4	S

Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTJS4160NT1G	SC–88 (Pb–Free)	3000 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

March, 2008 – Rev. 1

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NTJS4160N

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 3)	$R_{\theta JA}$	200	°C/W
Junction–to–Ambient – t ≤ 1 s (Note 3)	$R_{\theta JA}$	132	
Junction–to–Ambient – Steady State (Note 4)	$R_{\theta JA}$	420	

3. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			20		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V				100	nA
		V_{DS} = 0 V, V_{GS} = –20 V				–200	
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.8		2.4	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				–5.0		mV/°C
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.6 A			45	60	mΩ
		V_{GS} = 4.5 V, I_D = 2.2 A			65	85	
Forward Transconductance	g_{FS}	V_{GS} = 5.0 V, I_D = 3.0 A			4.2		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 10 V			230		pF
Output Capacitance	C_{OSS}				62		
Reverse Transfer Capacitance	C_{RSS}				39		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 2.6 A			2.75		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.37		
Gate–to–Source Charge	Q_{GS}				0.87		
Gate–to–Drain Charge	Q_{GD}				1.1		
SWITCHING CHARACTERISTICS (Note 6)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 15 V, I_D = 1.0 A, R_G = 6.0 Ω			8.7	15	ns
Rise Time	t_r				7.2	13	
Turn–Off Delay Time	$t_{d(OFF)}$				10.9	19	
Fall Time	t_f				1.9	4.0	
DRAIN–SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1.3 A	T_J = 25°C		0.79	1.2	V
			T_J = 125°C		0.67		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 1.3 A			10.3		ns
Charge Time	T_a				7.2		
Discharge Time	T_b				3.1		
Reverse Recovery Charge	Q_{RR}				4.0		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)
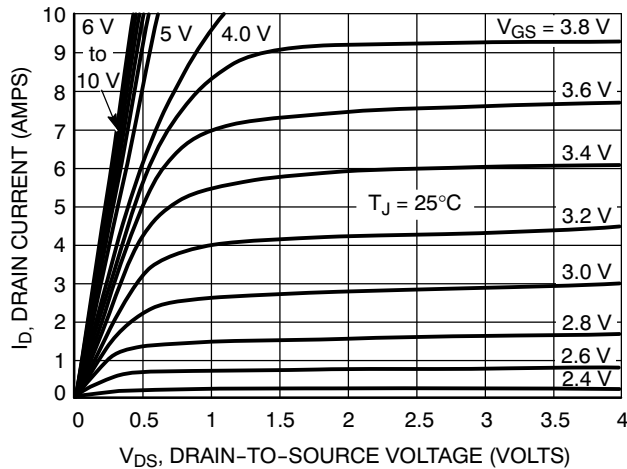

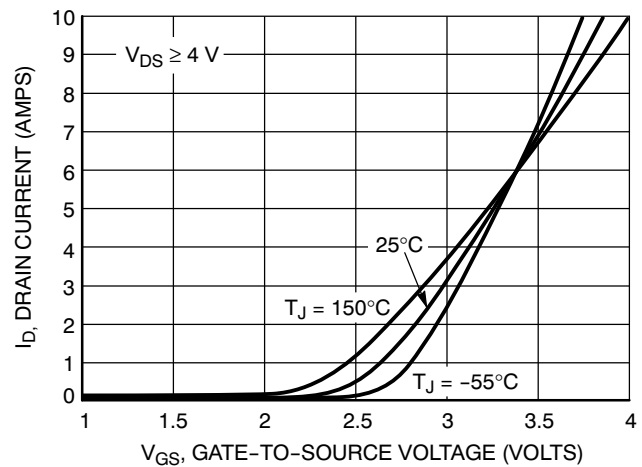Figure 1. On−Region Characteristics
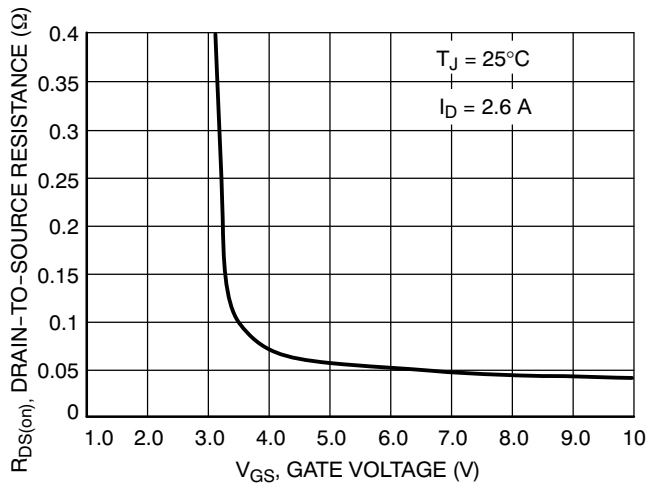

Figure 2. Transfer Characteristics

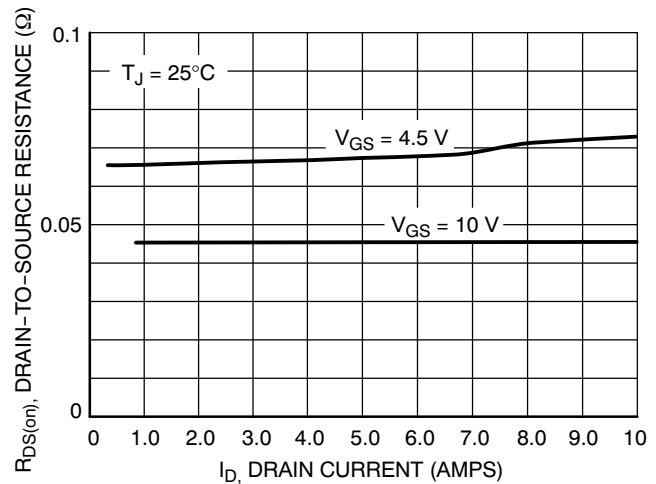Figure 3. On−Resistance vs. Gate Voltage

Figure 4. On−Resistance vs. Drain Current and Gate Voltage
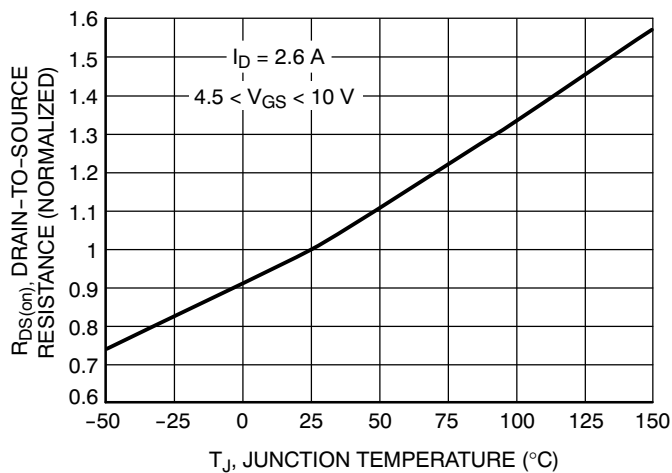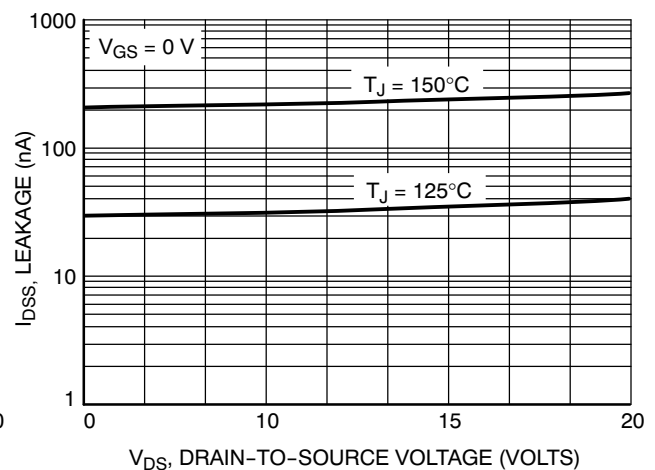

Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage

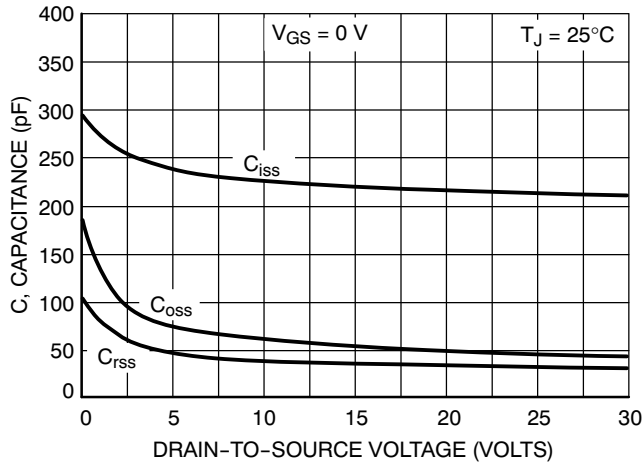**TYPICAL PERFORMANCE CURVES** (T_J = 25°C unless otherwise noted)
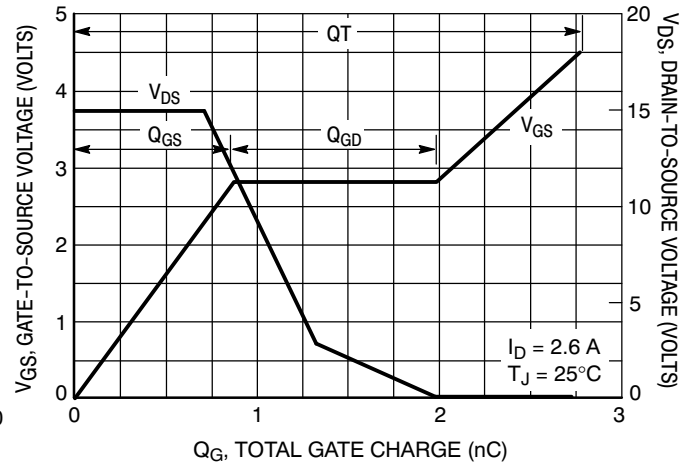

Figure 7. Capacitance Variation

Figure 8. Gate−to−Source and
Drain−to−Source Voltage vs. Total Charge
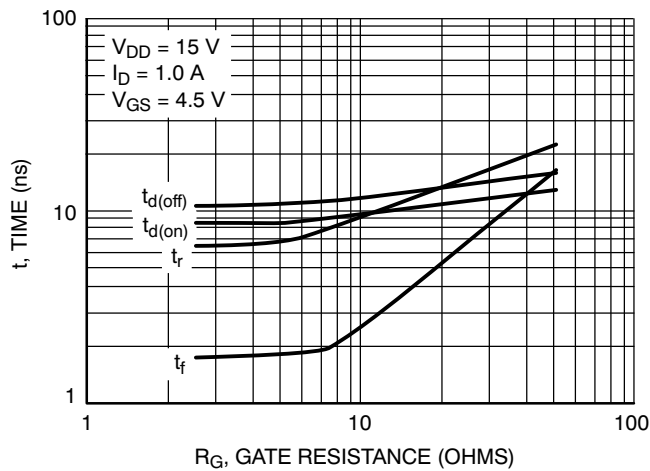
Figure 9. Resistive Switching Time Variation
vs. Gate Resistance
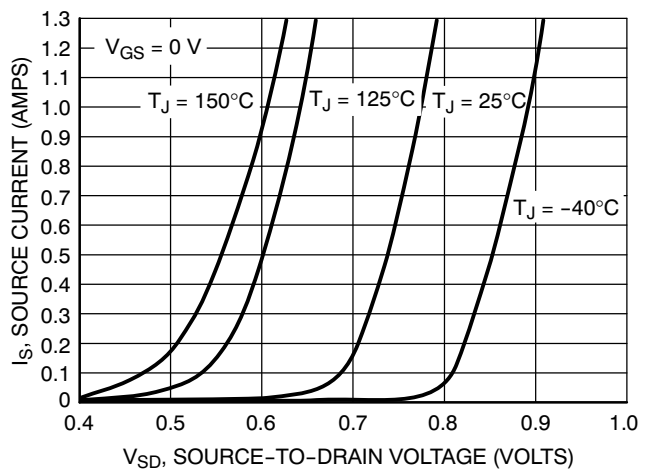
Figure 10. Diode Forward Voltage vs. Current

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

TOP VIEW

SIDE VIEW

DETAIL A

END VIEW

DETAIL A
SCALE 2:1
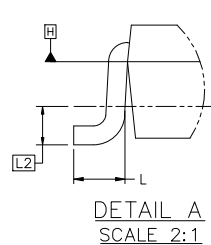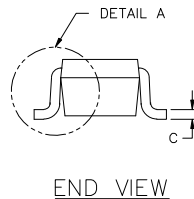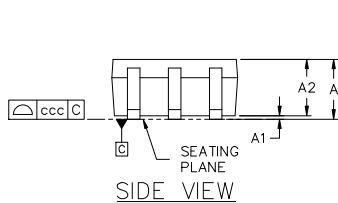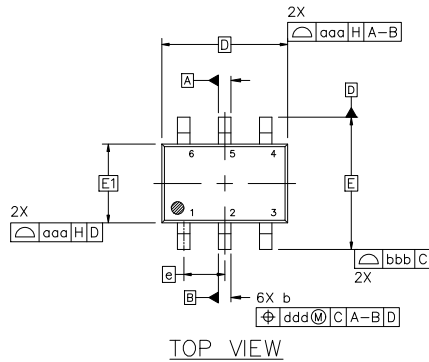
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	–––	–––	1.10
A1	0.00	–––	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

6X 0.30
6X 0.66
2.50
0.65 PITCH
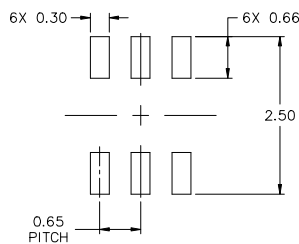
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

6

XXXM▪

1
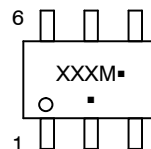
XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88 2.00x1.25x0.90, 0.65P		PAGE 1 OF 2

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for
style callout. If style type is not called
out in the datasheet refer to the device
datasheet pinout or pin assignment.

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DESCRIPTION:	SC−88 2.00x1.25x0.90, 0.65P		PAGE 2 OF 2

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