MC33364

Critical Conduction GreenLine™ SMPS Controller

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Integration of the high voltage startup saves approximately 0.7 W of power compared to the value of the resistor bootstrapped circuits.

Each MC33364 features an on−board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, a CMOS driver and cycle−by−cycle current limiting.

The MC33364D1 has an internal 126 kHz frequency clamp. The MC33364D2 is available without an internal frequency clamp. The MC33364D has an internal 126 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance.

Features

- Lossless Off−Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Operating Temperature Range −25°C to +125°C
- Shutdown Capability
- Over Temperature Protection
- Optional/Adjustable Frequency Clamp to Limit EMI
- This is a Pb−Free and Halide−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
MC33364D1G	SO−8 (Pb−Free)	96 Units / Rail
MC33364D1R2G		2500 Units / Tape & Reel
MC33364D2G		96 Units / Rail
MC33364D2R2G		2500 Units / Tape & Reel
MC33364DG	SO−16 (Pb−Free)	48 Units / Rail
MC33364DR2G		2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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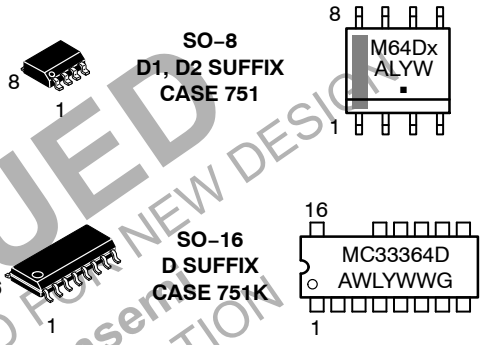
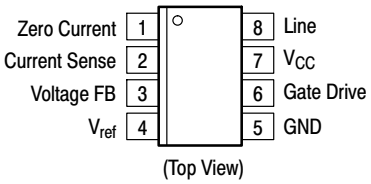
MARKING DIAGRAMS



x = 1 or 2
A = Assembly Location
WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

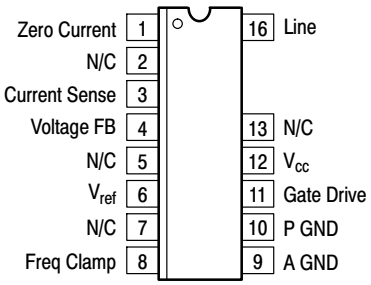
PIN CONNECTIONS

MC33364D1
MC33364D2



(Top View)

MC33364D



(Top View)

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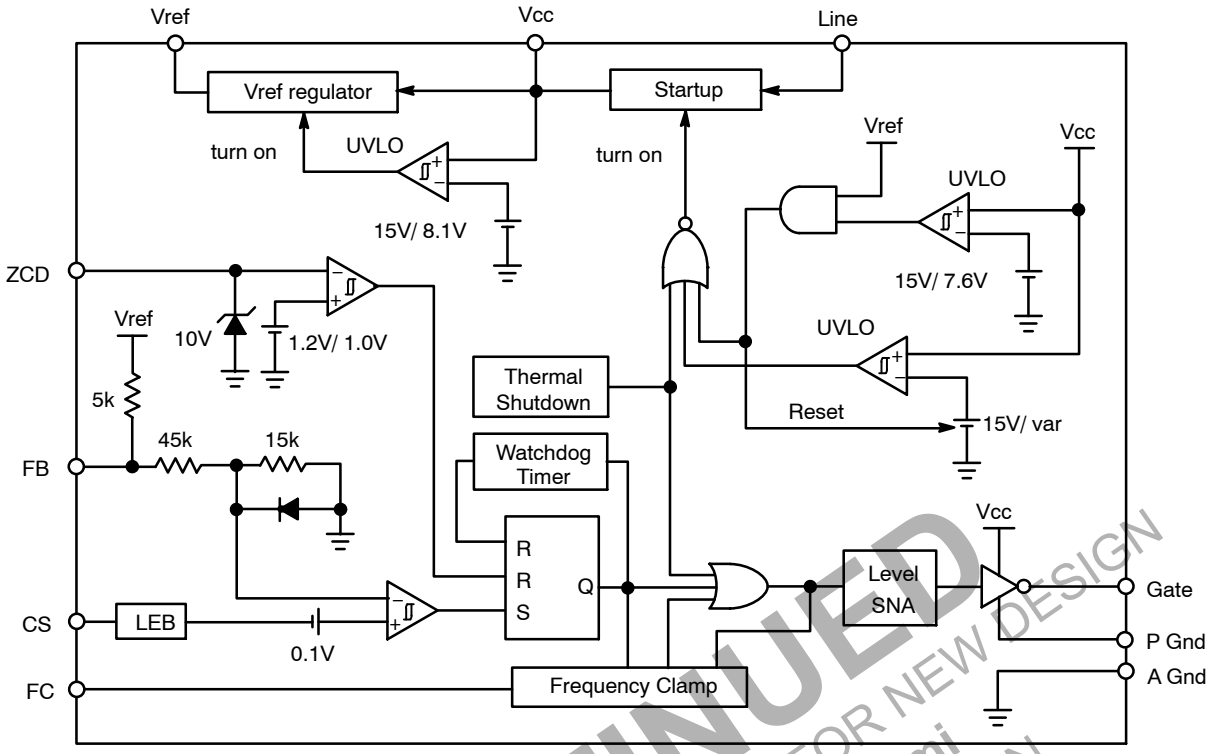

Figure 1. Representative Block Diagram

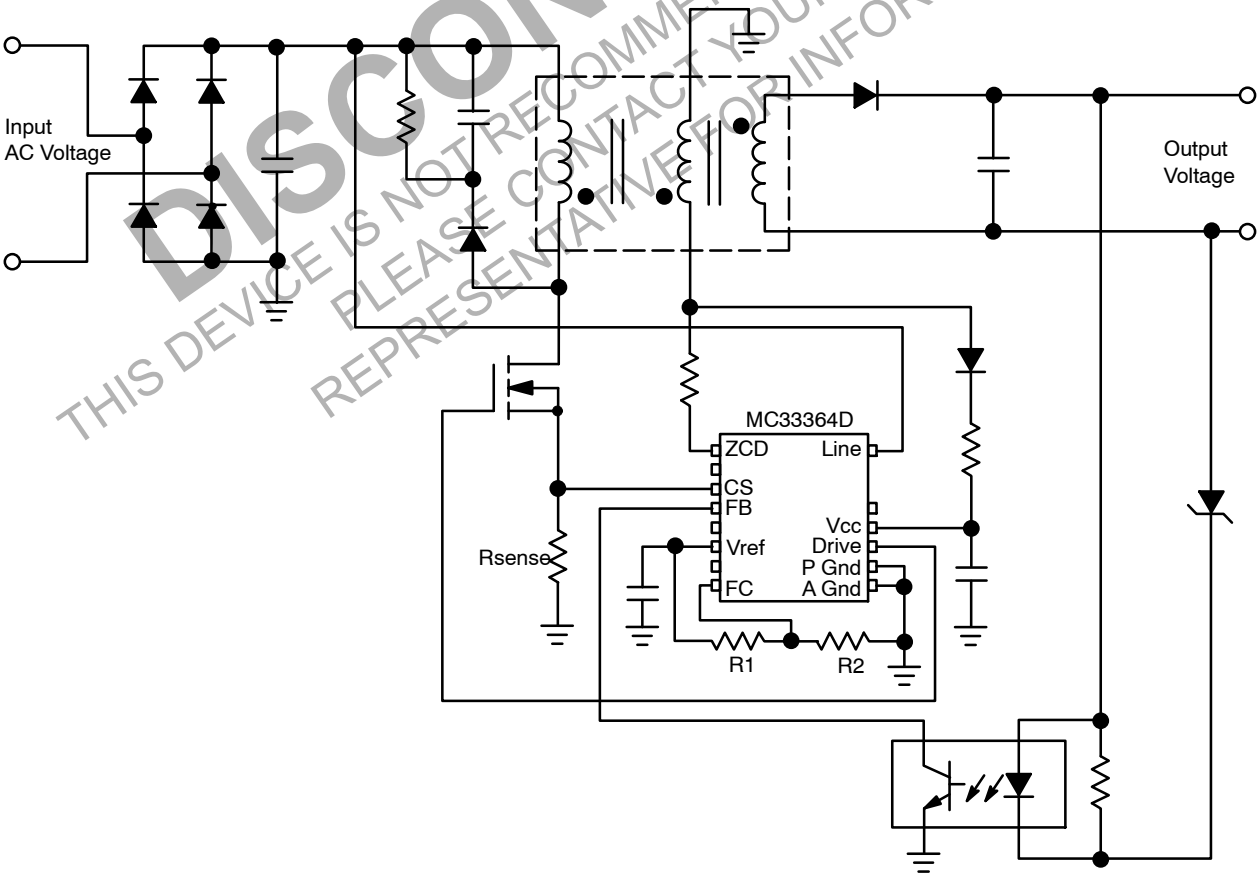

Figure 2. Typical Application Circuit

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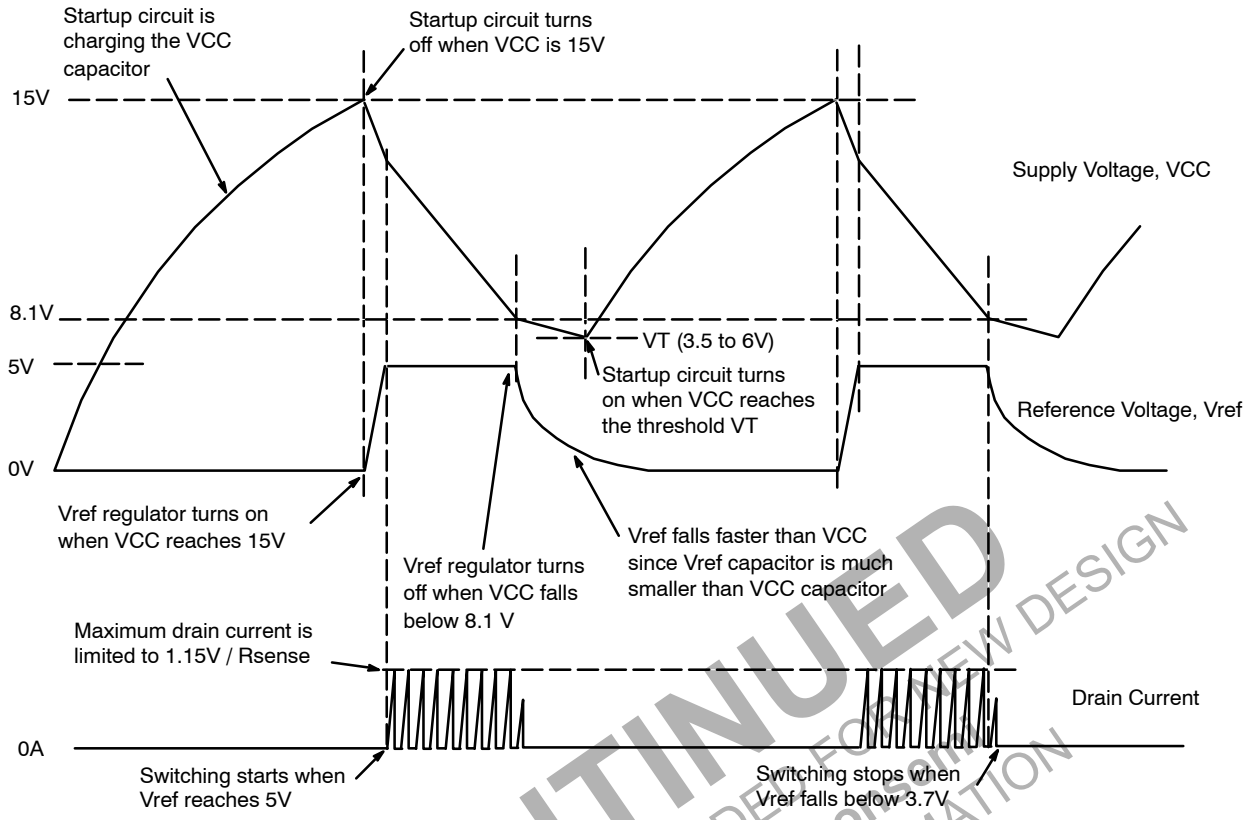

Figure 3. Timing Diagram in Fault Condition

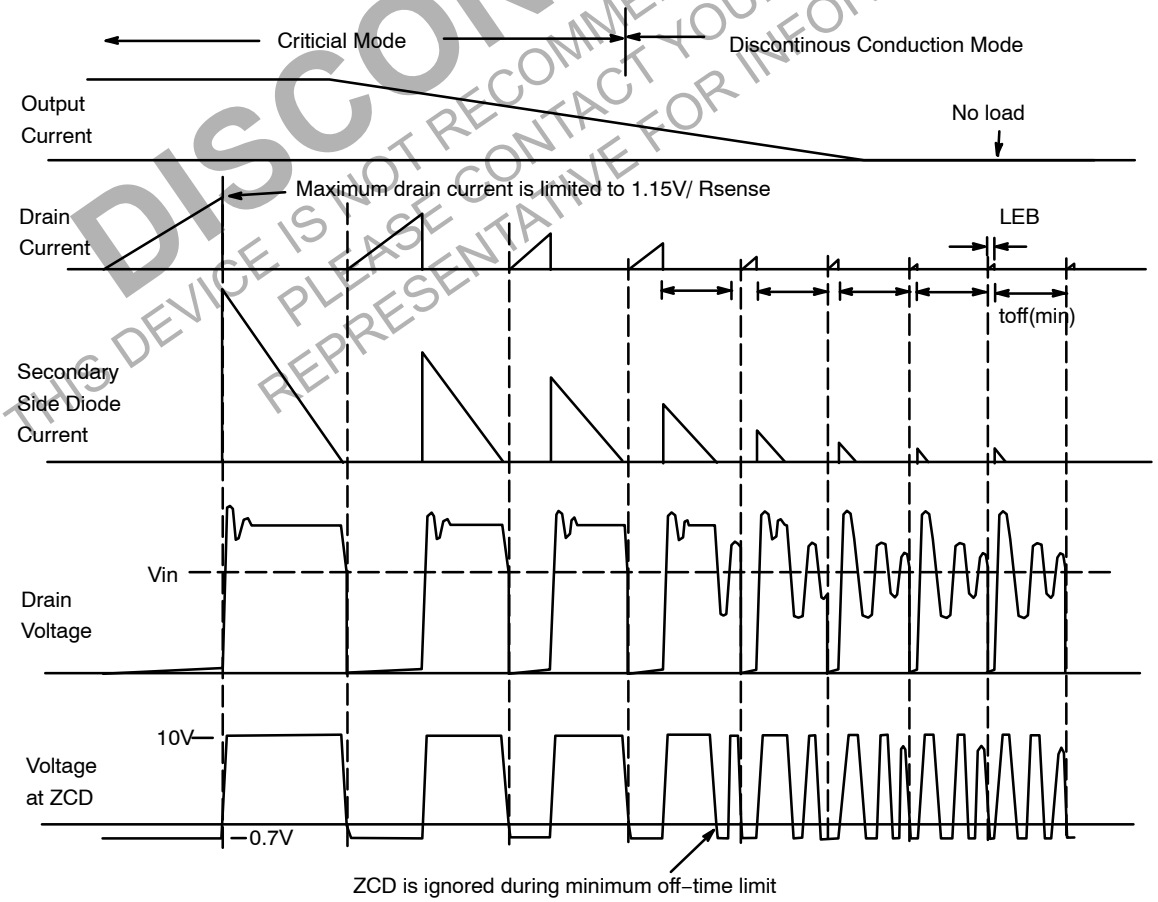

Figure 4. Timing Diagram in Normal Condition

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PIN DESCRIPTION

Pin	Function	Description
1 (1)	Zero Current Detect	The ZCD Pin ensures critical conduction mode. ZCD monitors the voltage on the auxiliary winding, during the demagnetization phase of the transformer, comparing it to an internal reference. The ZCD sets the latch for the output driver.
3 (2)	Current Sense	The Current Sense Pin monitors the current in the power switch by measuring the voltage across a resistor. Leading Edge Blanking is utilized to prevent false triggering. The voltage is compared to a resistor divider connected to the Voltage Feedback Pin. A 110 mV voltage off−set is applied to compensate the natural optocoupler saturation voltage.
4 (3)	Voltage Feedback	The Voltage Feedback Pin is typically connected to the collector of the optocoupler for feedback from the isolated secondary output. The Feedback is connected to the V_{ref} Pin via a 5 k resistor providing bias for the external optocoupler.
6 (4)	V_{ref}	The V_{ref} Pin is a buffered internal 5.0 V reference with Undervoltage Lockout.
8 (NA)	Frequency Clamp	The Frequency Clamp Pin ensures a minimum off−time value, typically 6.9 μs. It prevents the MOSFET from restarting within a fixed (33364D1) or adjustable (33364D) delay. The minimum off−time is disabled in the 33364D2. Therefore the maximum switching frequency cannot exceed $1/(T_{ON} + T_{OFFmin})$.
9 (5)	A GND	This pin is the ground for the internal circuitry excluding the gate drive stage.
10 (5)	P GND	This pin is the ground for the gate drive stage.
11 (6)	Gate Drive	The gate drive is the output to drive the gate of the power MOSFET.
12 (7)	V_{CC}	Provides the voltage for all internal circuitry including the gate drive stage and V_{ref}. This pin has Undervoltage Lockout with hysteresis.
16 (8)	Line	The Line Pin provides the initial power to the V_{CC} pins. Internally the line pin is a high voltage current source, eliminating the need for an external startup network.

NOTE: For further information please refer to the following Application Notes;
AN1594: Critical Conduction Mode, Flyback Switching Power Supply Using the MC33364.
AN1681: How to keep a Flyback Switch−Mode Power Supply Stable with a Critical−Mode Controller.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	700	V
Current Sense, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	−1.0 to +10	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics			
D1 and D2 Suffix, Plastic Package Case 751			
Maximum Power Dissipation @ T_A = 70°C	P_D	450	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	178	°C/W
D Suffix, Plastic Package Case 751B−05			
Maximum Power Dissipation @ T_A = 70°C	P_D	550	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	145	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	−25 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: ESD data available upon request.

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ELECTRICAL CHARACTERISTICS (V_{CC} = 15.5 V, for typical values T_A = 25°C, for min/max values T_J = −25 to 125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REFERENCE					
Reference Output Voltage (I_{Out} = 0 mA, T_J = 25°C)	V_{ref}	4.90	5.05	5.20	V
Line Regulation (V_{CC} = 10 V to 20 V)	Reg_{line}	–	2.0	50	mV
Load Regulation (I_{Out} = 0 mA to 5.0 mA)	Reg_{load}	–	0.3	50	mV
Maximum V_{ref} Output Current	I_O	–	5	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Decreasing)	V_{th}	0.9	1.0	1.1	V
Hysteresis (V_{in} Decreasing)	V_H	–	200	–	mV
Input Clamp Voltage – High State (I_{DET} = 3.0 mA) – Low State (I_{DET} = −3.0 mA)	V_{IH} V_{IL}	9.0 −1.1	10.33 −0.75	12 0.5	V
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	−0.5	0.02	0.5	μA
Built In Offset	V_{IO}	50	108	170	mV
Feedback Pin Input Range	V_{FB}	1.1	1.24	1.4	V
Feedback Pin to Output Delay	t_{DLY}	100	232	400	ns
DRIVE OUTPUT					
Source Resistance (Drive = 0 V, V_{Gate} = V_{CC} – 1.0 V) Sink Resistance (Drive = V_{CC}, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	10 5	36 11	70 25	Ω Ω
Output Voltage Rise Time (25% – 75%) (C_L = 1.0 nF)	t_r	–	67	150	ns
Output Voltage Fall Time (75% – 25%) (C_L = 1.0 nF)	t_f	–	28	50	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	–	0.01	0.03	V
LEADING EDGE BLANKING					
Delay to Current Sense Comparator Input (V_{FB} = 2.0 V, V_{CS} = 0 V to 4.0 V step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	–	250	–	ns
THERMAL SHUTDOWN					
Shutdown (Junction Temperature Increasing) Hysteresis (Junction Temperature Decreasing)	T_{sd} T_H	– –	180 50	– –	°C
TIMER					
Watchdog Timer	t_{DLY}	200	360	700	μs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	14	15	16	V
Minimum Operating Voltage After Turn−On (V_{CC} Decreasing)	$V_{Shutdown}$	6.5	7.6	8.5	V
FREQUENCY CLAMP					
Internal FC Function (pin open)	f_{max}	104	126	145	kHz
Internal FC Function (pin grounded)	f_{max}	400	564	800	kHz
Frequency Clamp Input Threshold	$V_{th(FC)}$	1.89	1.95	2.01	V
Frequency Clamp Control Current Range (Sink)	$I_{Control}$	30	70	110	μA
Dead Time (FC pin = 1.7 V)	T_d	3.5	5.0	6.5	μs
TOTAL DEVICE					
Line Startup Current (V_{Line} = 50 V) (V_{CC} = $V_{th(on)}$ – 1.0 V) Restart Delay Time	I_{Line} t_{DLY}	5.0	8.5 100	12	mA ms
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	0.5	32	70	μA
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{Line}	6.0	10	12	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF)	I_{CC}	1.5	2.75	4.5	mA
V_{CC} Off State Consumption (V_{CC} = 11 V)	$I_{CC\ Off}$	300	544	800	μA

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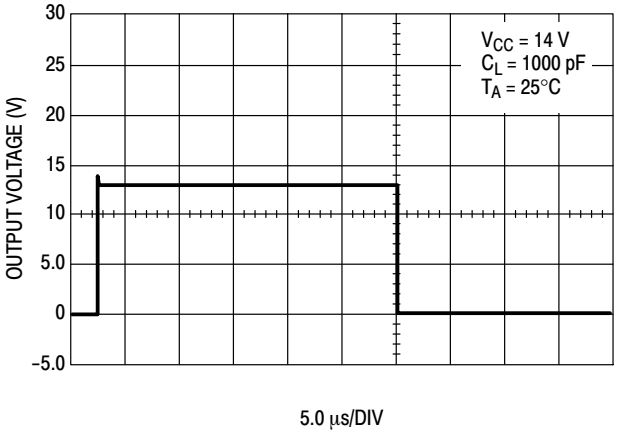

Figure 5. Drive Output Waveform

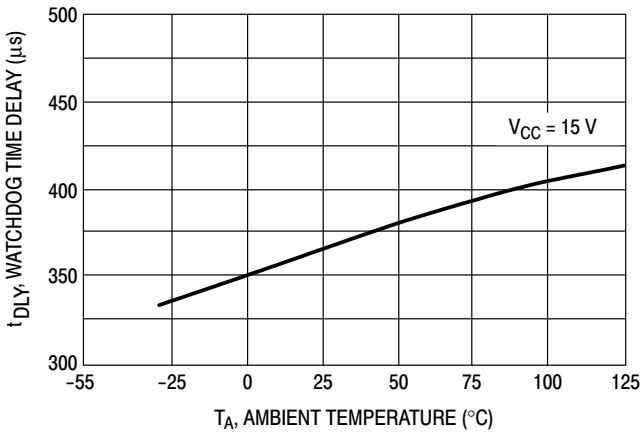

Figure 6. Watchdog Timer Delay versus Temperature

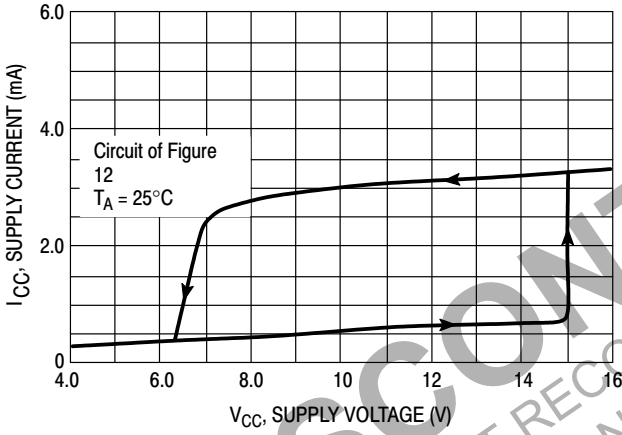

Figure 7. Supply Current versus Supply Voltage

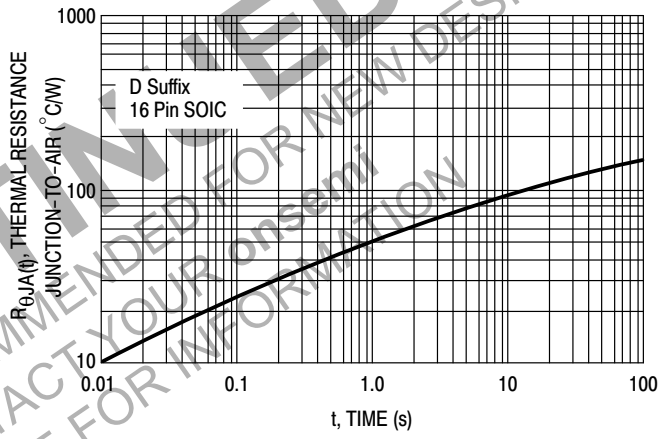

Figure 8. Transient Thermal Resistance

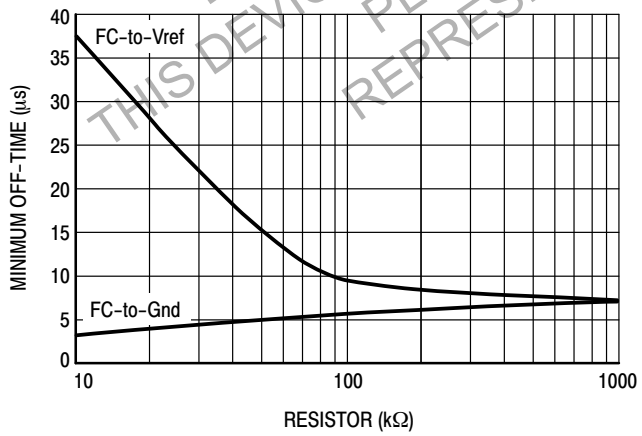

Figure 9. Minimum Off−time versus Timing Resistor on the FC Pin

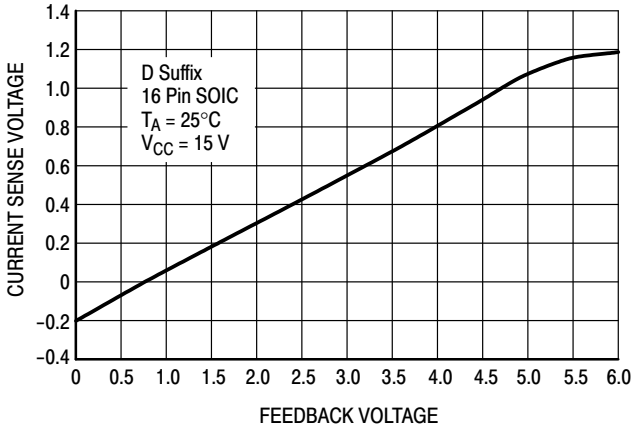

Figure 10. Feedback Voltage versus Current Sense Voltage

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OPERATING DESCRIPTION

Introduction

The MC33364 series represents a variable−frequency current−mode critical−conduction solution with integrated high voltage startup and protection circuitry to implement an off−line flyback converter for modern consumer electronic power supplies. Different frequency clamp options offer different customized needs. This device series includes an integrated 700 V Very High−Voltage (VHV) start−up circuit. Thus, it is possible to design an application with universal input voltage from 85 Vac to 265 Vac without any additional startup circuits or components.

The critical conduction feature offers some advantages. First, the MOSFET turns on at zero current and the diode turns off at zero current. The zero current reduces these turn−on and turn−off switching losses. It also reduces the Electro−Magnetic Interface (EMI) of the SMPS and a less expensive rectifier can be used. Second, by preventing the SMPS from entering the discontinuous conduction mode (DCM), the peak MOSFET drain current is limited to only twice the average input current. It needs a smaller and less expensive MOSFET. Third, by preventing the SMPS from entering the Continuous Conduction Mode (CCM), the flyback topology transfer function stays first−order and its feedback compensation network is considerably simplified. It also maximizes the power transfer by the flyback transformer to its 1/2 L I^2 limits.

A description of each of the functional blocks is given below. The representative block diagram and typical application circuit are in Figure 1 and Figure 2.

Line, V_{CC}, Startup Circuit and Reference Voltage

The Line pin is capable of a maximum 700 V so that it is possible to connect this pin directly to the rectified high−voltage Alternating Current (AC) input for minimizing the number of external components. There is a startup circuit block that regulates voltage from the Line pin to the V_{CC} pin in an abnormal situation. In normal conditions, the auxiliary winding powers up the V_{CC} and this startup circuit is opened and saves approximate 0.7 W of power compared to the resistor bootstrapped circuits.

In normal operation, the auxiliary winding powers up the V_{CC} voltage. This voltage is a constant value between the UVLO limits (7.6 V and 15 V). It is further regulated to a constant 5 V reference voltage V_{ref} for the internal circuitry usage. As long as the V_{CC} voltage is between 7.6 V and 15 V, it means the auxiliary winding can provide voltage as in normal condition. The device recognizes that there is no fault in the circuit and the device remains in the normal operation status.

However, when the auxiliary winding cannot power up V_{CC}, the V_{CC} voltage will reach its UVLO limit. The device recognizes that it is an abnormal situation (such as startup or output short−circuited). The V_{CC} voltage is not constant in this case. Figure 3 shows the timing diagram in a fault condition. There are three Under−Voltage Lock−Out (UVLO) thresholds with respect to V_{CC}. The upper threshold is 15 V. When this limit is reached, the startup circuit block turns off and V_{CC} declines due to power consumption of the circuitry. The startup circuit block turns on when V_{CC} reaches 7.6 V and if V_{ref} is higher than 3.7 V. It is the second threshold of V_{CC}. If V_{ref} is smaller than 3.7 V, the startup circuit will turn on when V_{CC} reaches a temperature dependent value V_T ranging between 3.5 V and 6 V. It is the last threshold of V_{CC}. This temperature dependent threshold is lower when temperature is higher so that it takes a longer time to restore the V_{CC}. It is a protection feature, which allows more dead time for cooling in high temperature condition.

There is an UVLO in the V_{ref} regulator block. When V_{CC} falls below typical 8.1 V in abnormal situation, the V_{ref} regulator block stops. V_{ref} and V_{CC} collapses due to power consumption of the circuitry. When V_{ref} collapses to below 3.7 V, the device cannot provide the Drive output and makes a dead time. This dead time is designed for minimal power transfer in the abnormal conditions. The dead time ends when V_{CC} reaches 15 V after reaching the UVLO limit V_T (3.5 to 6 V). Reaching V_T enables the startup circuit block, charging up the V_{CC} capacitor again. When V_{CC} reaches 15 V again, the V_{ref} regulator block turns on and allows the output to work again.

It is recommended to put a 0.1 uF capacitor on V_{ref} pin for stability of the voltage buffer. The V_{CC} capacitor is relatively larger than this 0.1 uF capacitor, making a longer V_{CC} charging time from V_T to 15 V and a longer dead time in the abnormal or fault conditions.

Zero Current Detect

To achieve critical conduction mode, MOSFET conduction is always initiated by sensing a zero current signal from the Zero Current Detect (ZCD) pin. The ZCD pin indirectly monitors the inductor current by sensing the auxiliary winding voltage. When the voltage falls below a threshold of 1.0V, the comparator resets the RS latch to turn the MOSFET on. There is 200 mV of hysteresis built into the comparator for noise immunity and to prevent false tripping. There are 10 V and 0.7 V clamps in the ZCD pin for protection. An external resistor is recommended to limit the input current to 2 mA to protect the clamps.

Watchdog Timer

A watchdog timer block is added to the device to start or restart the Drive output when something goes wrong in the ZCD. When the inductor current reaches zero for longer than approximate 410 ms, the timer reset the RS latch and that turns the MOSFET on.

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Current Sense and Feedback Regulation

Current−mode control is implemented with the Current Sense (CS) pin and Feedback (FB) pin. The FB pin is internally pulled up with a 5 kOhm resistor from the 5 V V_{ref}. There is a resistor divider circuit and a 0.1 V offset in this functional block. The following equation describes the relation between the voltages of the FB and CS pins, V_{FB} and V_{CS} respectively.

$$V_{CS(max)} = V_{FB}/4 - 0.1\ V$$

When the output is short circuited, there is no feedback signal from the opto coupler and the FB pin is opened. It gives V_{FB} = 5 V and the maximum voltage of the CS pin is 1.15 V. When the voltage exceeds 1.15 V, the current sense comparator turns on and terminates the MOSFET conduction. It stops current flowing through the sense resistor (R_{Sense}) and hence the sense resistor limits the maximum MOSFET drain current by the following equation.

$$\text{Maximum Drain Current} = 1.15/R_{sense}$$

When the output voltage is too high, the FB pin voltage is pulled down by the opto coupler current and the duty ratio is reduced. The output voltage is then regulated.

There is a Leading Edge Blanking (LEB) circuit with 250 ns propagation delay to prevent false triggering due to parasitics in the CS pin. It makes a minimum on−time of the MOSFET ($t_{on(min)}$).

Thermal Shutdown

There is a thermal shutdown block to prevent overheating condition and protect the device from overheating. When temperature is over 180°C, the Drive output and startup circuit block are disable. The device resumes operation when temperature falls below 130°C.

Gate Drive Output

The IC contains a CMOS output driver specifically designed for direct drive of power MOSFET. The Drive Output typical rise and fall times are 50 ns with a 1.0 nF load. Unbalanced Source and Sink eliminates the need for an external resistor between the device Drive output and the Gate of the external MOSFET. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull−down resistor.

Frequency Clamp Options

The drawback of critical conduction mode is variable switching frequency. The switching frequency can increase dramatically to hundreds of kHz when the output current is too low or vanishes. It is a big problem when EMI above 150 kHz is concerned. Frequency Clamp (FC) is an optional feature in the device to limit the upper switching frequency to nominal 126 kHz by inserting a minimum off−time ($t_{off(min)}$). When a minimum off−time is inserted, the maximum frequency (f_{max}) limit is set.

$$f_{max} = \frac{1}{t_{on(min)} + t_{off(min)}}$$

The SMPS is forced to operate in DCM when the maximum frequency is reached. The minimum off−time is immediately counted after the driving signal goes low. If the ZCD signal comes within this minimum off−time, the ZCD information is ignored until the minimum off−time expires. The next ZCD signal starts the MOSFET conduction.

There are three available FC options: MC33364D − adjustable minimum off−time by external resistor, MC33364D1 − 6.9 us fixed minimum off−time, and MC33364D2 − no minimum off−time (FC disable).

The MC33364D has a FC pin, which can vary the minimum off−time (or the maximum frequency) externally in Figure 11. If the FC pin is opened, the minimum off−time is fixed at 6.9 us. If the FC pin is grounded, the clamp is disabled, and the SMPS will always operate in critical mode. It is generally not recommended to sink or source more than 80 uA from the FC pin because high currents may cause unstable operation.

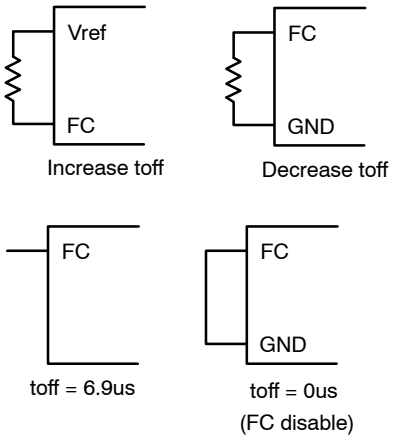

Figure 11. Frequency Clamp Setting

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APPLICATION INFORMATION

Design Example

Design an off−line Flyback converter according to the following requirements:

Output Power: 12 W
Output: 6.0 V @ 2 Amperes
Input voltage range: 90 Vac – 270 Vac, 50/60 Hz

The operation for the circuit shown in Figure 12 is as follows: the rectifier bridge D1−D4 and the capacitor C1 convert the ac line voltage to dc. This voltage supplies the primary winding of the transformer T1 and the startup circuit in U1 through the line pin. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R7. The resistors R5, R6, diode D6 and capacitor C4 create a snubber clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C3, diode D5 and resistor R1 provides a V_{CC} supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes V_{CC} more stable and resistant to noise. The resistor R2 reduces the current flow through the internal clamping and protection zener diode of the Zero Crossing Detector (ZCD) within U1. C3 is the decoupling capacitor of the supply voltage. The resistor R3 can provide additional bias current for the optoisolator's transistor. The diode D8 and the capacitor C5 rectify and filter the output voltage. The TL431, a programmable voltage reference, drives the primary side of the optoisolator to provide isolated feedback to the MC33364. The resistor divider consisting of R10 and R11 program the voltage of the TL431. The resistor R9 and the capacitors C7 and C8 provide frequency compensation of the feedback loop. Resistor R8 provides a current limit for the opto coupler and the TL431.

Since the critical conduction mode converter is a variable frequency system, the MC33364 has a built−in special block to reduce switching frequency in the no load condition. This block is named the "frequency clamp" block. MC33364 used in the design example has an internal frequency clamp set to 126 kHz. However, optional versions with a disabled or variable frequency clamp are available. The frequency clamp works as follows: the clamp controls the part of the switching cycle when the MOSFET switch is turned off. If this "off−time" (determined by the reset time of the transformer's core) is too short, then the frequency clamp does not allow the switch to turn−on again until the defined frequency clamp time is reached (i.e., the frequency clamp will insert a dead time).

There are several advantages of the MC33364's startup circuit. The startup circuit includes a special high voltage switch that controls the path between the rectified line voltage and the V_{CC} supply capacitor to charge that capacitor by a limited current when the power is applied to the input. After a few switching cycles the IC is supplied from the transformer's auxiliary winding. After V_{CC} reaches the undervoltage lockout threshold value, the startup switch is turned off by the undervoltage and the overvoltage control circuit. Because the power supply can be shorted on the output, causing the auxiliary voltage to be zero, the MC33364 will periodically start its startup block. This mode is named "hiccup mode". During this mode the temperature of the chip rises but remains protected by the thermal shutdown block. During the power supply's normal operation, the high voltage internal MOSFET is turned off, preventing wasted power, and thereby, allowing greater circuit efficiency.

Since a bridge rectifier is used, the resulting minimum and maximum dc input voltages can be calculated:

$$V_{in(min)}dc = \sqrt{2}\,xV_{in(min)}ac = \left(\sqrt{2}\right)(90\ Vac) = 127\ V$$

$$V_{in(\mu ax)}dc = \sqrt{2}\,xV_{in(\mu ax)}ac = \left(\sqrt{2}\right)(270\ Vac) = 382\ V$$

The maximum average input current is:

$$I_{in} = \frac{P_{out}}{nV_{in(min)}} = \frac{12\ W}{0.8(127\ V)} = 0.118\ A$$

where n = estimated circuit efficiency.

A TMOS switch with 600 V avalanche breakdown voltage is used. The voltage on the switch's drain consists of the input voltage and the flyback voltage of the transformer's primary winding. There is a ringing on the rising edge's top of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by the RCD network. Design this clamped wave for an amplitude of 50 V below the avalanche breakdown of the TMOS device. Add another 50 V to allow a safety margin for the MOSFET. Then a suitable value of the flyback voltage may be calculated:

$$V_{flbk} = V_{TMOS} - V_{in(max)} - 100\ V$$
$$= 600\ V - 382\ V - 100\ V = 118\ V$$

Since this value is very close to the $V_{in(min)}$, set:

$$V_{flbk} = V_{in(min)} = 127\ V$$

The V_{flbk} value of the duty cycle is given by:

$$\partial max = \frac{V_{flbk}}{V_{flbk} + V_{in(min)}} = \frac{127\ V}{[127\ V + 127\ V]} = 0.5$$

The maximum input primary peak current:

$$I_{ppk} = \frac{2\,I_{in}}{\partial max} = \frac{2.0(0.118\ A)}{0.5} = 0.472\ A$$

Choose the desired minimum frequency f_{min} of operation to be 70 kHz.

After reviewing the core sizing information provided by a core manufacturer, a EE core of size about 20 mm was chosen. Siemens' N67 magnetic material is used, which corresponds to a Philips 3C85 or TDK PC40 material.

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The primary inductance value is given by:

$$L_p = \frac{\partial max\, V_{in(min)}}{\left(I_{ppk}\right)\left(f_{min}\right)} = \frac{0.5(127\ V)}{(0.472\ A)(70\ kHz)} = 1.92\ mH$$

The manufacturer recommends for that magnetic core a maximum operating flux density of:

$$B_{max} = 0.2\ T$$

The cross−sectional area A_c of the EF20 core is:

$$A_c = 33.5\ mm^2$$

The operating flux density is given by:

$$B_{max} = \frac{L_p I_{ppk}}{N_p A_c}$$

From this equation the number of turns of the primary winding can be derived:

$$n_p = \frac{L_p I_{ppk}}{B_{max} A_c}$$

The A_L factor is determined by:

$$A_L = \frac{L_p}{n^2_p} = \frac{L_p\left(B_{max}A_c\right)^2}{\left[L_p\left(I_{ppk}\right)^2\right]}$$

$$= \frac{(0.2\ T)\left(33.5\ E{-}6\ m^2\right)^2}{(.00192\ H)(0.472\ A)^2} = 105\ nH$$

From the manufacturer's catalogue recommendation the core with an A_L of 100 nH is selected. The desired number of turns of the primary winding is:

$$n_p = \left(\frac{L_p}{A_L}\right)^{1/2} = \left[\frac{(0.00192\ H)}{(100\ nH)}\right]^{1/2} = 139\ turns$$

The number of turns needed by the 6.0 V secondary is (assuming a Schottky rectifier is used):

$$n_s = \frac{\left(V_s + V_{fwd}\right)(1{-}\partial max)n_p}{\left[\partial max\left(V_{in(min)}\right)\right]}$$

$$= \frac{(6.0\ V + 0.3\ V)(1 - 0.5)139}{\left[0.5(127\ V)\right]} = 7\ turns$$

The auxiliary winding to power the control IC is 16 V and its number of turns is given by:

$$naux = \frac{(V_{aux} + V_{fwd})(1 - \partial max)n_p}{\left[\partial max(V_{in(min)})\right]}$$

$$= \frac{(16\ V + 0.9\ V)(1 - 0.5)139}{[0.5(127\ V)]} = 19\ turns$$

The approximate value of rectifier capacitance needed is:

$$C1 = \frac{t_{off}(I_{in})}{V_{ripple}} = \frac{(5\ m\ sec)(0.118\ A)}{50\ V} = 11.8\ \mu F$$

where the minimum ripple frequency is 2 times the 50 Hz line frequency and t_{off}, the discharge time of C1 during the haversine cycle, is assumed to be half the cycle period.

Because we have a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency, since the ripple voltage will be greatest at this frequency. When selecting the output capacitor select a capacitor with low ESR to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C5 = \frac{I_{out}}{(f_{min})(V_{rip})} = \frac{2\ A}{(70\ kHz)(0.1\ V)} = 286\ \mu F$$

Determining the value of the current sense resistor (R7), one uses the peak current in the predesign consideration. Since within the IC there is a limitation of the voltage for the current sensing, which is set to 1.2 V, the design of the current sense resistor is simply given by:

$$R7 = \frac{V_{cs}}{I_{ppk}} = \frac{1.2\ V}{0.472\ A} = 2.54\ \Omega \approx 2.2\ \Omega$$

The error amplifier function is provided by a TL431 on the secondary, connected to the primary side via an optoisolator, the MOC8102.

The voltage of the optoisolator collector node sets the peak current flowing through the power switch during each cycle. This pin will be connected to the feedback pin of the MC33364, which will directly set the peak current.

Starting on the secondary side of the power supply, assign the sense current through the voltage−sensing resistor divider to be approximately 0.25 mA. One can immediately calculate the value of the lower and upper resistor:

$$R_{lower} = R11 = \frac{V_{ref}\,(TL431)}{I_{div}} = \frac{2.5\ V}{0.25\ mA} = 10\ k$$

$$R_{upper} = R10 = \frac{V_{out} - V_{ref}(TL431)}{I_{div}}$$

$$= \frac{6.0\ V - 2.5V}{0.25\ mA} = 14\ k$$

The value of the resistor that would provide the bias current through the optoisolator and the TL431 is set by the minimum operating current requirements of the TL431. This current is minimum 1.0 mA. Assign the maximum current through the branch to be 5 mA. That makes the bias resistor value equal to:

$$R_{bias} = R_S = \frac{V_{out} - [V_{ref}(TL431) + V_{LED}]}{I_{LED}}$$

$$= \frac{6.0\ V - [2.5V + 1.4V]}{5.0\ mA} = 420\ \Omega \approx 430\ \Omega$$

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The MOC8102 has a typical current transfer ratio (CTR) of 100% with 25% tolerance. When the TL431 is full−on, 5 mA will be drawn from the transistor within the MOC8102. The transistor should be in saturated state at that time, so its collector resistor must be

$$R_{collector} = \frac{V_{ref} - V_{sat}}{I_{LED}} = \frac{5.0\ V - 0.3\ V}{5.0\ mA} = 940\ \Omega$$

Since a resistor of 5.0 k is internally connected from the reference voltage to the feedback pin of the MC33364, the external resistor can have a higher value

$$R_{ext} = R3 = \frac{(R_{int})(R_{collector})}{(R_{int}) - (R_{collector})} = \frac{(5.0\ k)(940)}{5.0\ k - 940}$$

$$= 1157\ \Omega \approx 1200\ \Omega$$

This completes the design of the voltage feedback circuit.

In no load condition there is only a current flowing through the optoisolator diode and the voltage sense divider on the secondary side.

The load at that condition is given by:

$$R_{noload} = \frac{V_{out}}{(I_{LED} + I_{div})} = \frac{6.0\ V}{(5.0\ mA + 0.25\ mA)} = 1143\ \Omega$$

The output filter pole at no load is:

$$f_{ph} = \frac{1}{(2\pi\ R_{noload}\ C_{out})} = \frac{1}{(2\pi)(1143)(300\ \mu F)} = 0.46\ Hz$$

In heavy load condition the I_{LED} and I_{div} is negligible. The heavy load resistance is given by:

$$R_{heavy} = \frac{V_{out}}{I_{out}} = \frac{6.0\ V}{2.0\ A} = 3.0\ \Omega$$

The output filter pole at heavy load of this output is

$$f_{ph} = \frac{1}{(2\pi\ R_{heavy} C_{out})} = \frac{1}{(2\pi)(3)(300\ \mu F)} = 177\ Hz$$

The gain exhibited by the open loop power supply at the high input voltage will be:

$$A = \frac{\left(V_{in\ max} - V_{out}\right)^2 Ns}{\left((V_{in\ max})(V_{error})(Np)\right)} = \frac{(382\ V - 6.0\ V)^2 (7)}{(382\ V)(1.2\ V)(139)}$$

$$= 15.53 = 23.82\ dB$$

The maximum recommended bandwidth is approximately:

$$f_c = \frac{fs\ min}{5} = \frac{70\ kHz}{5} = 14\ kHz$$

The gain needed by the error amplifier to achieve this bandwidth is calculated at the rated load because that yields the bandwidth condition, which is:

$$Gc = 20\ log\left(\frac{f_c}{f_{ph}}\right) - A = 20\ log\left(\frac{14\ kHz}{177}\right) - 23.82\ dB$$

$$= 14.14\ dB$$

The gain in absolute terms is:

$$A_c = 10^{(Gc/20)} = 10^{(14.14/20)} = 5.1$$

Now the compensation circuit elements can be calculated. The output resistance of the voltage sense divider is given by the parallel combination of resistors in the divider:

$$R_{in} = R_{upper} \parallel R_{lower} = 10\ k \parallel 14\ k = 5833\ \Omega$$

$$R9 = (Ac)\ (R_{in}) = 29.75\ k \approx 30\ k$$

$$C8 = \frac{1}{\left[2\pi\ (A_c)\ (R_{in})\ (f_c)\right]} = 382\ pF \approx 390\ pF$$

The compensation zero must be placed at or below the light load filter pole:

$$C7 = \frac{1}{\left[2\pi\ (R9)\ (f_{pn})\right]} = 11.63\ \mu F \approx 10\ \mu F$$

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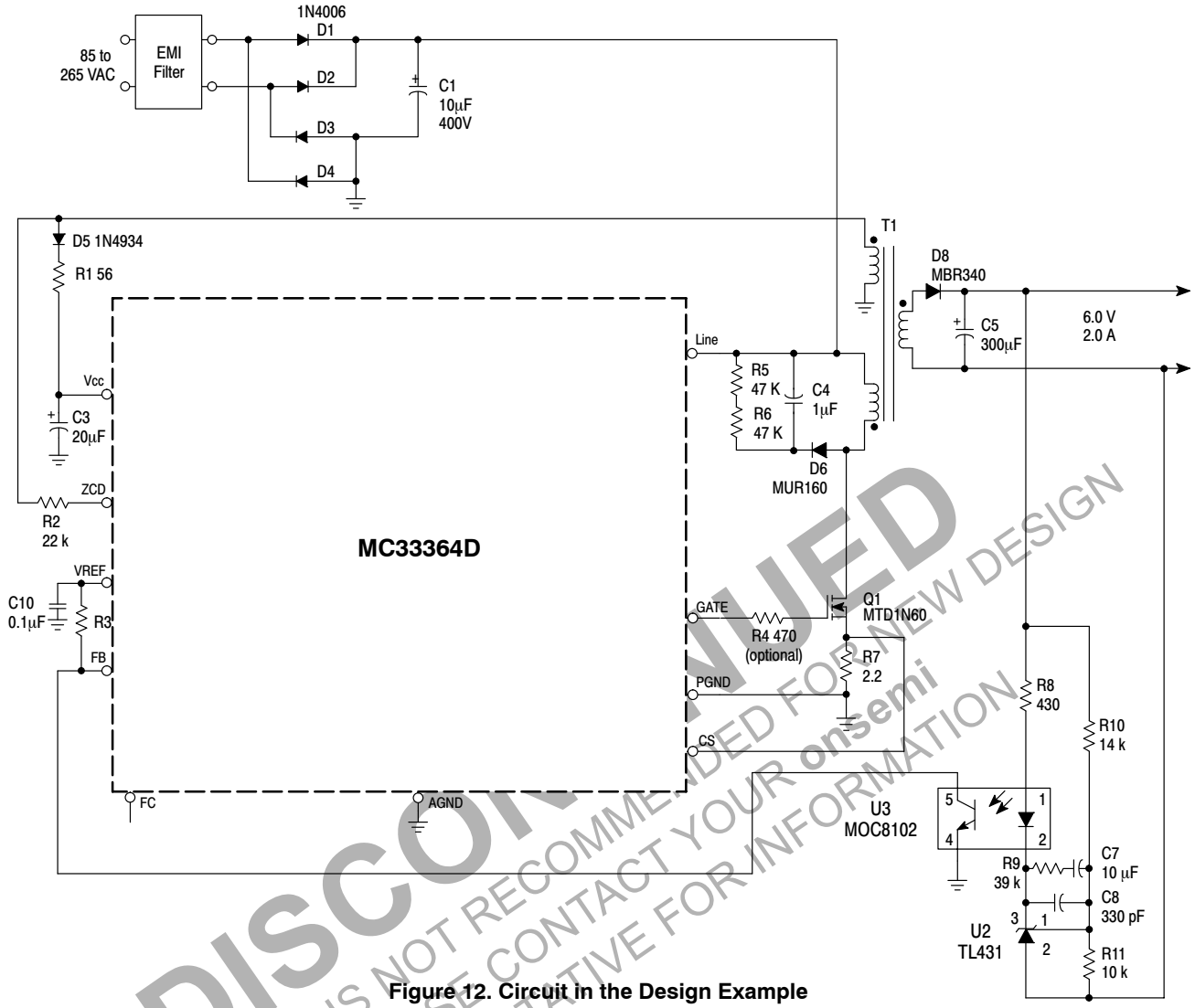

Figure 12. Circuit in the Design Example

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The described critical conduction mode flyback converter has the following performance and maximum ratings:

Output power	12W
Output	12V @ 1Amp max
Input voltage range	90VAC – 270VAC

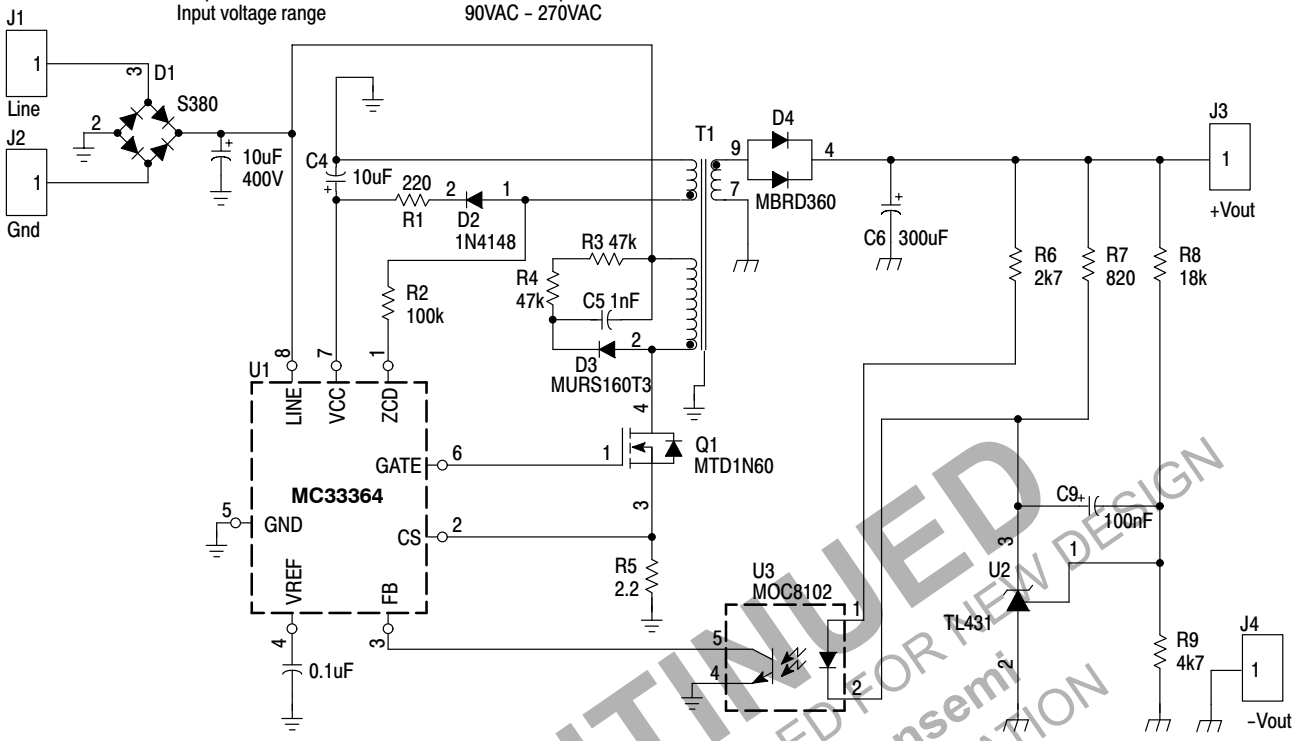

Figure 13. Critical Conduction Mode Flyback Converter

CONVERTER TEST DATA

Test	Conditions	Results
Line Regulation	V_{in} = 120VAC to 240VAC, I_{out} = 0.8A	ΔV = 50mV
Load	V_{in} = 120VAC, I_{out} = 0.2A to 0.8A	ΔV = 40mV
	V_{in} = 240VAC, I_{out} = 0.2A to 0.8A	ΔV = 40mV
Output Ripple	V_{in} = 120VAC, I_{out} = 0.8A	ΔV = 290mV
	V_{in} = 240VAC, I_{out} = 0.8A	ΔV = 24mV
Efficiency	V_{in} = 120VAC, I_{out} = 0.8A	η = 78.0%
	V_{in} = 240VAC, I_{out} = 0.8A	η = 79.4%
Power Factor	V_{in} = 120VAC, I_{out} = 0.8A	Pf = 0.491
	V_{in} = 240VAC, I_{out} = 0.8A	Pf = 0.505

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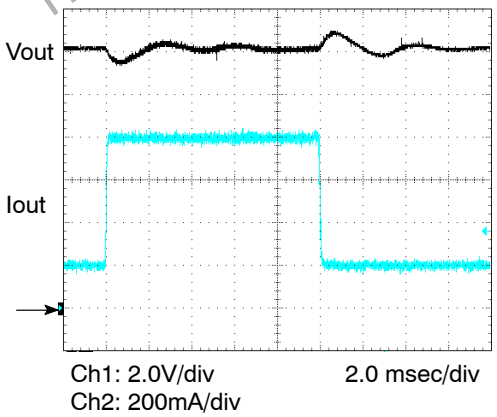

Figure 14. Load Regulation 120V

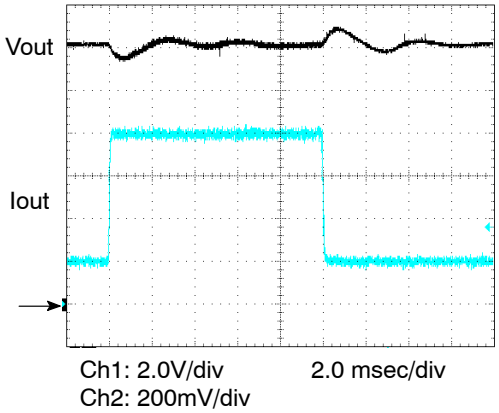

Figure 15. Load Regulation 240V

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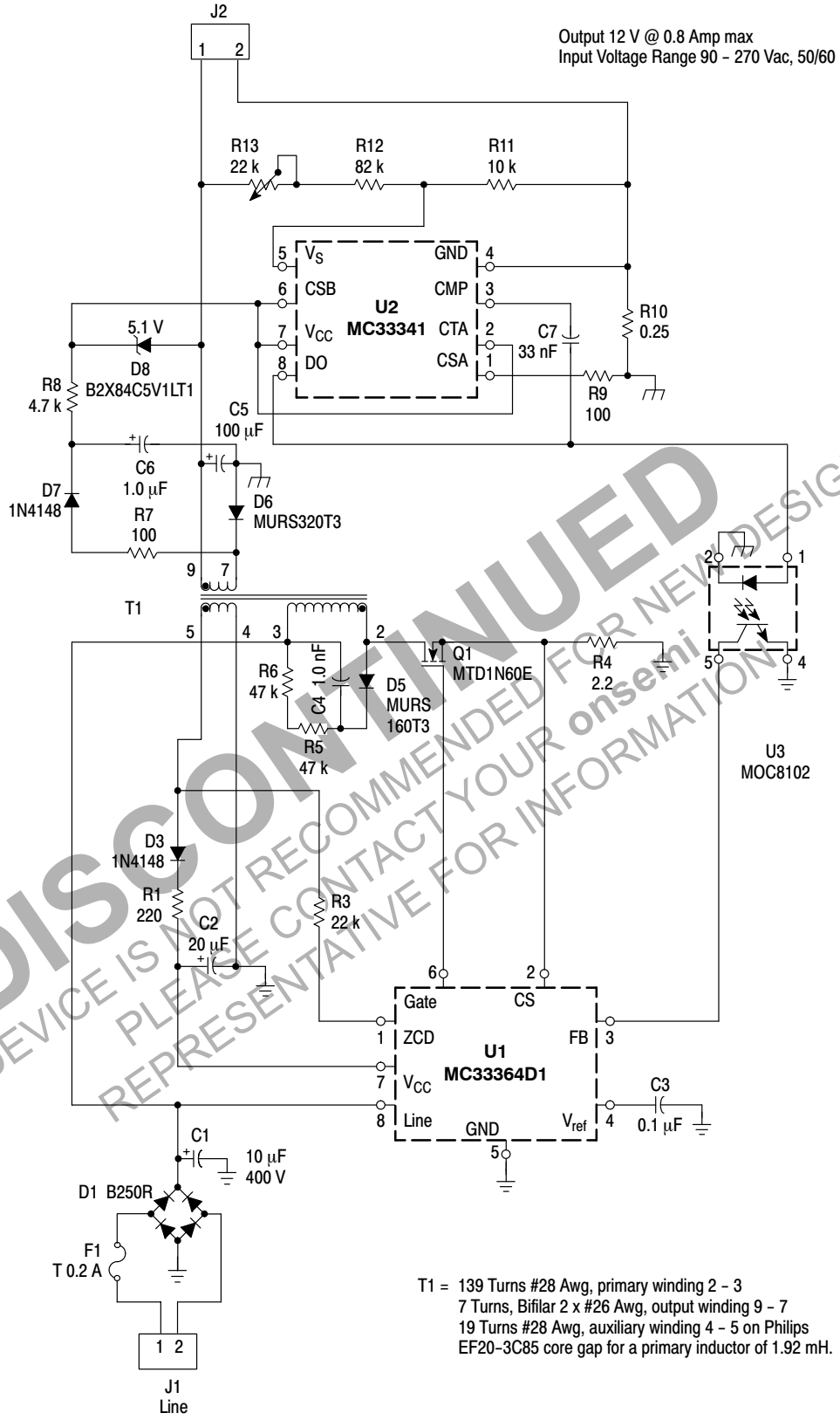

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Figure 16. Universal Input Battery Charger

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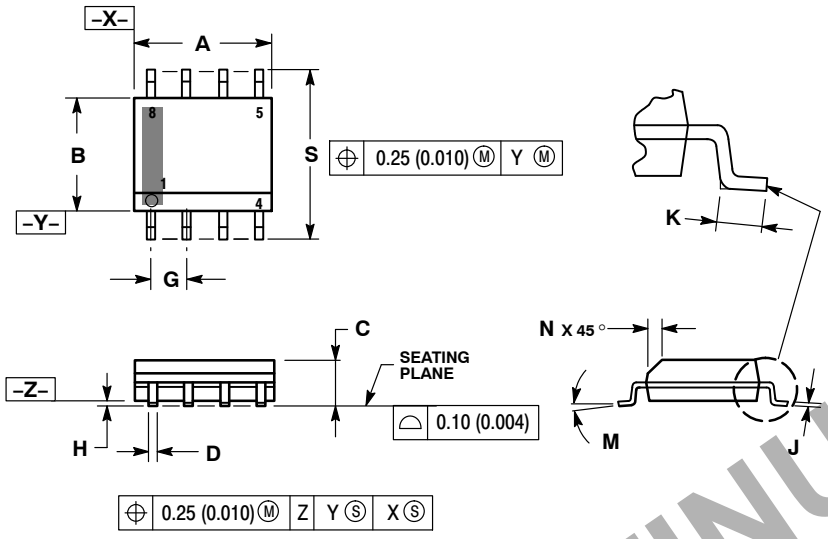
ISSUE AJ



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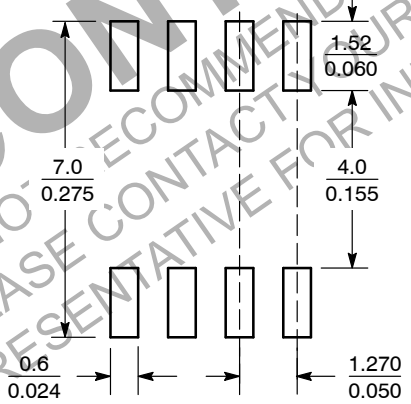
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



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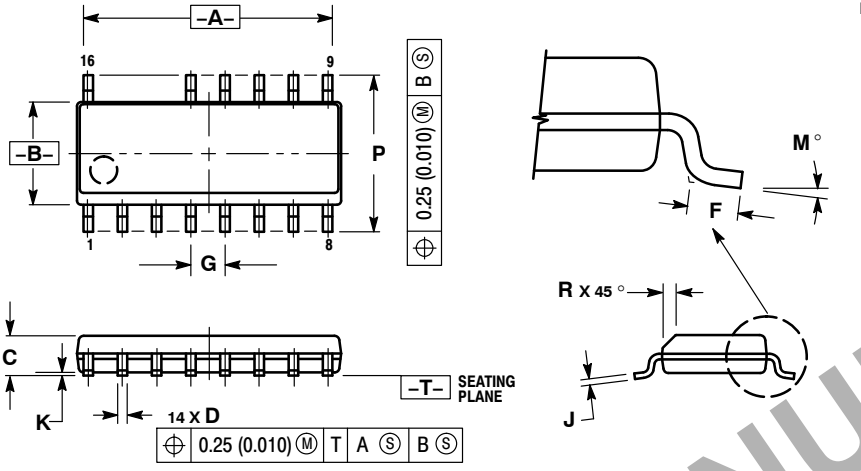
CASE 751K−01
ISSUE O



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5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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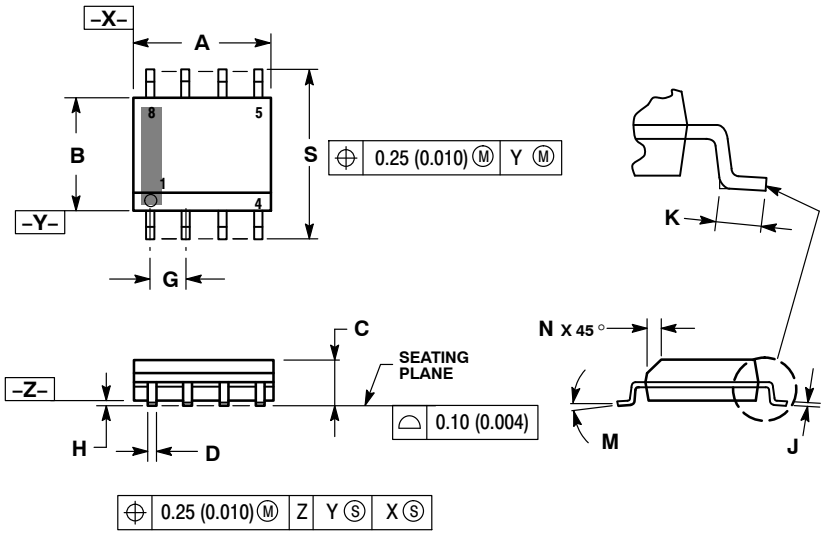

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M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
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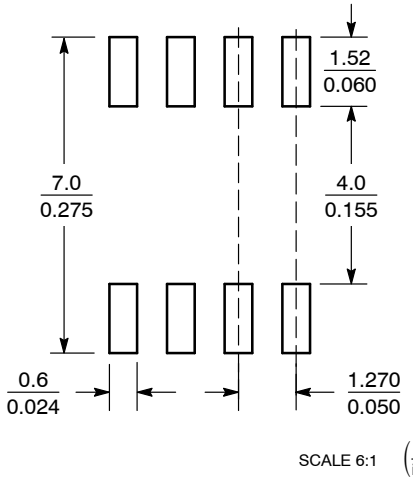

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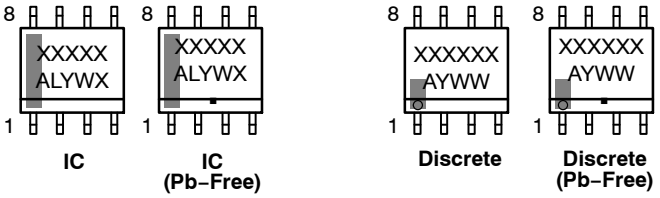

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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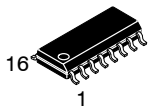

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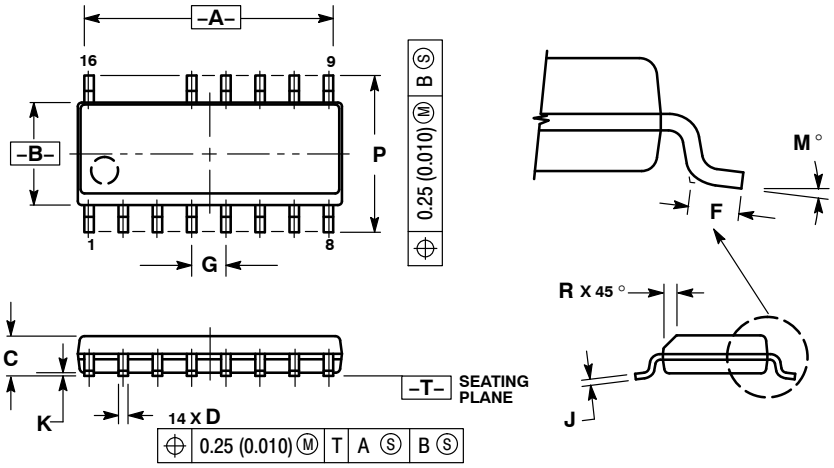
SOIC−16 MINUS PINS 14, 15
CASE 751K
ISSUE O

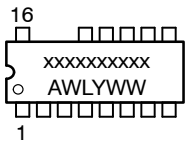
DATE 22 DEC 1993



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

GENERIC MARKING DIAGRAM*



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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