S-35740 A Series

CONVENIENCE TIMER

AUTOMOTIVE, 125°C OPERATION, 2-WIRE INTERVAL TIMER

www.ablic.com

Rev.2.0_00

The convenience timer is a CMOS timer IC which operates with low current consumption, and is suitable for the time management of the relative time.
The S-35740 Series outputs the fixed-cycle interrupt signal. The frequency and duty ratio of the fixed-cycle interrupt signal can be set freely by users via a 2-wire serial interface.
The S-35740 Series has a 24-bit timer. For example, users can obtain the cumulative energization time of the system since the timer performs a count-up action every second.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

- Fixed-cycle interrupt signal output function: Settable frequency and duty ratio, with an output control pin
- Low current consumption: 0.2 μA typ.
  (Quartz crystal: C_L = 6.0 pF, V_{DD} = 3.0 V, ENBL pin = "H", Ta = +25°C)
- Wide range of operation voltage: 1.8 V to 5.5 V
- 2-wire (I^2C-bus) CPU interface
- Built-in 32.768 kHz crystal oscillation circuit
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales office for details.

■ Application

- Intermittent operation of various systems
- Regular status monitoring of various systems

■ Package

- TMSOP-8

■ Block Diagram

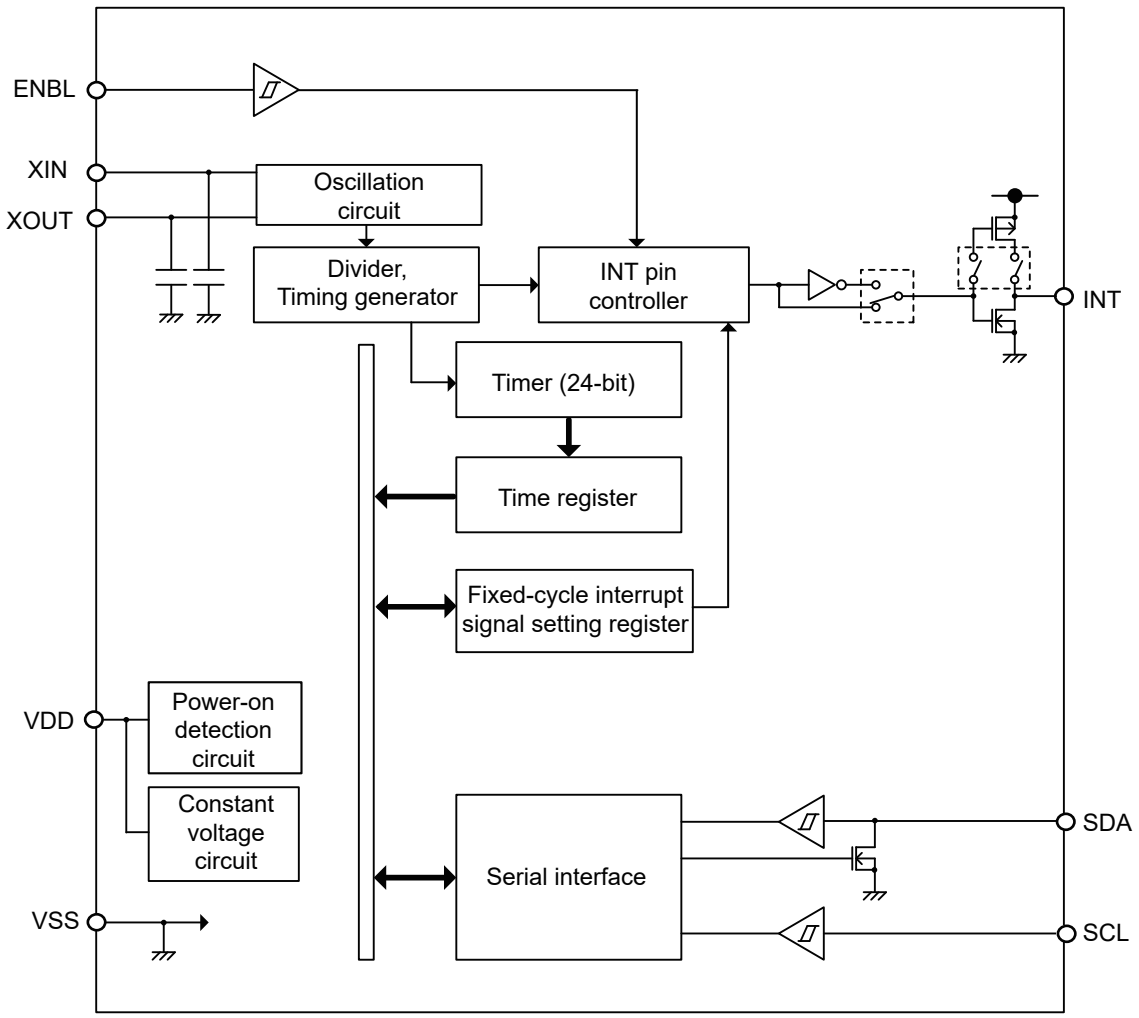


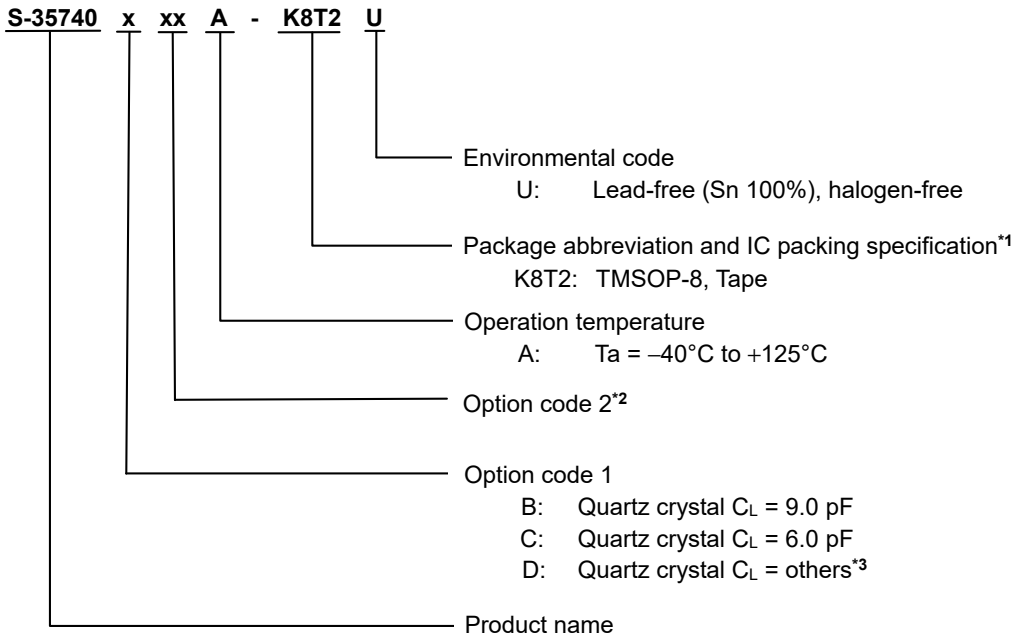
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** A sequence number added by the optional function that is user-selected.
***3.** Contact our sales office for details.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	INT Pin Output Form*1
S-35740C01A-K8T2U	CMOS output

***1.** The pin of Nch open-drain output / CMOS output is selectable. Refer to "■ **Pin Functions**".

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

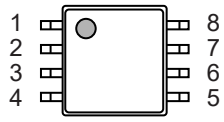


Figure 2

Table 3 List of Pins

Pin No.	Symbol	Description	I/O	Configuration
1	ENBL	Input pin for fixed-cycle interrupt signal output control	Input	Nch open-drain input
2	XOUT	Connection pins for quartz crystal	–	–
3	XIN			
4	VSS	GND pin	–	–
5	INT	Output pin for fixed-cycle interrupt signal	Output	Nch open-drain output / CMOS output is selectable
6	SDA	I/O pin for serial data	Bi-directional	Nch open-drain output, CMOS input
7	SCL	Input pin for serial clock	Input	CMOS input
8	VDD	Pin for positive power supply	–	–

■ Pin Functions

1. SDA (I/O for serial data) pin

This is a data input / output pin for I^2C-bus interface. The SDA pin inputs / outputs data by synchronizing with a clock pulse from the SCL pin. This pin has CMOS input and Nch open-drain output. Generally in use, the SDA pin is pulled up to V_{DD} potential via a resistor, and is used with wired-OR connection of other device of Nch open-drain output or open collector output.

2. SCL (Input for serial clock) pin

This is a clock input pin for I^2C-bus interface. The SDA pin inputs / outputs data by synchronizing with this clock

3. ENBL (Input for fixed-cycle interrupt signal output control) pin

This pin controls the clock pulse output from the INT pin. The INT pin outputs the fixed-cycle interrupt signal when the ENBL pin is "H". The INT pin is fixed when the ENBL pin is "L".

4. INT (Output for fixed-cycle interrupt signal) pin

This pin outputs a fixed-cycle interrupt signal. The fixed-cycle interrupt signal of the frequency and duty ratio, which is set to the fixed-cycle interrupt signal setting register, is output. Regarding the operation of the fixed-cycle interrupt signal output, refer to "**■ INT Pin Fixed-cycle Interrupt Signal Output**".
Also, the INT pin output form of Nch open-drain output / CMOS output can be selected.

5. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

6. VDD (Positive power supply) pin

Connect this pin with a positive power supply. Regarding the values of voltage to be applied, refer to "**■ Recommended Operation Conditions**".

7. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

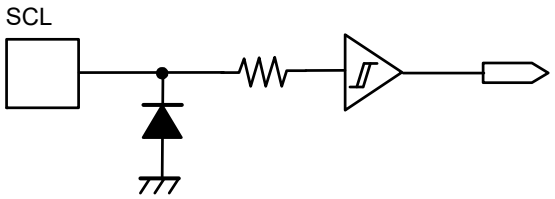


Figure 3 SCL pin

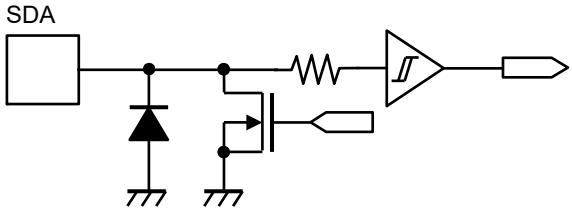


Figure 4 SDA pin

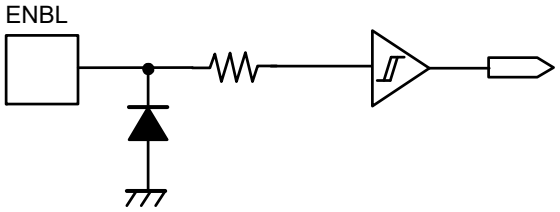


Figure 5 ENBL Pin

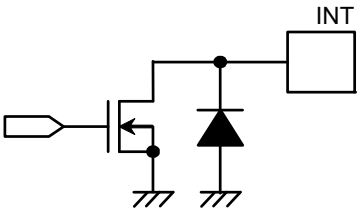


Figure 6 INT Pin (Nch Open-drain Output)

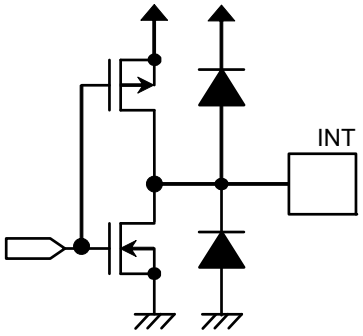


Figure 7 INT Pin (CMOS Output)

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SDA, SCL, ENBL	V_{SS} – 0.3 to V_{SS} + 6.5	V
Output voltage	V_{OUT}	SDA, INT*1	V_{SS} – 0.3 to V_{SS} + 6.5	V
		INT*2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Operation ambient temperature*3	T_{opr}	–	–40 to +125	°C
Storage temperature	T_{stg}	–	–55 to +150	°C

***1.** When an Nch open-drain output product is selected.
***2.** When a CMOS output procut is selected.
***3.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 5

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V_{DD}	Ta = –40°C to +125°C	1.8	–	5.5	V

■ Oscillation Characteristics

Table 6

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.8	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–20	–	+20	ppm

***1.** Reference value

■ DC Electrical Characteristics

Table 7

(Ta = –40°C to +125°C, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1*1	I_{DD1}	–	V_{DD} = 3.0 V, Ta = –40°C to +85°C, Out of communication, ENBL pin = V_{SS}, INT pin = no load	–	1.7	3.0	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication, ENBL pin = V_{SS}, INT pin = no load	–	2.7	4.5	µA
Current consumption 2	I_{DD2}	–	V_{DD} = 3.0 V, Ta = –40°C to +85°C, Out of communication, ENBL pin = V_{DD}, INT pin output = 1.024 kHz, INT pin = no load*1	–	0.2	0.38	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication, ENBL pin = V_{DD}, INT pin output = 1.024 kHz, INT pin = no load*1	–	0.7	0.98	µA
			V_{DD} = 3.0 V, Ta = –40°C to +85°C, Out of communication, ENBL pin = V_{DD}, INT pin output = 1.024 kHz, INT pin = no load*2	–	0.35	0.55	µA
			V_{DD} = 3.0 V, Ta = +125°C, Out of communication, ENBL pin = V_{DD}, INT pin output = 1.024 kHz, INT pin = no load*2	–	1.0	1.4	µA
Current consumption 3	I_{DD3}	–	V_{DD} = 3.0 V, f_{SCL} = 1 MHz, During communication, ENBL pin = V_{DD}, INT pin = no load	–	170	300	µA
High level input leakage current	I_{IZH}	SDA, SCL, ENBL	V_{IN} = V_{DD}	–0.5	–	0.5	µA
Low level input leakage current	I_{IZL}	SDA, SCL, ENBL	V_{IN} = V_{SS}	–0.5	–	0.5	µA
High level output leakage current	I_{OZH}	SDA, INT*1	V_{OUT} = V_{DD}	–0.5	–	0.5	µA
Low level output leakage current	I_{OZL}	SDA, INT*1	V_{OUT} = V_{SS}	–0.5	–	0.5	µA
High level input voltage	V_{IH}	SDA, SCL, ENBL	–	0.7 × V_{DD}	–	V_{SS} + 5.5	V
Low level input voltage	V_{IL}	SDA, SCL, ENBL	–	V_{SS} – 0.3	–	0.3 × V_{DD}	V
High level output voltage*2	V_{OH}	INT	I_{OH} = –0.4 mA	0.8 × V_{DD}	–	–	V
Low level output voltage	V_{OL}	SDA, INT	I_{OL} = 2.0 mA	–	–	0.4	V

***1.** When an Nch open-drain output product is selected.
***2.** When a CMOS output product is selected.

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.8 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$
Input pulse rise / fall time	20 ns
Output reference voltage	$V_{OH} = 0.7 \times V_{DD}$, $V_{OL} = 0.3 \times V_{DD}$
Output load	100 pF

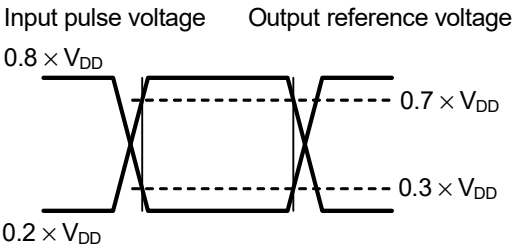


Figure 8 Input / Output Waveform during AC Measurement

Table 9 AC Electrical Characteristics

(Ta = –40°C to +125°C)

Item	Symbol	V_{DD} = 1.8 V to 2.5 V		V_{DD} = 2.5 V to 5.5 V		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	400	0	1000	kHz
SCL clock "L" time	t_{LOW}	1.3	–	0.4	–	µs
SCL clock "H" time	t_{HIGH}	0.6	–	0.3	–	µs
SDA output delay time*1	t_{AA}	–	0.9	–	0.5	µs
Start condition set-up time	$t_{SU.STA}$	0.6	–	0.25	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	0.25	–	µs
Data input set-up time	$t_{SU.DAT}$	100	–	80	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition set-up time	$t_{SU.STO}$	0.6	–	0.25	–	µs
SCL, SDA rise time	t_R	–	0.3	–	0.3	µs
SCL, SDA fall time	t_F	–	0.3	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	0.5	–	µs
Noise suppression time	t_I	–	50	–	50	ns

*1. Since the output form of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance and load capacitance outside the IC. **Figure 10** shows the relationship between the output load values.

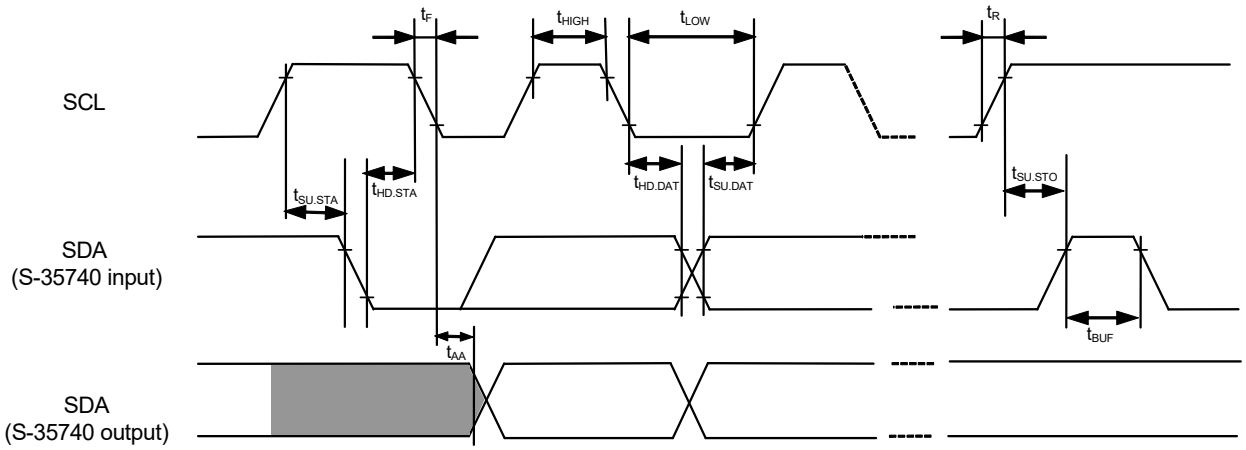


Figure 9 Bus Timing

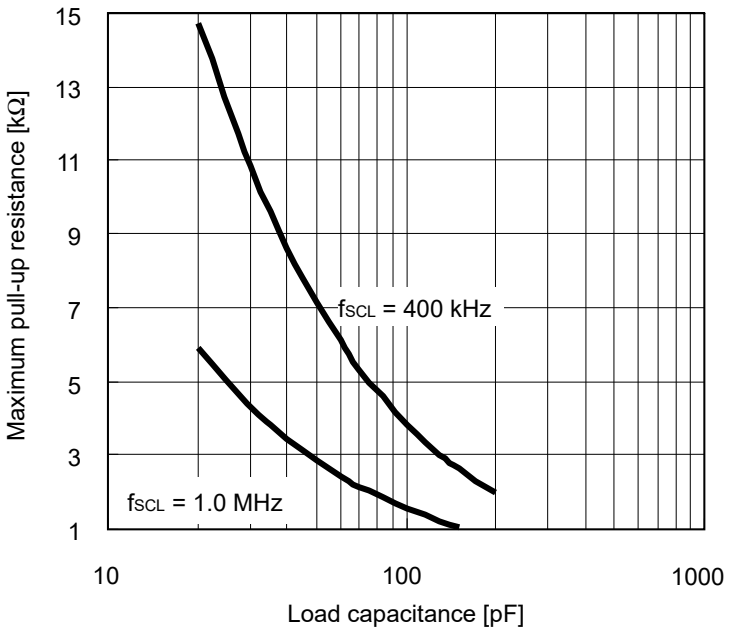


Figure 10 Output Load

■ INT Pin Fixed-cycle Interrupt Signal Output

1. Frequency and duty ratio

The frequency and duty ratio of the fixed-cycle interrupt signal output is set in the fixed-cycle interrupt signal setting register. By setting "1" to each bit of the fixed-cycle interrupt signal setting register, the frequency corresponding to each bit (1 Hz to 1.024 kHz) is output depending on NAND logic, and the frequency and the duty ratio are changed.
The example of the fixed-cycle Interrupt signal output when 512 Hz = "1", 256 Hz = "1", 128 Hz = "1", 64 Hz = "1" and others = "0" is shown below.
When all bits of the fixed-cycle interrupt signal setting register are "0", the INT pin outputs are fixed to Nch open-drain output = "H" or CMOS output = "L".

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the frequency corresponding to each bit (1 Hz to 1.024 kHz) is output depending on AND logic.

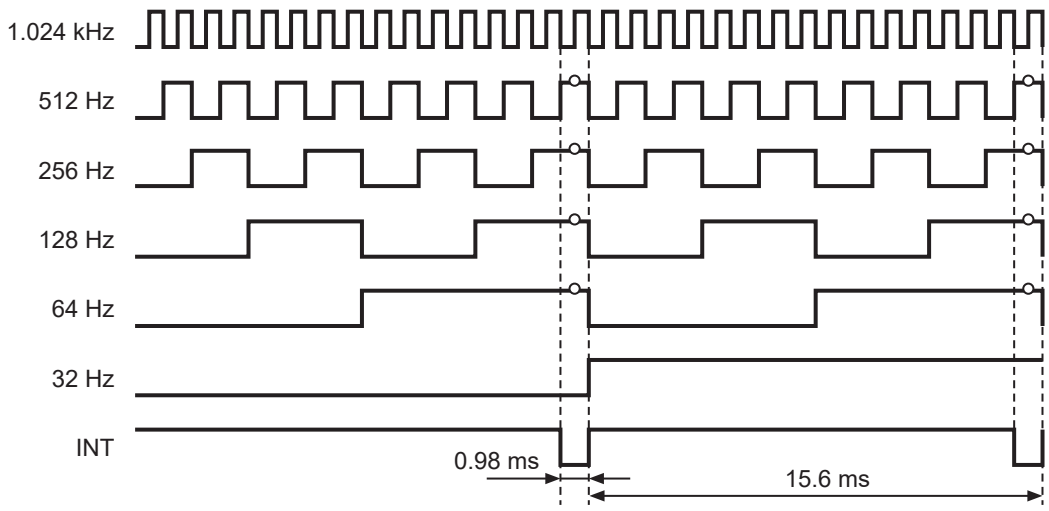


Figure 11 Example of Fixed-cycle Interrupt Signal Output (Nch Open-drain output)

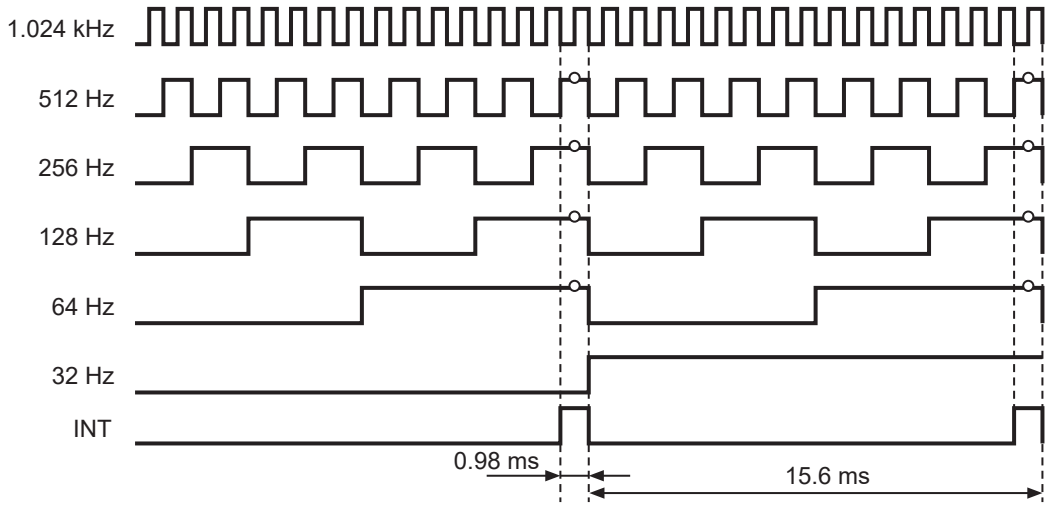


Figure 12 Example of Fixed-cycle Interrupt Signal Output (CMOS output)

2. ENBL pin and INT pin clock pulse output

The INT pin outputs the fixed-cycle interrupt signal when the ENBL pin is "H". The INT pin is fixed to Nch open-drain output = "L" or CMOS output = "H" when the ENBL pin is "L".
Duty ratio of the INT pin may change when the "H" and "L" of the ENBL pin changes. The example of the INT pin output timing is shown below.

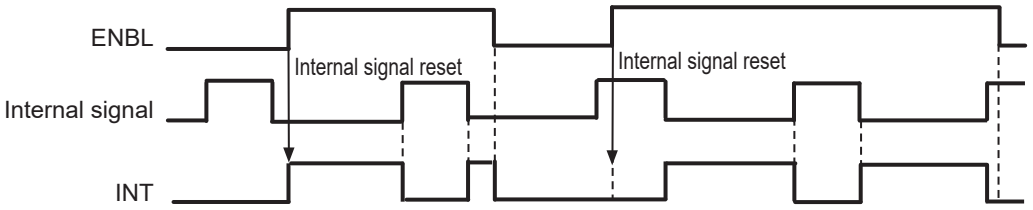


Figure 13 INT Pin Output Timing Example 1 (Nch Open-drain Output)

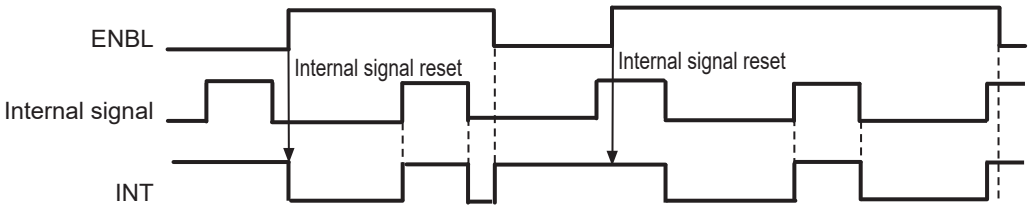


Figure 14 INT Pin Output Timing Example 1 (CMOS Output)

3. Write operation of fixed-cycle interrupt signal setting register and INT pin clock pulse output

Even if the write operation of the fixed-cycle interrupt signal setting register is performed when the INT pin does not output the fixed-cycle interrupt signal, the INT pin maintains Nch open-drain output = "L" or CMOS output = "H". Therefore, when the ENBL pin is set to "H", the INT pin outputs the fixed-cycle interrupt signal according to the value written to the fixed-cycle interrupt signal setting register immediately before the setting.
The divider is reset if the write operation of the fixed-cycle interrupt signal setting register is performed when the INT pin outputs the fixed-cycle interrupt signal. Therefore, the duty ratio of the INT pin may change. The example of the INT pin output timing is shown below.

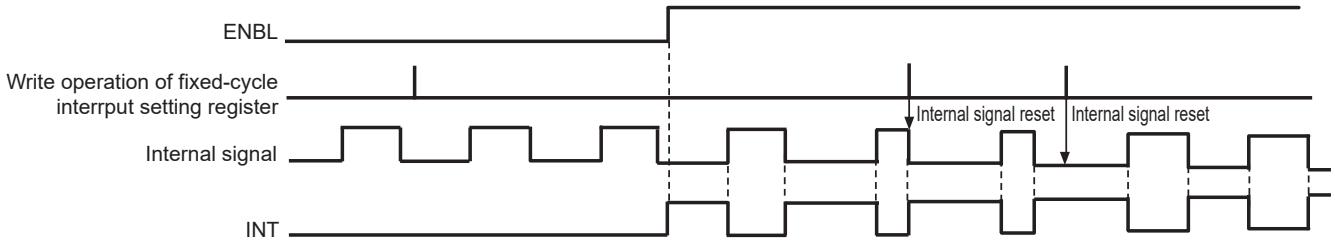


Figure 15 INT Pin Output Timing Example 2 (Nch Open-drain Output)

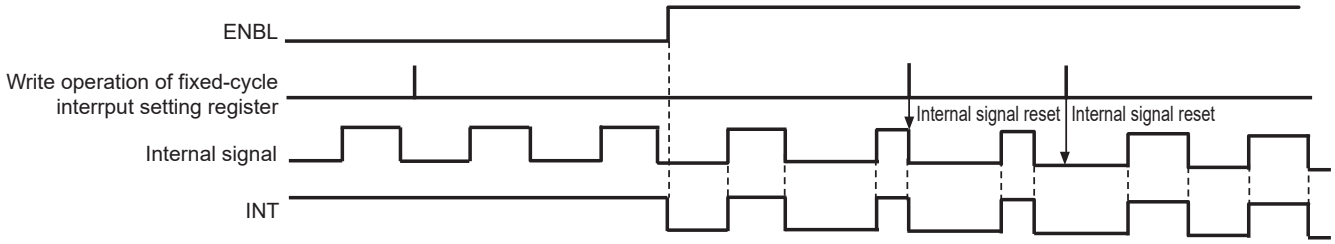


Figure 16 INT Pin Output Timing Example 2 (CMOS Output)

Moreover, since the crystal oscillation circuit is unstable immediately after power-on, regardless of the status of the ENBL pin, the INT pin is fixed to Nch open-drain output = "H" or CMOS output = "L" for about 0.5 seconds after power-on. The write operation of the fixed-cycle interrupt signal setting register is possible even during this time.
When the ENBL pin is set to "H" without the write operation of the fixed-cycle interrupt signal setting register after power-on, the INT pin is fixed to Nch open-drain output = "H" or CMOS output = "L". Therefore, the write operation of the fixed-cycle interrupt signal setting register should be performed after power-on.

■ Timer

The S-35740 Series has a 24-bit timer. The timer performs a count-up action every second and stops at "FFFFFF h". Even if the timer stops, the clock pulse output of INT pin is not affected.
Input a timer reset command to the S-35740 Series in order to reset the timer. Thereby, the timer restarts the operation. Refer to "**Figure 21 Acknowledge Output Timing**" and "**Figure 22 Data Transmission Format of Serial Interface**" regarding the timer reset command.
As shown in "**Figure 13 INT Pin Output Timing Example 1 (Nch Open-drain Output)**" and "**Figure 15 INT Pin Output Timing Example 2 (Nch Open-drain Output)**", the S-35740 Series resets the internal signal when the write operation of the fixed-cycle interrpt signal setting register is performed. The internal signal generates a count-up signal of the timer every second. Therefore, the count-up action of the timer will be delayed for up to 1 second when the write operation of the fixed-cycle interrupt signal setting register is performed. **Figure 17** shows the operation outline.

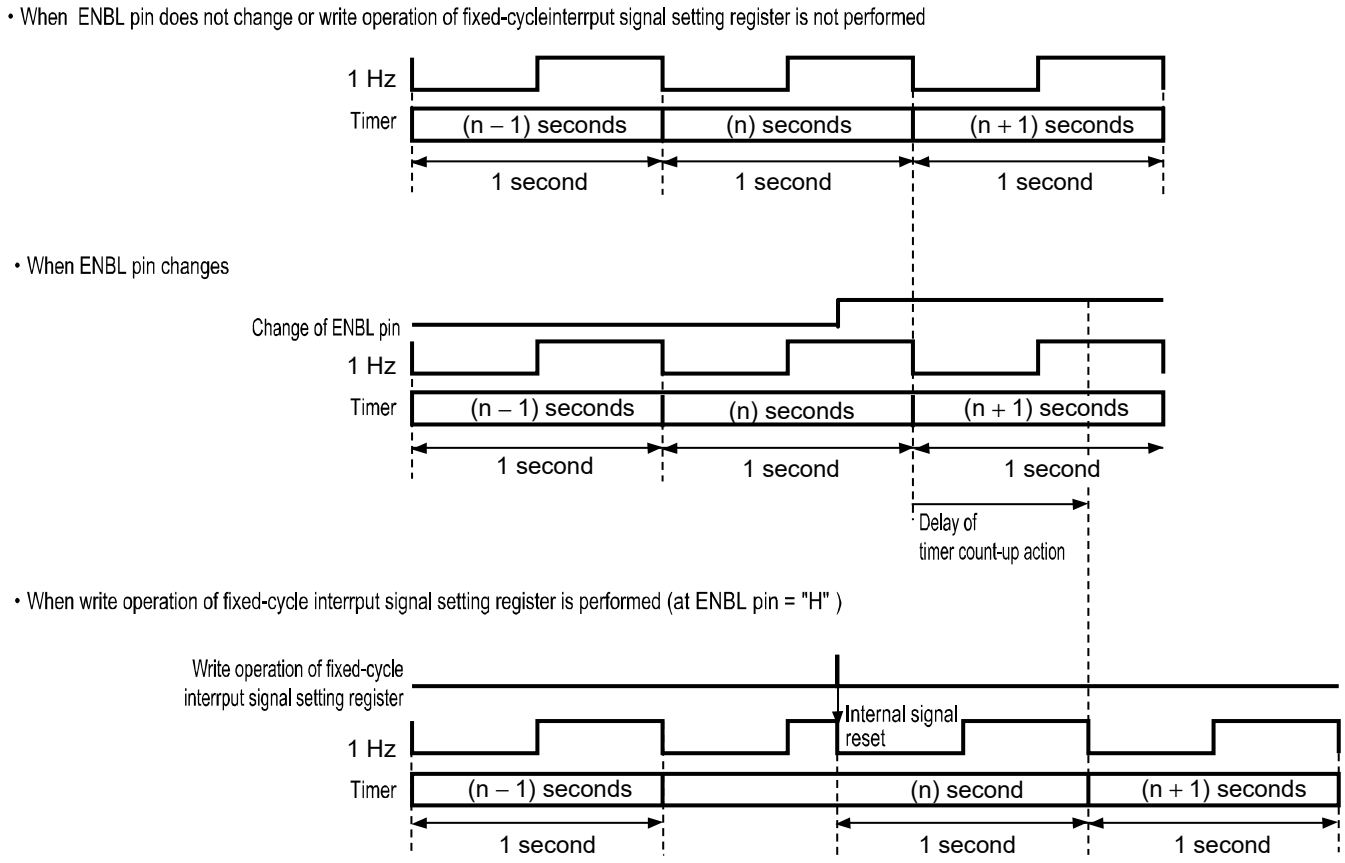


Figure 17 Timer Count-up Action and Internal Signal Reset

■ Configuration of Registers

1. Time register

The time register is a 3-byte register that stores the timer value in the binary code.
The time register is read-only.
Perform the read operation of the time register in 3-byte unit from TM23 to TM0.

Example: 3 seconds (0000_0000_0000_0000_0000_0011)
45 minutes (0000_0000_0000_1010_1000_1100)
5 hours 30 minutes (0000_0000_0100_1101_0101_1000)

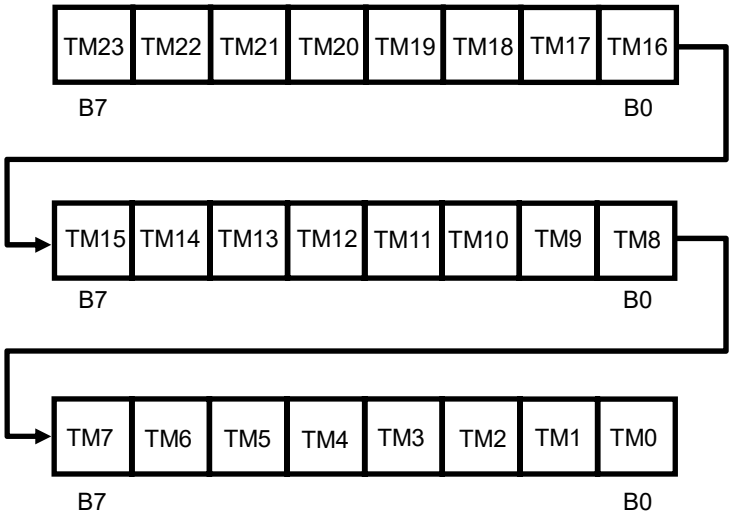


Figure 18

2. Fixed-cycle interrupt signal setting register

The fixed-cycle interrupt signal setting register is a 2-byte register that sets the fixed-cycle interrupt signal at the upper 10 bits. By setting "1" to each bit, the frequency corresponding to each bit is output from the INT pin depending on NAND logic. Refer to "■ **INT Pin Fixed-cycle Interrupt Signal Output**" for details.
The lower 3 bits, RST2 to RST0 are used as a register to input the timer reset command. The timer is reset by writing RST2 = "0", RST1 = "1" and RST0 = "0". The fixed-cycle interrupt signal setting register is not reset even if the timer reset command is input. Therefore, it is unnecessary to write to the fixed-cycle interrupt signal setting register again. Moreover, when only a fixed-cycle interrupt signal is set without resetting the timer, write the data except for the above mentioned ones, such as RST2 = "1", RST1 = "1" and RST0 = "1" to the fixed-cycle interrupt signal setting register.
Set DM1 and DM0 to "0" or "1" since they are dummy data.
The fixed-cycle interrupt signal setting register is possible for write and read.
Perform the write and read operation of the fixed-cycle interrput signal setting register in 2-byte unit.
When performing the read operation of fixed-cycle interrupt signal setting register, set the ENBL pin to "H". If the ENBL pin is set to "L", the time register data is read.

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the frequency corresponding to each bit (1 Hz to 1.024 kHz) is output depending on AND logic.

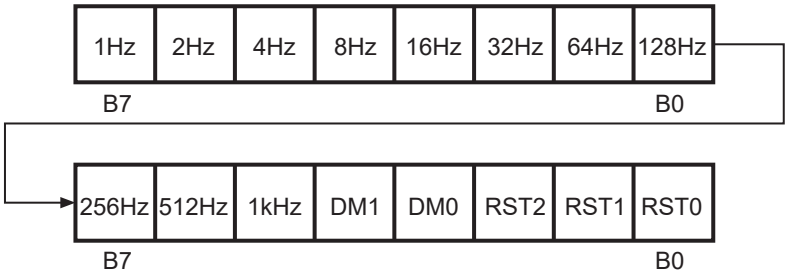


Figure 19

■ Serial Interface

The S-35740 Series transmits and receives various commands via I²C-bus serial interface to read / write data.

1. Start condition

When SDA changes from "H" to "L" with SCL at "H", the S-35740 Series recognizes start condition and the access operation is started.

2. Stop condition

When SDA changes from "L" to "H" with SCL at "H", the S-35740 Series recognizes stop condition and the access operation is completed. The S-35740 Series enters standby mode, consequently.

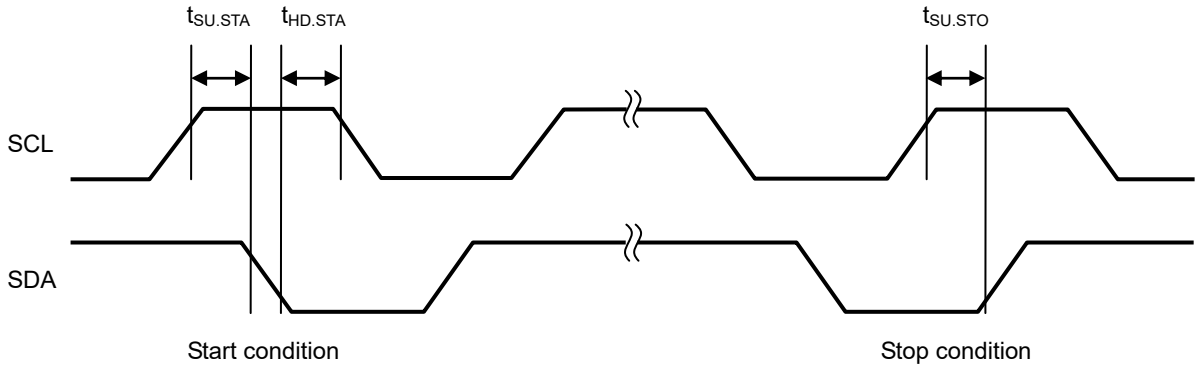


Figure 20 Start / Stop Condition

3. Data transmission and acknowledge

The data transmission is performed at every one byte after the start condition detection. Pay attention to the specification of $t_{SU.DAT}$ and $t_{HD.DAT}$ when changing SDA, and perform the operation when SCL is "L". If SDA changes when SCL is "H", the start / stop condition is recognized even during the data transmission, and the access operation will be interrupted.

Whenever a one-byte data is received during data transimmion, the receiving device returns an acknowledge. For example, as shown in **Figure 21**, assume that the S-35740 Series is a receiving device, and the master device is a transmitting device. If the clock pulse at the 8th bit falls, the master device releases SDA. Consequently, the S-35740 Series, as an acknowledge, sets SDA to "L" during the 9th bit pulse. The access operation is not performed properly when the S-35740 Series does not output an acknowledge.

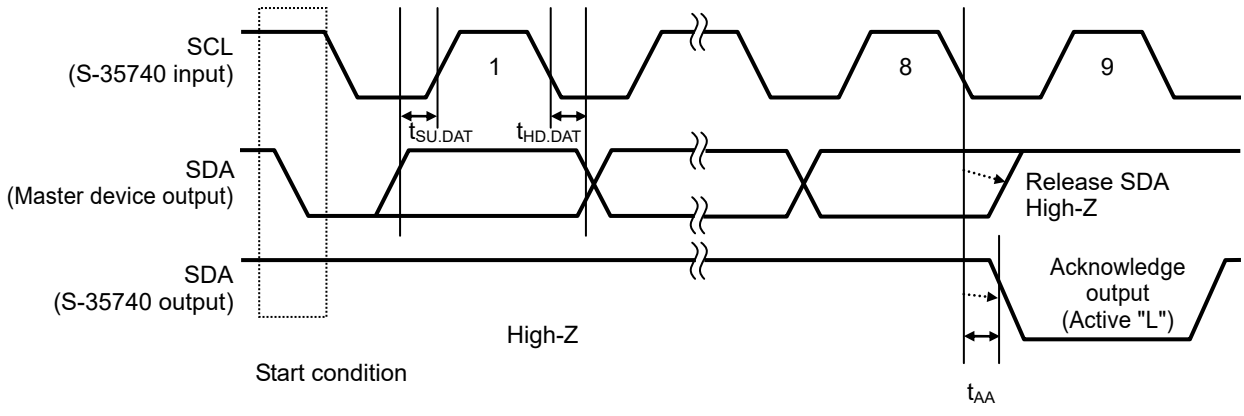


Figure 21 Acknowledge Output Timing

4. Data transmission format

After the start condition transmission, the 1st byte is a slave address and a command (read / write bit) that shows the transmission direction at the 2nd byte or subsequent bytes.

The slave address of the S-35740 Series is specified to "0110010". The data can be written to the fixed-cycle interrupt signal setting register when read / write bit is "0", and the data of the fixed-cycle interrupt signal setting register or the time register can be read when read / write bit is "1".

When the data can be written to fixed-cycle interrupt signal setting register, input the data from the master device in order of B7 to B0. The acknowledge ("L") is output from the S-35740 Series whenever a one-byte data is input.

When the data of the fixed-cycle interrupt signal setting register or the timer register can be read, the data from the S-35740 Series is output in order of B7 to B0 in byte unit. Input the acknowledge ("L") from the master device whenever a one-byte data is input. However, do not input the acknowledge for the last byte (NO_ACK). By this, the end of the data read is informed.

After the master device receives / transmits the acknowledge for the last byte data, input the stop condition to the S-35740 Series to finish the access operation.

When the master device inputs start condition instead of stop condition, the S-35740 Series becomes restart condition, and can transmit / receive the data if the master device inputs the slave address continuously.

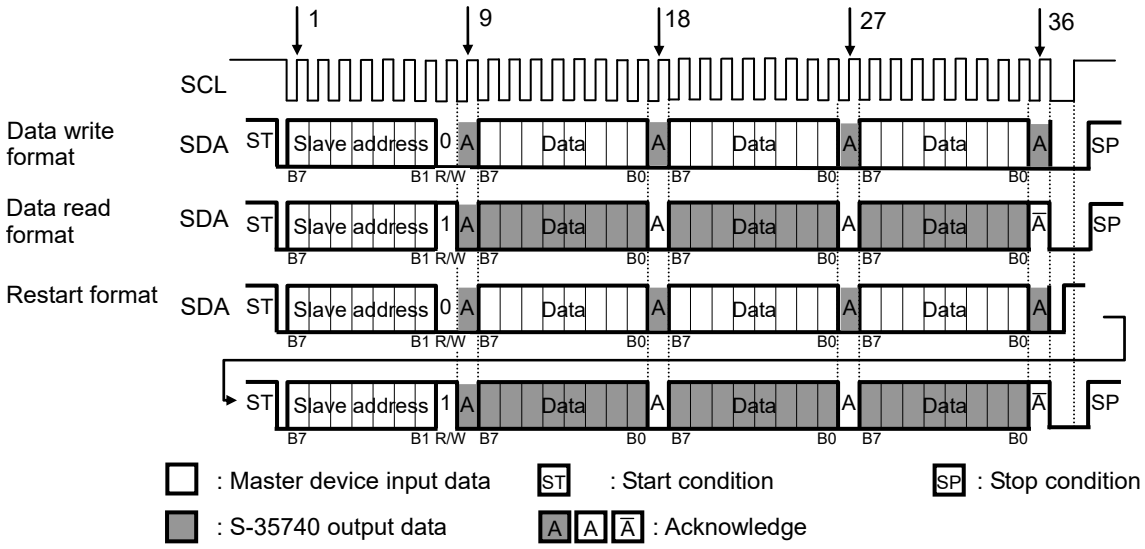


Figure 22 Data Transmission Format of Serial Interface

5. Read operation of time register

Transmit the start condition and slave address from the master device. The slave address of the S-35740 Series is specified to "0110010". The data of the time register can be read when the read / write bit is "1".
The 2nd byte to the 4th byte are used as the time register. Each byte from B7 is transmitted.
When the read operation of the time register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 is output from the master device, and then transmit the stop condition.
The time register is a 3-byte register. "1" is read if the read operation is performed continuously after reading 3 bytes of the time register. Regarding the time register, refer to "■ **Configuration of Registers**".

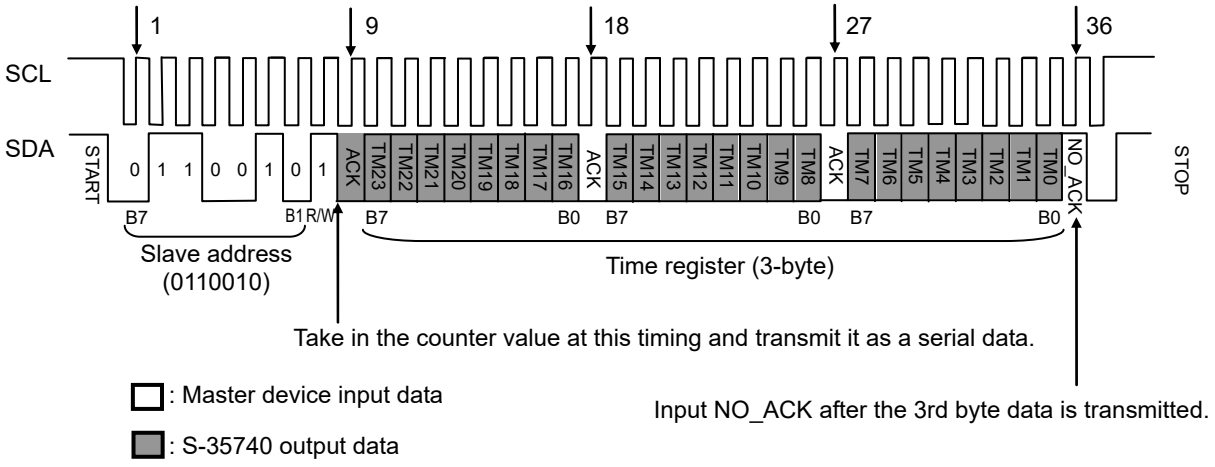
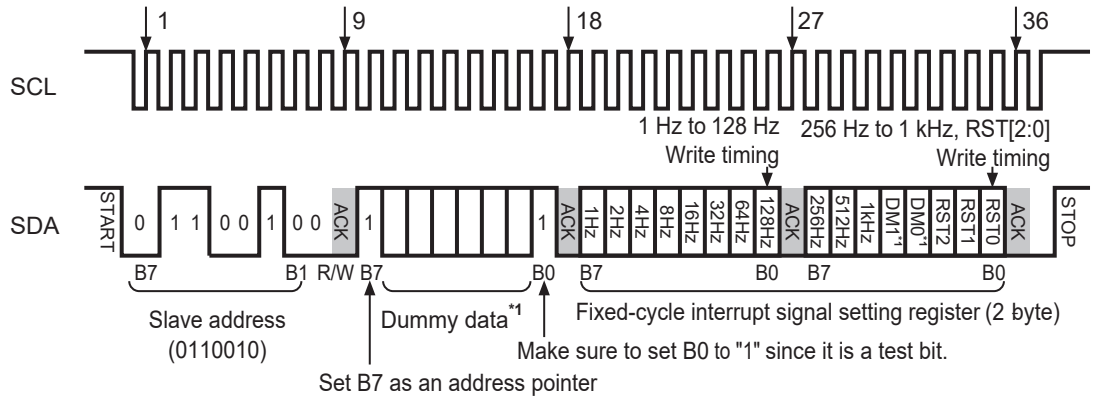


Figure 23 Read Timing of Time Register

6. Write operation of fixed-cycle interrupt signal setting register

Transmit the start condition and slave address from the master device. The slave address of the S-35740 Series is specified to "0110010". Next, transmit "0" to the the read / write bit.
Transmit dummy data to the 2nd byte. However, make sure to set B0 to "1" since it is a test bit.
B7 to B0 in the 3rd byte and B7 to B5 in the 4th byte are used as the fixed-cycle interrupt signal setting register.
Set B6 to B1 in the 2nd byte and B4 to B3 in the 4th byte to "0" or "1" since they are dummy data.
B2 to B0 (RST2 to RST0) in the 4th byte are used as a register to input the timer reset command. The timer is reset when transmitting RST2 = "0", RST1 = "1" and RST0 = "0". When not resetting the timer, transmit the data except for the above mentioned ones, such as RST2 = "1", RST1 = "1" and RST0 = "1" to the fixed-cycle interrupt signal setting register.
Transmit the stop condition from the master device to finish the access operation.
Regarding the fixed-cycle interrupt signal setting register, refer to "■ **Configuration of Registers**".
Write operation of the fixed-cycle interrupt signal setting register is performed each byte, so transmit the data in 2-byte unit. Note that the S-35740 Series may not operate as desired if the data is not transmitted in 2-byte unit.



*1. Set "0" or "1" since they are dummy data.

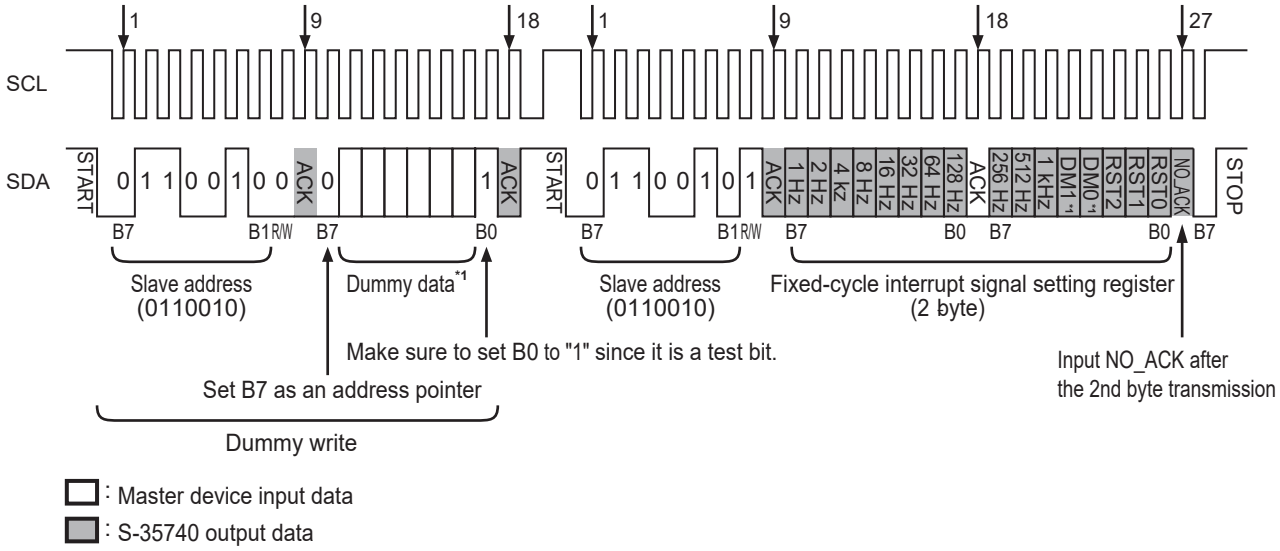
Figure 24 Write Timing of Fixed-cycle Interrupt Signal Setting Register

7. Read operation of fixed-cycle interrupt signal setting register

Perform the read operation of fixed-cycle interrupt signal setting register with the restart format. Regarding the restart format, refer to "**4. Data transmission format**".
When performing the read operation of fixed-cycle interrupt signal setting register, set the ENBL pin to "H". If the ENBL pin is set to "L", the time register data is read.

Transmit the start condition and the slave address from the master device. The slave address of the S-35740 Series is specified to "0110010". Next, transmit "0" to the read / write bit.
B7 in the 2nd byte is an address pointer. Set B7 to "0" when reading the fixed-cycle interrupt signal setting register. Next, transmit the dummy data to B6 to B1. Make sure to set B0 to "1" since it is a test bit. This processing is called "dummy write".
Then transmit the start condition, the slave address and the read / write bit. The data of the fixed-cycle interrupt setting register can be read when the read / write bit is set to "1".
Consequently, the fixed-cycle interrupt signal setting register is output from the S-35740 Series. Each byte from B7 is transmitted.
When the read operation of the fixed-cycle interrupt signal setting register is finished, transmit "1" (NO_ACK) to the acknowledge after B0 output from the master device, and then transmit the stop condition.
The fixed-cycle interrupt signal setting register is a 2-byte register. "1" is read if the read operation is performed continuously after reading 2 bytes of the fixed-cycle interrupt signal setting register.
Regarding the fixed-cycle interrput signal setting register, refer to "■ **Configuration of Registers**".

Moreover, the internal address pointer is reset if recognizing the stop condition. Therefore, do not transmit the stop condition after dummy write operation. The time register is read if performing the read operation of the register after transmitting the stop condition.



*1. Set "0" or "1" since they are dummy data.

Figure 25 Read Timing of Fixed-cycle Interrpt Signal Setting Register

■ Release of SDA

The ENBL pin of the S-35740 Series does not perform the reset operation of the communication interface. Therefore, the stop condition is input to reset the internal interface circuit usually.

However, the S-35740 Series does not accept the stop condition from the master device when in the status that SDA outputs "L" (at the time of acknowledge outputting or reading). Consequently, it is necessary to finish the acknowledge output or read operation. **Figure 26** shows the SDA release method.

First, input the start condition from the master device (since SDA of the S-35740 Series outputs "L", the S-35740 Series can not detect the start condition). Next, input the clocks for 1-byte data access (9 clocks) from SCL. During the time, release SDA of the master device. By this, the SDA input / output before communication interrupt is completed, and SDA of the S-35740 Series becomes release status. Continuously, if the stop condition is input, the internal circuit resets and the communication returns to normal status.

It is strongly recommended that the SDA release method is performed at the time of system initialization after the power supply voltage of the master device rises.

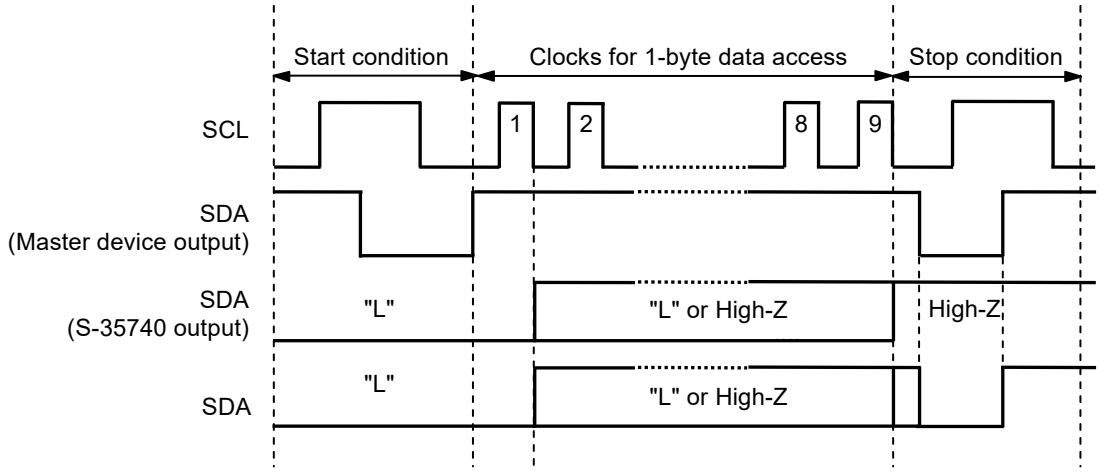
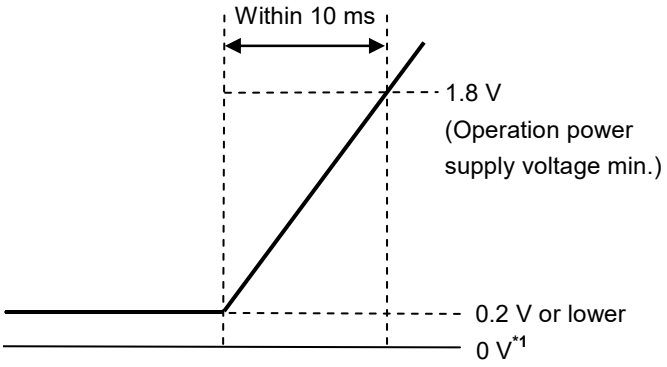


Figure 26 SDA Release Method

■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 27**.



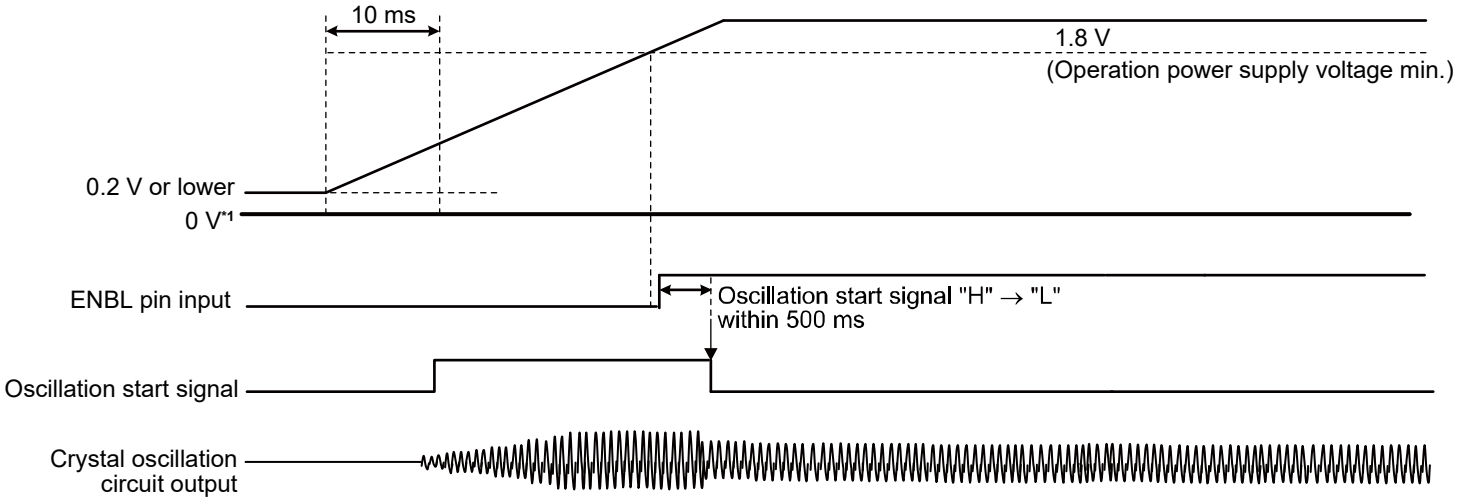
***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35740 Series.

Figure 27 How to Raise the Power Supply Voltage

If the power supply voltage of the S-35740 Series cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start. In such case, perform the operations shown in "**1. When power supply voltage is raised at ENBL pin = "L"** " and "**2. When power supply voltage is raised at ENBL pin = "H"** ".

1. When power supply voltage is raised at ENBL pin = "L"

Set the ENBL pin to "L" until the power supply voltage reaches 1.8 V or higher. While the ENBL pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the ENBL pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.
The current consumption increases by 1.7 μA typ. while the ENBL pin is set to "L".

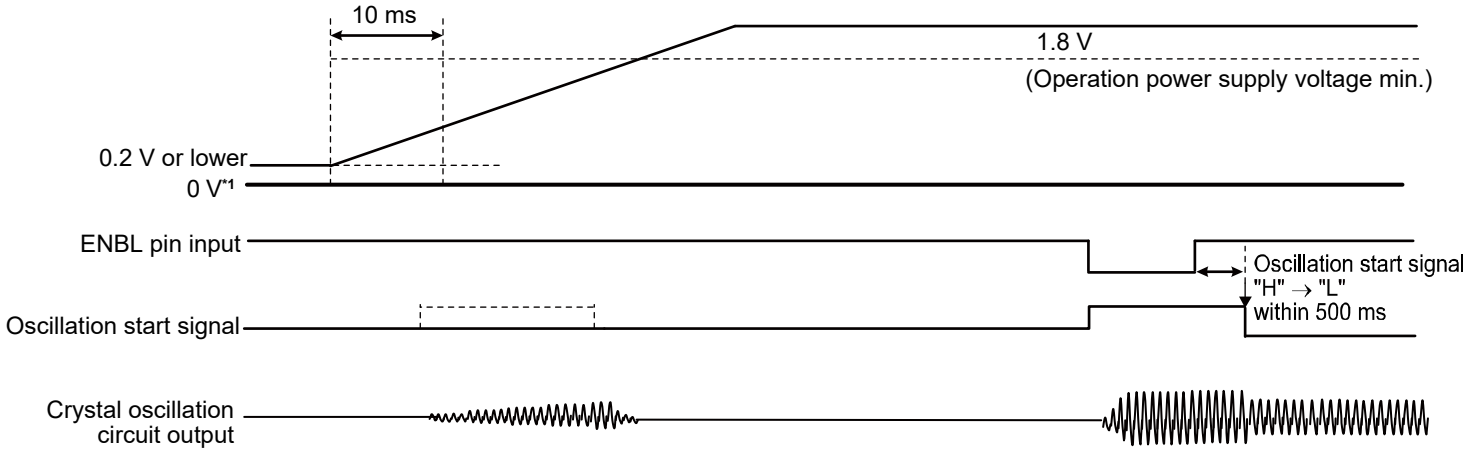


***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35740 Series.

Figure 28 When Power Supply Voltage is Raised at ENBL Pin = "L"

2. When power supply voltage is raised at ENBL pin = "H"

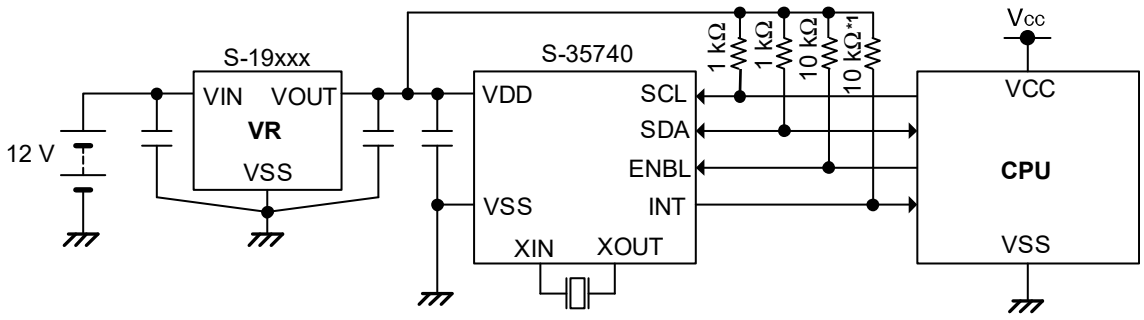
Set the ENBL pin to "L" after the power supply voltage reaches 1.8 V or higher. If the ENBL pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the ENBL pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.
The current consumption increases by 1.7 μA typ. while the ENBL pin is set to "L".



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35740 Series.

Figure 29 When Power Supply Voltage is Raised at ENBL Pin = "H"

■ Example of Application Circuit



***1.** This resistor is unnecessary when a CMOS output product is selected.

Figure 30

Caution 1. Start communication under stable condition after turning on the the system power supply.
2. The above connection diagram does not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Configuration of Crystal Oscillation Circuit

Since the S-35740 Series has built-in capacitors (C_g and C_d), adjustment of oscillation frequency is unnecessary. However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance (C_P), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of the crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35740 Series.
- Place the S-35740 Series and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.
  (In the case of a multi-layer board, only the layer farthest from the oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

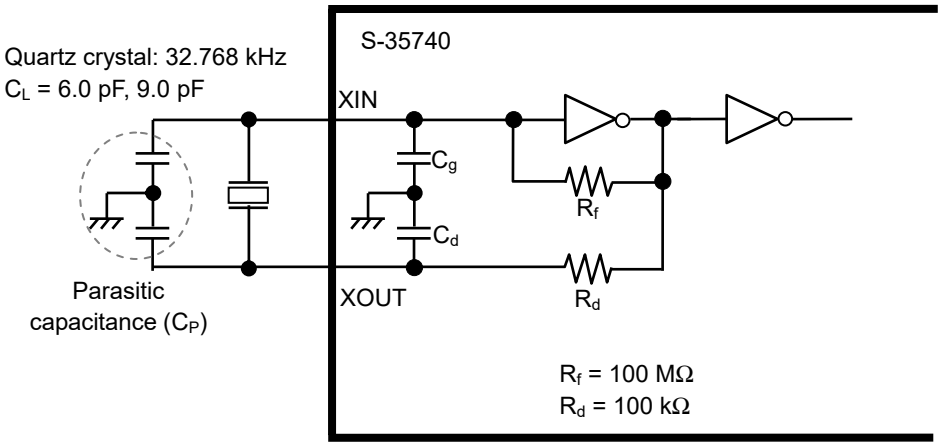


Figure 31 Configuration of Crystal Oscillation Circuit

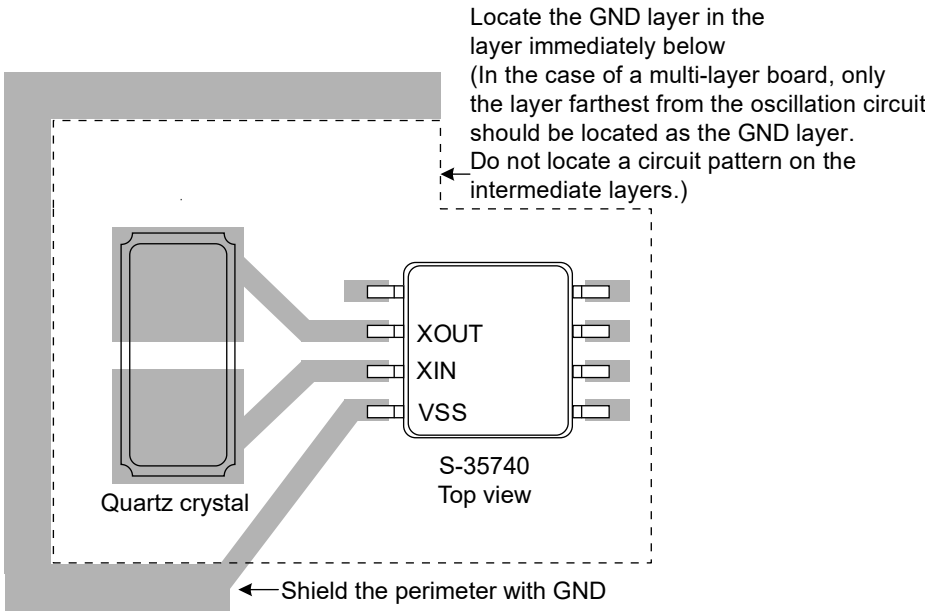


Figure 32 Example of Recommended Connection Pattern Diagram

Caution 1. Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal and external capacitor. When configuring the crystal oscillation circuit, pay sufficient attention for them.

2. When using the product in automobile equipment, select the components which can be automobile carried for each component such as quartz crystal, external capacitor and board.

■ Cautions When Using Quartz Crystal

Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.
Refer to **Table 10** for recommended quartz crystal characteristics values. When using a product in an environment over Ta = +85°C, it is recommended to ensure the oscillation allowance shown in **Table 10** at room temperature.

Table 10 Quartz Crystal Characteristics

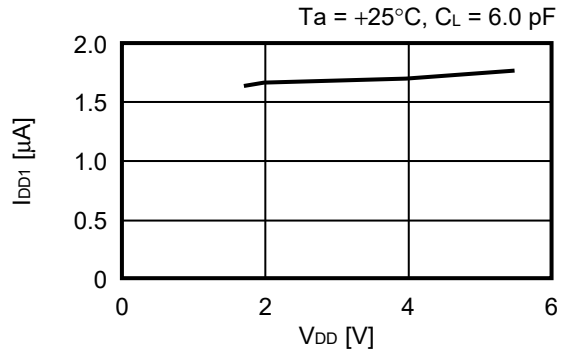
Quartz Crystal C_L Value (Load Capacitance)	R_1 Value (Equivalent Series Resistance)	Oscillation Allowance at Power-on
9.0 pF	80 kΩ max.	5 times or more
6.0 pF	80 kΩ max.	5 times or more

■ Precautions

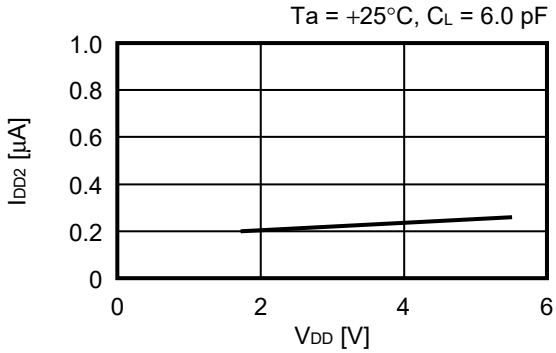
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

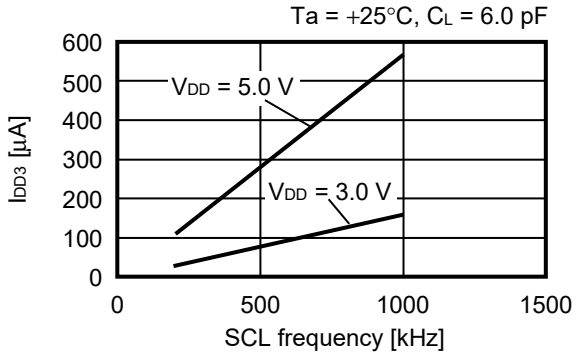
1. Current consumption 1 vs. Power supply voltage characteristics



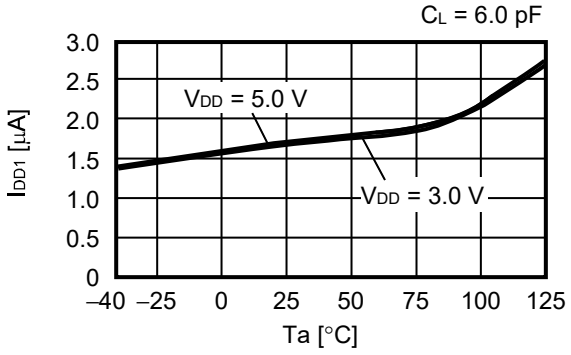
2. Current consumption 2 vs. Power supply voltage characteristics



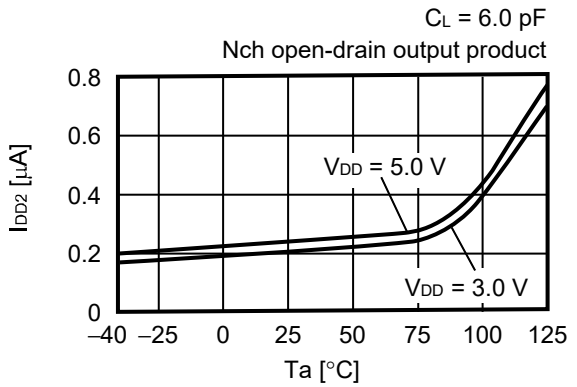
3. Current consumption 3 vs. SCL frequency characteristics



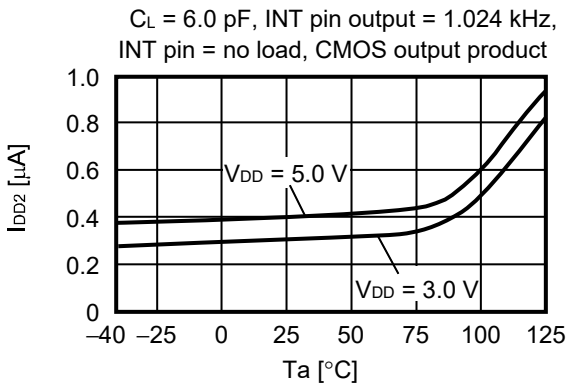
4. Current consumption 1 vs. Temperature characteristics



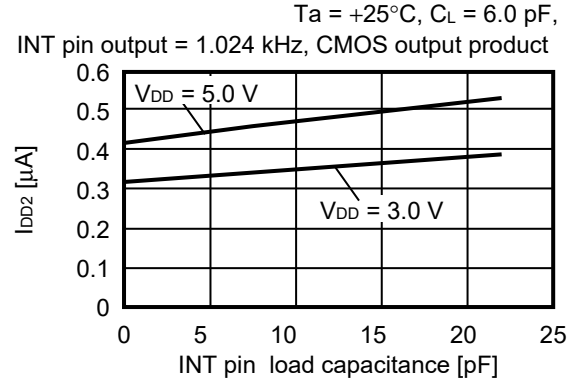
5. Current consumption 2 vs. Temperature characteristics



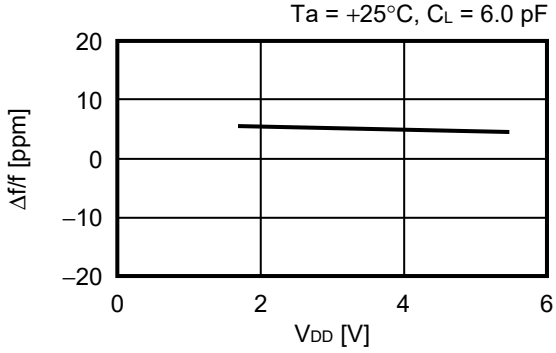
6. Current consumption 2 vs. Temperature characteristics



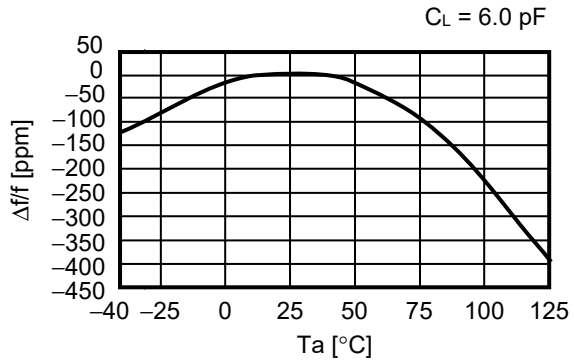
7. Current consumption 2 vs. INT pin load capacitance characteristics



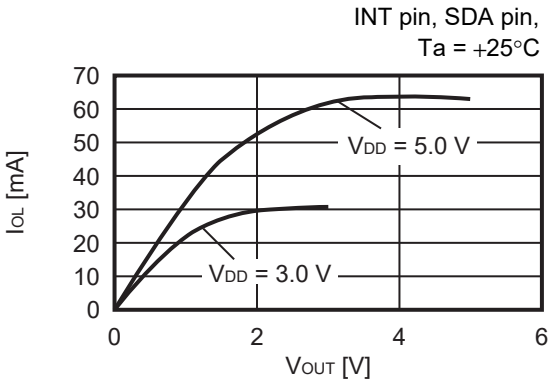
8. Oscillation frequency vs. Power supply voltage characteristics



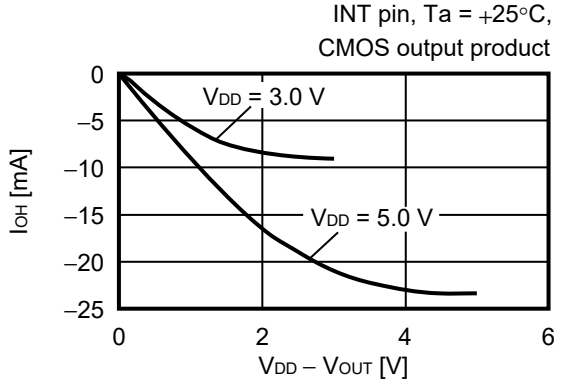
9. Oscillation frequency vs. Temperature characteristics

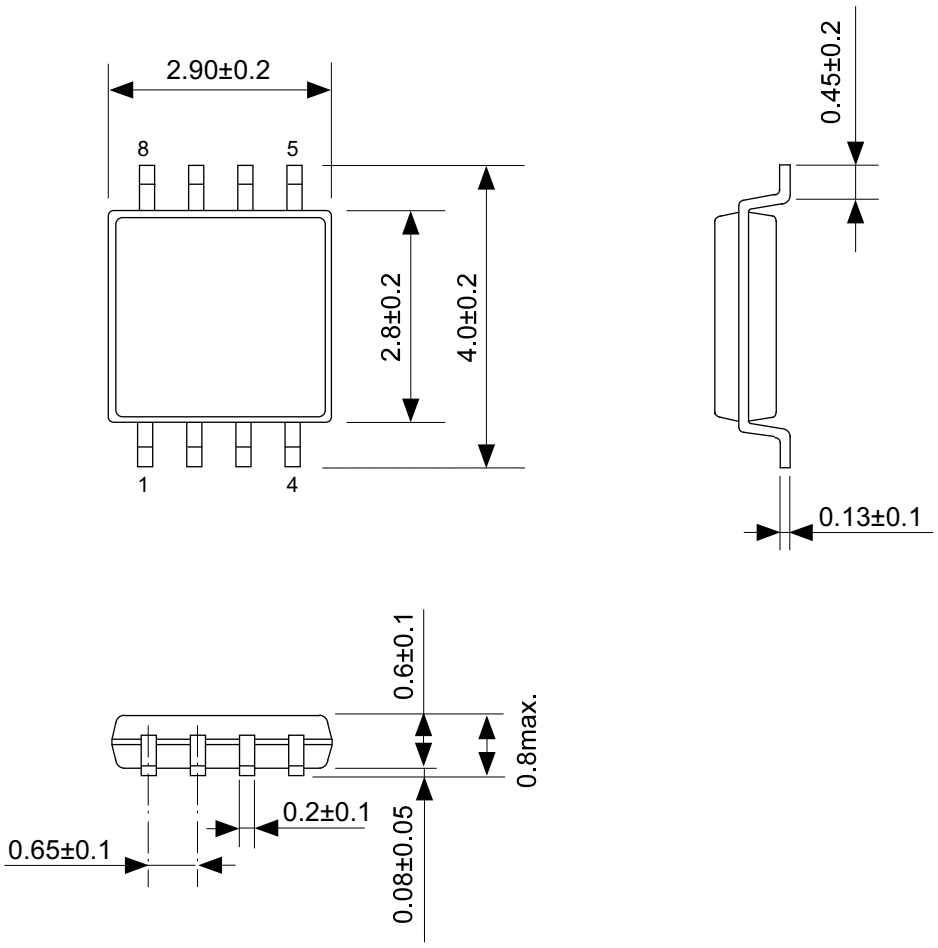


10. Low level output current vs. Output voltage characteristics



11. High level output current vs. $V_{DD} - V_{OUT}$ characteristics





No. FM008-A-P-SD-1.2

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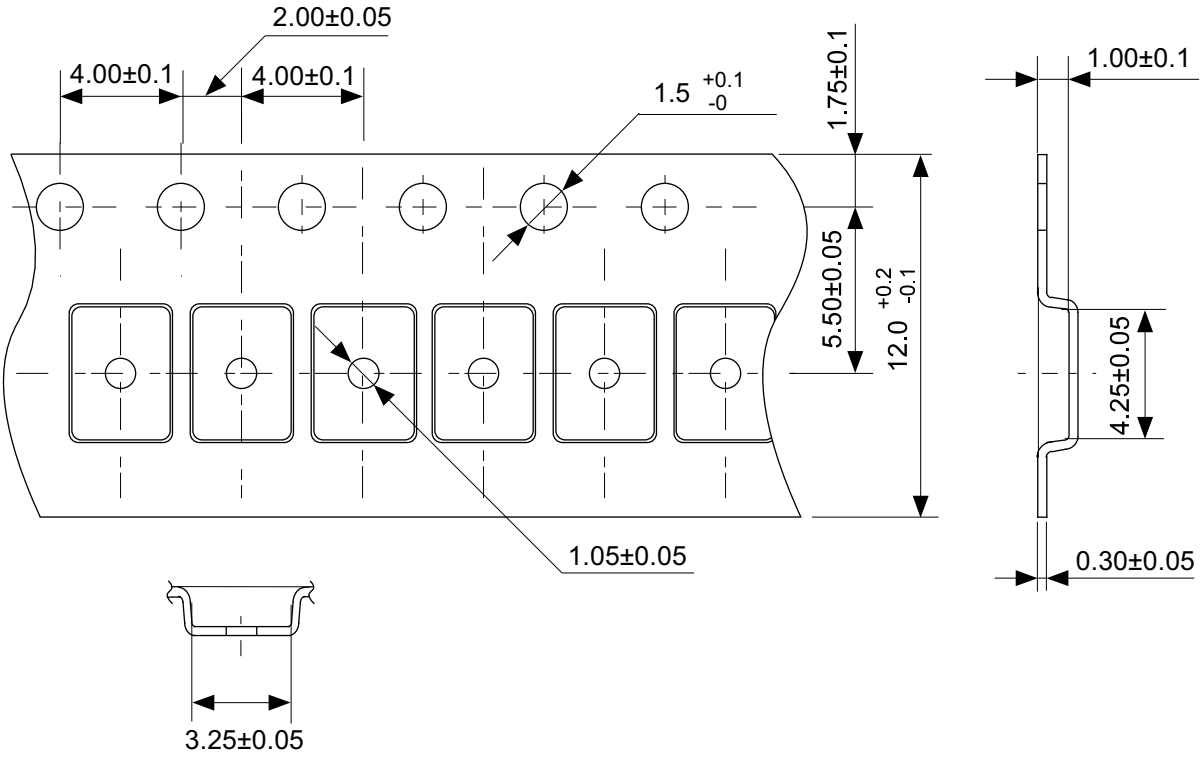
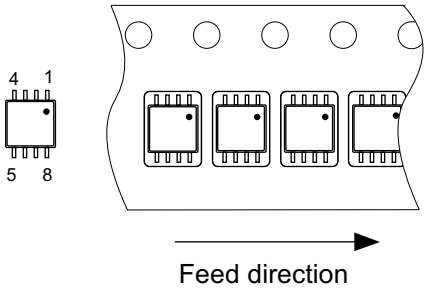
UNIT	mm
ABLIC Inc.	





No. FM008-A-C-SD-2.0

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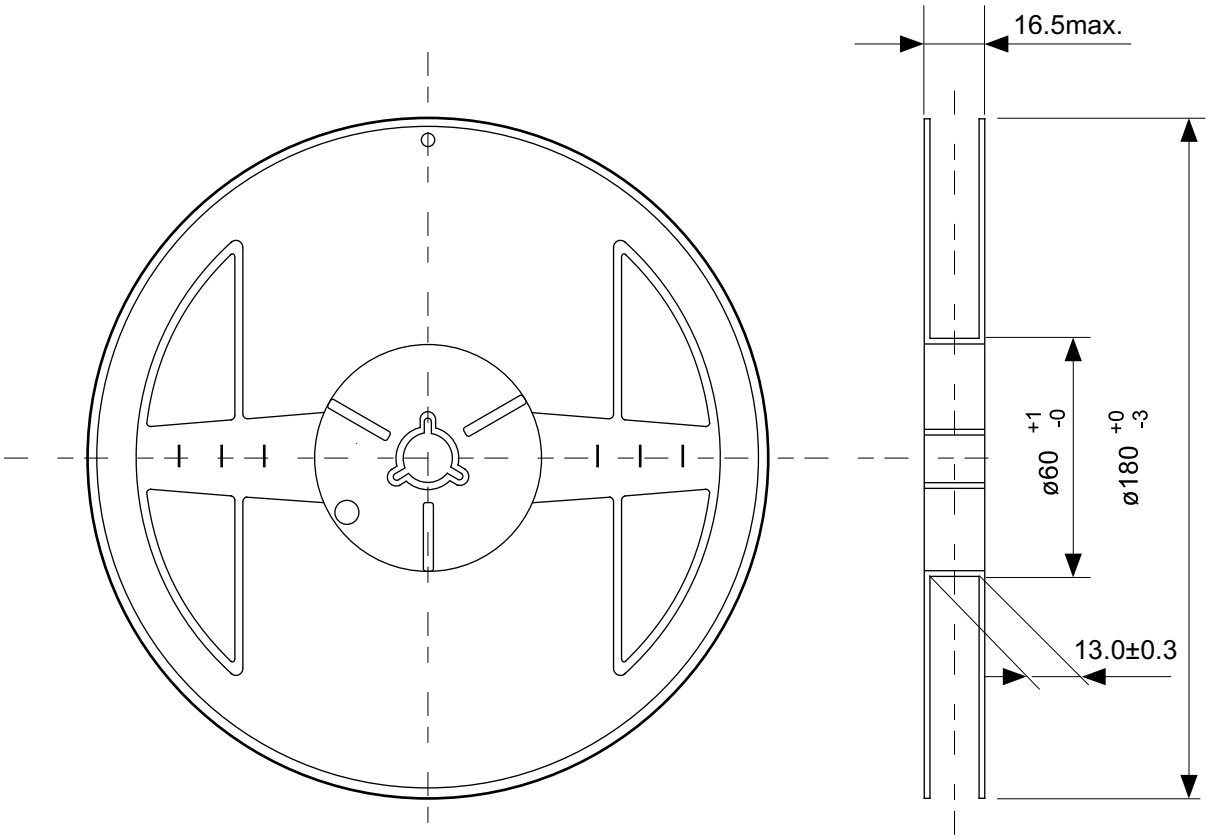
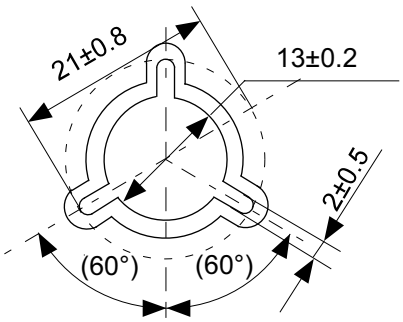
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
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ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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