

NTMS4802N

MOSFET – Power, N-Channel, SO-8 30 V, 18 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- This is a Pb-Free Device

Applications

- DC-DC Converters
- Synchronous MOSFET
- Printers

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	30	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	15	A
		12	
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	1.66	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	11.1	A
		8.9	
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	0.91	W
Continuous Drain Current $R_{\theta JA}$, $t \leq 10$ s (Note 1)	I_D	18	A
		15	
Power Dissipation $R_{\theta JA}$, $t \leq 10$ s (Note 1)	P_D	2.5	W
Pulsed Drain Current	I_{DM}	60	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	2.5	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 29$ A _{pk} , $L = 1.0$ mH, $R_G = 25$ Ω)	E_{AS}	420	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

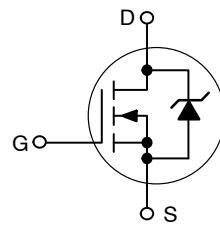
ON

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	4.0 m Ω @ 10 V	
	5.5 m Ω @ 4.5 V	18 A

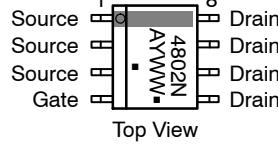
N-Channel



MARKING DIAGRAM/ PIN ASSIGNMENT



1
SO-8
CASE 751
STYLE 12



Top View

4802N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMS4802NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	75.5	°C/W
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	50.5	
Junction-to-Foot (Drain)	$R_{\theta JF}$	22	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	138	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surfacemounted on FR4 board using 1 in² pad size.
2. Surfacemounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0$ V, $I_D = 250$ μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}/T_J}$			26		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0$ V, $V_{\text{DS}} = 24$ V	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 85^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0$ V, $V_{\text{GS}} = \pm 20$ V			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250$ μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})/T_J}$			7.0		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10$ V, $I_D = 18$ A		3.2	4.0	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5$ V, $I_D = 15$ A		4.3	5.5	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 1.5$ V, $I_D = 18$ A		55		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{\text{GS}} = 0$ V, $f = 1.0$ MHz, $V_{\text{DS}} = 25$ V		5300		pF
Output Capacitance	C_{oss}			880		
Reverse Transfer Capacitance	C_{rss}			460		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 4.5$ V, $V_{\text{DS}} = 15$ V, $I_D = 18$ A		36		nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			6.5		
Gate-to-Source Charge	Q_{GS}			14		
Gate-to-Drain Charge	Q_{GD}			13		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10$ V, $V_{\text{DS}} = 15$ V, $I_D = 18$ A		75		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10$ V, $V_{\text{DS}} = 15$ V, $I_D = 1.0$ A, $R_{\text{G}} = 6.0$ Ω		18		ns
Rise Time	t_r			42		
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			70		
Fall Time	t_f			56		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0$ V, $I_S = 2.5$ A	$T_J = 25^\circ\text{C}$	0.7	1.0	V
			$T_J = 125^\circ\text{C}$	0.6		

NTMS4802N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE DIODE CHARACTERISTICS

Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 2.5 A	40		ns
Charge Time	t _a		20		
Discharge Time	t _b		20		
Reverse Recovery Charge	Q _{RR}		40		

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C	0.66		nH
Drain Inductance	L _D		0.20		nH
Gate Inductance	L _G		1.5		nH
Gate Resistance	R _G		1.0	1.5	Ω

3. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

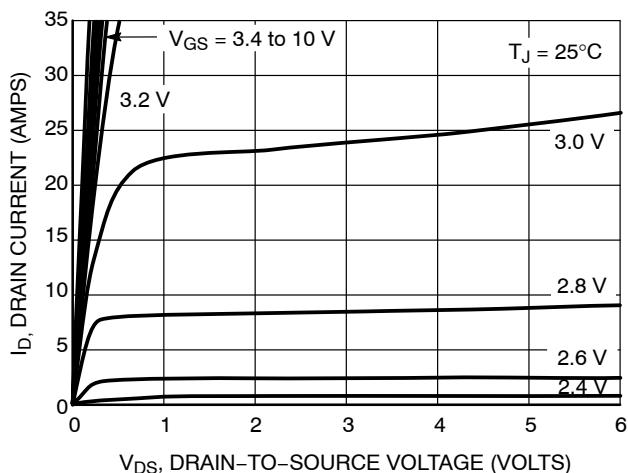


Figure 1. On-Region Characteristics

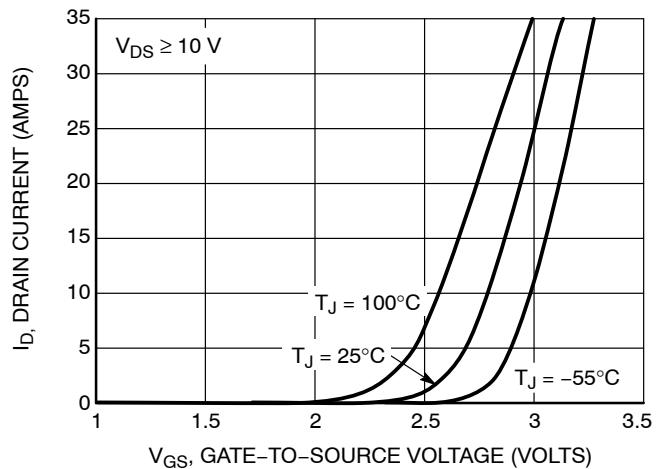


Figure 2. Transfer Characteristics

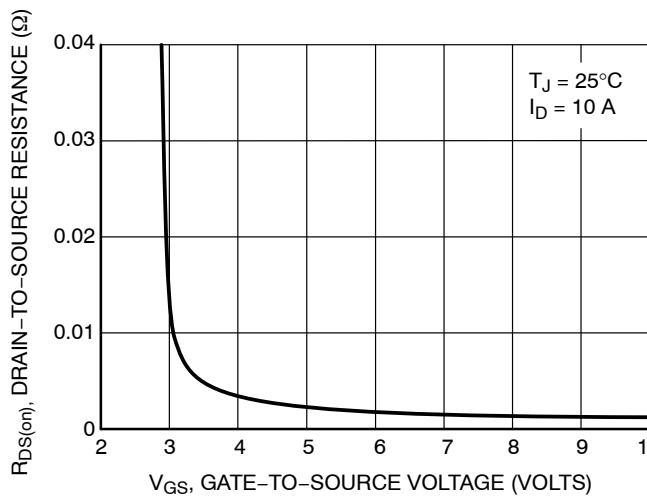


Figure 3. On-Resistance vs. Gate-to-Source Voltage

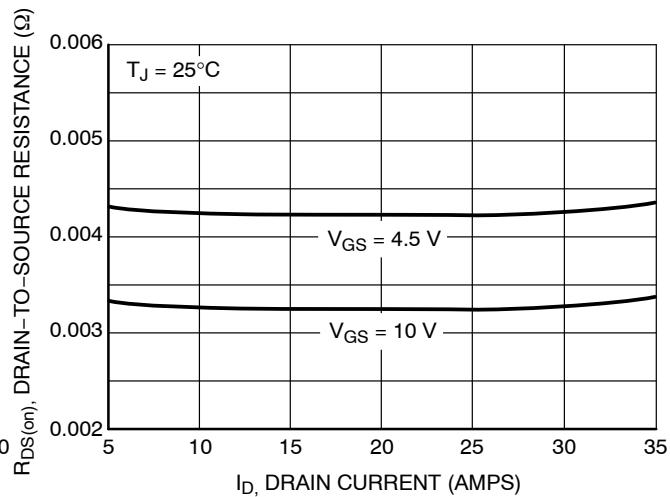


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

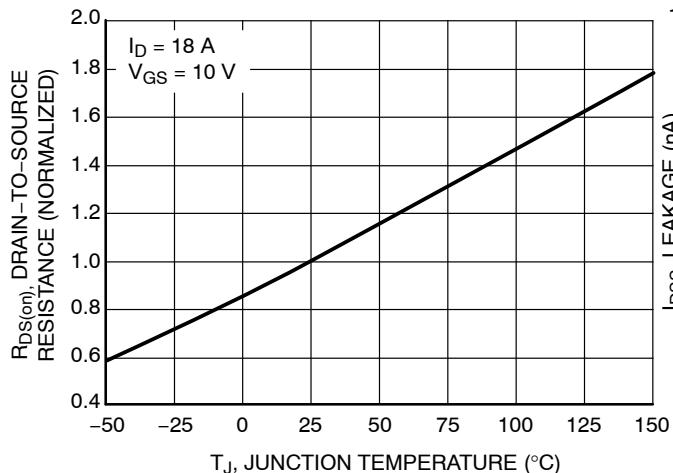


Figure 5. On-Resistance Variation with Temperature

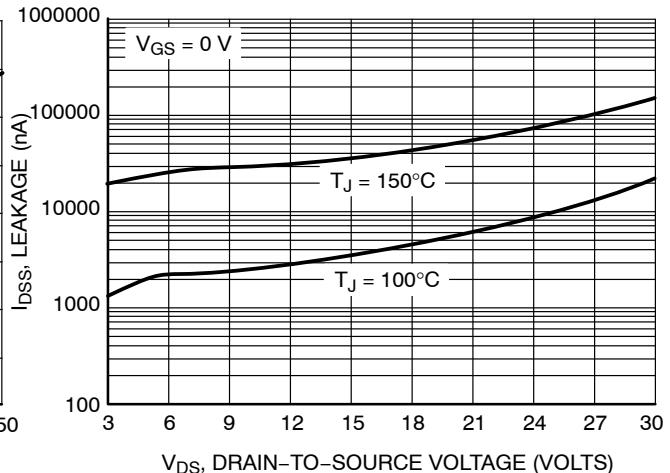
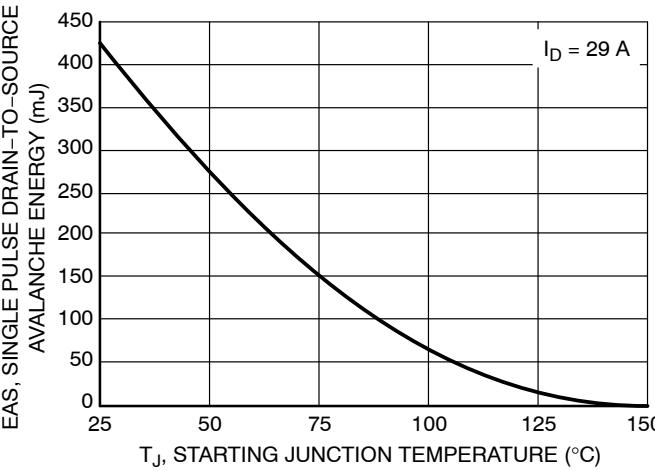
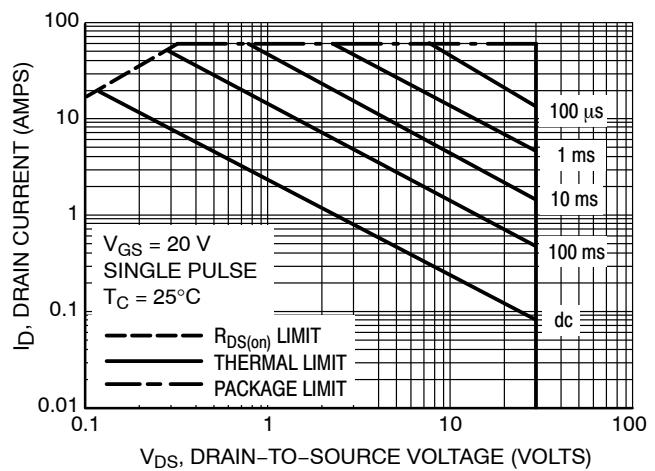
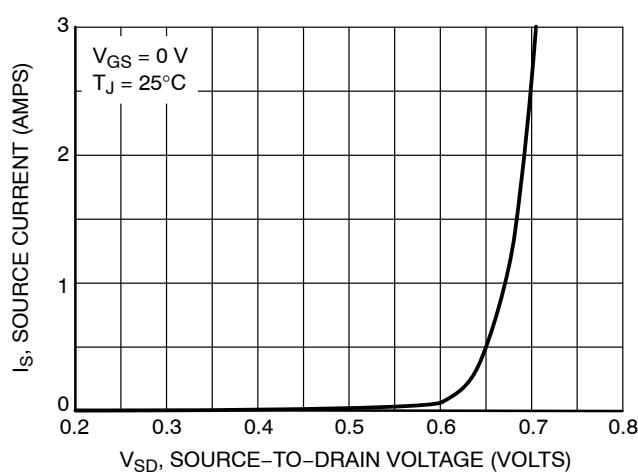
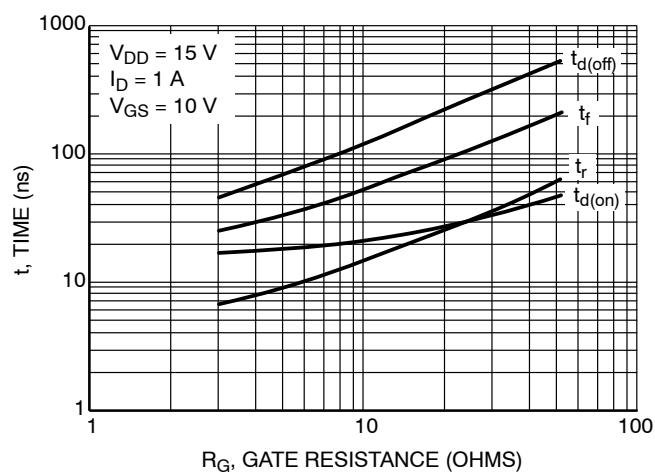
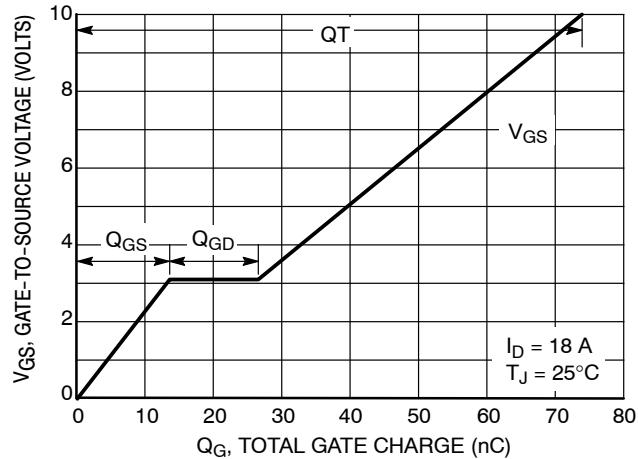
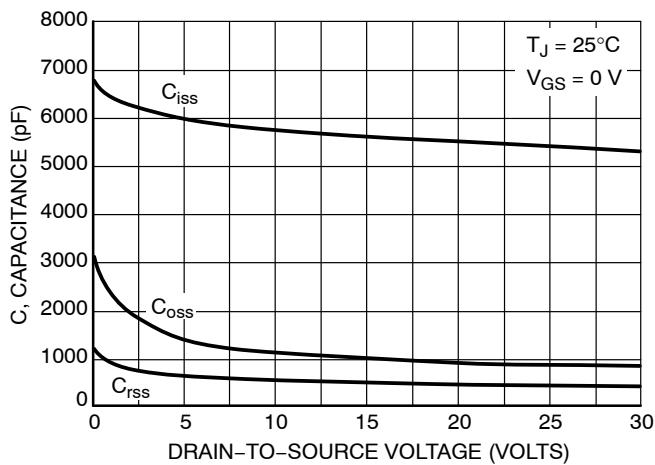


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

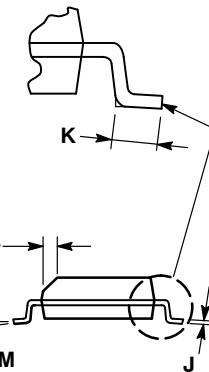
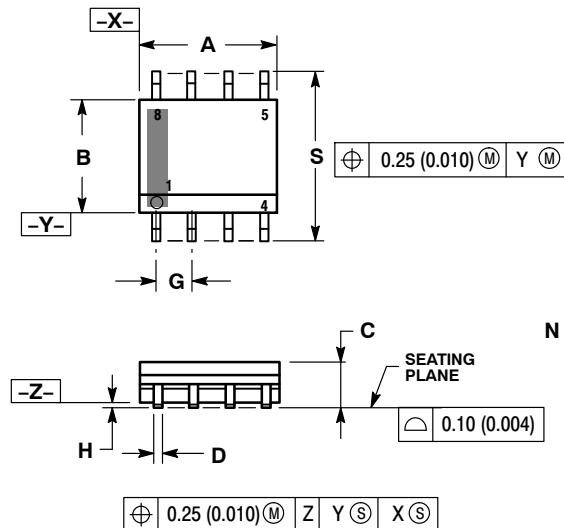




SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

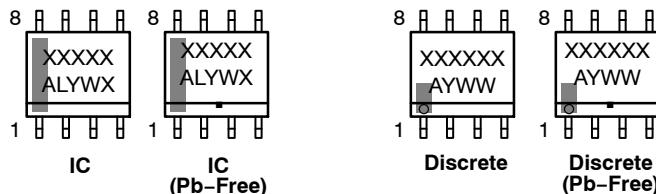
DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*

XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. Emitter 2. Collector 3. Collector 4. Emitter 5. Emitter 6. Base 7. Base 8. Emitter	STYLE 2: PIN 1. Collector, Die #1 2. Collector, #1 3. Collector, #2 4. Collector, #2 5. Base, #2 6. Emitter, #2 7. Base, #1 8. Emitter, #1	STYLE 3: PIN 1. Drain, Die #1 2. Drain, #1 3. Drain, #2 4. Drain, #2 5. Gate, #2 6. Source, #2 7. Gate, #1 8. Source, #1	STYLE 4: PIN 1. Anode 2. Anode 3. Anode 4. Anode 5. Anode 6. Anode 7. Anode 8. Common Cathode
STYLE 5: PIN 1. Drain 2. Drain 3. Drain 4. Drain 5. Gate 6. Gate 7. Source 8. Source	STYLE 6: PIN 1. Source 2. Drain 3. Drain 4. Source 5. Source 6. Gate 7. Gate 8. Source	STYLE 7: PIN 1. Input 2. External Bypass 3. Third Stage Source 4. Ground 5. Drain 6. Gate 3 7. Second Stage Vd 8. First Stage Vd	STYLE 8: PIN 1. Collector, Die #1 2. Base, #1 3. Base, #2 4. Collector, #2 5. Collector, #2 6. Emitter, #2 7. Emitter, #1 8. Collector, #1
STYLE 9: PIN 1. Emitter, Common 2. Collector, Die #1 3. Collector, Die #2 4. Emitter, Common 5. Emitter, Common 6. Base, Die #2 7. Base, Die #1 8. Emitter, Common	STYLE 10: PIN 1. Ground 2. Bias 1 3. Output 4. Ground 5. Ground 6. Bias 2 7. Input 8. Ground	STYLE 11: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Drain 2 7. Drain 1 8. Drain 1	STYLE 12: PIN 1. Source 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 13: PIN 1. N.C. 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain	STYLE 14: PIN 1. N-Source 2. N-Gate 3. P-Source 4. P-Gate 5. P-Drain 6. P-Drain 7. N-Drain 8. N-Drain	STYLE 15: PIN 1. Anode 1 2. Anode 1 3. Anode 1 4. Anode 1 5. Cathode, Common 6. Cathode, Common 7. Cathode, Common 8. Cathode, Common	STYLE 16: PIN 1. Emitter, Die #1 2. Base, Die #1 3. Emitter, Die #2 4. Base, Die #2 5. Collector, Die #2 6. Collector, Die #2 7. Collector, Die #1 8. Collector, Die #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. Anode 2. Anode 3. Source 4. Gate 5. Drain 6. Drain 7. Cathode 8. Cathode	STYLE 19: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Mirror 2 7. Drain 1 8. Mirror 1	STYLE 20: PIN 1. Source (N) 2. Gate (N) 3. Source (P) 4. Gate (P) 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 21: PIN 1. Cathode 1 2. Cathode 2 3. Cathode 3 4. Cathode 4 5. Cathode 5 6. Common Anode 7. Common Anode 8. Cathode 6	STYLE 22: PIN 1. I/O Line 1 2. Common Cathode/VCC 3. Common Cathode/VCC 4. I/O Line 3 5. Common Anode/GND 6. I/O Line 4 7. I/O Line 5 8. Common Anode/GND	STYLE 23: PIN 1. Line 1 IN 2. Common Anode/GND 3. Common Anode/GND 4. Line 2 IN 5. Line 2 OUT 6. Common Anode/GND 7. Common Anode/GND 8. Line 1 OUT	STYLE 24: PIN 1. Base 2. Emitter 3. Collector/Anode 4. Collector/Anode 5. Cathode 6. Cathode 7. Collector/Anode 8. Collector/Anode
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. Enable 4. ILIMIT 5. Source 6. Source 7. Source 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBUCK 7. VBUCK 8. VIN
STYLE 29: PIN 1. Base, Die #1 2. Emitter, #1 3. Base, #2 4. Emitter, #2 5. Collector, #2 6. Collector, #2 7. Collector, #1 8. Collector, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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