

Dual-Channel Digital Isolator

FEATURES

- ▶ Narrow body, RoHS-compliant, 8-lead SOIC
- ▶ Low power operation
 - ▶ 5 V operation
 - ▶ 1.1 mA per channel maximum @ 0 Mbps to 2 Mbps
 - ▶ 3.7 mA per channel maximum @ 10 Mbps
 - ▶ 3 V operation
 - ▶ 0.8 mA per channel maximum @ 0 Mbps to 2 Mbps
 - ▶ 2.2 mA per channel maximum @ 10 Mbps
- ▶ 3 V/5 V level translation
- ▶ High temperature operation: 105°C
- ▶ High data rate: dc to 10 Mbps (NRZ)
- ▶ Precise timing characteristics
 - ▶ 3 ns maximum pulse width distortion
 - ▶ 3 ns maximum channel-to-channel matching
- ▶ High common-mode transient immunity: >25 kV/μs
- ▶ Safety and regulatory approvals
 - ▶ UL 1577
 - ▶ $V_{ISO} = 2500 V_{RMS}$ for 1 minute
 - ▶ IEC/EN/CSA 62368-1
 - ▶ IEC/CSA 61010-1
 - ▶ CQC GB4943.1
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ $V_{IORM} = 560 V_{PEAK}$

APPLICATIONS

- ▶ Size-critical multichannel isolation
- ▶ SPI interface/data converter isolation
- ▶ RS-232/RS-422/RS-485 transceiver isolation
- ▶ Digital field bus isolation
- ▶ Gate drive interface

FUNCTIONAL BLOCK DIAGRAM

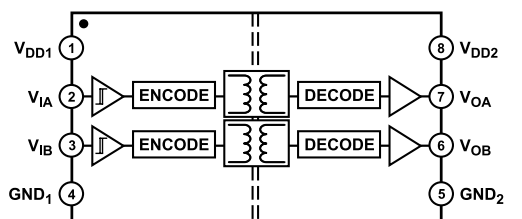


Figure 1.

GENERAL DESCRIPTION

The ADuM1210¹ is a dual-channel, digital isolator based on Analog Devices, Inc., iCoupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, iCoupler devices remove the design difficulties commonly associated with optocouplers. The concerns of the typical optocoupler regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple iCoupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with iCoupler products. Furthermore, iCoupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM1210 isolator provides two independent isolation channels operable with the supply voltage on either side, ranging from 2.7 V to 5.5 V. This provides compatibility with lower voltage systems and enables voltage translation functionality across the isolation barrier. In addition, the ADuM1210 provides low pulse width distortion (<3 ns) and tight channel-to-channel matching (<3 ns). Unlike other optocoupler alternatives, the ADuM1210 isolator has a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions. Furthermore, as an alternative to the ADuM1200 dual-channel digital isolator that defaults to an output high condition, the ADuM1210 outputs default to a logic low state when input power is off.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329.

TABLE OF CONTENTS

Features.....	1	ESD Caution.....	10
Applications.....	1	Maximum Continuous Working Voltage.....	10
Functional Block Diagram.....	1	Pin Configuration and Function Descriptions.....	11
General Description.....	1	Typical Performance Characteristics.....	12
Specifications.....	3	Applications Information.....	13
Electrical Characteristics—5 V Operation.....	3	PC Board Layout.....	13
Electrical Characteristics—3 V Operation.....	4	Propagation Delay-Related Parameters.....	13
Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation.....	5	DC Correctness and Magnetic Field Immunity.....	13
Package Characteristics.....	7	Power Consumption.....	14
Regulatory Information.....	7	Insulation Lifetime.....	14
Insulation and Safety-Related Specifications.....	8	Outline Dimensions.....	15
DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics.....	8	Ordering Guide.....	15
Recommended Operating Conditions.....	9	Number of Inputs, Maximum Data Rate, Maximum Propagation Delay, and Maximum Pulse Width Distortion Options.....	15
Absolute Maximum Ratings.....	10		

REVISION HISTORY**3/2025—Rev. D to Rev. E**

Changes to Features Section.....	1
Changes to Regulatory Information Section and Table 5.....	7
Changes to Table 6.....	8
Changed DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section.....	8
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section and Table 7.....	8
Changes to Figure 2 Caption.....	9
Changes to Table 10.....	10
Changes to Insulation Lifetime Section.....	14
Deleted Figure 12 to Figure 14.....	14
Added Number of Inputs, Maximum Data Rate, Maximum Propagation Delay, and Maximum Pulse Width Distortion Options.....	15

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. All voltages are relative to their respective ground.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DD1(Q)}$		0.50	0.60	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$		0.19	0.25	mA	
Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1(10)}$		4.3	5.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(10)}$		1.3	2.0	mA	5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0\text{ V} \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	5.0		V	$I_{OX} = -20\text{ }\mu\text{A}$, $V_{IX} = V_{IXH}$
		$V_{DD2} - 0.5$	4.8		V	$I_{OX} = -4\text{ mA}$, $V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}$, $V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400\text{ }\mu\text{A}$, $V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4\text{ mA}$, $V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
Minimum Pulse Width ²	PW			100	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Maximum Data Rate ³		10			Mbps	$C_L = 15\text{ pF}$, CMOS signal levels
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		50	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/ $^\circ\text{C}$	$C_L = 15\text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁵	t_{PSK}			15	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t_{PSKCD}			3	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁶	t_{PSKOD}			15	ns	$C_L = 15\text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	$C_L = 15\text{ pF}$, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁷	$ CM_H $	25	35		kV/ μs	$V_{IX} = V_{DD1}$, $V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁷	$ CM_L $	25	35		kV/ μs	$V_{IX} = 0\text{ V}$, $V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current, per Channel ⁸	$I_{DD1(D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	$I_{DDO(D)}$		0.05		mA/Mbps	

¹ Supply current values are for both channels running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the [Power Consumption](#) section. See [Figure 4](#) through [Figure 6](#) for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See [Figure 7](#) and [Figure 8](#) for total V_{DD1} and V_{DD2} supply currents as a function of data rate.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

SPECIFICATIONS

- ³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
- ⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.
- ⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- ⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
- ⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
- ⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

$2.7 V \leq V_{DD1} \leq 3.6 V$, $2.7 V \leq V_{DD2} \leq 3.6 V$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ C$, $V_{DD1} = V_{DD2} = 3.0 V$. All voltages are relative to their respective ground.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DD1(Q)}$		0.26	0.35	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$		0.11	0.20	mA	
Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1(10)}$		2.2	3.4	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(10)}$		0.7	1.1	mA	5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 V \leq V_{IA}, V_{IB}, \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	3.0		V	$I_{OX} = -20 \mu A, V_{IX} = V_{IXH}$
		$V_{DD2} - 0.5$	2.8		V	$I_{OX} = -4 \mu A, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	$I_{OX} = 20 \mu A, V_{IX} = V_{IXL}$
			0.04	0.1	V	$I_{OX} = 400 \mu A, V_{IX} = V_{IXL}$
			0.2	0.4	V	$I_{OX} = 4 \mu A, V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
Minimum Pulse Width ²	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ³		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁴	t_{PHL}, t_{PLH}	20		60	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁵	t_{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t_{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁶	t_{PSKOD}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	$C_L = 15$ pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output ⁷	$ CM_H $	25	35		kV/ μ s	$V_{IX} = V_{DD1}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁷	$ CM_L $	25	35		kV/ μ s	$V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current, per Channel ⁸	$I_{DDI(D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	$I_{DDO(D)}$		0.03		mA/Mbps	

¹ The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the [Power Consumption](#) section. See [Figure 4](#) through [Figure 6](#) for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See [Figure 7](#) and [Figure 8](#) for total V_{DD1} and V_{DD2} supply currents as a function of data rate.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See [Figure 4](#) through [Figure 6](#) for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the [Power Consumption](#) section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$. 3 V/5 V operation: $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.0\text{ V}$, $V_{DD2} = 5.0\text{ V}$; or $V_{DD1} = 5.0\text{ V}$, $V_{DD2} = 3.0\text{ V}$. All voltages are relative to their respective ground.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI(Q)}$				mA	
5 V/3 V Operation			0.50	0.6	mA	
3 V/5 V Operation			0.26	0.35	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$				mA	
5 V/3 V Operation			0.11	0.20	mA	
3 V/5 V Operation			0.19	0.25	mA	
Total Supply Current, Two Channels ¹						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			1.1	1.4	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			0.6	1.0	mA	DC to 1 MHz logic signal frequency

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.2	0.6	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			0.5	0.8	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1(10)}$					
5 V/3 V Operation			4.3	5.5	mA	5 MHz logic signal frequency
3 V/5 V Operation			2.2	3.4	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(10)}$					
5 V/3 V Operation			0.7	1.1	mA	5 MHz logic signal frequency
3 V/5 V Operation			1.3	2.0	mA	5 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 V \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$ $V_{DD2} - 0.5$	V_{DD2} $V_{DD2} - 0.2$		V V	$I_{OX} = -20 \mu A, V_{IX} = V_{IXH}$ $I_{OX} = -4 \text{ mA}, V_{IX} = V_{IXH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0 0.04 0.2	0.1 0.1 0.4	V V V	$I_{OX} = 20 \mu A, V_{IX} = V_{IXL}$ $I_{OX} = 400 \mu A, V_{IX} = V_{IXL}$ $I_{OX} = 4 \text{ mA}, V_{IX} = V_{IXL}$
SWITCHING SPECIFICATIONS						
Minimum Pulse Width ²	PW			100	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Maximum Data Rate ³		10			Mbps	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay ⁴	t_{PHL}, t_{PLH}	15		55	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴	PWD			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Change vs. Temperature			5		ps/ $^{\circ}C$	$C_L = 15 \text{ pF}$, CMOS signal levels
Propagation Delay Skew ⁵	t_{PSK}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels ⁶	t_{PSKCD}			3	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels ⁶	t_{PSKOD}			22	ns	$C_L = 15 \text{ pF}$, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					$C_L = 15 \text{ pF}$, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output ⁷	$ CM_H $	25	35		kV/ μs	$V_{IX} = V_{DD1}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output ⁷	$ CM_L $	25	35		kV/ μs	$V_{IX} = 0 \text{ V}, V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel ⁸	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel ⁸	$I_{DDO(D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

¹ The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the [Power Consumption](#) section. See [Figure 4](#) through

SPECIFICATIONS

Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 7 and Figure 8 for total V_{DD1} and V_{DD2} supply currents as a function of data rate.

- ² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
- ³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
- ⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.
- ⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
- ⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
- ⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 V$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
- ⁸ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the [Power Consumption](#) section for guidance on calculating per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) ¹	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output) ¹	C_{I-O}		1.0		pF	$f = 1 \text{ MHz}$
Input Capacitance ²	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance						
Side 1	θ_{JCI}		46		$^{\circ}\text{C/W}$	Thermocouple located at center of package underside
Side 2	θ_{JCO}		41		$^{\circ}\text{C/W}$	

¹ The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM1210 certification approvals are listed in Table 5. See Table 10 and the [Insulation Lifetime](#) section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

UL	CSA	CQC	VDE
UL 1577 ¹ Single Protection, 2500 V_{RMS}	IEC/EN/CSA 62368-1 Basic insulation, 400 V_{RMS} Reinforced insulation, 150 V_{RMS} IEC/CSA 61010-1 Basic insulation, 300 V_{RMS} Reinforced insulation, 150 V_{RMS}	CQC GB4943.1 Basic insulation, 400 V_{RMS} Reinforced insulation, 150 V_{RMS}	DIN EN IEC 60747-17 (VDE 0884-17) ² Reinforced insulation, 560 V_{PEAK}
File E214100	File No. 205078	Certificate No. CQC16001151061	Certificate No. 40011599

¹ In accordance with UL 1577, each ADuM1210 is proof-tested by applying an insulation test voltage $\geq 3000 V_{RMS}$ for 1 second (current leakage detection limit = 5 μA).

² In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM1210 is proof-tested by applying an insulation test voltage $\geq 1050 V_{PEAK}$ for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

SPECIFICATIONS

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V _{RMS}	1-minute duration
Minimum External Air Gap (Clearance) ^{1, 2}	L(I01)	4.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage) ¹	L(I02)	4.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index) ³	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

¹ In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

² Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

³ CTI rating for the ADuM1210 is >400 V and a Material Group II isolation group.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. Note that the asterisk (*) marked on the package denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V _{RMS}			I to IV	
For Rated Mains Voltage ≤ 300 V _{RMS}			I to III	
For Rated Mains Voltage ≤ 400 V _{RMS}			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V _{IORM}	560	V _{PEAK}
Maximum Working Isolation Voltage		V _{IOWM}	396	V _{RMS}
Input-to-Output Test Voltage, Method B1	V _{IORM} × 1.875 = V _{PR} , 100% production test, t _m = 1 sec, partial discharge < 5 pC	V _{PR}	1050	V _{PEAK}
Input-to-Output Test Voltage, Method A	V _{IORM} × 1.6 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC	V _{PR}		
After Environmental Tests Subgroup 1			896	V _{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC		672	V _{PEAK}
Maximum Transient Isolation Voltage	V _{TEST} = 1.2 × V _{IOTM} , t = 1 sec (100% production)	V _{IOTM}	4000	V _{PEAK}
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V _{IMP}	4000	V _{PEAK}
Maximum Surge Isolation Voltage	V _{TEST} ≥ 1.3 × V _{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5	V _{IOSM}	10,000	V _{PEAK}
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 2			
Case Temperature		T _S	150	°C
Side 1 Current		I _{S1}	160	mA
Side 2 Current		I _{S2}	170	mA
Insulation Resistance at T _S	V _{IO} = 500 V	R _S	>10 ⁹	Ω

SPECIFICATIONS

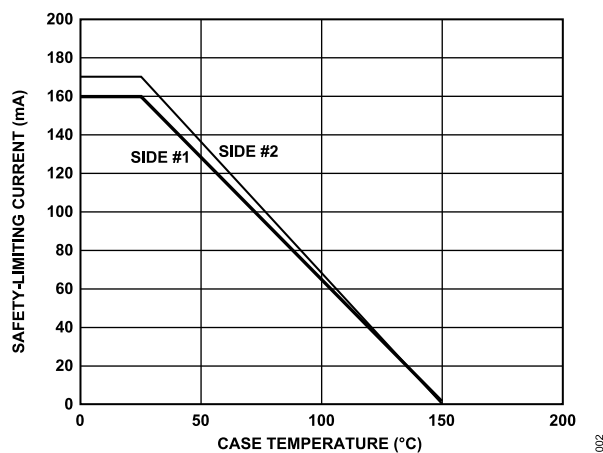


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN EN IEC 60747-17 (VDE 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-40	+105	°C
Supply Voltages ¹	V_{DD1}, V_{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

¹ All voltages are relative to their respective ground. See the [DC Correctness and Magnetic Field Immunity](#) section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 9.

Parameter	Rating
Storage Temperature (T_{ST}) Range	-55°C to $+150^\circ\text{C}$
Ambient Operating Temperature(T_A) Range	-40°C to $+105^\circ\text{C}$
Supply Voltages (V_{DD1} , V_{DD2}) ¹	-0.5 V to $+7.0\text{ V}$
Input Voltage (V_{IA} , V_{IB}) ¹	-0.5 V to $V_{DDI} + 0.5\text{ V}$
Output Voltage (V_{OA} , V_{OB}) ¹	-0.5 V to $V_{DDO} + 0.5\text{ V}$
Average Output Current, Per Pin (I_O) ²	-35 mA to $+35\text{ mA}$
Common-Mode Transients (CM_L , CM_H) ³	$-100\text{ kV}/\mu\text{s}$ to $+100\text{ kV}/\mu\text{s}$

¹ All voltages are relative to their respective ground.

² See Figure 2 for maximum rated current values for various temperatures.

³ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating may cause latch-up or permanent damage.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 10. Maximum Continuous Working Voltage¹

Parameter	Max	Unit	Constraint
AC Voltage			
Bipolar Waveform	560	V_{PEAK}	Reinforced insulation rating per IEC 60747-17 (VDE 0884-17).

¹ Refers to continuous voltage magnitude imposed across the isolation barrier. See the [Insulation Lifetime](#) section for more details.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

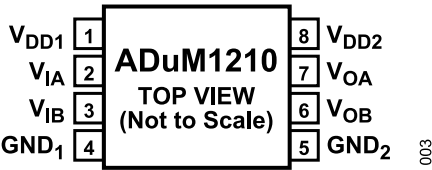


Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. Ground reference for Isolator Side 1.
5	GND ₂	Ground 2. Ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

Table 12. ADuM1210 Truth Table (Positive Logic)

V _{IA} Input	V _{IB} Input	V _{DD1} State	V _{DD2} State	V _{OA} Output	V _{OB} Output	Description
H	H	Powered	Powered	H	H	Outputs return to the input state within 1 μ s of V _{DD1} power restoration.
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μ s of V _{DD0} power restoration.

TYPICAL PERFORMANCE CHARACTERISTICS

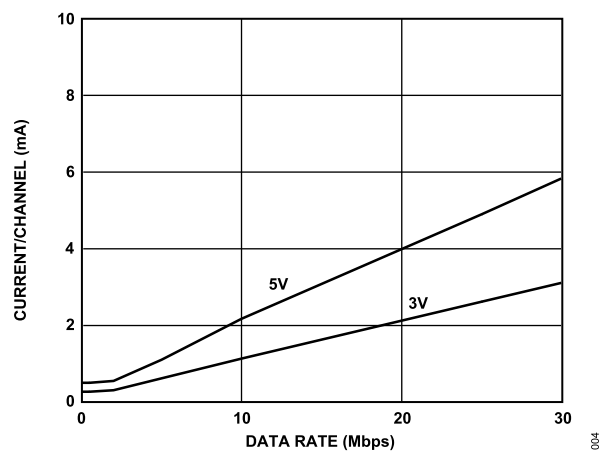


Figure 4. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

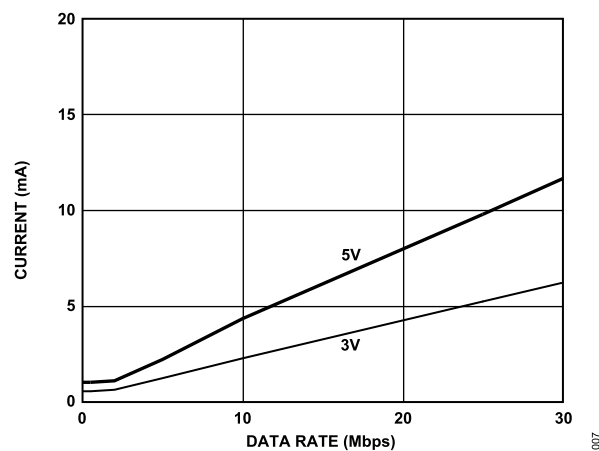


Figure 7. Typical V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

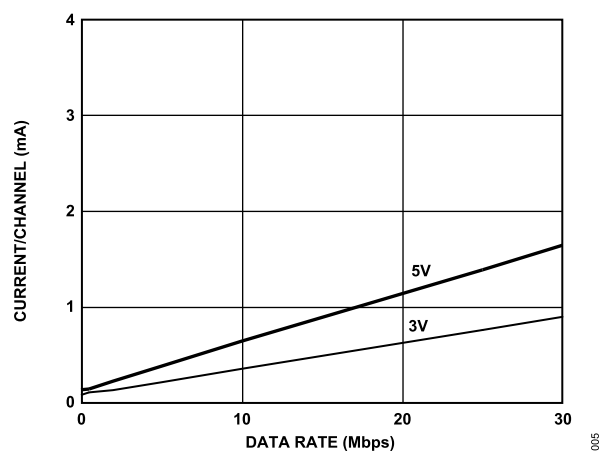


Figure 5. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

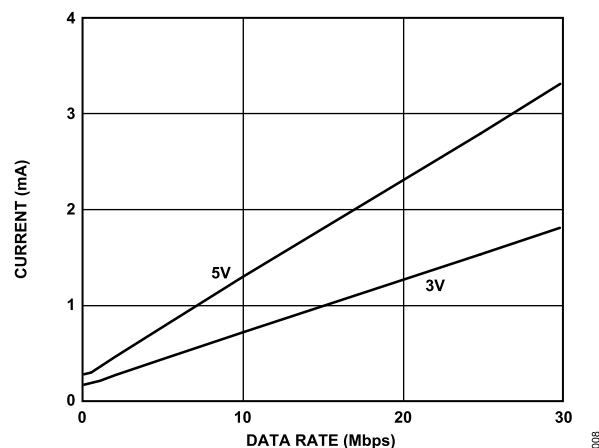


Figure 8. Typical V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

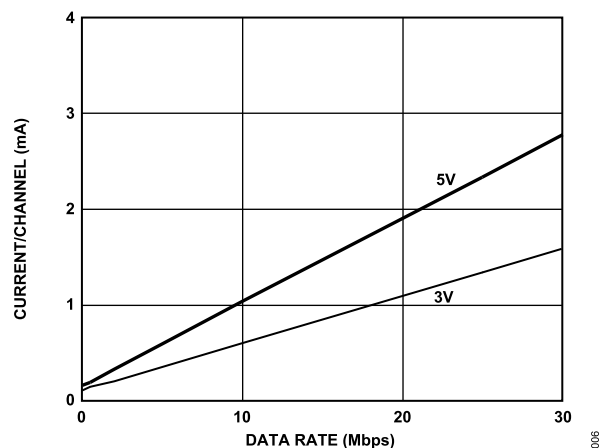


Figure 6. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM1210 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

See the [AN-1109 Application Note](#) for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

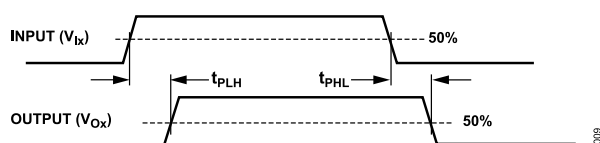


Figure 9. Propagation Delay Parameters

Pulse width distortion is the maximum difference between the two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM1210 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM120x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~ 1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than ~ 1 μs at the input, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see [Table 12](#)) by the watchdog timer circuit.

The ADuM1210 is extremely immune to external magnetic fields. The limitation on the ADuM1210 magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can

occur. The 3 V operating condition of the ADuM1210 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N \quad (1)$$

where:

β is the magnetic flux density (gauss).

r_n is the radius of the n th turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1210 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in [Figure 10](#).

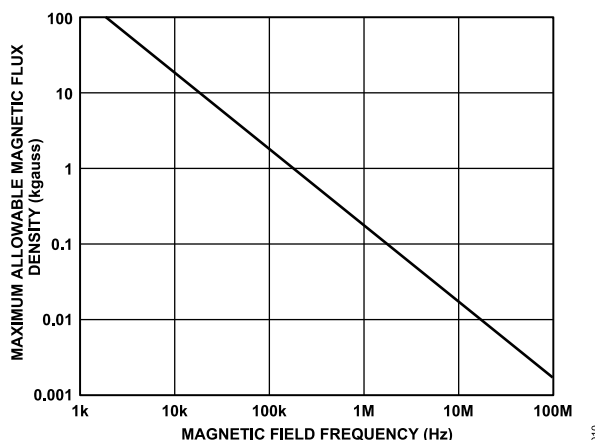


Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1210 transformers. [Figure 11](#) expresses these allowable current magnitudes as a function of frequency for selected distances. As seen in [Figure 11](#), the ADuM1210 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example, a 0.5 kA current would have to be placed 5 mm away from the ADuM1210 to affect the component's operation.

APPLICATIONS INFORMATION

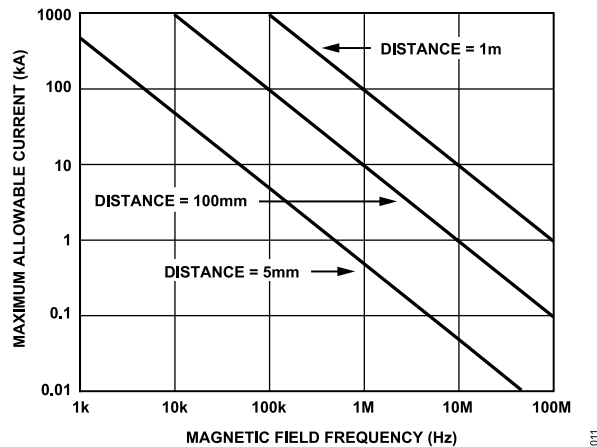


Figure 11. Maximum Allowable Current for Various Current-to-ADuM1210 Spacings

Note that, at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces can induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1210 isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r \quad (2)$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r \quad (3)$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r \quad (4)$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r \quad (5)$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 4 and Figure 5 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 6 shows per-channel supply current

as a function of data rate for a 15 pF output condition. Figure 7 and Figure 8 show total V_{DD1} and V_{DD2} supply current as a function of data rate.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1210.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at these high working voltages can lead to shortened insulation life in some cases.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-8	SOIC_N	8-Lead Standard Small Outline Package, Narrow Body

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM1210BRZ	−40°C to +105°C	8-Lead SOIC_N	Tube, 98	R-8
ADuM1210BRZ-RL7	−40°C to +105°C	8-Lead SOIC_N	Reel, 1000	R-8

¹ Z = RoHS Compliant Part.

NUMBER OF INPUTS, MAXIMUM DATA RATE, MAXIMUM PROPAGATION DELAY, AND MAXIMUM PULSE WIDTH DISTORTION OPTIONS

Model ¹	Number of Inputs, V _{DD1} Side	Number of Inputs, V _{DD2} Side	Maximum Data Rate	Maximum Propagation Delay, 5 V	Maximum Pulse Width Distortion
ADuM1210BRZ	2	0	10 Mbps	50 ns	3 ns
ADuM1210BRZ-RL7	2	0	10 Mbps	50 ns	3 ns

¹ Z = RoHS Compliant Part.