Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) module in WeEnTOP-B for use in applications requiring high blocking voltage capability, high inrush current capability and high thermal cycling performance.

2. Features and benefits

- · Planar passivated thyristor chips for voltage ruggedness and reliability
- Top-side cooling
- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminum oxide ceramic (DBC)
- · Package is RoHS compliant

3. Applications

- · Soft starters
- UPS
- · Temperature control
- · Lighting control
- AC power control

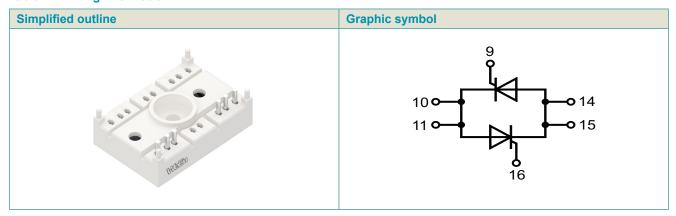
4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Notes | | Values | | Unit |
|---------------------|---------------------------------|--|-------|--------------|--------|------|------|
| Absolute | maximum rating | | | | | | |
| V_{DRM} | repetitive peak forward voltage | | | | 1600 | | V |
| V_{RRM} | repetitive peak reverse voltage | | | | 1600 | | V |
| I _{T(RMS)} | RMS on-state current | half sine wave | | | 101 | | А |
| | non-repetitive peak on- | half sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 10 \text{ ms}$ | | 1500 | | | А |
| | state current | half sine wave; $T_{j(init)}$ = 125 °C; t_p = 10 ms | | | 1350 | | А |
| | | half sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 8.3 \text{ ms}$ | | 1650 1485 | | | А |
| | | half sine wave; $T_{j(init)}$ = 125 °C; t_p = 8.3 ms | | | | | А |
| Symbol | Parameter | Conditions | Notes | Min | Тур | Max | Unit |
| Static ch | aracteristics | | | | | | |
| I _{GT} | gate trigger current | $V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C}$ | | 30 | - | 100 | mA |
| V_{GT} | gate trigger voltage | $V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C}$ | | - | - | 1.50 | V |
| V _T | on-state voltage | I _T = 200 A; T _j = 25 °C | | - | - | 1.70 | V |

5. Pinning information

Table 2. Pinning information



6. Ordering information

Table 3. Ordering information

| Type number | Package Name | Orderable part number | _ | | Package version | Package issue date |
|-------------|-----------------|-----------------------|-----|----|-----------------|--------------------|
| WAT100TBS16 | WeEnTOP-B | WAT100TBS16T | EPE | 30 | WeEnTOP-BPAT-A | 05-Nov-2024 |

7. Marking

Table 4. Marking codes

| Type number | Marking codes |
|-------------|---------------|
| WAT100TBS16 | WAT100TBS16 |

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Notes | Values | Unit |
|---------------------|----------------------------------|--|-------|------------|------|
| V_{DRM} | repetitive peak forward voltage | | | 1600 | V |
| V_{RRM} | repetitive peak reverse voltage | | | 1600 | V |
| I _{T(RMS)} | RMS on-state current | half sine wave | | 101 | А |
| I _{TSM} | non-repetitive peak onstate | half sine wave; $T_{J(init)}$ = 25 °C; t_p = 10 ms | | 1500 | Α |
| | current | half sine wave; $T_{j(init)}$ = 125 °C; t_p = 10 ms | | 1350 | Α |
| | | half sine wave; $T_{J(init)}$ = 25 °C; t_p = 8.3 ms | | 1650 | Α |
| | | half sine wave; $T_{j(init)}$ = 125 °C; t_p = 8.3 ms | | 1485 | Α |
| I ² t | I ² t for fusing | t _p = 10 ms; sine-wave pulse | | 11.25 | kA²s |
| dl _⊤ /dt | rate of rise of on-state current | I _G = 200 mA; T _j = 125 °C | | 200 | A/µs |
| I _{GM} | peak gate current | | | 10 | А |
| V_{RGM} | peak reverse gate voltage | | | 5 | V |
| P_GM | peak gate power | | | 20 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | 0.5 | W |
| T_{vj} | virtual junction temperature | | | -40 to 125 | °C |
| T _{op} | operation temperature | | | -40 to 125 | °C |
| T _{stg} | storage temperature | | | -40 to 125 | °C |

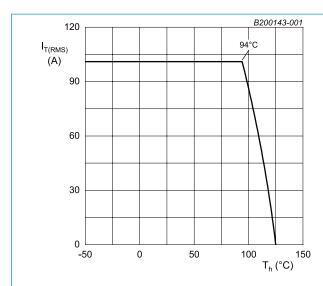
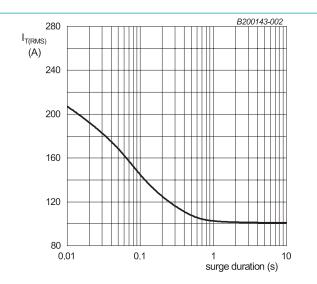


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



 $f = 50 Hz; T_h = 94 °C$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

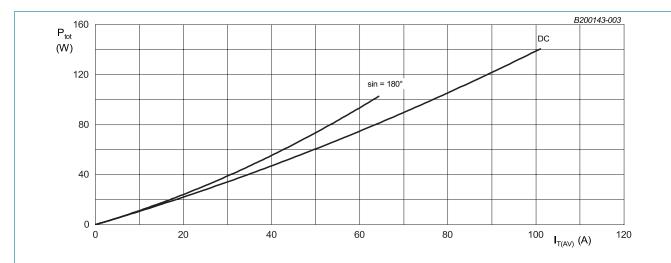
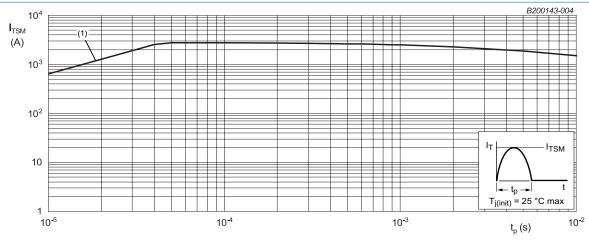


Fig. 3. Total power dissipation as a function of average on-state current; maximum values



t_p ≤ 10 ms

(1) dl_T/dt limit

Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Notes | Min | Тур | Max | Unit |
|----------------------|--|---------------|-------|-----|-----|-----|------|
| R _{th(j-h)} | thermal resistance from junction to heatsink | per thyristor | | - | - | 0.6 | K/W |
| | | per module | | - | - | 0.3 | K/W |

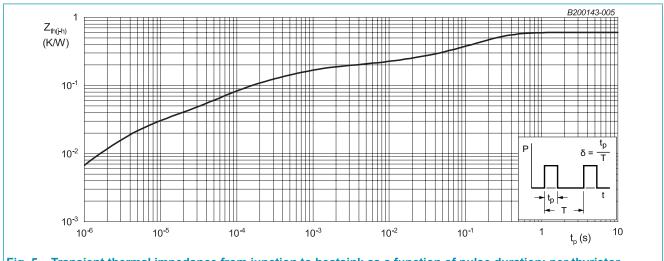


Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration; per thyristor

10. Package characteristics

Table 7. Isolation characteristics

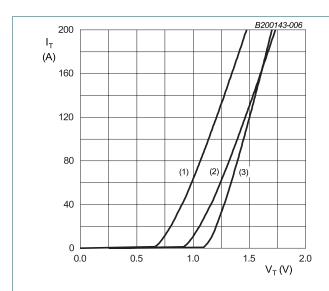
| Symbol | Parameter | Conditions | Notes | Min | Тур | Max | Unit |
|-------------------|-------------------|--|-------|-----|-----|------|------|
| V _{isol} | isolation voltage | 50/60 Hz; RMS; $I_{ISOL} \le 1$ mA; t = 1 second; AC | | - | - | 3600 | V |
| | _ I | 50/60 Hz; RMS; I _{ISOL} ≤ 1 mA; t = 1 minute; AC | | - | - | 2500 | V |

11. Characteristics

Table 8. Characteristics

| Symbol | Parameter | Conditions | Notes | Min | Тур | Max | Unit |
|---------------------|-----------------------------------|---|-------|------|-----|------|------|
| Static ch | aracteristics | | | , | | | ' |
| I _{GT} | gate trigger current | $V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C}$ | | 30 | - | 100 | mA |
| V_{GT} | gate trigger voltage | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C | | - | - | 1.50 | V |
| | | $V_D = 2/3 V_{DRM}; I_T = 0.1 A; T_j = 125 °C$ | | 0.25 | - | - | V |
| I_{GD} | gate non-trigger current | T _j = 125 °C | | - | - | 8.5 | mA |
| V_{GD} | gate non-trigger voltage | T _j = 125 °C | | - | - | 0.2 | V |
| IL | latching current | $V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C}$ | | - | - | 300 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C | | - | - | 200 | mA |
| V _T | on-state voltage | I _T = 200 A; T _j = 25 °C | | - | - | 1.70 | V |
| V_{TO} | threshold voltage | T _j = 125 °C | | - | - | 1.0 | V |
| r _T | slope resistance | T _j = 125 °C | | - | - | 3.5 | mΩ |
| I _D | off-state current | V _D = 1600 V; T _j = 25 °C | | - | - | 100 | μΑ |
| | | V _D = 1600 V; T _j = 125 °C | | - | - | 15 | mA |
| I _R | reverse current | V _R = 1600 V; T _j = 25 °C | | - | - | 100 | μΑ |
| | | V _R = 1600 V; T _j = 125 °C | | - | - | 15 | mA |
| Dynamic | characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V_{DM} = 1072 V; T_j = 125 °C; $(V_{DM}$ = 67% of V_{DRM}); exponential waveform; gate open circuit | | 1500 | - | - | V/µs |
| t _{gt} | gate-controlled turn-on time | $I_{TM} = 40 \text{ A}; V_D = 800 \text{ V}; I_G = 100 \text{ mA};$ $(dI_G/dt)_M = 1 \text{ A/µs}; T_J = 25 ^{\circ}\text{C}$ | | - | 2 | - | μs |
| t _q | commutated turn-off time | $I_{TM} = 2 \text{ A}; t_p = 50 \mu\text{s}; dV/dt = 5 V/\mu\text{s};$ $dI/dt = 30 A/\mu\text{s}; T_i = 25 ^{\circ}\text{C}$ | | - | 150 | - | μs |

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 $V_{TO} = 1.034 \text{ V}; r_T = 0.0035 \Omega$

(1) $T_j = 125$ °C; typical values (2) $T_i = 125$ °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 6. On-state current as a function of on-state voltage

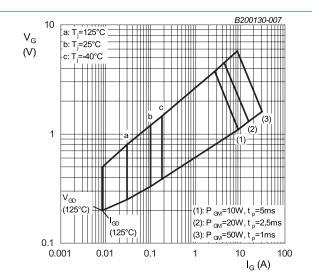


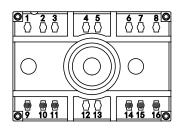
Fig. 7. Gate voltage as a function of gate current

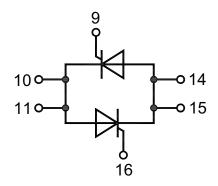
Product data sheet

12. Package outline

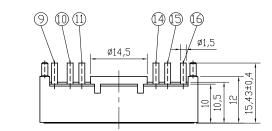
Dimensions in mm

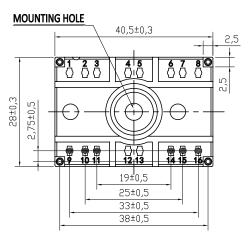
Pinout

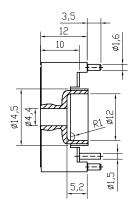




Package Outline







Suggested hole diameter in the PCB for solder pins and mounting pins: 2mm

13. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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- Please consult the most recently issued document before initiating or completing a design.
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WAT100TBS16

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