The documentation and process conversion measures necessary to comply with this document shall be completed by 25 March 2015.

INCH-POUND
MIL-PRF-19500/561K
25 November 2015
SUPERSEDING
MIL-PRF-19500/561J
11 July 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, PNP, SILICON, SWITCHING,

TYPES 2N6193, JAN, JANTX, JANTXV, JANS, JANHC, JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for PNP silicon switching transistors. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device type as specified in MIL-PRF-19500. Radiation hardness assurance (RHA) level designators “M”, “D”, “P“, “L”, “R”, “F”, “G”, and “H” are appended to the device prefix to identify devices which have passed RHA requirements. Provisions for (RHA) to two radiation levels (“R” and “F”) are provided for JANTXV product assurance level.

* 1.2 Physical dimensions. See figure 1 (TO-39), The dimensions and topography for JANHC and JANKC unencapsulated die is as follows: The A version die in accordance with figure 2, B version die in accordance with figure 3, and C version die in accordance with figure 4. Figure 5 (U3 surface mount), and D version die in accordance with figure 6.

1.3 Maximum ratings unless otherwise specified T_A = +25°C.

Types	P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	$R_{\theta JA}$	$R_{\theta JC}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_B	T_J and T_{STG}
	W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	°C
2N6193	1.0	17.5	175	10	-100	-100	-6.0	-5.0	-1.0	-65 to
2N6193U3	1.0	100	175	1.75	-100	-100	-6.0	-5.0	-1.0	+200

(1) See figure 6.
(2) See figure 7 and figure 8.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

AMSC N/A

FSC 5961

1.4 Primary electrical characteristics T_A = +25°C. (Unless otherwise indicated, applies to all devices.)

Types	h_{FE1} (1) V_{CE} = -2.0 V dc; I_C = -0.5 A dc		h_{FE2} (1) V_{CE} = -2.0 V dc; I_C = -2.0 A dc		h_{FE3} (1) V_{CE} = -2.0 V dc; I_C = -5.0 A dc	
	Min	Max	Min	Max	Min	Max
2N6193	60		60	240	40	
2N6193U3	60		60	240	40	

Limits	$\|h_{FE}\|$ V_{CE} = -10 V dc I_C = -0.5 A dc f = 10 MHz	C_{obo} V_{CB} = -10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	Switching		$V_{CE(SAT)1}$ I_C = -2.0 A dc I_B = -0.2 A dc (1)	$V_{BE(SAT)1}$ I_C = -2.0 A dc I_B = -0.2 A dc (1)
			See figure 6 t_{on}	See figure 7 t_{off}		
		pF	µs	µs	V dc	V dc
Min	3.0					
Max	15	300	0.2	2.2	-0.7	-1.2

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level designators.

* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", “JANTXV”, and "JANS".

* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANS quality levels are as follows: "M", "D", "P", "L", “R”, “F’, “G”, and “H”. For the RHA levels for TXV quality levels are as follows: “R” and “F’.

* 1.5.3 Device type. The designation system for the device types covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols "2N".

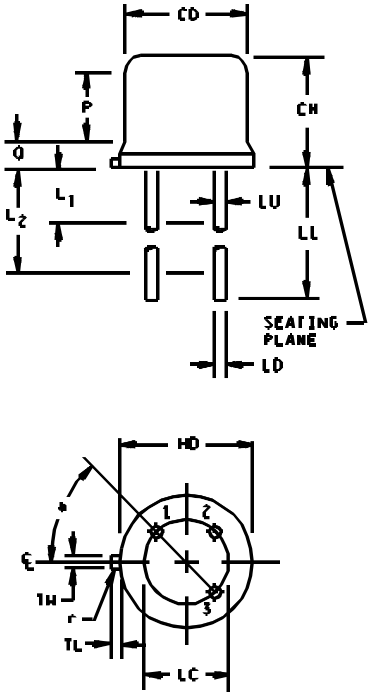
* 1.5.3.2 Second number symbols. The second number symbols for the semiconductors covered by this specification sheet are as follows: "6193".

* 1.5.4 Suffix symbols. The following suffix letters are incorporated in the PIN for this specification sheet.

	A blank first suffix symbol indicates encapsulated devices. Applicable for the 2N6193 (see figure 1, TO-39).
U3	Indicates a surface mount 2N6193U3, (see figure 5).

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

* 1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet is "A".

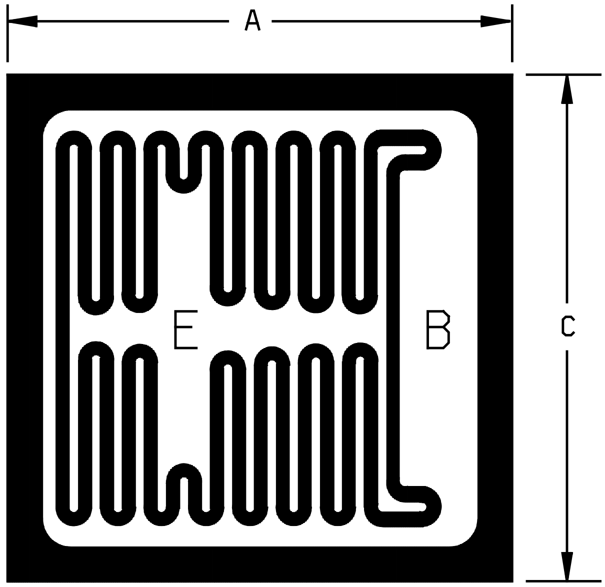


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.355	7.75	9.02	
CH	.240	.260	6.10	6.60	
HD	.355	.370	9.02	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7
LL	.500	.750	12.70	19.05	7
LU	.016	.019	0.41	0.48	7
L1		.050		1.27	7
L2	.250		6.35		7
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	10
P	.100		2.54		5
Q		.040		1.02	4
R		.010		0.25	11
α	45° TP		45° TP		6
Notes	1, 2, 8, 9				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum.
8. Lead designation, depending on device type, shall be as follows: 1 Emitter, 2 Base, and 3 Collector
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

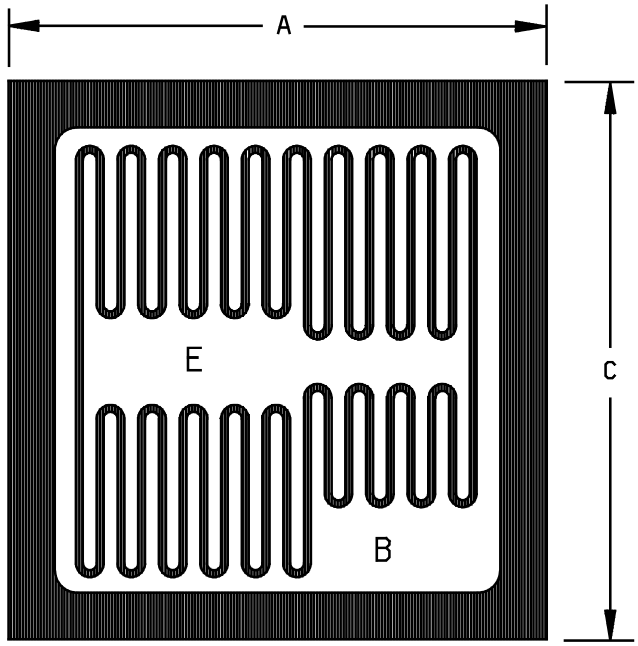
FIGURE 1. Physical dimensions (TO-39).



Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.120	.124	3.05	3.15
C	.120	.124	3.05	3.15

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Thickness: ....008 inch (0.20 mm) to .012 inch (0.30 mm).
   Top metal:..Aluminum 40,000 Å minimum, 50,000 Å nominal.
   Back metal:......................................Gold 2,500 Å minimum, 3,000 Å nominal.
   Back side:..Collector.
   Bonding pad: ....B = .015 inch (0.38 mm) x .072 inch (1.83 mm).
   E = .015 inch (0.38 mm) x .060 inch (1.52 mm).
4. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions JANHCA and JANKCA.

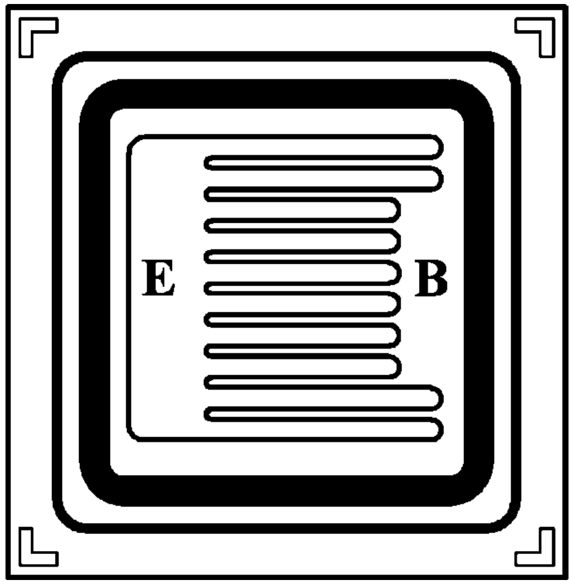


Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.098	.102	2.49	2.59
C	.098	.102	2.49	2.59

NOTES:

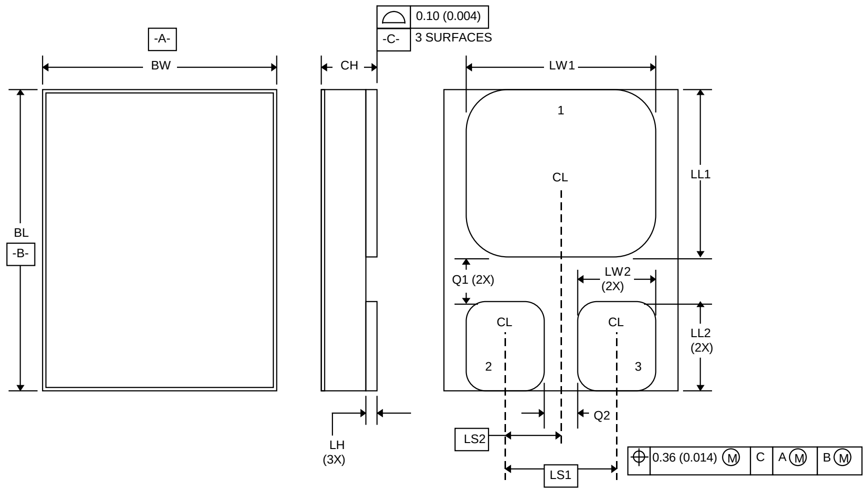
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Thickness: ....006 inch (0.15 mm) to .010 inch (0.25 mm).
   Top metal:..........................Aluminum 25,000 Å minimum, 33,000 Å nominal.
   Back metal:........................Gold 1,500 Å minimum, 2,500 Å nominal.
   Back side:..........................Collector.
   Bonding pad: ....B = .014 inch (0.36 mm) x .030 inch (0.76 mm).
4. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions JANHCB and JANKCB.



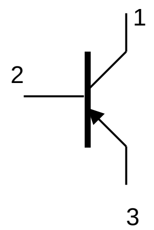
NOTES:
1. Chip size ....128 x .128 inch ±.002 inch, (3.25 x 3.25 mm ±0.051mm).
2. Chip thickness.....................................010 ±.0015 inch nominal, (.254 ±0.038 mm)
3. Top metal ....Aluminum 30,000Å minimum, 33,000Å nominal.
4. Back metal ....A. Al/Ti/Ni/Ag15kÅ/2kÅ/7kÅ/7kÅmin.18kÅ/3kÅ/10kÅ/10kÅ nom.
   B. Gold 2,500Å minimum, 3,000Å nominal.
5. Backside ....Collector
6. Bonding pad..B = .052 x .012 inch, (1.32 x 0.30 mm).
   E = .084 x .012 inch, (2.13 x 0.30 mm).

FIGURE 4. Physical dimensions JANHCC and JANKCC.



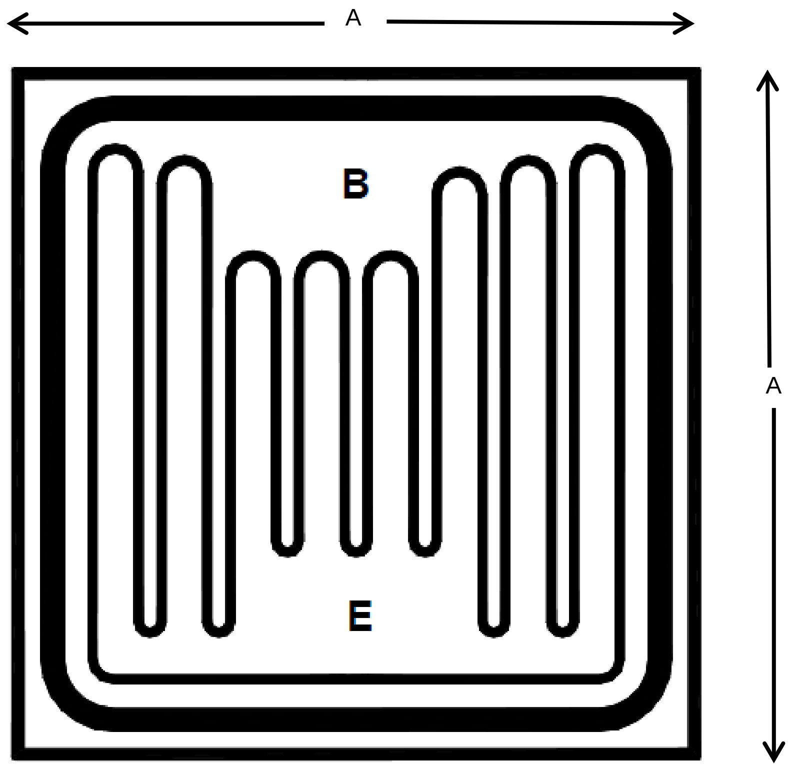
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH	.1085	.1205	2.76	3.06
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	

SCHEMATIC



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
4. Terminal 1 - collector, terminal 2 -base, terminal 3 - emitter.

FIGURE 5. Physical dimensions and configuration 2N6193U3.



Backside: Collector

Dimensions				
LTR	Inches		Millimeters	
	Min	Max	Min	Max
A	.118	.122	3.0	3.1

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).
4. The physical characteristics of the die are:

Thickness: .0135 inch (0.34 mm) nominal, tolerance is ±.0015 inch (0.04 mm).
Top metal: Aluminum, 54,000 Å minimum, 60,000 Å nominal.
Back metal: Gold 6,400 Å minimum, 8,000 Å nominal.
Back side: Collector.
Bonding pad: B = .038 x .022 inch (0.97 x 0.56 mm)
E = .042 x .020 inch (1.07 mm x 0.51 mm)

* FIGURE 6. JANHC and JANKC (D-version) die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

$R_{\theta JA}$ .... Thermal resistance junction to ambient.
$R_{\theta JC}$ .... Thermal resistance junction to case.

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-39), figure 2, figure 3, and figure 4 (JANHC and JANKC), figure 5 (surface mount), and figure 6 (JANHC and JANKC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.8 Marking. Devices shall be marked in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I and table II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening.

4.3.1 Screening of encapsulated devices (JANS, JANTX, and JANTXV levels only). Screening of packaged devices shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750	Thermal impedance, method 3131 of MIL-STD-750
9	I_{CBO1} and h_{FE2}	Not applicable
11	I_{CBO1}; h_{FE2}, ΔI_{CBO1} = ±100 percent of initial value or 1.0 μA dc whichever is greater; Δh_{FE2} = ±15 percent	I_{CBO1} and h_{FE2}
12	See 4.3.1.1	See 4.3.1.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO1} = ±100 percent of initial value or 1.0 μA dc, whichever is greater; Δh_{FE2} = ±15 percent	Subgroup 2 of table I herein; ΔI_{CBO1} = ±100 percent of initial value or 1.0 μA dc, whichever is greater; Δh_{FE2} = ±15 percent.
* 17	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein. N/A for ceramic U3 devices.	For U3 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein. N/A for ceramic U3 devices.

(1) Shall be performed anytime after temperature cycling, screen 3a; TX and TXV devices do not need to be repeated in screening requirements.

4.3.1.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc, T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750, power shall be applied to the device to achieve T_J = minimum +175°C and minimum power dissipation of P_D = 75 percent P_T max as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Screening of unencapsulated die (JANHC and JANKC). Screening of JANHC and JANKC unencapsulated die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit used in screen 3c and subgroup 2 of table I shall comply with the thermal impedance graph in figures 9 and 10 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage..600 V dc.

b. Duration of application of test voltage......................15 seconds (min).

c. Points of application of test voltage ....All leads to case (bunch connection).

d. Method of connection..Mechanical.

e. Kilovolt-ampere rating of high voltage source...........1,200 V/1.0 mA (min).

f. Maximum leakage current.......................................1.0 mA.

g. Voltage ramp up time..500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa of MIL-PRF-19500 (JANS) and 4.4.2.1 herein. See 4.4.2.2 herein for JAN, JANTX, and JANTXV group B testing.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
* B4	1037	$V_{CB} \geq$ -10 V dc, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum sample size in accordance with table VIa, of MIL-PRF-19500, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjusted T_A or P_D to achieve a T_J = +225°C minimum.
B5	2037	Test condition D.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a group B failure, the manufacturer may pull a new sample at double size from either the failed assembly lot or from another assembly lot from the same wafer lot. If the new assembly lot option is exercised, the failed assembly lot shall be scrapped.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = -10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, not applicable for U3.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ (see 1.3) and applied thermal impedance curves.
C6	1026	Steady-state life: 1,000 hours, V_{CB} = -10 dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, not applicable for U3.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and applied thermal impedance curves).
C6		Not applicable.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750 for total ionizing dose, or method 1017 of MIL-STD-750 for neutron fluence, as applicable (see 6.2.f herein), except group D, subgroup 2 may be performed separate from other subgroups. Group D inspection may also be performed ahead of the screening lot using die selected in accordance with MIL-PRF-19500 and related documents. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Thermal resistance (to be performed for qualification inspection only). The thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following details shall apply:

a. Collector current magnitude during power application shall be -0.15 A dc.

b. Collector to emitter voltage magnitude shall be -20 V dc.

c. Reference temperature measuring point shall be the case.

d. Reference point temperature shall be + 25°C $\leq T_R \leq$ +35°C and recorded before the test is started.

e. Mounting arrangement shall be with heat sink to case.

f. Maximum limit shall be $R_{\theta JC}$ = 10°C/W for TO-39 devices and 1.75°C/W for U3 devices.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical Inspection	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
* Salt atmosphere (corrosion)	1041	N = 6 devices, c = 0 (For laser marked devices only.)				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Hermetic seal 4/ 6/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -50 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-100		V dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = -100 V dc	I_{CEO}		-100	µA dc
* Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = +1.5 V dc; V_{CE} = -90 V dc	I_{CEX1}		-10	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -100 V dc	I_{CBO}		-10	µA dc
Emitter to base, cutoff current	3061	Bias condition D; V_{EB} = -6.0 V dc	I_{EBO}		-100	µA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750 Method	MIL-STD-750 Conditions	Symbol	Limit Min	Limit Max	Unit
Subgroup 2 – Continued						
Forward - current transfer ratio	3076	V_{CE} = -2.0 V dc; I_C = -0.5 A dc, pulsed (see 4.5.1)	h_{FE1}	60		
Forward - current transfer ratio	3076	V_{CE} = -2.0 V dc; I_C = -2.0 A dc; pulsed (see 4.5.1)	h_{FE2}	60	240	
Forward - current transfer ratio	3076	V_{CE} = -2.0 V dc; I_C = -5.0 A dc; pulsed (see 4.5.1)	h_{FE3}	40		
Collector to emitter voltage (saturated)	3071	I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		-0.7	V dc
Collector to emitter voltage (saturated)	3071	I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		-1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)1}$		-1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		-1.8	V dc
Subgroup 3						
High - temperature operation		T_A = +150°C				
* Collector to emitter cutoff current		Bias condition A; V_{CE} = -90 V dc; V_{BE} = +1.5 V dc	I_{CEX2}		-15	μA dc
Low - temperature operation		T_A = -55°C				
Forward - current transfer ratio	3076	V_{CE} = -2.0 V dc; I_C = -2.0 A dc; pulsed (see 4.5.1)	h_{FE4}	12		
Subgroup 4						
Small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = -10 V dc; I_C = -0.5 A dc; f = 10 MHz	$\|h_{fe}\|$	3	15	
Open circuit output capacitance	3236	V_{CB} = -10 V dc; I_E = 0; 100 kHz $\leq f \leq$ 1 MHz	C_{obo}		300	pF
Input capacitance (output open-circuited)	3240	V_{BE} = -2.0 V dc; I_C = 0; 100 kHz $\leq f \leq$ 1 MHz	C_{ibo}		1,250	pF

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4 – Continued						
Pulse response						
Pulse delay time	3251	See figure 11	t_d		100	ns
Pulse rise time	3251	See figure 11	t_r		100	ns
Pulse storage time	3251	See figure 12	t_s		2	µs
Pulse fall time	3251	See figure 12	t_f		200	ns
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +25°C; t ≥ 0.5 s; 1 cycle				
Test 1		V_{CE} = -2.0 V dc; I_C = -5.0 A dc				
Test 2		V_{CE} = -90 V dc; I_C = -55 mA dc				
End-point electrical Measurements		See table I, subgroup 2 herein.				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed in table I, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

* TABLE II. Group D inspection and end-point limits.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0V				
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -50 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-100		V dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = -100 V	I_{CEO}		-200	µA dc
* Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = +1.5 V; V_{CE} = -90 V dc	I_{CEX1}		-20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -100 V dc	I_{CBO}		-20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = -6.0 V dc	I_{EBO}		-200	µA dc
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -0.5 A dc; pulsed (see 4.5.1)	[h_{FE1}] 5/	[30]		
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -2.0 A dc; pulsed (see 4.5.1)	[h_{FE2}] 5/	[30]	240	
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -5.0 A dc; pulsed (see 4.5.1)	[h_{FE3}] 5/	[20]		
Collector to emitter voltage (saturated)	3071	I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		-0.81	V dc
Collector to emitter voltage (saturated)	3071	I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.07	V dc

See footnotes at end of table.

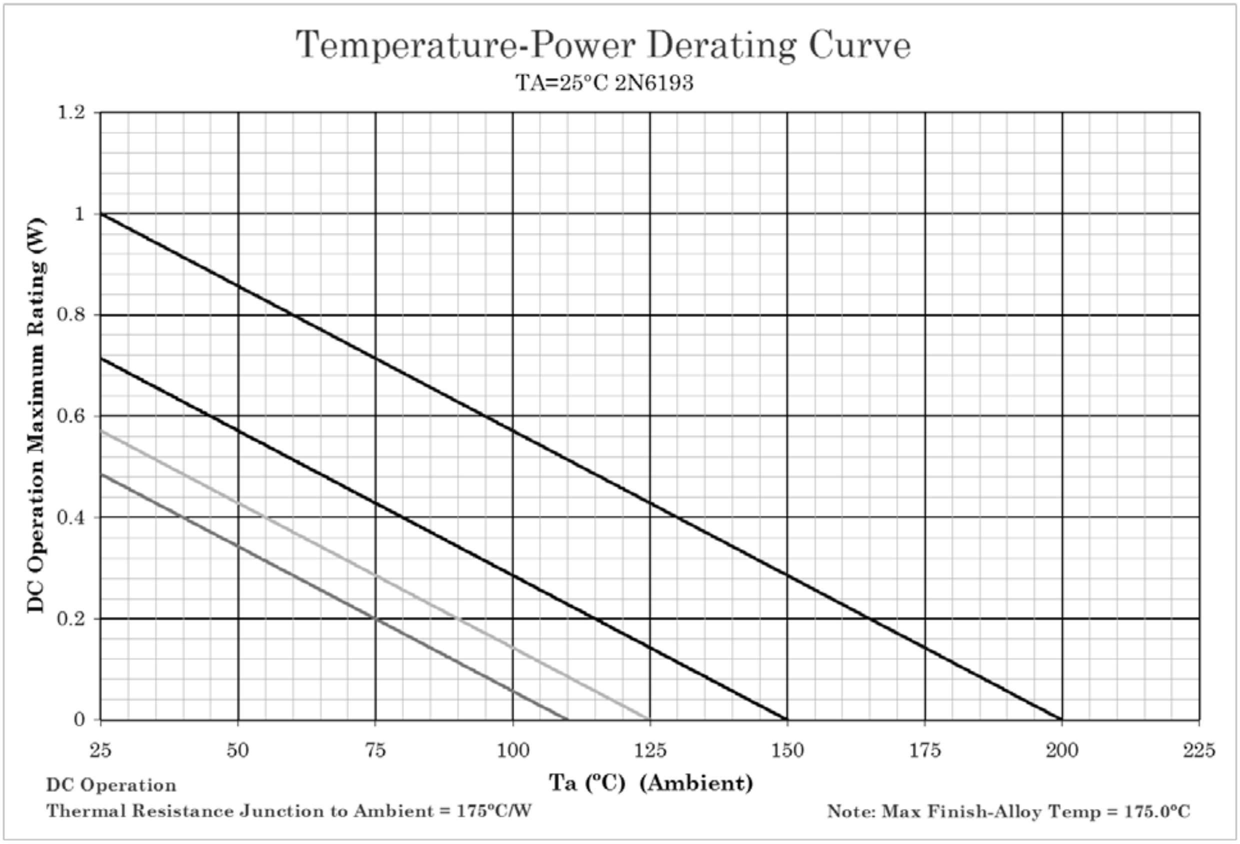
* TABLE II. Group D inspection and end-point limits – Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 4/						
Steady-state total dose irradiation	1019	Gamma exposure V_{CES} = -80 V				
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -50 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-100		V dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = -100 V	I_{CEO}		-200	µA dc
* Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = +1.5 V; V_{CE} = -90 V dc	I_{CEX1}		-20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -100 V dc	I_{CBO}		-20	µA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = -6.0 V dc	I_{EBO}		-200	µA dc
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -0.5 A dc; pulsed (see 4.5.1)	[h_{FE1}] 5/	[30]		
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -2.0 A dc; pulsed (see 4.5.1)	[h_{FE2}] 5/	[30]	240	
Forward-current transfer ratio	3076	V_{CE} = -2.0 V dc, I_C = -5.0 A dc; pulsed (see 4.5.1)	[h_{FE3}] 5/	[20]		
Collector to emitter voltage (saturated)	3071	I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		-0.81	V dc
Collector to emitter voltage (saturated)	3071	I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -2.0 A dc; I_B = -0.2 A dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = -5.0 A dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.07	V dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to the corresponding AL, UA, UB, and UBC suffix versions unless otherwise noted.
4/ See 6.2.f herein.
5/ See method 1019 of MIL-STD-750 for how to determine [h_{FE}] by first calculating the delta (1/h_{FE}) from the pre- and Post-radiation h_{FE}. Notice the [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

TABLE III. Group E inspection (all quality levels) - for qualification only.

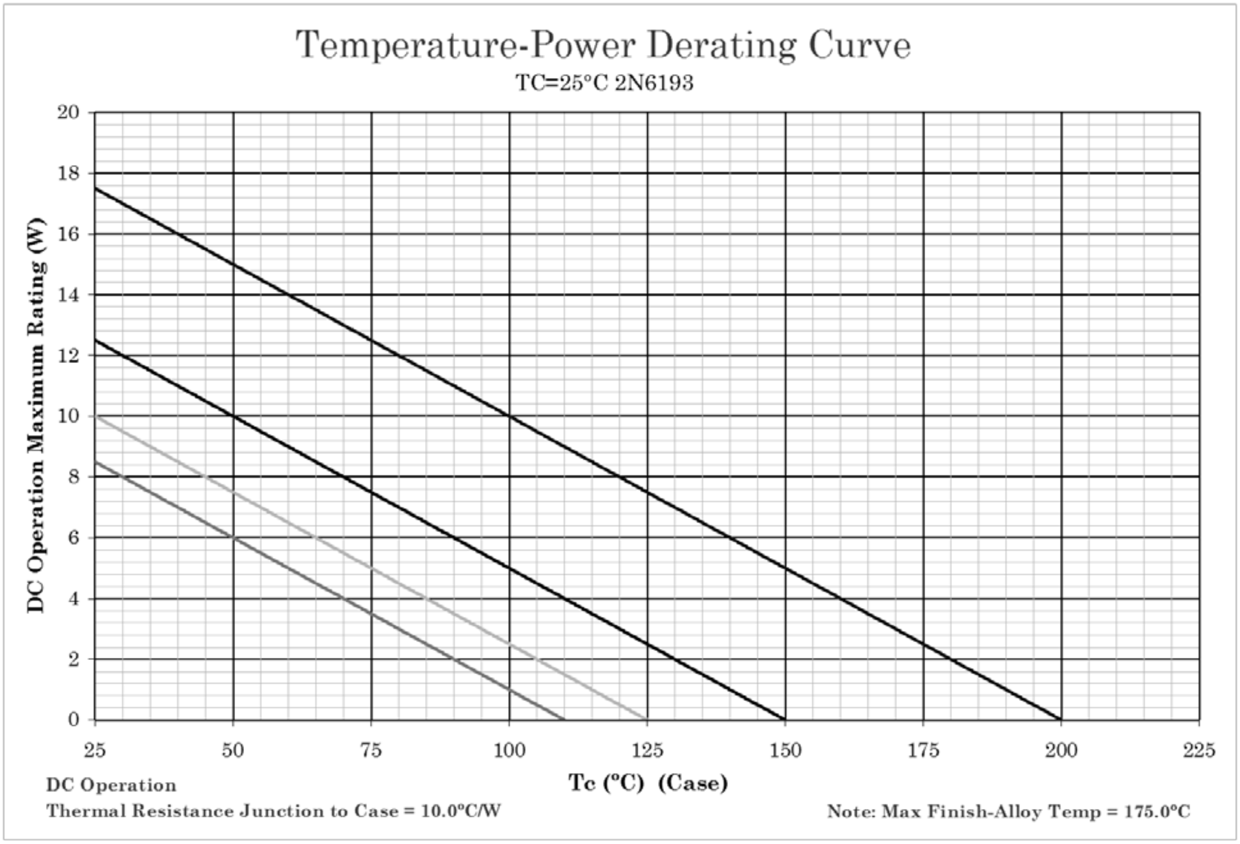
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices, c = 0
Intermittent life	1037	6,000 cycles $t_{(on)}$, $t_{(off)}$ = 1 minute minimum. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			
Thermal impedance curves		See table E-IX of MIL-PRF-19500, group E, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 6			11 devices
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

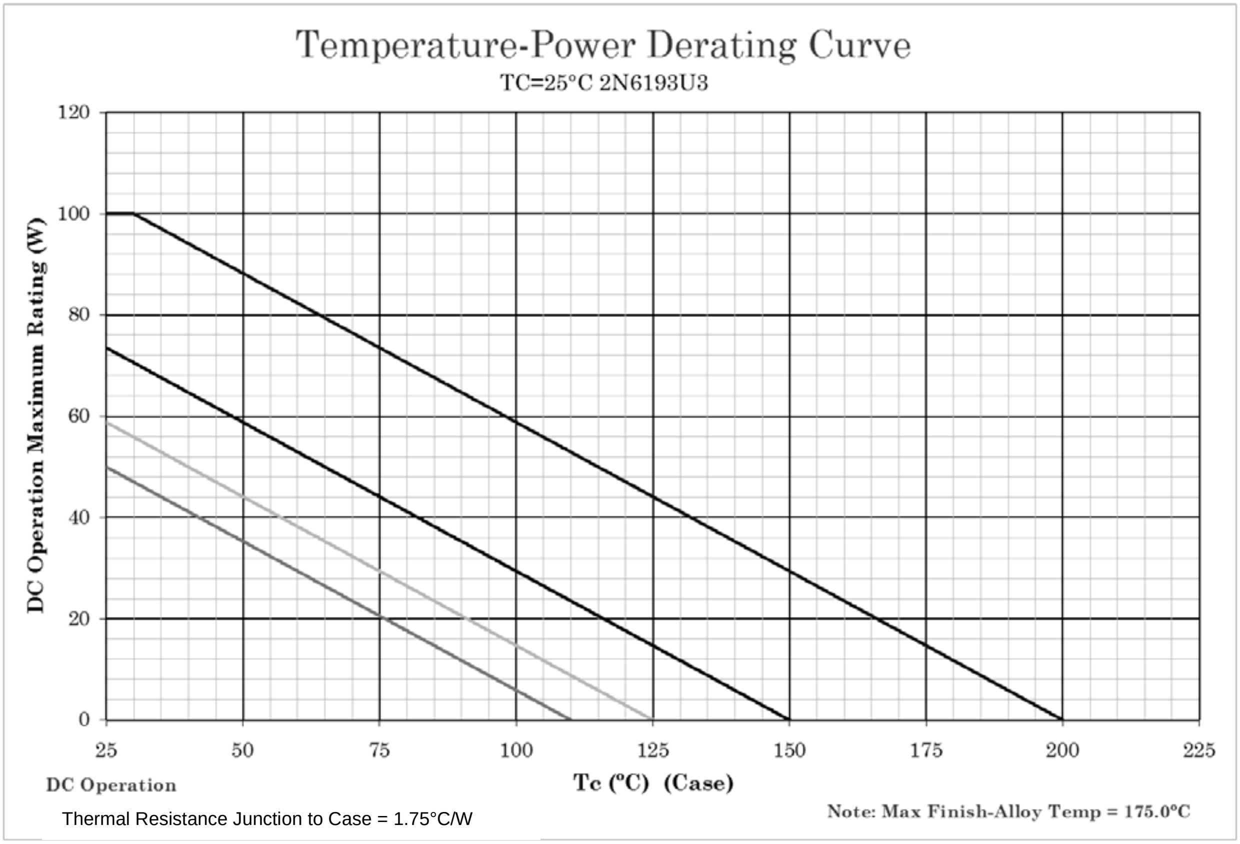
FIGURE 6. Temperature-power derating for 2N6193 $R_{\theta JA}$ (TO-39 Kovar).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

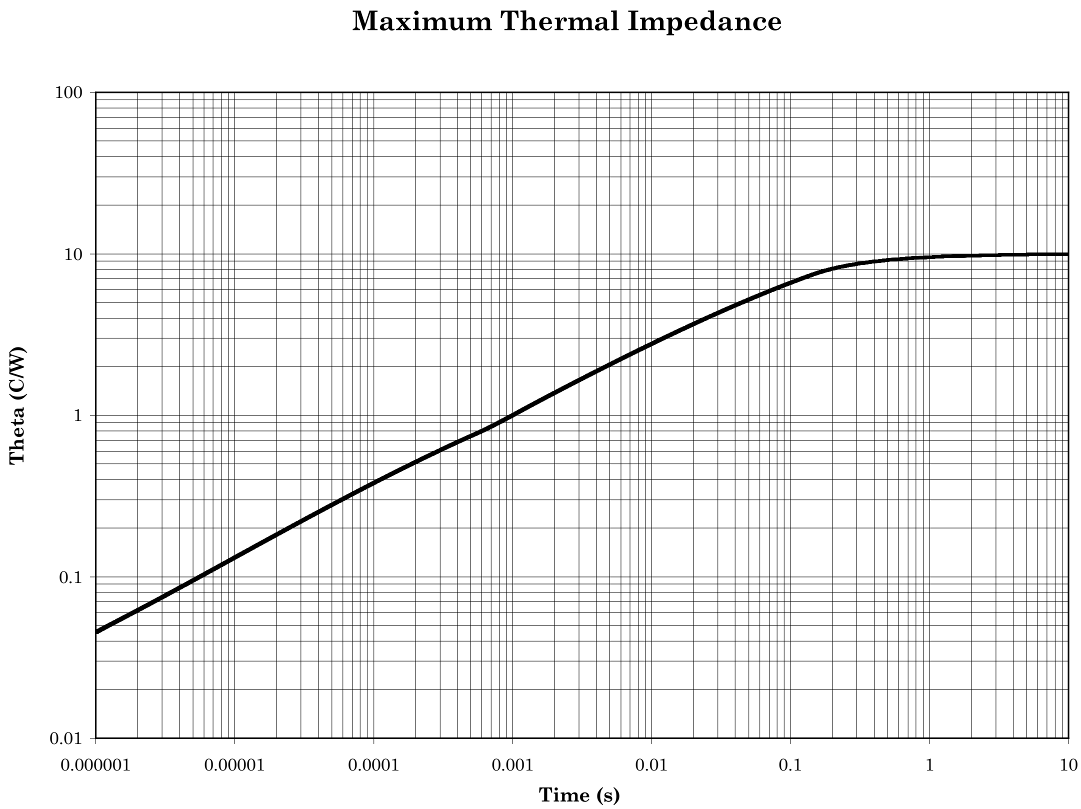
FIGURE 7. Temperature-power derating for 2N6193 $R_{\theta JC}$ (TO-39 Kovar).



NOTES:

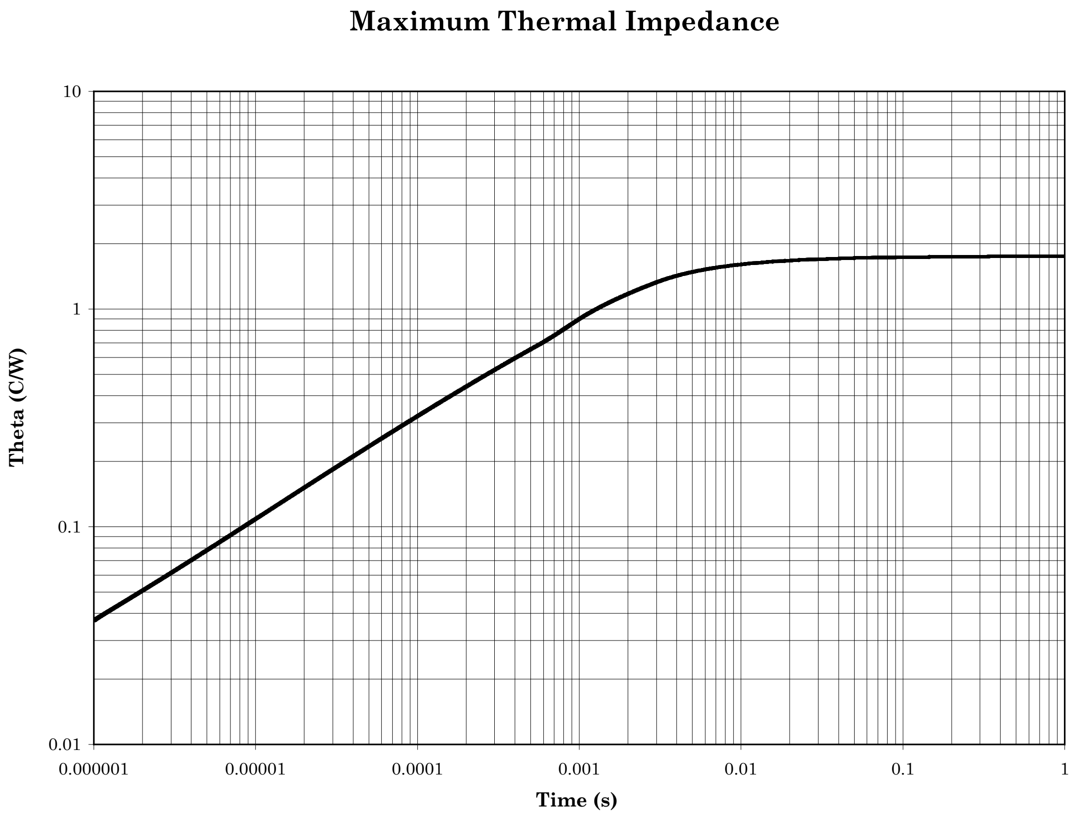
1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ 200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ 150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature-power derating for 2N6193U3 $R_{\theta JC}$ (U3 package).



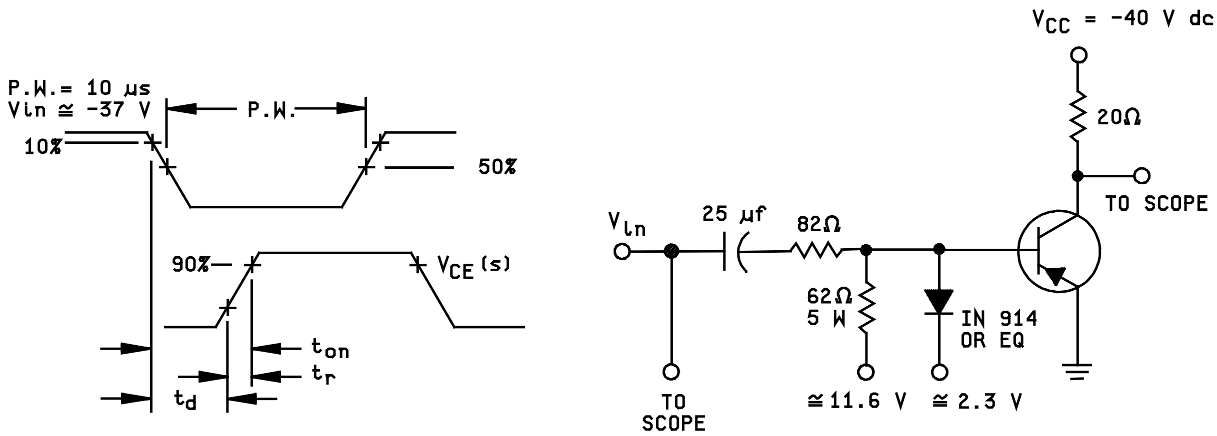
T_C = 25°C, thermal resistance $R_{\theta JC}$ = 10°C/W.

FIGURE 9. Thermal impedance graph ($R_{\theta JC}$) for 2N6193 (TO-39 Kovar).



Solder mounted to copper heatsink at T_C = +25°C thermal resistance = 1.75°C/W, Pdiss = 100W.

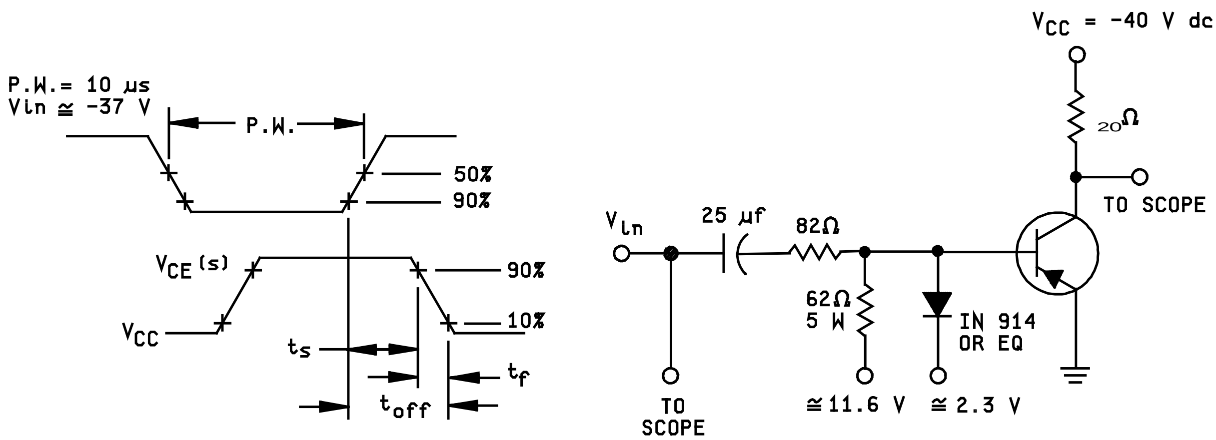
FIGURE 10. Thermal impedance graph ($R_{\theta JC}$) for 2N6193U3 (U3).



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF, rise time ≤ 0.2 ns.
3. I_C = 2 A, I_{B1} = 200 mA.

FIGURE 11. Saturated turn-on switching waveform and time test circuit.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF, rise time ≤ 0.20 ns.
3. C_I = 2 A, I_{B1} = I_{B2} = 200 mA.

FIGURE 12. Pulse response test circuit for t_s and t_f.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead material and finish may be specified (see 3.4.1).

d. The complete Part or Identifying Number (PIN), see title and section 1.5

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figure 2, figure 3, and figure 4 herein).

f. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it should be specified in the contract.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Application guidance. The following NPN type transistor is complimentary to the PNP device listed herein.

NPN	PNP
2N5339	2N6193

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.

JANS M 2N 6193 U3

JAN certification mark and quality level (see 1.5.1.1) — JANS

RHA designator (see 1.5.2) — M

First number and first letter symbols (see 1.5.3.1) — 2N

Second number symbols (see 1.5.3.2) — 6193

Suffix symbol (see 1.5.4) — U3

* 6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.

JANHC A M 2N 6193

JAN certification mark and quality level (see 1.5.1.2) — JANHC

Die identifier for unencapsulated devices (see 1.5.6) — A

RHA designator (see 1.5.2) — M

First number and first letter symbols (see 1.5.3.1) — 2N

Second number symbols (see 1.5.3.2) — 6193

* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for type 2N6193.	
JAN2N6193	JAN2N6193U3
JANTX2N6193	JANTX2N6193U3
JANTXV2N6193	JANTXV2N6193U3
JANTXVF2N6193	JANTXVF2N6193U3
JANTXVR2N6193	JANTXVR2N6193U3
JANS#2N6193	JANS#2N6193U3

* (1) The number sign (#) represent one of eight RHA designators available (M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

* 6.6.1 List of PINs for unencapsulated devices. The following is a list of possible PINs for unencapsulated devices available on this specification sheet. The qualified die suppliers with the applicable letter version (e.g., JANHCA1N4614) will be identified on the QML.

JANHC and JANKC ordering information				
PIN	Manufacturers			
	33178	34156	43611	52GC4
2N6193	JANHCA2N6193 JANKCA2N6193	JANHCB2N6193 JANKCB2N6193	JANHCC2N6193 JANKCC2N6193	JANHCD2N6193 JANKCD2N6193

* (1) The number sign (#) represent one of eight RHA designators available (M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

* 6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - MI
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2015-096

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.