features

- Up to 150-mA Output Current
- Less Than 10-mV$_{pp}$ Output Voltage Ripple
- No Inductors Required/Low EMI
- Regulated 5-V ±4% Output
- Only Four External Components Required
- Up to 90% Efficiency
- 2.7-V to 5.4-V Input Voltage Range
- 60-µA Quiescent Supply Current
- 0.05-µA Shutdown Current
- Load Isolated in Shutdown
- Space-Saving Thermally-Enhanced TSSOP PowerPAD™ Package
- Evaluation Module Available (TPS60110EVM−132)

applications

Replaces DC/DC Converters With Inductors in

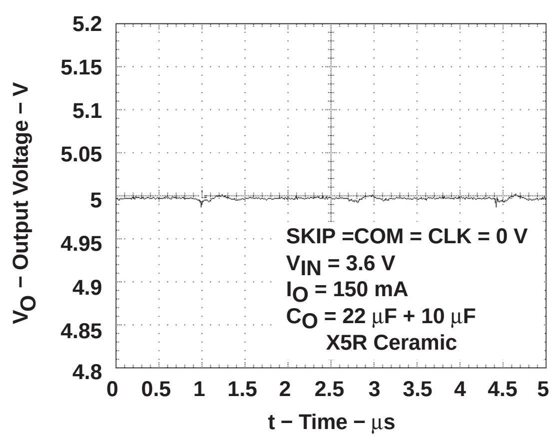
- Battery-Powered Applications
- Li-Ion Battery to 5-V Conversion
- Portable Instruments
- Battery-Powered Microprocessor Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs
- Laptops
- Handheld Instrumentation
- Medical Instruments

description

The TPS60111 step-up, regulated charge pump generates a 5-V ±4% output voltage from a 2.7-V to 5.4-V input voltage (three alkaline, NiCd, or NiMH batteries; or, one lithium or lithium ion battery). Output current is 150 mA from a 3-V input. Only four external capacitors are needed to build a complete low-noise dc/dc converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output. From a 3-V input, the TPS60111 can start into full load with loads as low as 33 Ω.

The TPS60111 features either constant frequency mode to minimize noise and output voltage ripple or the power-saving pulse-skip mode to extend battery life at light loads. The TPS60111 switching frequency is 300 kHz. The logic shutdown function reduces the supply current to 1-µA (max) and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors and has low EMI. It is available in the small 20-pin TSSOP PowerPAD™ package (PWP).

output voltage ripple



typical operating circuit

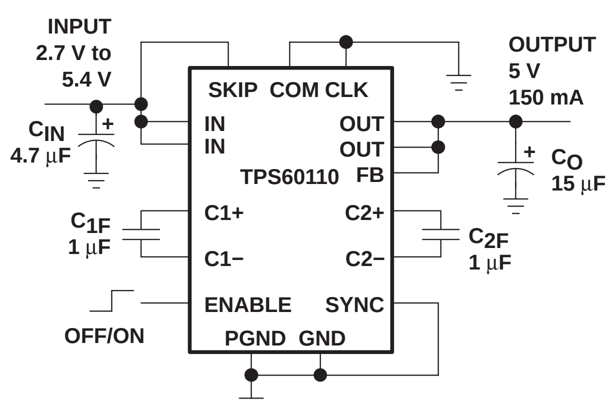
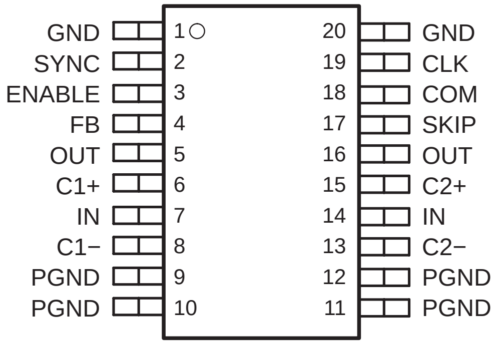


Figure 1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP PACKAGE
(TOP VIEW)



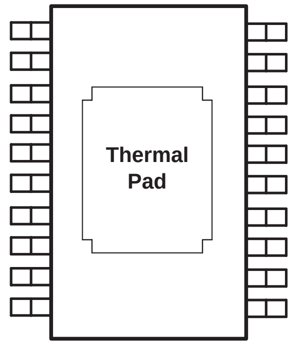


Figure 2. Bottom View of PWP Package, Showing the Thermal Pad

AVAILABLE OPTIONS

PACKAGE
TSSOP† **(PWP)**
TPS60111PWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TPS60111PWPR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	19	I	Input for external clock signal. If the internal clock is used, connect this terminal to GND.
C1+	6		Positive terminal of the charge-pump capacitor C_{1F}
C1−	8		Negative terminal of the charge-pump capacitor C_{1F}
C2+	15		Positive terminal of the charge-pump capacitor C_{2F}
C2−	13		Negative terminal of the charge-pump capacitor C_{2F}
COM	18	I	Mode selection. When COM is logic low the charge pump operates in push-pull mode to minimize output ripple. When COM is connected to IN the regulator operates in single-ended mode requiring only one flying capacitor.
ENABLE	3	I	ENABLE Input. The device turns off, the output disconnects from the input, and the supply current decreases to 0.05 µA when ENABLE is a logic low. ENABLE high may only be applied when VIN is inside the recommended operating range.
FB	4	I	FEEDBACK input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on-chip to match internal reference voltage of 1.22 V.
GND	1, 20		GROUND. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7, 14	I	Supply Input. Connect to an input supply in the 2.7-V to 5.4-V range. Bypass IN to GND with a (C_O/2) µF capacitor. Connect both INs through a short trace.
OUT	5, 16	O	Regulated 5-V power output. Connect both OUTs through a short trace and bypass OUT to GND with the output filter capacitor C_O.
PGND	9−12		PGND power ground. Charge-pump current flows through this pin. Connect all PGNDs together.
SKIP	17	I	Mode selection. When SKIP is logic low the charge pump operates in constant-frequency mode. Thus output ripple and noise are minimized. When SKIP is connected to IN, the regulator operates in low-quiescent-current pulse-skip mode.
SYNC	2	I	Selection for external clock signal. Connect to GND to use the internally generated clock signal. Connect to IN for external synchronization. In this case, the clock signal needs to be fed through CLK.

absolute maximum ratings (unless otherwise noted)†‡

Input voltage range, V_I (IN, OUT, ENABLE, SKIP, COM, CLK, FB, SYNC)	−0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND)	−0.3 V to (V_O + 0.3 V)
Differential input voltage, V_{ID} (C1−, C2− to GND)	−0.3 V to (V_{IN} + 0.3 V)
Continuous total power dissipation	See Dissipation Rating Tables
Continuous output current	200 mA
Storage temperature range, T_{stg}	−55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s	260°C
Maximum junction temperature, T_J	150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ V_{ENABLE}, V_{SKIP}, V_{COM}, V_{CLK} and V_{SYNC} can exceed V_{IN} up to the maximum rated voltage without increasing the leakage current drawn by these mode select inputs.

DISSIPATION RATING TABLE 1 − FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 − CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 W	285.7 mW/°C	22.9 W	18.5 W

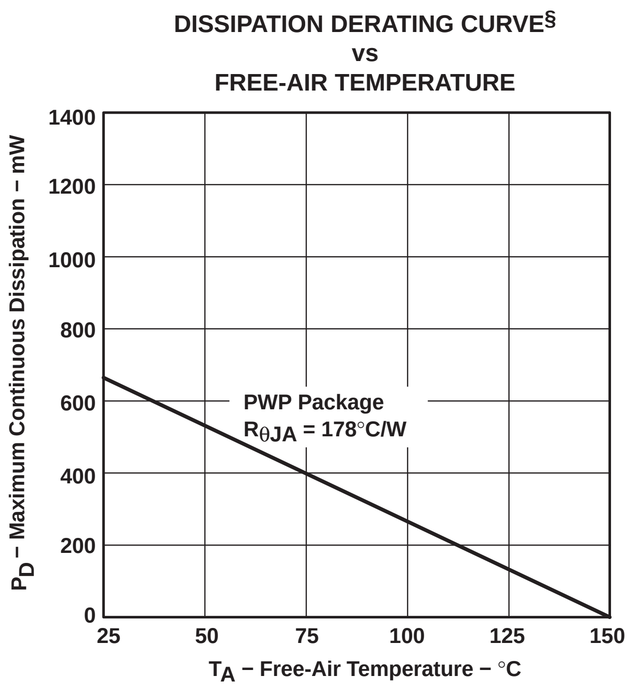


Figure 3

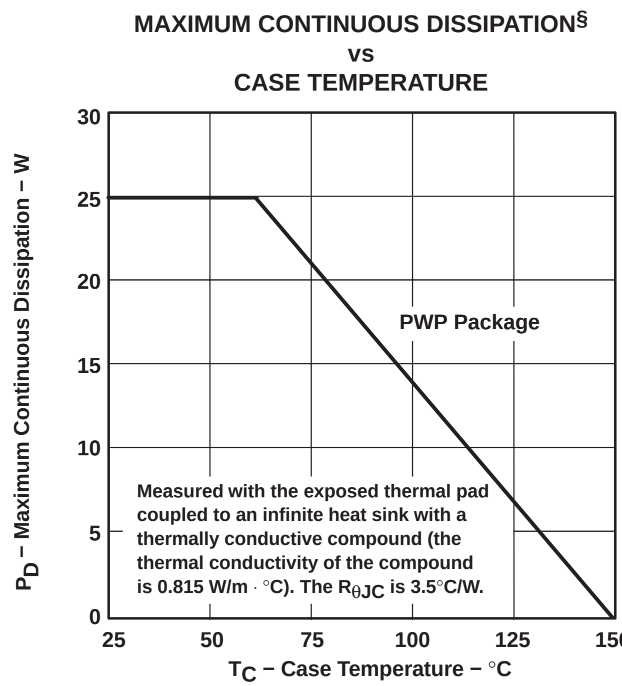


Figure 4

§ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

electrical characteristics at C_{IN} = 15 µF, C_{1F} = C_{2F} = 2.2 µF†, C_O = 33 µF, T_C = −40°C to 85°C, V_{IN} = 3 V, V_{FB} = V_O, V_{ENABLE} = V_{IN}, V_{SKIP} = V_{IN} or 0 V and V_{COM} = V_{CLK} = V_{SYNC} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.7		5.4	V
$I_{O(MAX)}$	Maximum output current		150			mA
V_O	Output voltage	2.7 V < V_{IN} < 3 V, 0 < I_O < 75 mA, $V_{O(Start\text{-}Up)}$ = 5 V, T_C = 25°C	4.8	5	5.2	V
		3 V < V_{IN} < 5 V, 0 < I_O < 150 mA	4.8	5	5.2	
		5 V < V_{IN} < 5.4 V, 0 < I_O < 150 mA	4.8	5	5.25	
$V_{O(RIP)}$	Output voltage ripple	I_O = 150 mA, V_{SKIP} = 0 V		10‡		mV_{PP}
$I_{O(LEAK)}$	Output leakage current	V_{IN} = 3.6 V, V_{ENABLE} = 0 V			1	µA
I_Q	Quiescent current (no-load input current)	V_{SKIP} = V_{IN} = 3.6 V		60	90	µA
		V_{SKIP} = 0 V, V_{IN} = 3.6 V		2.8		mA
$I_{DD(SDN)}$	Shutdown supply current	V_{IN} = 3.6 V, V_{ENABLE} = 0 V		0.05	1	µA
$f_{OSC(int)}$	Internal switching frequency	V_{IN} = 3.6 V	200	300	400	kHz
$f_{OSC(ext)}$	External clock frequency	V_{SYNC} = V_{IN}, V_{IN} = 2.7 V to 5.4 V	400	600	800	kHz
	External clock duty cycle	V_{SYNC} = V_{IN}, V_{IN}= 2.7V to 5.4 V	20%		80%	
	Efficiency	I_O = 75 mA		80%		
V_{INL}	Input voltage low, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 2.7 V			0.3 × V_{IN}	V
V_{INH}	Input voltage high, ENABLE, SKIP, COM, CLK, SYNC	V_{IN} = 5.4 V	0.7 × V_{IN}			V
$I_{I(LEAK)}$	Input leakage current, ENABLE, SKIP, COM, CLK, SYNC	V_{ENABLE} = V_{SKIP} = V_{COM} = V_{CLK} = V_{SYNC} = V_{GND} or V_{IN}		0.01	0.1	µA
	Output load regulation	V_O = 5 V, 1 mA < I_O < 150 mA, T_C = 25°C		0.002		%/mA
	Output line regulation	3 V < V_{IN} < 5 V, V_O = 5 V, I_O = 75 mA, T_C = 25°C		0.6		%/V
	Short circuit current	V_{IN} = 3.6 V, V_O = 0 V, T_C = 25°C		150		mA

† Use only ceramic capacitors with X5R or X7R dielectric as flying capacitors.
‡ Achieved with C_O = 22 µF + 10 µF X5R dielectric ceramic capacitor

TYPICAL CHARACTERISTICS†

EFFICIENCY
vs
OUTPUT CURRENT

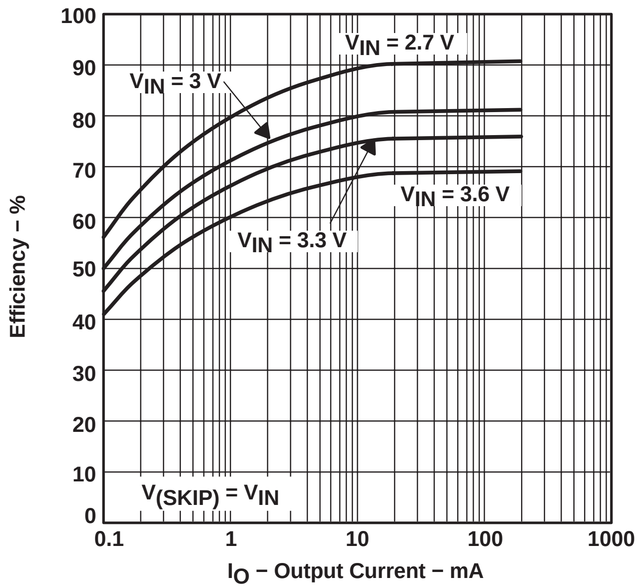


Figure 5

EFFICIENCY
vs
OUTPUT CURRENT

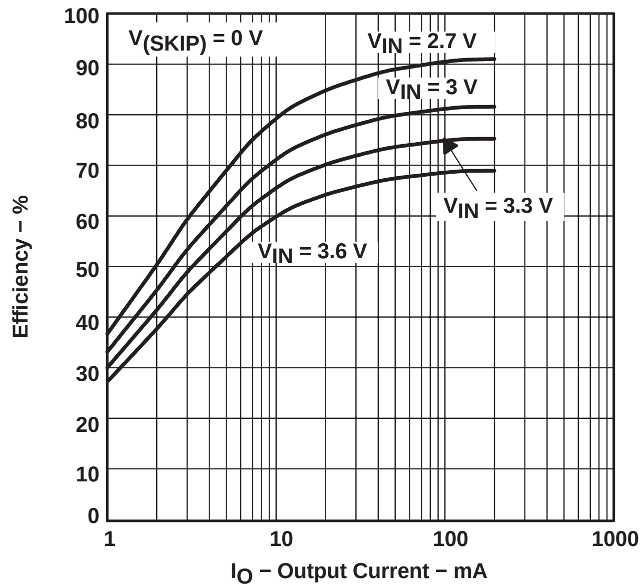


Figure 6

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

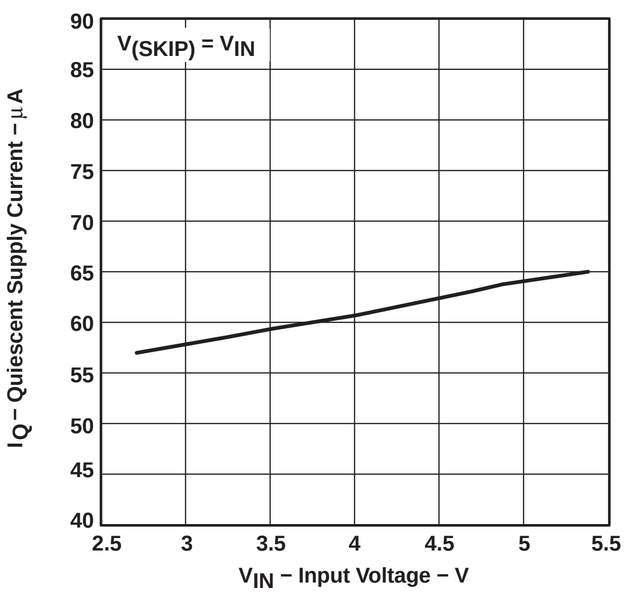


Figure 7

QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE

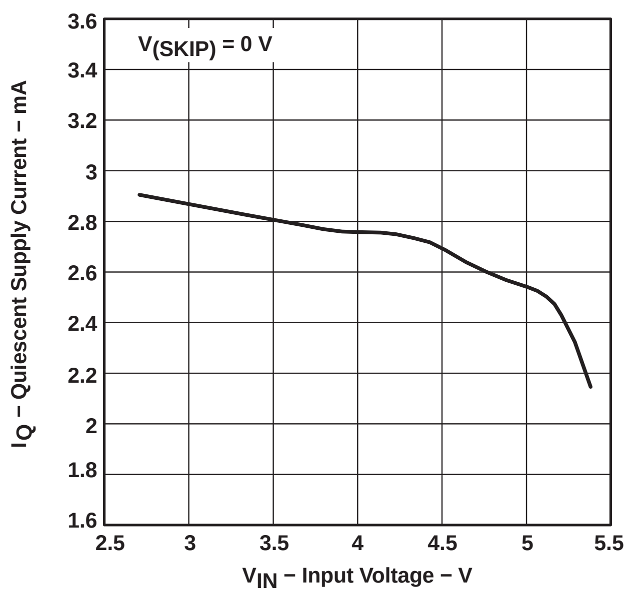


Figure 8

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

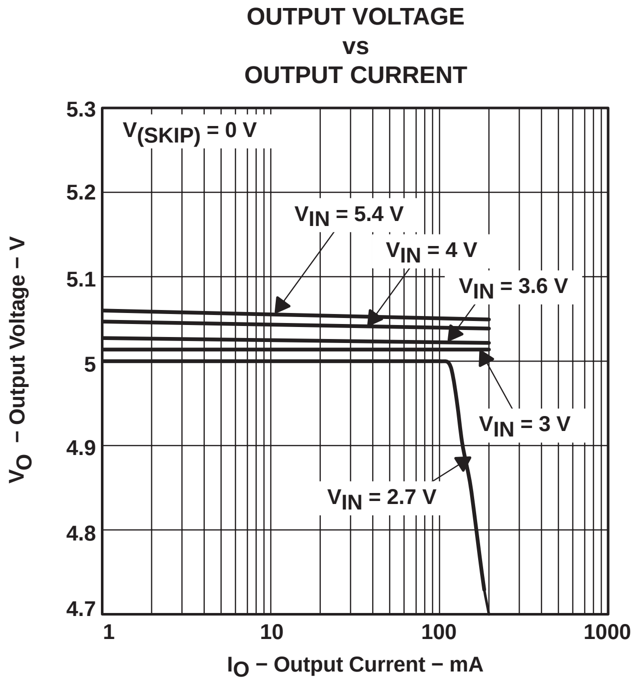


Figure 9

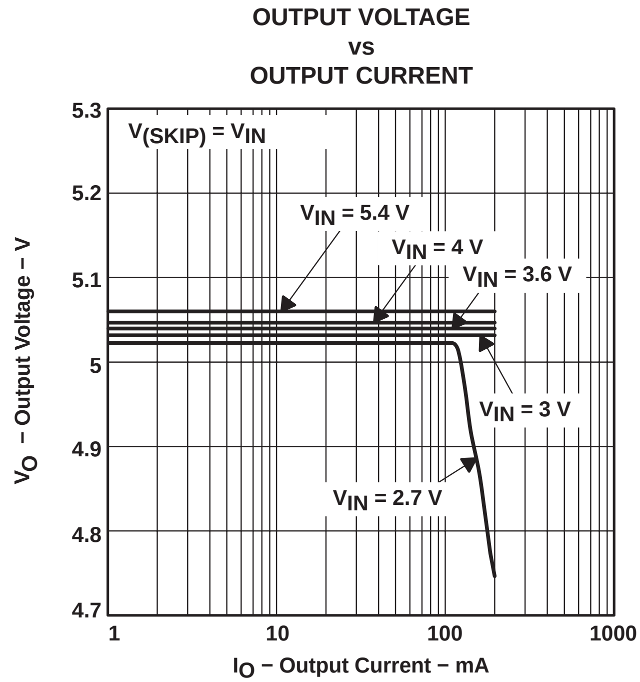


Figure 10

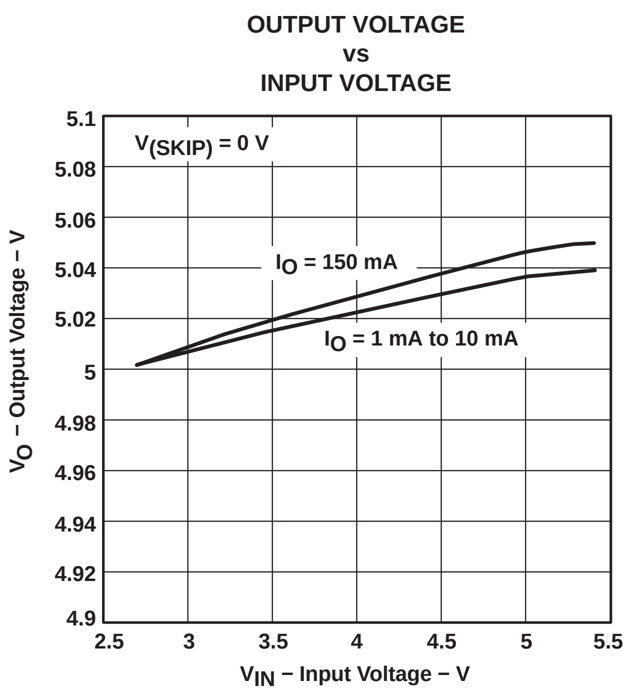


Figure 11

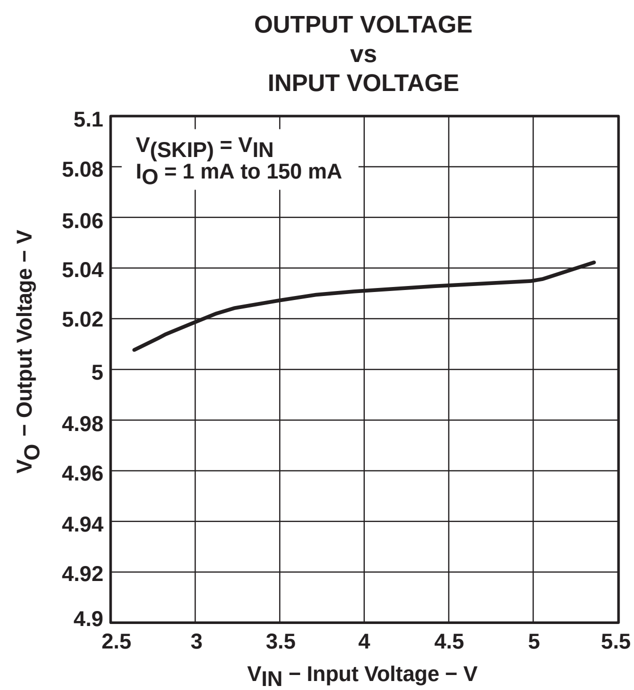


Figure 12

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs TIME

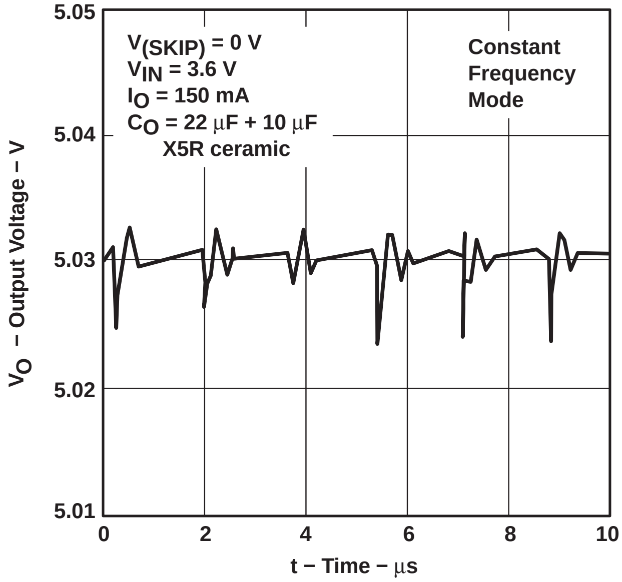


Figure 13

OUTPUT VOLTAGE vs TIME

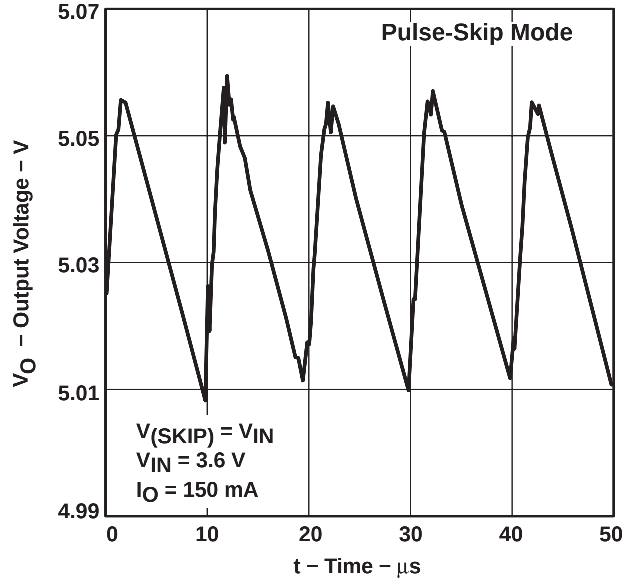


Figure 14

LOAD TRANSIENT RESPONSE

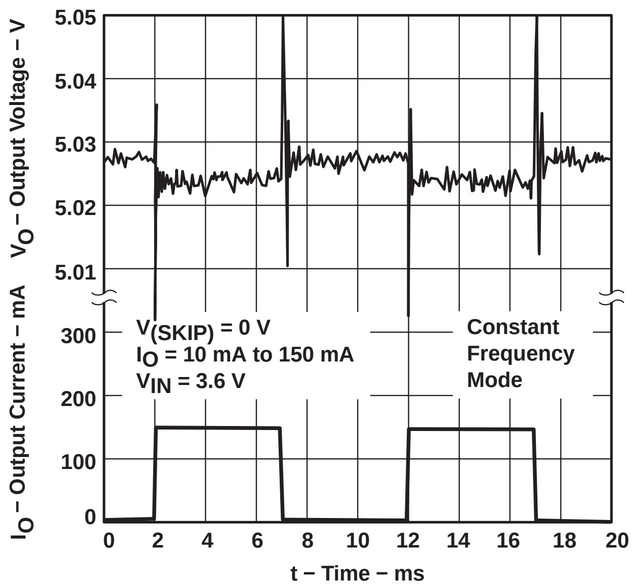


Figure 15

LOAD TRANSIENT RESPONSE

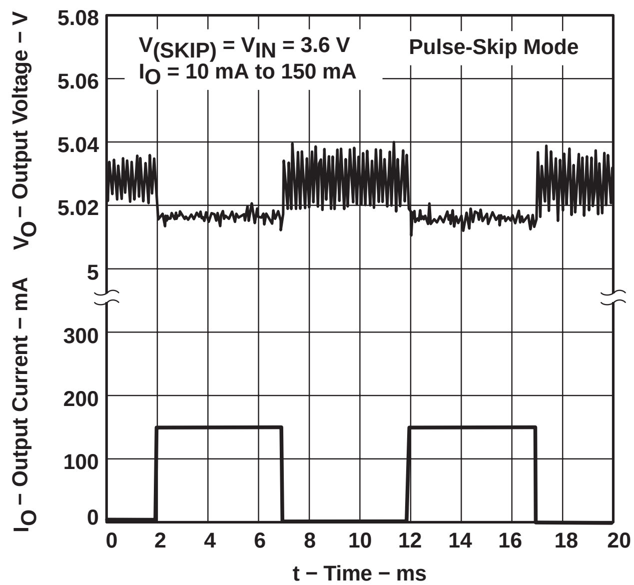


Figure 16

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted

TYPICAL CHARACTERISTICS†

LINE TRANSIENT RESPONSE

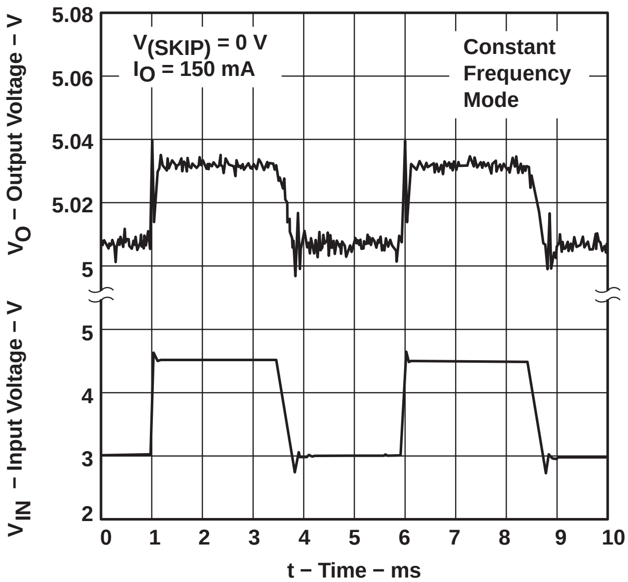


Figure 17

LINE TRANSIENT RESPONSE

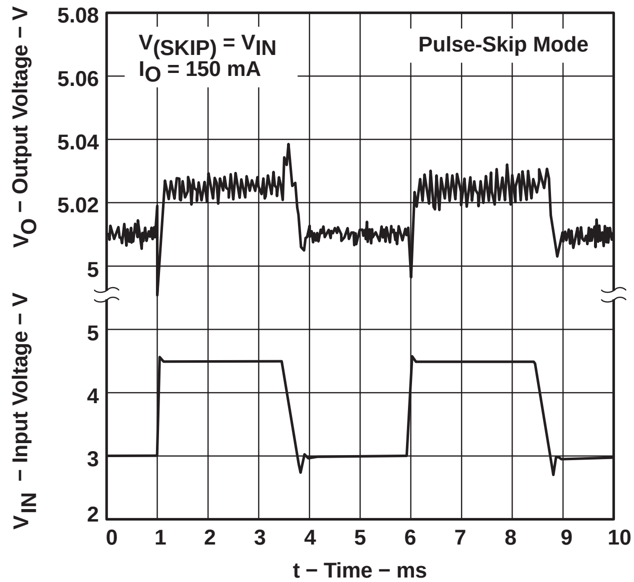


Figure 18

FREQUENCY SPECTRUM CONSTANT FREQUENCY MODE‡

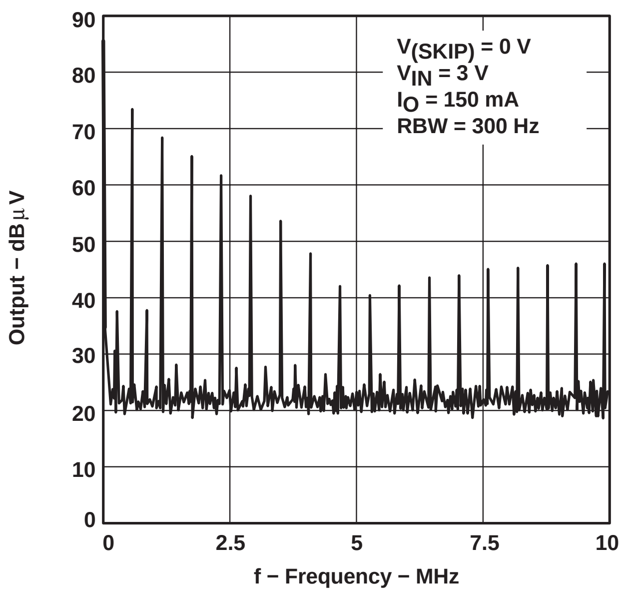


Figure 19

FREQUENCY SPECTRUM PULSE-SKIP MODE‡

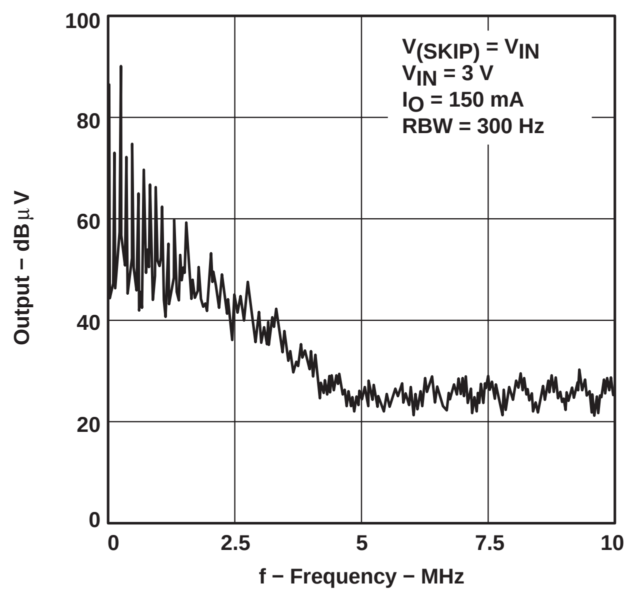


Figure 20

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 μF, C_{1F} and C_{2F} = 2.2 μF (X7R ceramic), C_O = 33 μF, unless otherwise noted
‡ Test circuit: TPS60110EVM−132 with TPS60111

TYPICAL CHARACTERISTICS†

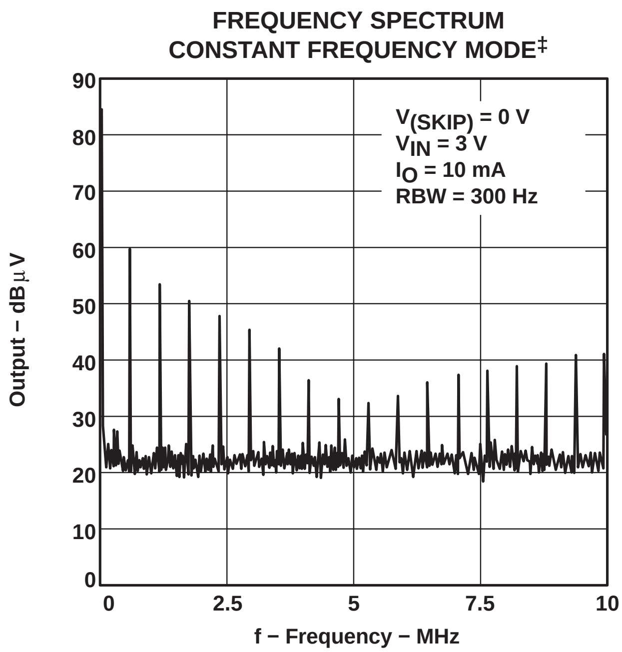


Figure 21

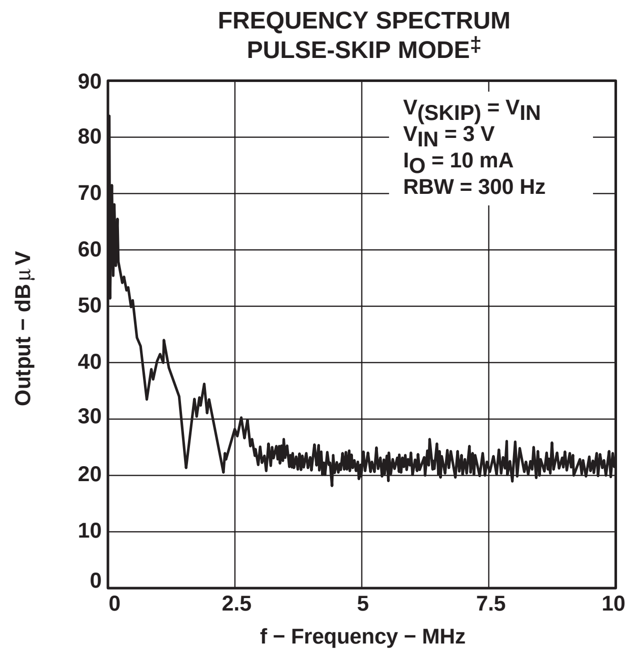


Figure 22

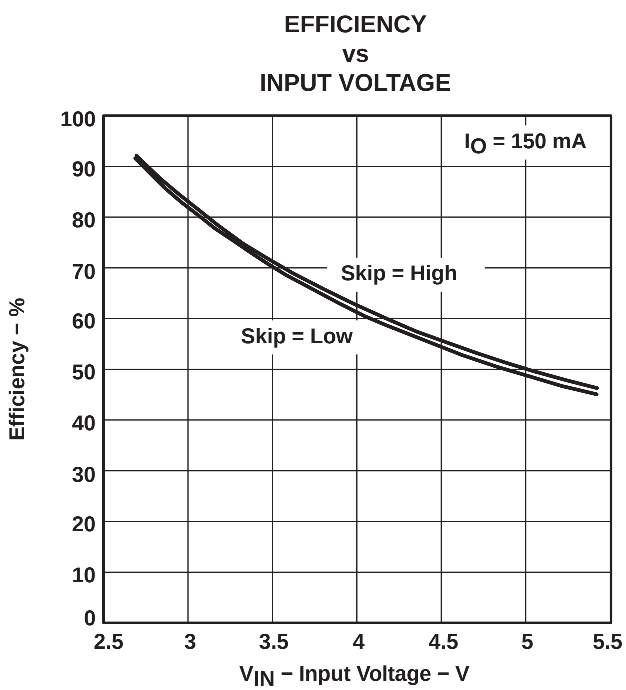


Figure 23

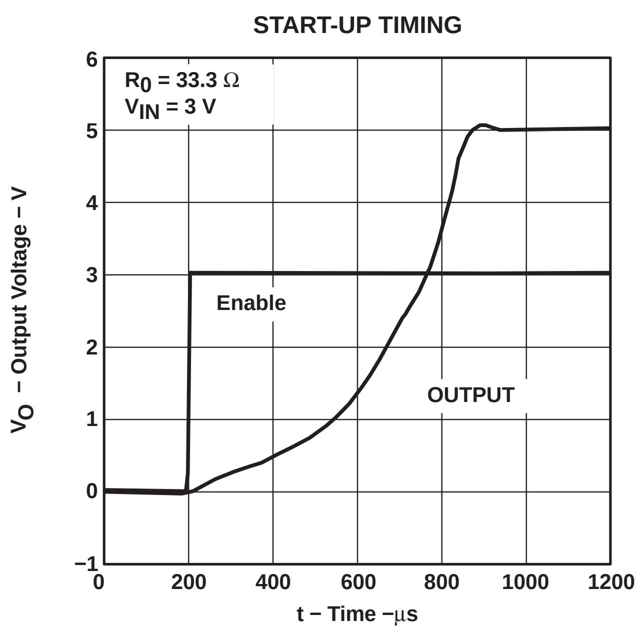


Figure 24

† T_C = 25°C, V_{COM} = V_{SYNC} = 0 V, C_{IN} = 15 µF, C_{1F} and C_{2F} = 2.2 µF (X7R ceramic), C_O = 33 µF, unless otherwise noted
‡ Test circuit: TPS60110EVM−132 with TPS60111

detailed description

operating principle

The TPS60111 charge pump provides a regulated 5-V output from a 2.7-V to 5.4-V input. It delivers a maximum load current of 150 mA. Designed specifically for space critical battery powered applications, the complete charge pump circuit requires only four external capacitors. The circuit can be optimized for highest efficiency at light loads or lowest output noise. The TPS60111 consists of an oscillator, a 1.22-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, and a control circuit (Figure 25).

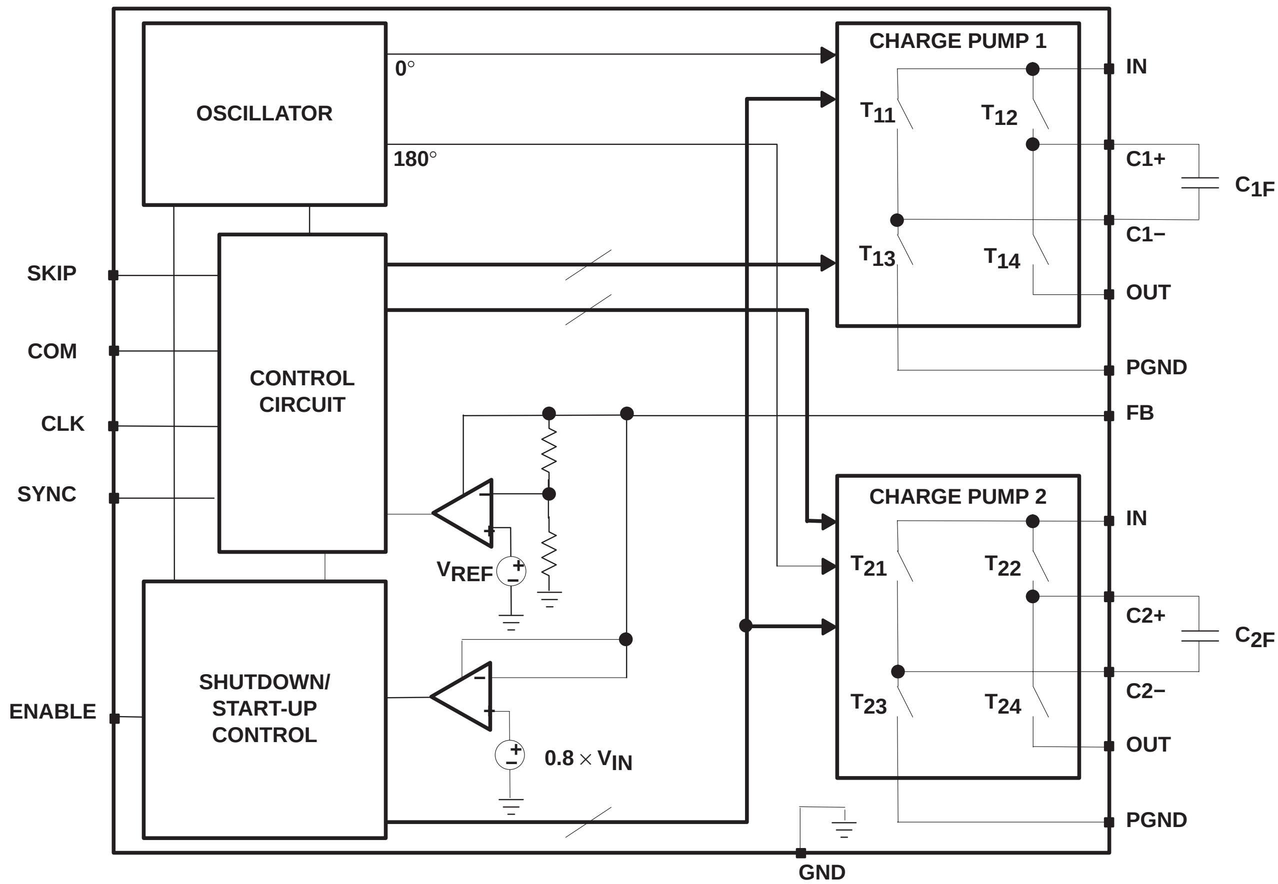


Figure 25. Functional Block Diagram TPS60111

The oscillator runs at a 50% duty cycle. The device consists of two single-ended charge pumps which operate with 180° phase shift. Each single ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name doubler). In order to provide a regulated fixed output voltage of 5 V, the TPS60111 uses either pulse-skip mode or constant-frequency mode. Pulse-skip mode and constant-frequency mode are externally selected via the SKIP input pin.

detailed description (continued)

start-up procedure

During start-up, i.e. when ENABLE is set from logic low to logic high, the switches T12 and T14 (charge pump 1), and the switches T22 and T24 (charge pump 2) are conducting to charge up the output capacitor until the output voltage V_O reaches $0.8 \times V_{IN}$. When the start-up comparator detects this limit, the IC begins to operate in the mode selected with SKIP and COM. This start-up charging of the output capacitor guarantees a short start-up time and eliminates the need for a Schottky diode between IN and OUT.

pulse-skip mode

In pulse-skip mode (SKIP = high), the error amplifier disables switching of the power stages when it detects an output higher than 5 V. The oscillator halts. The IC then skips switching cycles until the output voltage drops below 5 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference and error amplifier when the output is higher than 5 V. When switching is disabled from the error amplifier, the load is also isolated from the input. SKIP is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in pulse skip mode is shown in Figure 1.

constant-frequency mode

When SKIP is low, the charge pump runs continuously at the frequency f_{OSC}. The control circuit, fed from the error amplifier, controls the charge on C_{1F} and C_{2F} by driving the gates of the FETs T_{12}/T_{13} and T_{22}/T_{23}, respectively. When the output voltage falls, the gate drive increases, resulting in a larger voltage across C_{1F} and C_{2F}. This regulation scheme minimizes output ripple. Since the device switches continuously, the output noise contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads than pulse-skip mode.

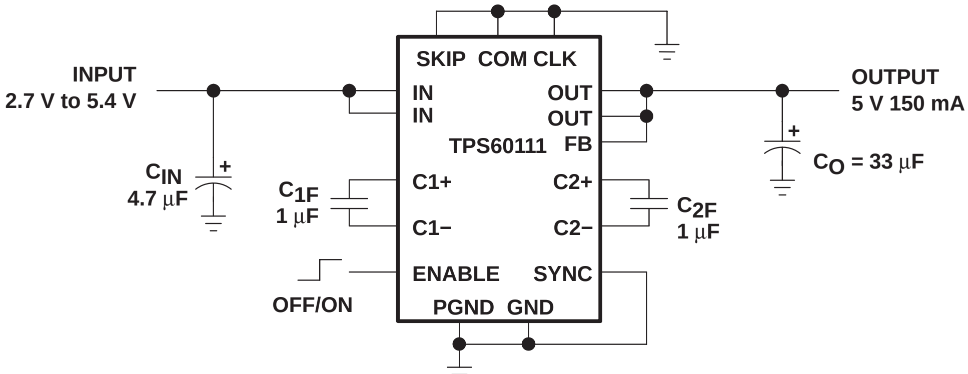


Figure 26. Typical Operating Circuit TPS60111 in Constant Frequency Mode

Table 1. Tradeoffs Between Operating Modes

FEATURE	PULSE-SKIP MODE (SKIP = High)	CONSTANT-FREQUENCY MODE (SKIP = Low)
Best light-load efficiency	X	
Smallest external component size for a given output ripple		X
Output ripple amplitude	Small amplitude	Very small amplitude
Output ripple frequency	Variable	Constant
Load regulation	Very good	Good

NOTE: Even in pulse-skip mode the output ripple amplitude is small if the push-pull operating mode is selected via COM.

detailed description (continued)

push-pull operating mode

In push-pull operating mode (COM = low), the two single-ended charge pumps operate with 180° phase shift. The oscillator signal has a 50% duty cycle. Each single-ended charge pump transfers charge into its transfer capacitor (C_{xF}) in one-half of the period. During the other half of the period (transfer phase), C_{xF} is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation guarantees an almost constant output current which ensures a low output ripple. COM is a logic input and should not remain floating. The typical operating circuit of the TPS60111 in push-pull mode is shown in Figure 1 and Figure 26.

single-ended operating mode

When COM is high, the device runs in single-ended operating mode. The two single-ended charge pumps operate in parallel without phase shift. They transfer charge into the transfer capacitor (C_F) in one half of the period. During the other half of the period (transfer phase), C_F is placed in series with the input to transfer its charge to C_O. In single-ended operating mode only one transfer capacitor ($C_F = C_{1F} + C_{2F}$) is required, resulting in less board space.

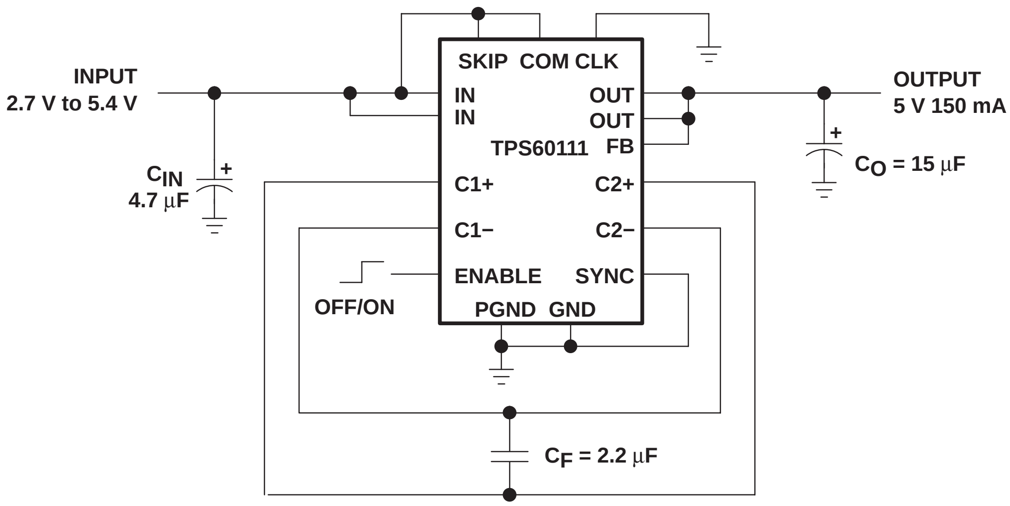


Figure 27. Typical Operating Circuit TPS60111 in Single-Ended Operating Mode

Table 2. Tradeoffs Between Operating Modes

FEATURE	PUSH-PULL MODE (COM = Low)	SINGLE-ENDED MODE (COM = High)
Output ripple amplitude	Small amplitude	Large amplitude
Smallest board space		X

detailed description (continued)

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05-µA (1-µA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 µA max. The device exits shutdown once ENABLE is set high level. The typical no-load shutdown exit time is 20 µs. When the device is in shutdown, the load is isolated from the input and the output is high impedance.

external clock signal

If the device operates at a user-defined frequency, an external clock signal can be used. Therefore, SYNC needs to be connected to IN and the external oscillator signal can drive CLK. The maximum external frequency is limited to 800 kHz. The switching frequency of the converter is half of the external oscillator frequency. It is recommended to operate the charge pump in constant-frequency mode if an external clock signal is used so that the output noise contains only well-defined frequency components.

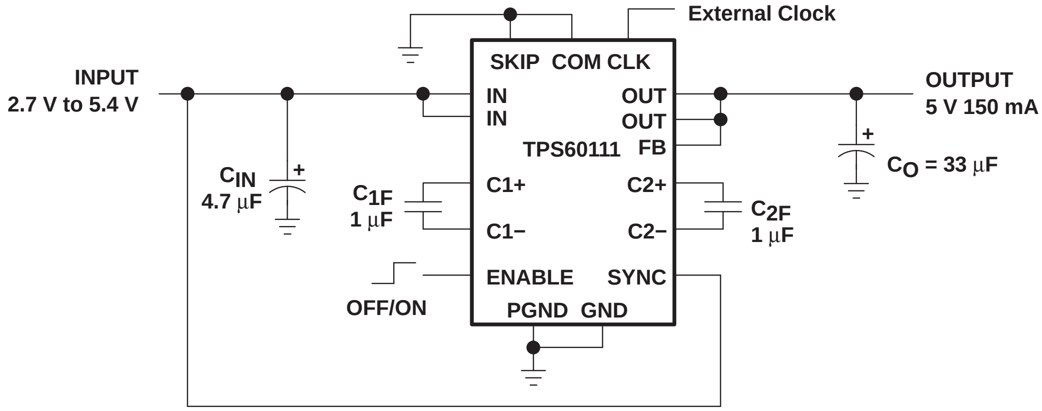


Figure 28. Typical Operating Circuit TPS60111 With External Synchronization

APPLICATION INFORMATION

capacitor selection

The TPS60111 requires only four external capacitors as shown in the basic application circuit. Their values are closely linked to the output current capacity, output noise requirements, and mode of operation. Generally, the transfer capacitors (C_{xF}) will be the smallest.

The input capacitor improves system efficiency by reducing the input impedance and stabilizes the input current. C_{IN} is recommended to be about two to four times as large as C_{xF}.

The output capacitor (C_O) can be selected from 8-times to 50-times larger than C_{xF}, depending on the mode of operation and ripple tolerance†. Tables 3 and 4 show capacitor values recommended for low quiescent-current operation (pulse-skip mode) and for low output voltage ripple operation (constant-frequency mode). A recommendation is given for smallest size.

Table 3. Recommended Capacitor Values for Low Quiescent-Current Operation† (pulse-skip mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	75	4.7		1	15		150
3.6	75		4.7 (X7R)	1		10 (X5R)	105
3.6	150	4.7		1	15		150
3.6	150		4.7 (X7R)	1		10 (X5R)	105

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

Table 4. Recommended Capacitor Values for Low Output Voltage Ripple Operation† (constant-frequency mode)

V_{IN} [V]	I_O [mA]	C_{IN} [µF]		C_{xF} [µF]	C_O [µF]		OUTPUT VOLTAGE RIPPLE V_{PP} [mV]
		TANTALUM	CERAMIC		TANTALUM	CERAMIC	
3.6	75	4.7		1	33		10
3.6	75		4.7 (X7R)	1		22 + 10, (X5R)	6
3.6	150	4.7		1	33		17
3.6	150		4.7 (X7R)	1		22 + 10, (X5R)	10

† All measurements are done with additional 1-µF X7R ceramic capacitors at input and output.

† In constant-frequency mode always select $C_O \geq 33$ µF

APPLICATION INFORMATION

For the TPS60111, the smallest board space size can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these type of capacitors might soon become competitive in size.

Table 5. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	TYPE
Taiyo Yuden	LMK212BJ105KG−T LMK212BJ225MG−T LMK316BJ475KL−T JMK316BJ106ML−T LMK432BJ226MM−T	1 µF 2.2 µF 4.7 µF 10 µF 22 µF	Ceramic Ceramic Ceramic Ceramic Ceramic
AVX	0805ZC105KAT2A 1206ZC225KAT2A TPSC475K035R0600 TPSC156K020R0450 TPSC336K010R0375	1 µF 2.2 µF 4.7 µF 15 µF 33 µF	Ceramic Ceramic Tantalum Tantalum Tantalum
Sprague	595D475X0016A2T 595D156X06R3A2T 595D156X0016B2T 595D336X06R3A2T 595D336X0016B2T 595D336X0016C2T	4.7 µF 15 µF 15 µF 33 µF 33 µF 33 µF	Tantalum Tantalum Tantalum Tantalum Tantalum Tantalum
Kemet	T494B475M010AS T494C156K010AS T494C336K010AS	4.7 µF 15 µF 33 µF	Tantalum Tantalum Tantalum

Table 6 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 6. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t−yuden.com
AVX	X7R/X5R ceramic TPS−series tantalum	www.avxcorp.com
Sprague	595D−series tantalum 593D−series tantalum	www.vishay.com
Kemet	T494−series tantalum	www.kemet.com

power dissipation

The power dissipated in the TPS60111 depends on output current and is approximated by:

$$P_{DISS} = I_O \times \left(2\,V_{IN} - V_O\right) \text{ for } I_Q << I_O$$

P_{DISS} must be less than that allowed by the package rating. See the ratings for 20-PowerPAD™ package power-dissipation limits and deratings.

APPLICATION INFORMATION

layout

All capacitors should be soldered in close proximity to the IC. A PCB layout proposal for a two-layer board is given in Figure 29. Care has been taken to connect both single-ended charge pumps symmetrically to the load to achive optimized output voltage ripple performance. The proposed layout also provides improved thermal performance as the exposed leadframe is soldered to the PCB. The bottom layer of the PCB is a ground plain only. All ground areas on the PCB should be connected. Connect ground areas on top layer to the bottom layer via through hole connections.

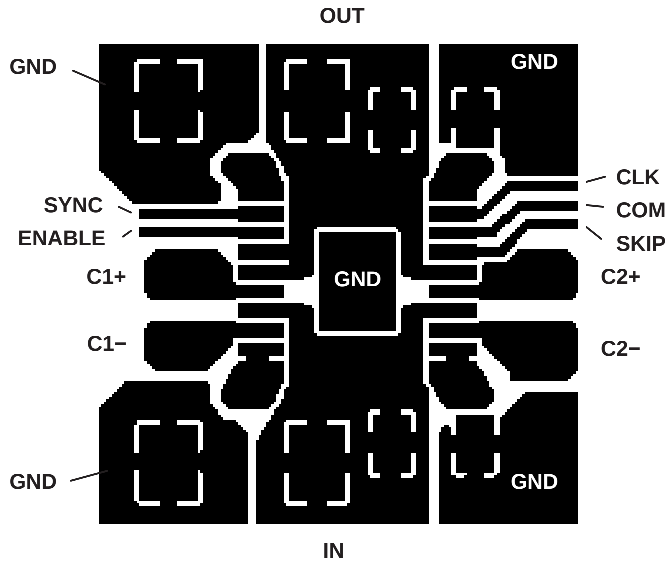


Figure 29. Recommended PCB Layout for TPS60111 (top view)

The evaluation module designed for the TPS60110 can, with slight modifications, be used for evaluation of the TPS60111. The EVM can be ordered under literature code SLVP132 or under product code TPS60110EVM−132.

APPLICATION INFORMATION

applications proposals

TPS60111 with LC output filter for ultra low ripple

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 30. The addition of a small inductor and filter capacitor will reduce the output ripple well below what could be achieved with capacitors alone. The corner frequency of 500 kHz was chosen above the 300 kHz switching frequency to avoid loop stability issues in case the feedback is taken from the output of the LC filter. Leaving the feedback (FB) connection point before the LC filter, the filter capacitance value can be increased to achieve even higher ripple attenuation without affecting stability margin.

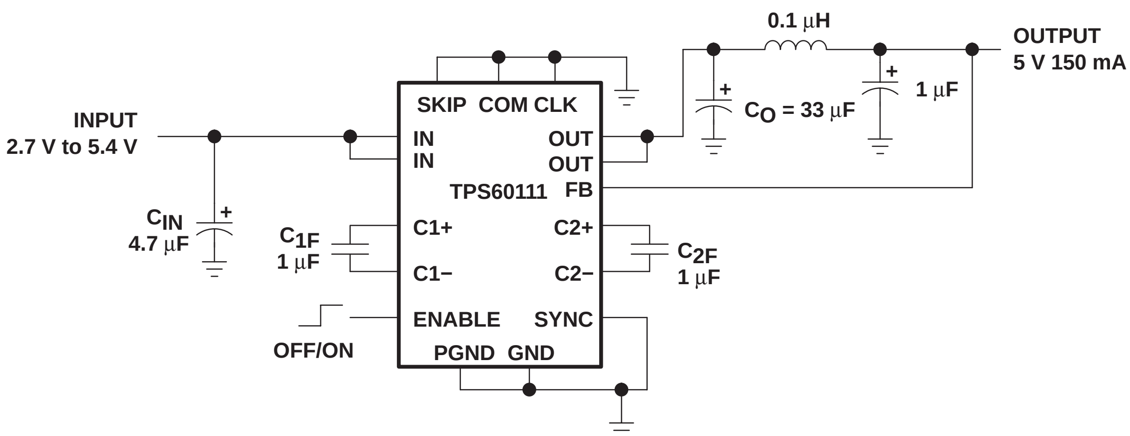


Figure 30. TPS60111 With LC Filter for Ultra Low Output Ripple Applications

related information

application reports

For more application information see:

- *PowerPAD™ Application Report* (Literature Number: SLMA002)
- *TPS6010x/TPS6011x Charge Pump Application Report* (Literature Number: SLVA070)

device family products

Other devices in this family are:

PART NUMBER	LITERATURE NUMBER	DESCRIPTION
TPS60100	SLVS213	Regulated 3.3-V, 200-mA Low-Noise Charge Pump DC/DC Converter
TPS60101	SLVS214	Regulated 3.3-V, 100-mA Low-Noise Charge Pump DC/DC Converter
TPS60110	SLVS215	Regulated 5-V, 300-mA Low-Noise Charge Pump DC/DC Converter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60111PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60111	Samples
TPS60111PWPG4	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60111	Samples
TPS60111PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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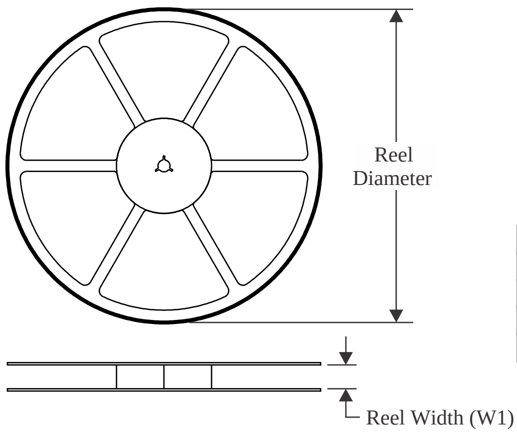
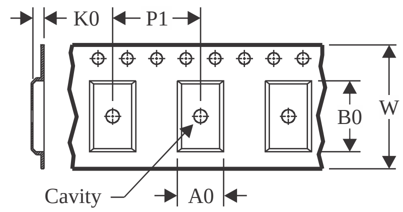
TAPE AND REEL INFORMATION

REEL DIMENSIONS

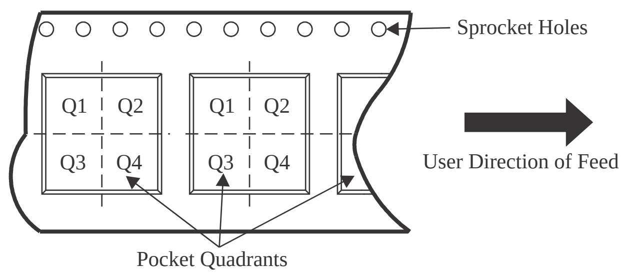


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

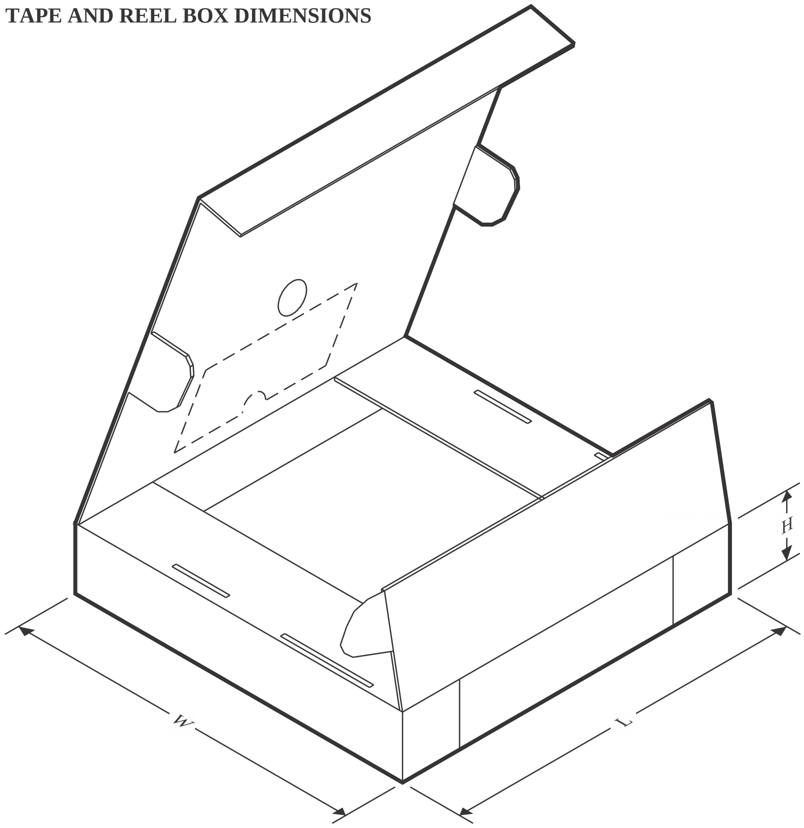
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60111PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

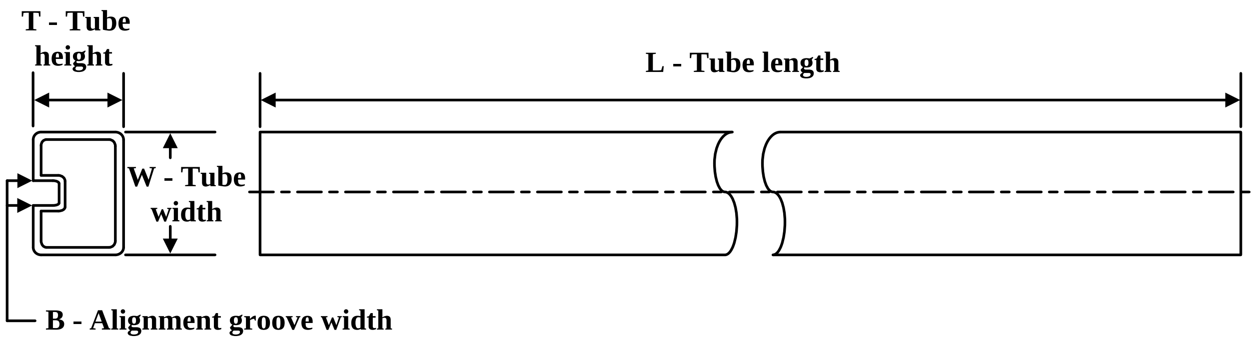
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60111PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

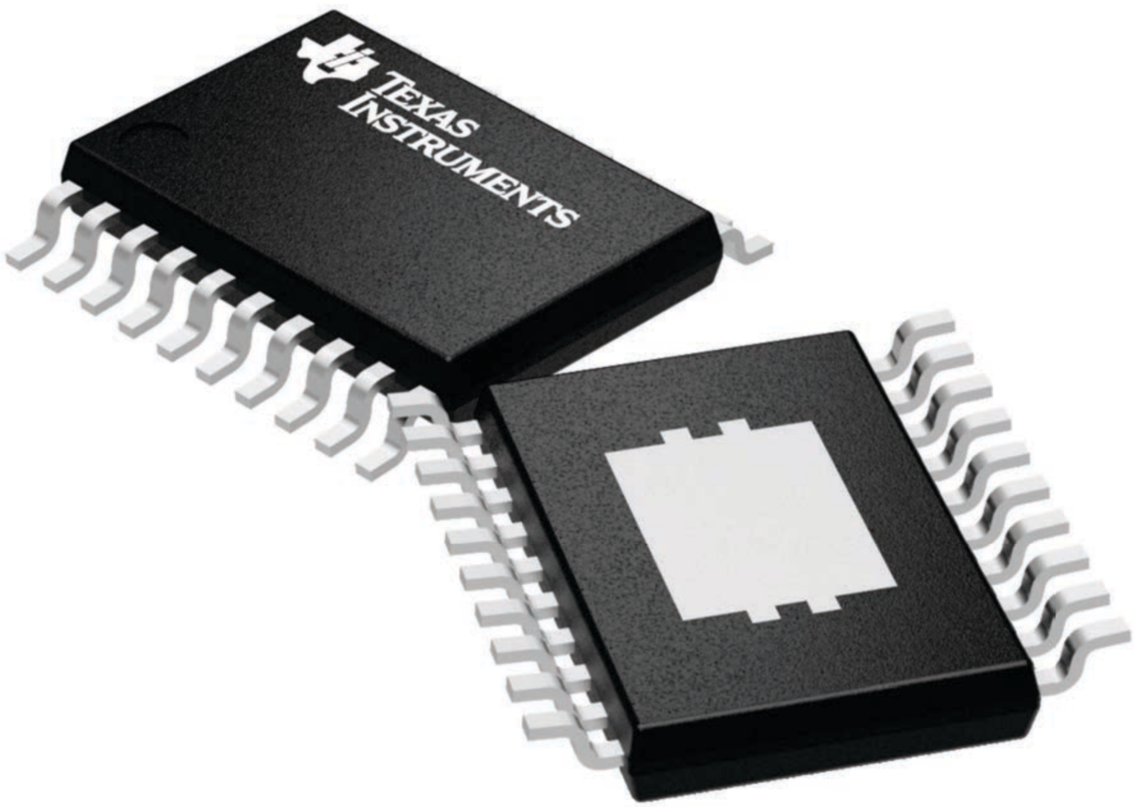
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60111PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS60111PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

PWP 20 — **HTSSOP - 1.2 mm max height**

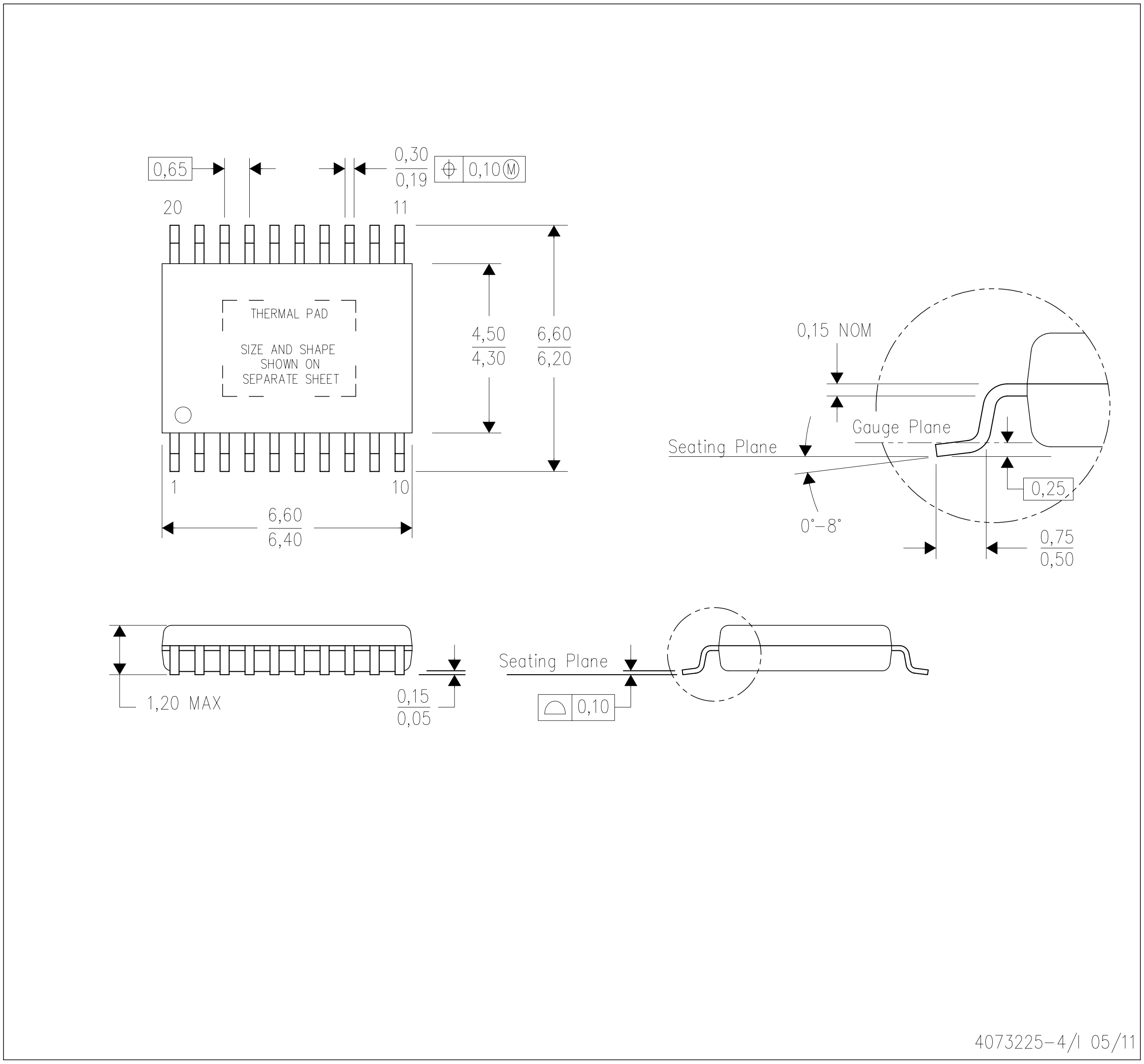
6.5 x 4.4, 0.65 mm pitch — SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

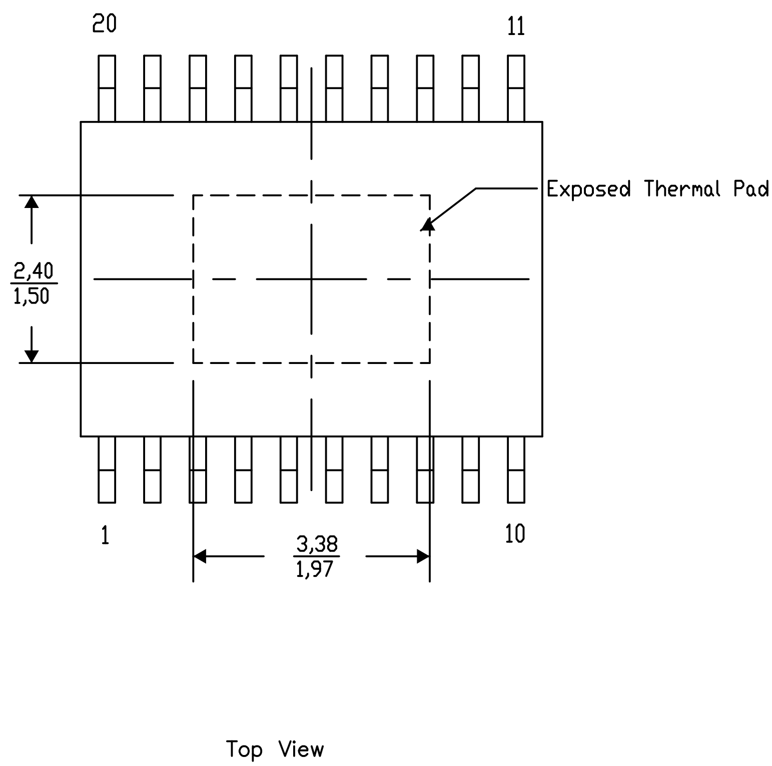
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



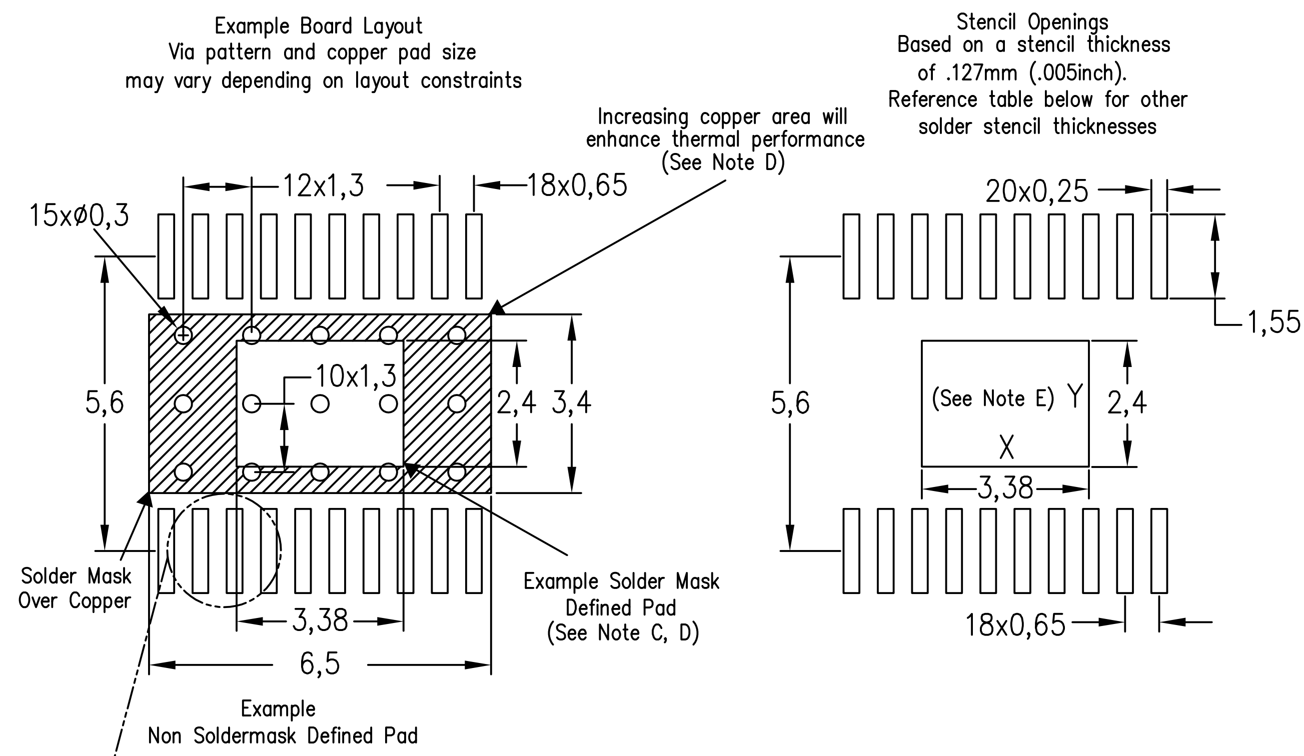
Exposed Thermal Pad Dimensions

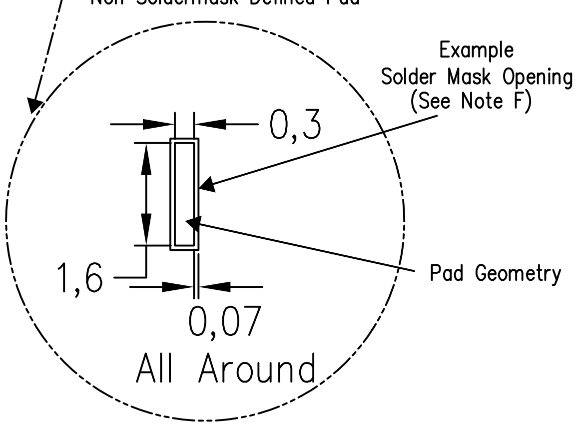
4206332-19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609-7/W 09/15

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265