ON Semiconductor

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MOSFET - Power, N-Channel, SUPERFET® III, FAST

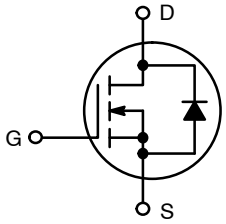
650 V, 67 mΩ, 40 A

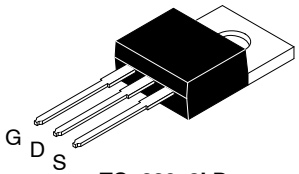
NTP067N65S3H

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V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	67 mΩ @ 10 V	40 A





TO−220−3LD
CASE 340AT

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

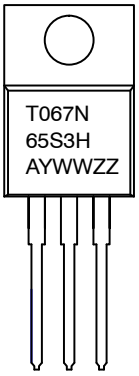
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 55 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 80 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 691 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

MARKING DIAGRAM



T067N65S3H	= Specific Device Code
A	= Assembly Plant Code
YWW	= Date Code (Year & Week)
ZZ	= Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	40	A
		Continuous (T_C = 100°C)	25	
I_{DM}	Drain Current	Pulsed (Note 1)	112	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		422	mJ
I_{AS}	Avalanche Current (Note 2)		6.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.66	mJ
dv/dt	MOSFET dv/dt		120	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	266	W
		Derate Above 25°C	2.13	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 6.5 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.47	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NTP067N65S3H	T067N65S3H	TO−220−3LD (Pb-Free / Halogen Free)	50 Units / Tube

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C		0.63		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			2	μA
		V_{DS} = 520 V, T_C = 125°C		1.6		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.9 mA	2.4		4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A		55	67	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A		28		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz		3750		pF
C_{oss}	Output Capacitance			60		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		691		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		107		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 10 V (Note 4)		80		nC
Q_{gs}	Gate to Source Gate Charge			21		nC
Q_{gd}	Gate to Drain “Miller” Charge			20		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.6		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)		29		ns
t_r	Turn-On Rise Time			8.5		ns
$t_{d(off)}$	Turn-Off Delay Time			80		ns
t_f	Turn-Off Fall Time			2.6		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				40	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				112	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs		403		ns
Q_{rr}	Reverse Recovery Charge			7.4		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

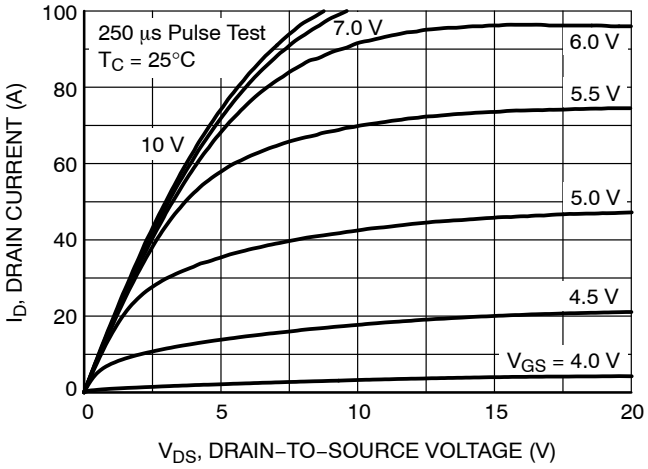


Figure 1. On−Region Characteristics

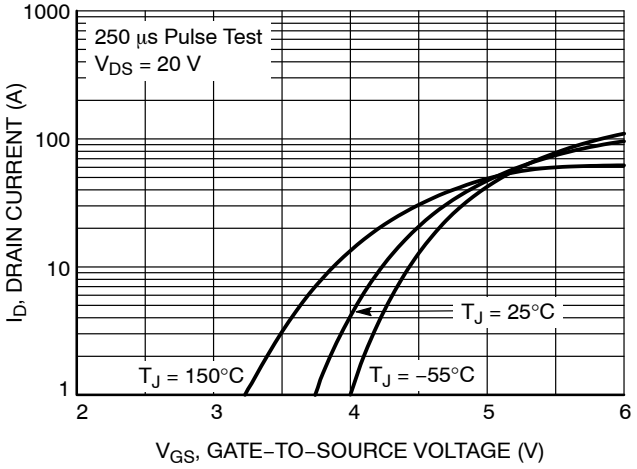


Figure 2. Transfer Characteristics

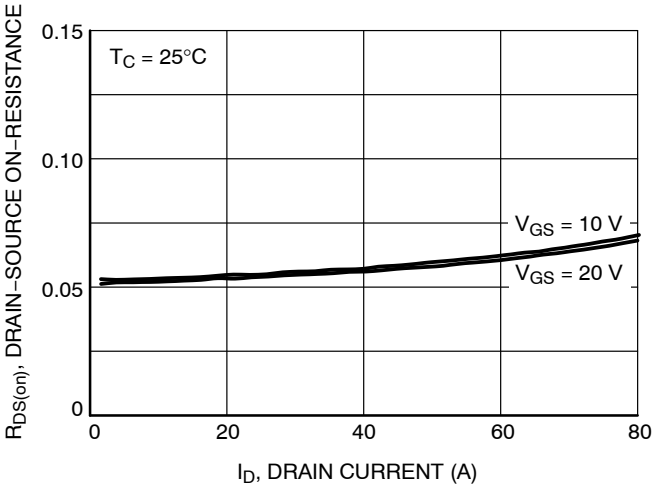


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

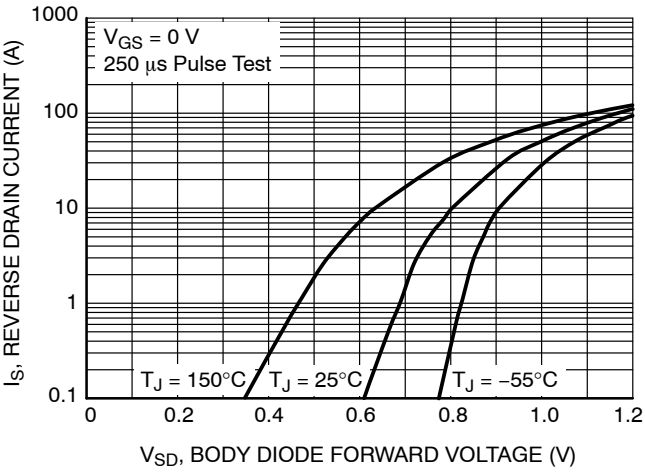


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

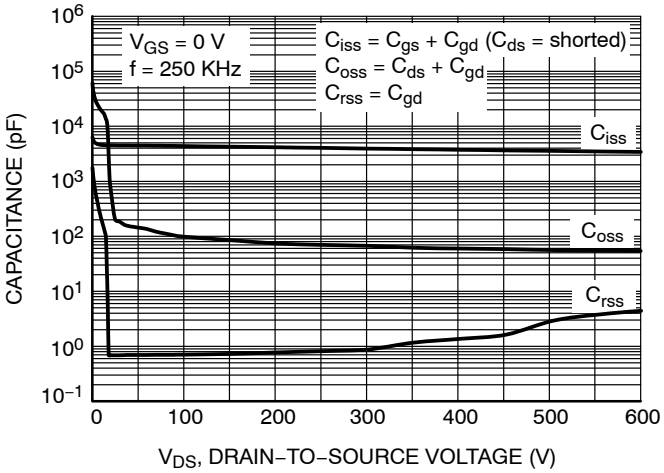


Figure 5. Capacitance Characteristics

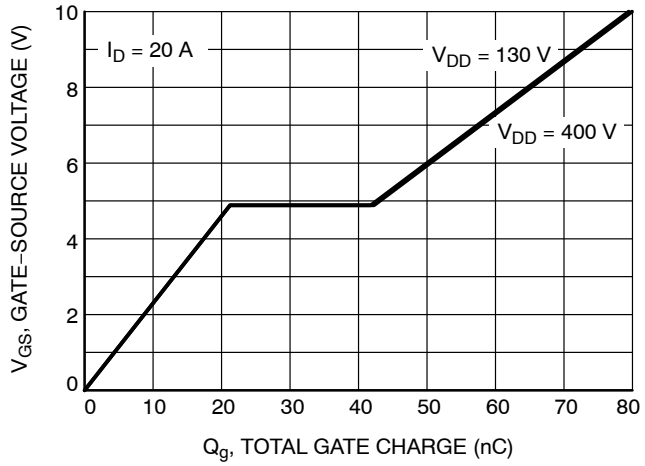


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

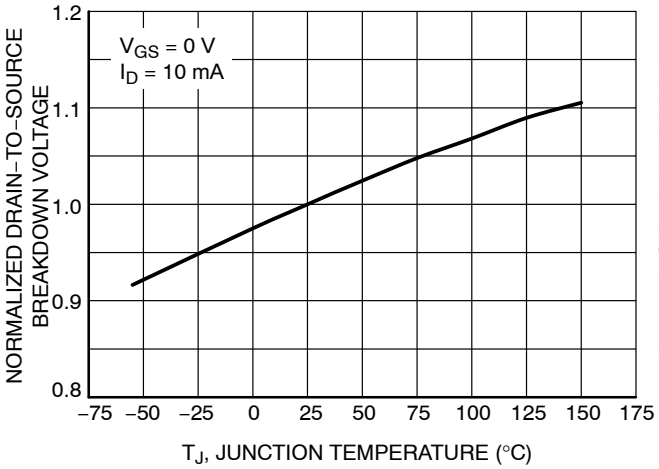


Figure 7. Breakdown Voltage Variation vs. Temperature

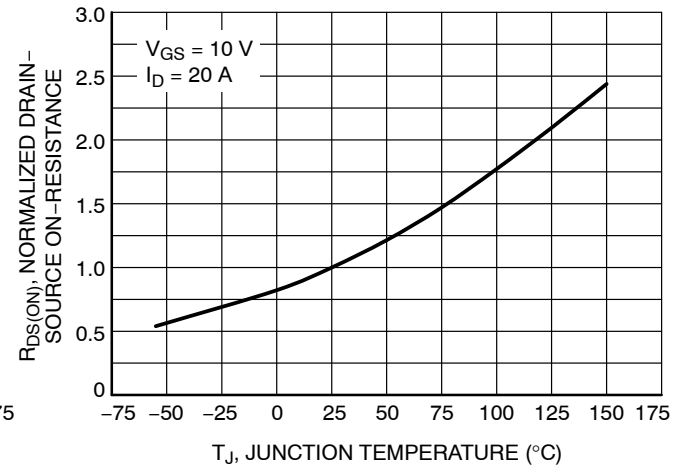


Figure 8. On−Resistance Variation vs. Temperature

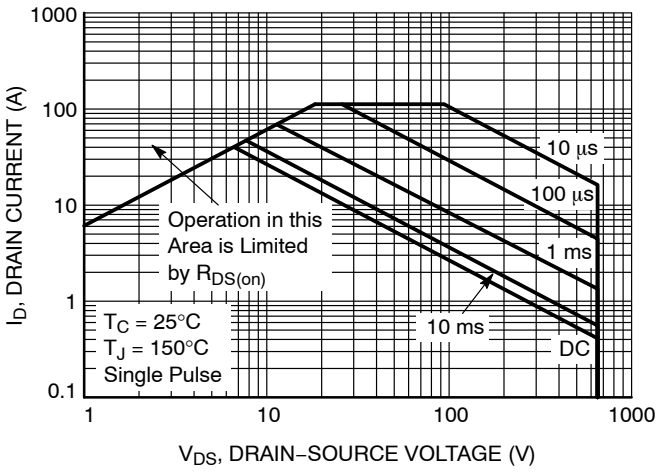


Figure 9. Maximum Safe Operating Area

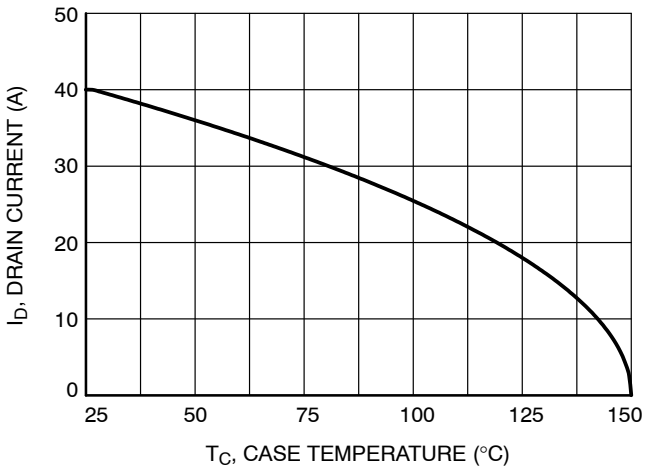


Figure 10. Maximum Drain Current vs. Case Temperature

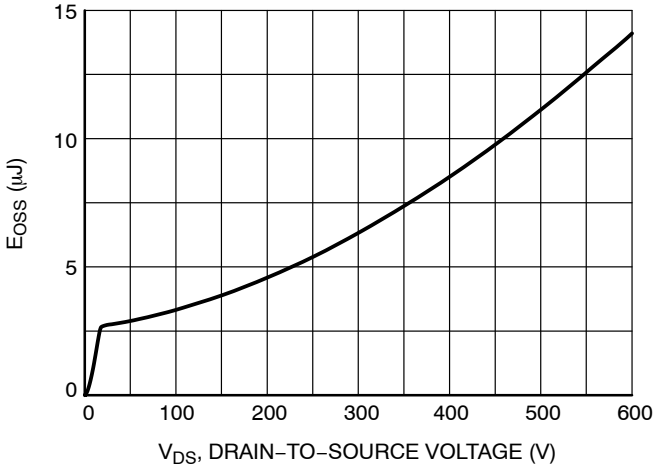


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

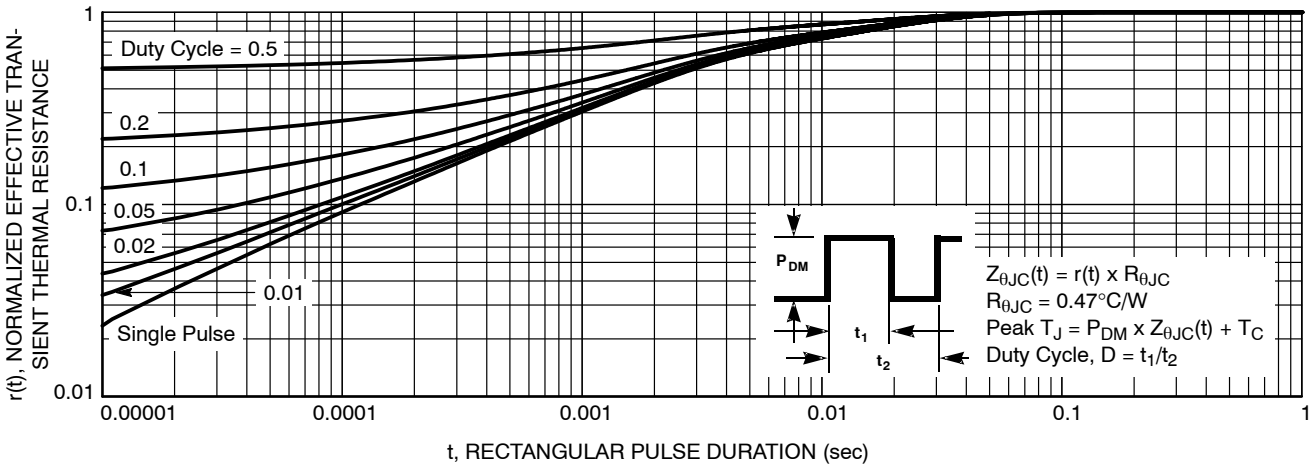


Figure 12. Transient Thermal Impedance

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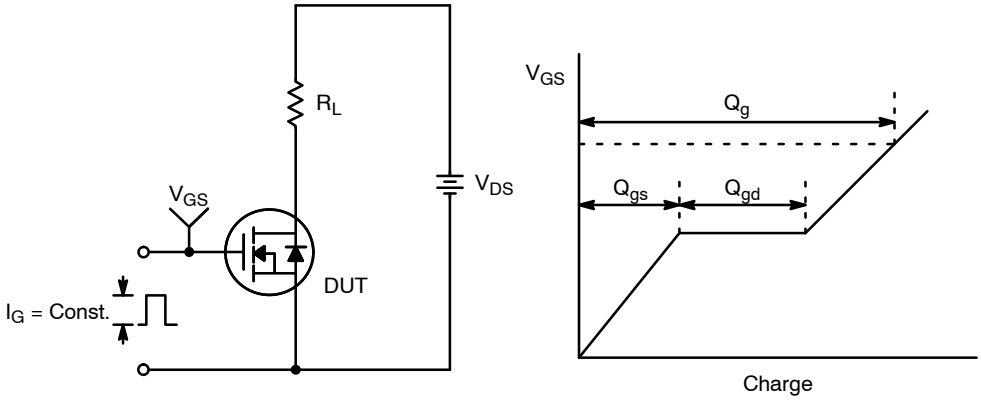


Figure 13. Gate Charge Test Circuit & Waveform

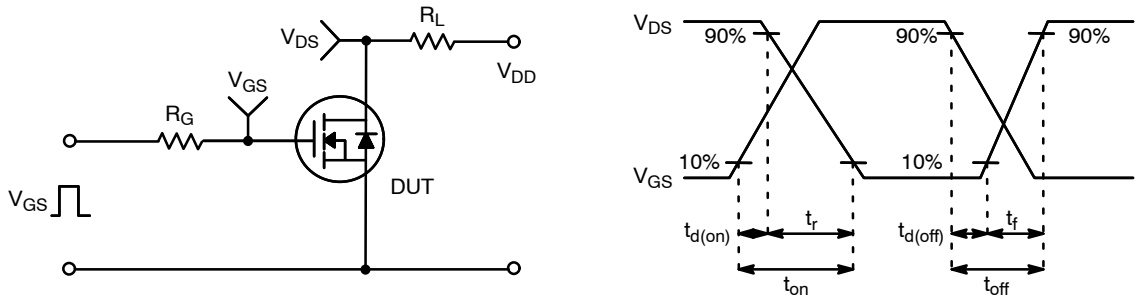


Figure 14. Resistive Switching Test Circuit & Waveforms

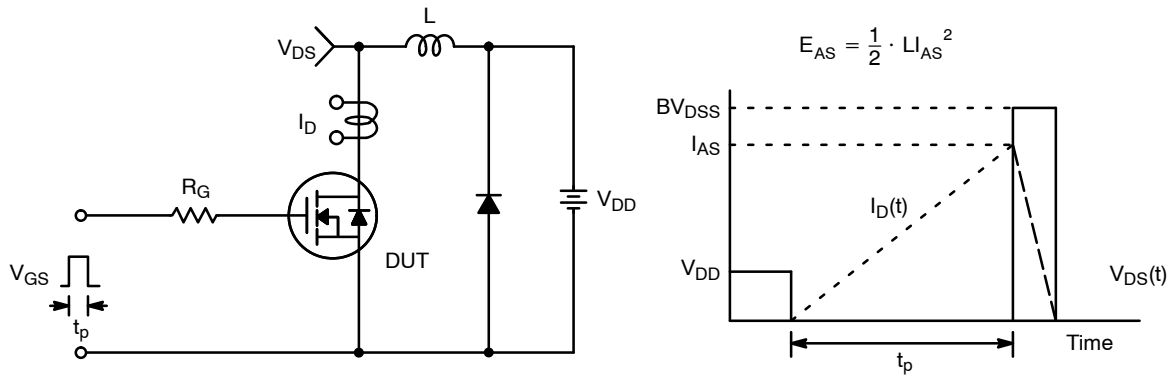


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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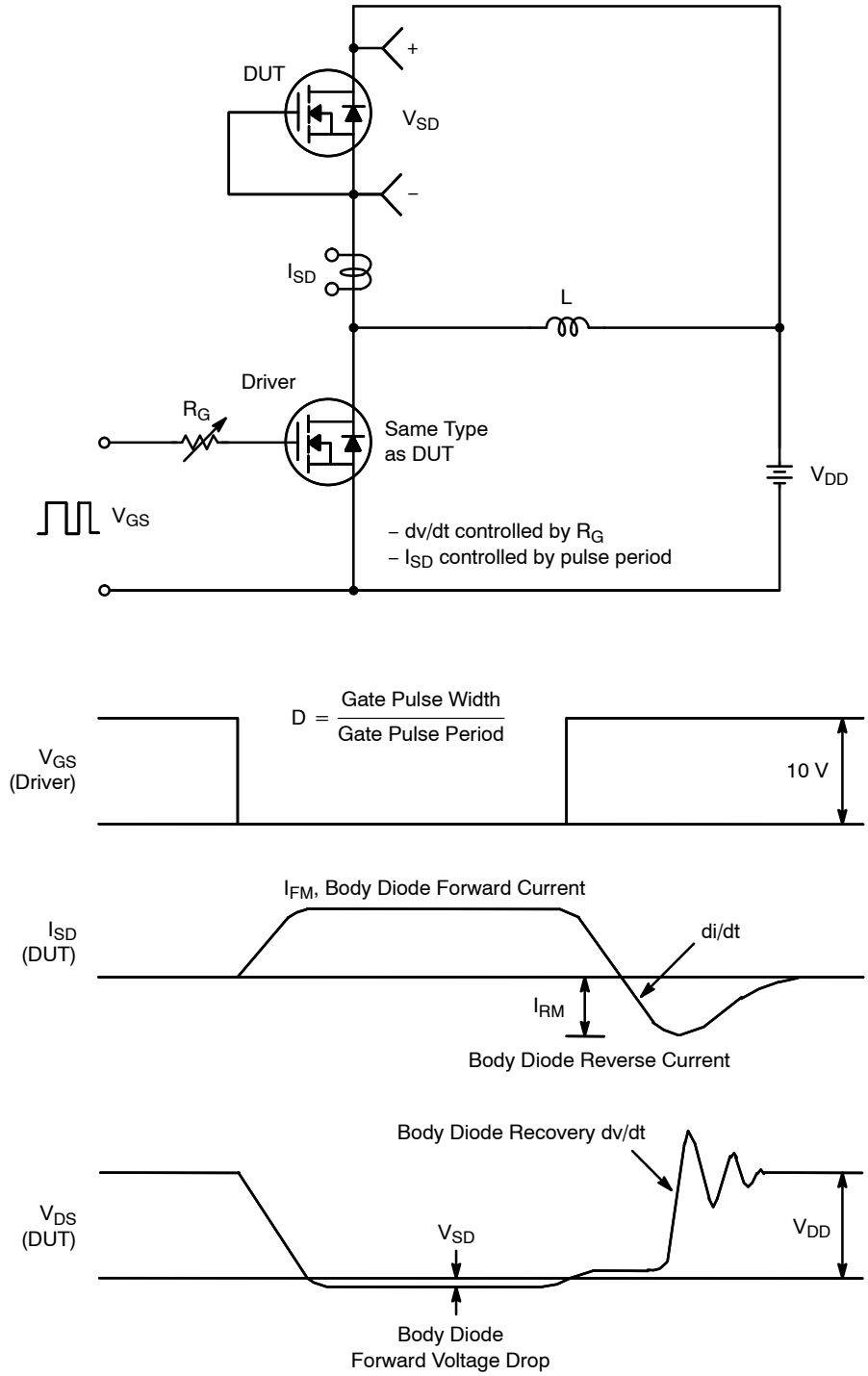


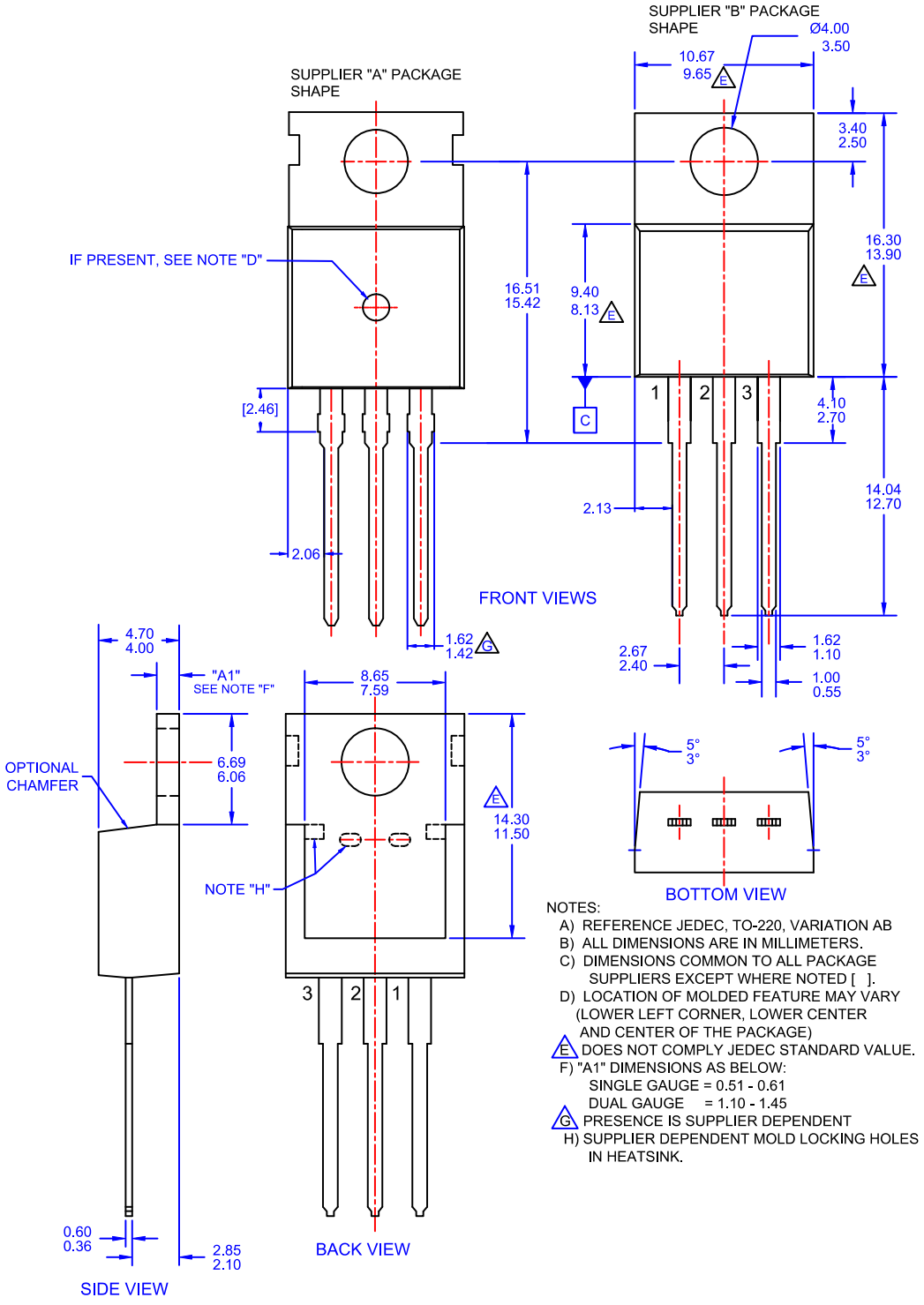
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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PACKAGE DIMENSIONS

TO−220−3LD
CASE 340AT
ISSUE A



NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
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DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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