

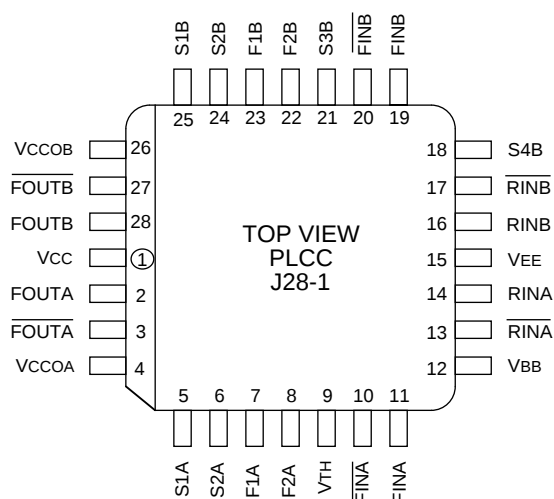
## FEATURES

- 3.3V and 5V power supply options
- 1.12GHz maximum VCO frequency
- 30MHz to 560MHz reference input operating frequency
- Frequency doubler mode
- Low jitter design
- PECL differential outputs
- PECL and TTL reference voltages available
- External loop filter optimizes performance/cost
- Available in 28-pin PLCC package

## APPLICATIONS

- Workstations
- Advanced communications
- High-end consumer
- High-performance computing

## PIN CONFIGURATION



## DESCRIPTION

The SY89420V device consists of two identical, low jitter, digital Phase Locked Loops based on Micrel-Synergy's differential PLL technology. Each of the PLLs (PLLA and PLLB) is capable of operating in the 30MHz to 560MHz input reference frequency range independently of the other and is configurable separately. The PLLs can be configured to be matched in all regards, or can be configured so that PLLB is used as a frequency doubler, while PLLA is used to regenerate the undoubled frequency.

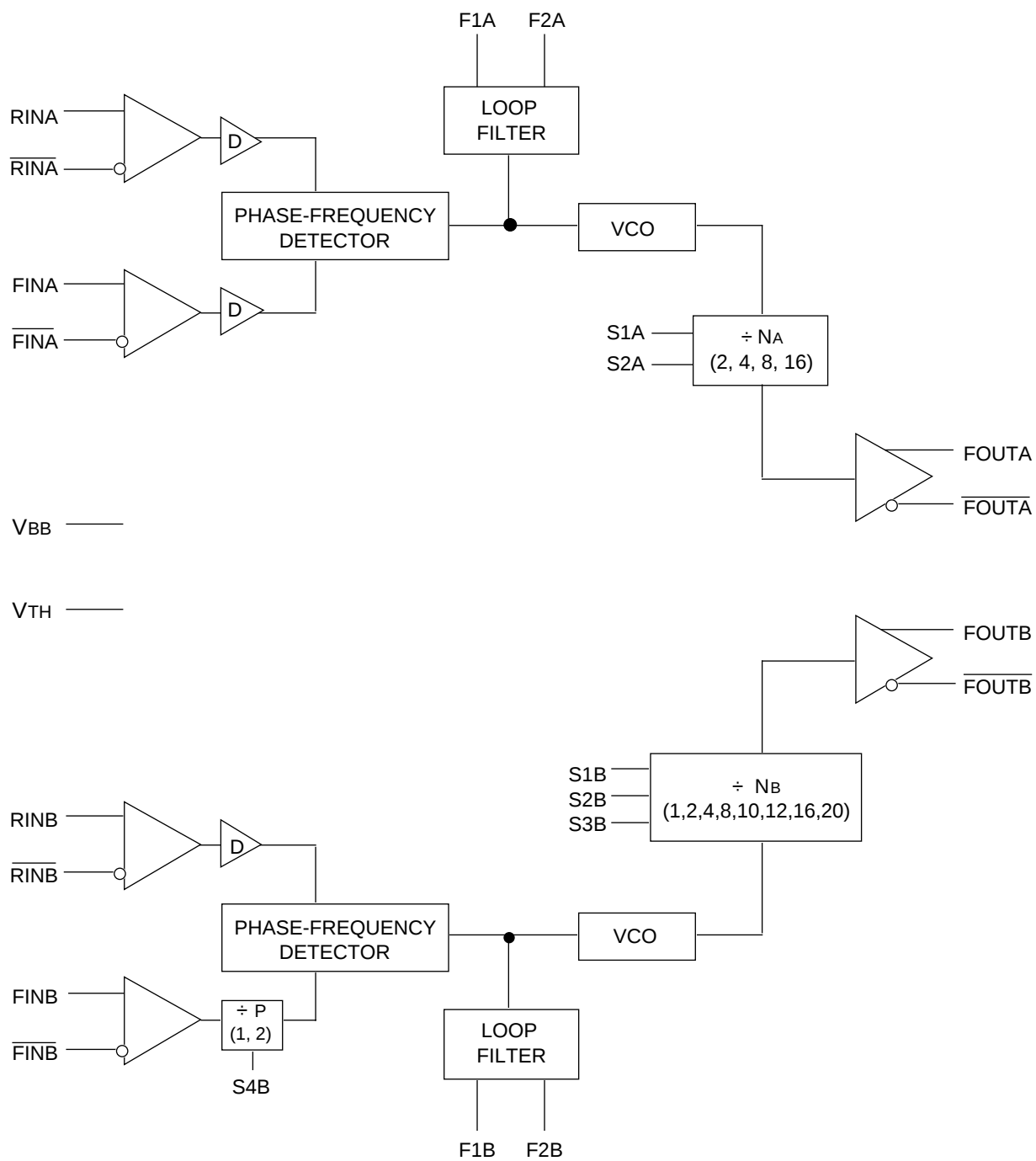
Two reference inputs (RINX and RINX), two feedback inputs (FINX and FINX), two filter pins (F1X and F2X) and two differential outputs (FOUTX and FOUTX) are provided for each of the two PLLs. The reference and feedback inputs can be used as either differential or single-ended inputs. In single-ended mode RINX and FINX can be connected to either VBB for normal 100K PECL levels or VTH for normal TTL levels.

Feedback for the loops is realized by connecting FOUTX, FOUTX to FINX, FINX by means of external circuitry. This allows the user the flexibility of inserting additional circuitry off-chip in the feedback paths, such as a divider. Pulldown resistors are required for the FOUTX and FOUTX pins.

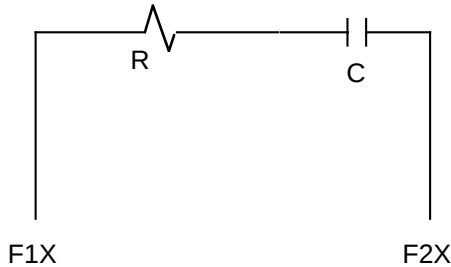
Use of a phase-frequency detector results in excellent PLL locking and tracking characteristics. Error correction voltages are generated by the detector if either phase or frequency deviations occur. The VCO has a frequency range covering more than a 2:1 ratio from 480MHz to 1120MHz.

Select pins S1X and S2X are used to program the N dividers for optimum VCO operation, in other words with the VCO in the center of its range. Additional select pins, S3B and S4B, are provided for PLLB. When both S3B and S4B are low, PLLB is identical to PLLA. When S3B is high, Nb can be set to 1, 10, 18, or 20. When S4B is high, the frequency doubler option is enabled (P = 2). All Select pins are TTL compatible.

## BLOCK DIAGRAM



## LOOP FILTER COMPONENT SELECTION



$$C = 1.0\mu\text{F} \pm 10\% \text{ (X7R dielectric)}$$

$$R = 560\Omega \pm 10\%$$

## PIN NAMES

| Pin                       | Function                    | I/O |
|---------------------------|-----------------------------|-----|
| F1A                       | Filter Pin 1A               | I/O |
| F2A                       | Filter Pin 2A               | I/O |
| RINA                      | Reference Input A           | I   |
| $\overline{\text{RINA}}$  | Inverted Reference Input A  | I   |
| FINA                      | Feedback Input A            | I   |
| $\overline{\text{FINA}}$  | Inverted Feedback Input A   | I   |
| FOUTA                     | Frequency Output A          | O   |
| $\overline{\text{FOUTA}}$ | Inverted Frequency Output A | O   |
| F1B                       | Filter Pin 1B               | I/O |
| F2B                       | Filter Pin 2B               | I/O |
| RINB                      | Reference Input B           | I   |
| $\overline{\text{RINB}}$  | Inverted Reference Input B  | I   |
| FINB                      | Feedback Input B            | I   |
| $\overline{\text{FINB}}$  | Inverted Feedback Input B   | I   |
| FOUTB                     | Frequency Output B          | O   |
| $\overline{\text{FOUTB}}$ | Inverted Frequency Output B | O   |
| VCC                       | VCC                         | —   |
| VCCOA                     | Output A VCC                | —   |
| VCCOB                     | Output B VCC                | —   |
| VEE                       | VEE (0V)                    | —   |
| VBB                       | PECL Threshold Voltage      | O   |
| VTH                       | TTL Threshold Voltage       | O   |
| S1A                       | Select Input 1A (TTL)       | I   |
| S2A                       | Select Input 2A (TTL)       | I   |
| S1B                       | Select Input 1B (TTL)       | I   |
| S2B                       | Select Input 2B (TTL)       | I   |
| S3B                       | Select Input 3B (TTL)       | I   |
| S4B                       | Select Input 4B (TTL)       | I   |

## PIN DESCRIPTION

**RINA,  $\overline{\text{RINA}}$ , RINB,  $\overline{\text{RINB}}$** 

Reference frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

**FINA,  $\overline{\text{FINA}}$ , FINB,  $\overline{\text{FINB}}$** 

Feedback frequency inputs for loop A and B. These are differential signal pairs and may be driven differentially or single-ended.

**VBB, VTH**

These are the reference voltages for use as bias for the frequency inputs. The references are generated on-chip. VBB is PECL compatible, while VTH is TTL compatible.

**F1A, F2A, F1B, F2B**

These pins are connection points for the loop filters, which are to be provided off-chip. F1X is the high impedance side, F2X is the reference side. The loop filter should be a first order, low pass with a DC block. The difference voltage on these pins will be a DC level, which is controlled by the loop feedback and determined by the required VCO frequency.

**FOUTA,  $\overline{\text{FOUTA}}$ , FOUTB,  $\overline{\text{FOUTB}}$** 

Frequency outputs for the loops. These are differential, positive referenced, emitter-follower signals and must be terminated off-chip. Termination in 50 ohms is recommended.

**S1A, S2A, S1B, S2B, S3B, S4B**

These inputs are used to select the configuration for PLLA and PLLB. They are compatible with standard TTL signal levels. See the Frequency Selection Table for details of the logic.

**VCC**

This is the positive supply for the entire chip excluding output buffers. It should be decoupled and present a very low impedance in order to assure low-jitter operation.

**VCCOA, VCCOB**

These are the positive supplies for the output buffers. They are constrained to be equal to the value of VCC. They should be decoupled and present a very low impedance in order to assure low-jitter operation.

**VEE**

This pin is the negative supply for the chip and is normally connected to ground (0V).

**FREQUENCY SELECTION TABLE****PLLA**

| S2A | S1A | Divide-by-N | Output Frequency Range (MHz) |
|-----|-----|-------------|------------------------------|
| 0   | 0   | N = 2       | 240 – 560                    |
| 0   | 1   | N = 4       | 120 – 280                    |
| 1   | 0   | N = 8       | 60 – 140                     |
| 1   | 1   | N = 16      | 30 – 70                      |

**PLLB**

| S3B | S2B | S1B | Divide-by-N | Output Frequency Range (MHz) |
|-----|-----|-----|-------------|------------------------------|
| 0   | 0   | 0   | N = 2       | 240 – 560                    |
| 0   | 0   | 1   | N = 4       | 120 – 280                    |
| 0   | 1   | 0   | N = 8       | 60 – 140                     |
| 0   | 1   | 1   | N = 16      | 30 – 70                      |
| 1   | 0   | 0   | N = 1       | 480 – 1120                   |
| 1   | 0   | 1   | N = 10      | 48 – 112                     |
| 1   | 1   | 0   | N = 12      | 40 – 93.3                    |
| 1   | 1   | 1   | N = 20      | 24 – 56                      |

| S4B | Divide-by-P | Max. Feedback Frequency (MHz) |
|-----|-------------|-------------------------------|
| 0   | P = 1       | 560                           |
| 1   | P = 2       | 1120                          |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol             | Parameter                                     | Value        | Unit |
|--------------------|-----------------------------------------------|--------------|------|
| V <sub>CC</sub>    | Power Supply Voltage                          | –0.5 to +7.0 | V    |
| V <sub>I</sub>     | TTL Input Voltage <sup>(2)</sup>              | –0.5 to 6.0  | V    |
| I <sub>I</sub>     | TTL Input Current <sup>(2)</sup>              | –30 to +5.0  | mA   |
| I <sub>OUT</sub>   | ECL Output Current<br>— Continuous<br>— Surge | 50<br>100    | mA   |
| T <sub>store</sub> | Storage Temperature                           | –65 to +150  | °C   |
| T <sub>A</sub>     | Operating Temperature Range <sup>(3)</sup>    | 0 to +85     | °C   |

**NOTES:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect input.
3. All DC and AC electrical characteristics are specified over the operating temperature range.

**5V DC ELECTRICAL CHARACTERISTICS**

VCC = VCCOA = VCCOB = 5.0V ±5%

| Symbol | Parameter                   | Min. | Typ. | Max. | Unit | Condition             |
|--------|-----------------------------|------|------|------|------|-----------------------|
| VCC    | Power Supply Voltage        | 4.75 | —    | 5.25 | V    | VCC = VCCO            |
| ICC    | Power Supply Current (VCC)  | —    | —    | 200  | mA   |                       |
| ICCO   | Power Supply Current (VCCO) | —    | —    | 28   | mA   | PECL outputs are open |

**3.3V DC ELECTRICAL CHARACTERISTICS**

VCC = VCCOA = VCCOB = 3.3V ±5%

| Symbol | Parameter                   | Min.  | Typ. | Max.  | Unit | Condition             |
|--------|-----------------------------|-------|------|-------|------|-----------------------|
| VCC    | Power Supply Voltage        | 3.135 | —    | 3.465 | V    | VCC = VCCO            |
| ICC    | Power Supply Current (VCC)  | —     | —    | 200   | mA   |                       |
| ICCO   | Power Supply Current (VCCO) | —     | —    | 28    | mA   | PECL outputs are open |

**PECL DC ELECTRICAL CHARACTERISTICS**

VCC = VCCOA = VCCOB = 3.3V or 5.0V ±5%

| Symbol | Parameter           | Min.        | Typ.       | Max.        | Unit | Condition |
|--------|---------------------|-------------|------------|-------------|------|-----------|
| VOH    | Output HIGH Voltage | VCC – 1.025 | —          | VCC – 0.780 | V    |           |
| VOL    | Output LOW Voltage  | VCC – 1.810 | —          | VCC – 1.520 | V    |           |
| VIH    | Input HIGH Voltage  | VCC – 1.165 | —          | VCC – 0.780 | V    |           |
| VIL    | Input LOW Voltage   | VCC – 1.810 | —          | VCC – 1.475 | V    |           |
| VBB    | PECL Threshold      | —           | VCC – 1.35 | —           | V    |           |

**TTL DC ELECTRICAL CHARACTERISTICS**

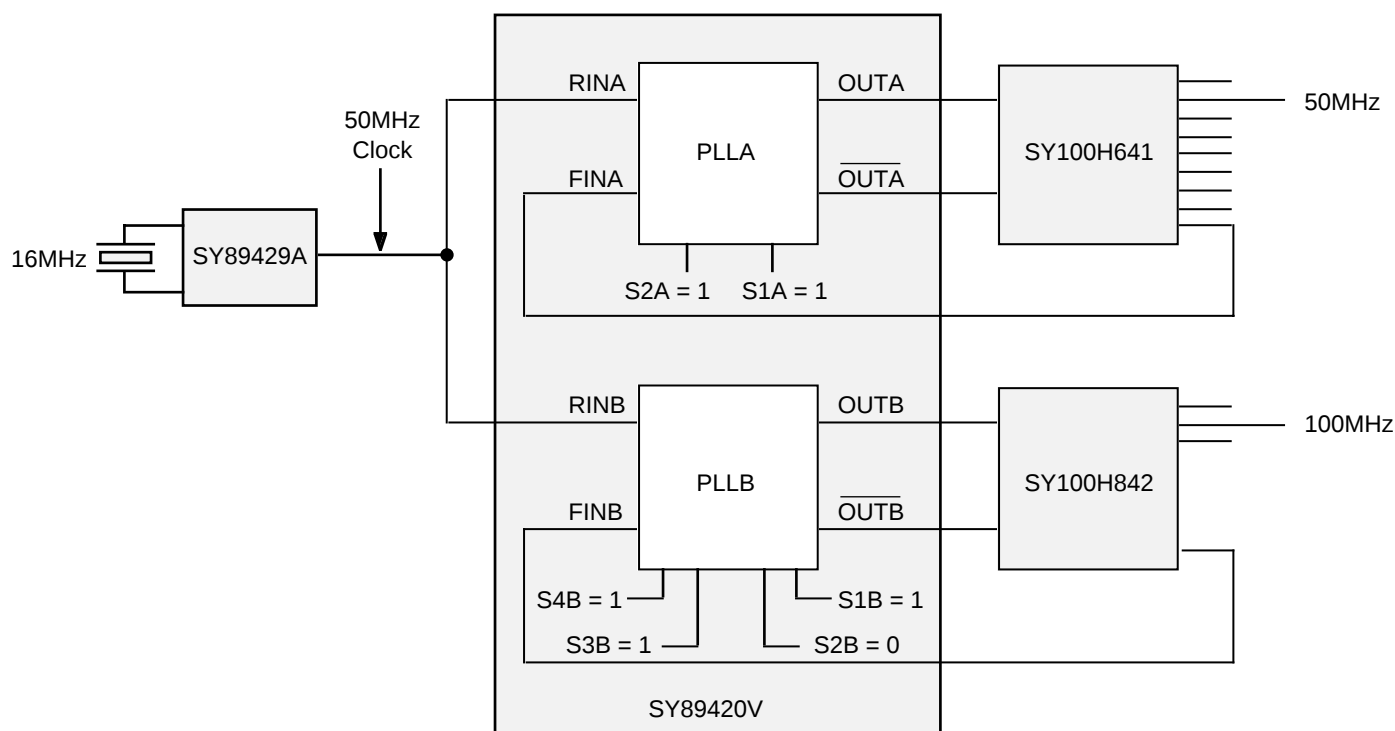
VCC = VCCOA = VCCOB = 3.3V or 5.0V ±5%

| Symbol | Parameter           | Min. | Typ. | Max.      | Unit | Condition               |
|--------|---------------------|------|------|-----------|------|-------------------------|
| VIH    | Input HIGH Voltage  | 2.0  | —    | —         | V    |                         |
| VIL    | Input LOW Voltage   | —    | —    | 0.8       | V    |                         |
| IIH    | Input HIGH Current  | —    | —    | 20<br>100 | μA   | VIN = 2.7V<br>VIN = VCC |
| IIL    | Input LOW Current   | —    | —    | –0.3      | mA   | VIN = 0.5V              |
| VIK    | Input Clamp Voltage | —    | —    | –1.2      | V    | IIN = –12mA             |
| VTH    | TTL Threshold       | —    | 1.5  | —         | V    |                         |

**AC ELECTRICAL CHARACTERISTICS**

VCC = VCCOA = VCCOB = 3.3V or 5.0V ± 5%

| Symbol     | Parameter                             | Min.   | Typ.       | Max.       | Unit   | Condition |
|------------|---------------------------------------|--------|------------|------------|--------|-----------|
| $\Delta T$ | Output Period Jitter                  | —      | 10         | 15         | ps rms |           |
| PPW        | Output Duty Cycle                     | 45     | 50         | 55         | %      |           |
| tr<br>tf   | Output Rise/Fall Time<br>(20% to 80%) | —<br>— | 300<br>300 | 550<br>550 | ps     | —         |
| FOUTA      | Output Frequency PLLA                 | —      | —          | 560        | MHz    |           |
| FOUTB      | Output Frequency PLLB                 | —      | —          | 1120       | MHz    | S4B=1     |
| RINA, B    | Input Frequency PLLA, B               | —      | —          | 560        | MHz    |           |

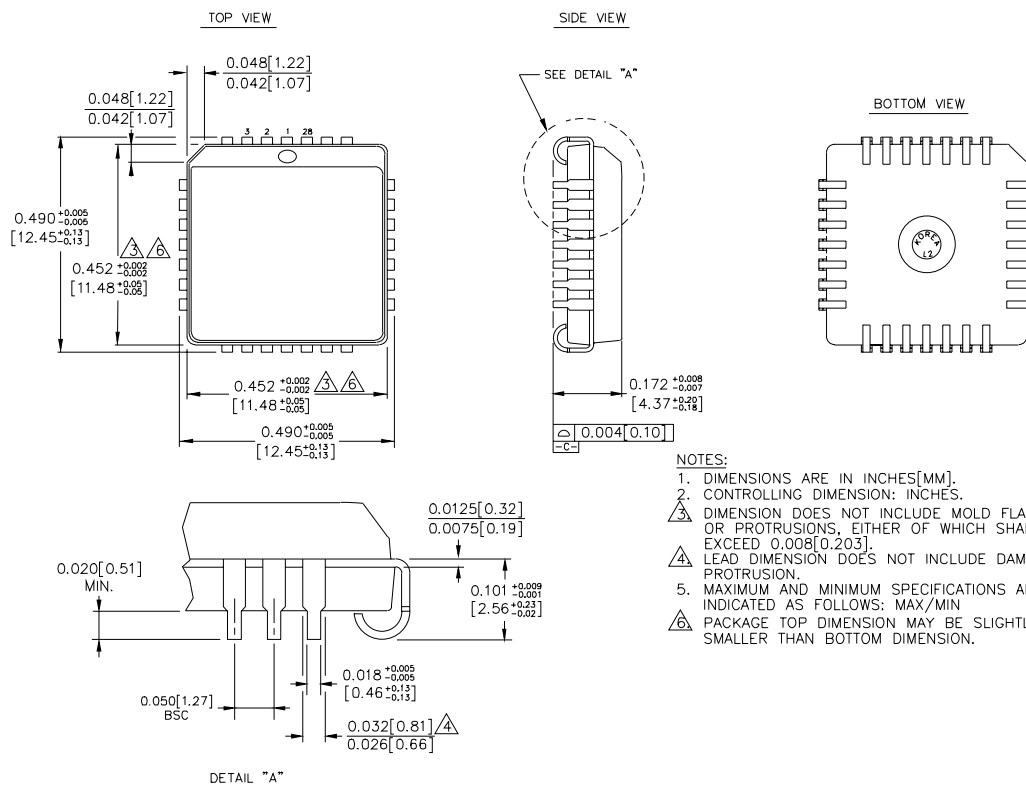
**APPLICATION**

50MHz Low Skew Clock System with 100MHz Clock to CPU

**PRODUCT ORDERING CODE**

| Ordering Code | Package Type | Operating Range |
|---------------|--------------|-----------------|
| SY89420VJC    | J28-1        | Commercial      |
| SY89420VJCTR  | J28-1        | Commercial      |

## 28 LEAD PLCC (J28-1)



## NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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