OptiMOS™-T2 Power-Transistor

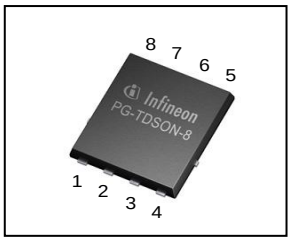
Product Summary

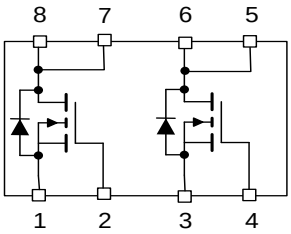
V_{DS}	40	V
$R_{DS(on),max}$ [4]	7.2	mΩ
I_D	20	A

Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

PG-TDSON-8





Type	Package	Marking
IPG20N04S4L-07A	PG-TDSON-8	4N04L07

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	T_C=25 °C, V_{GS}=10 V [1]	20	A
		T_C=100 °C, V_{GS}=10 V [2]	20	
Pulsed drain current [2] one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse [2, 4]	E_{AS}	I_D=10A	230	mJ
Avalanche current, single pulse [4]	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	T_C=25 °C	65	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Downloaded from Arrow.com.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.3	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm^2 cooling area[3]	-	60	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= 30µA	1.2	1.7	2.2	
Zero gate voltage drain current[4]	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=18 V, V_{GS}=0 V, T_j=85 °C[2]	-	1	100	
Gate-source leakage current[4]	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance[4]	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=10 A	-	8.0	9.2	mΩ
		V_{GS}=10 V, I_D=17 A	-	6.5	7.2	

Downloaded from Arrow.com.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance[4]	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	3060	3980	pF
Output capacitance[4]	C_{oss}		-	560	730	
Reverse transfer capacitance[4]	C_{rss}		-	25	58	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=11 Ω	-	9	-	ns
Rise time	t_r		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	50	-	
Fall time	t_f		-	25	-	
Gate Charge Characteristics[2, 4]						
Gate to source charge	Q_{gs}	V_{DD}=32 V, I_D=20 A, V_{GS}=0 to 10 V	-	8.2	11	nC
Gate to drain charge	Q_{gd}		-	4	9	
Gate charge total	Q_g		-	39	50	
Gate plateau voltage	$V_{plateau}$		-	2.7	-	V
Reverse Diode						
Diode continous forward current[2] one channel active	I_S	T_C=25 °C	-	-	20	A
Diode pulse current[2] one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=17 A, T_j=25 °C	-	0.9	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=20 V, I_F=I_S, di_F/dt=100 A/µs	-	36	-	ns
Reverse recovery charge[2, 4]	Q_{rr}		-	34	-	nC

[1] Current is limited by bondwire; with an R_{thJC}=2.3 K/W the chip is able to carry 73A at 25°C.

[2] Specified by design. Not subject to production test.

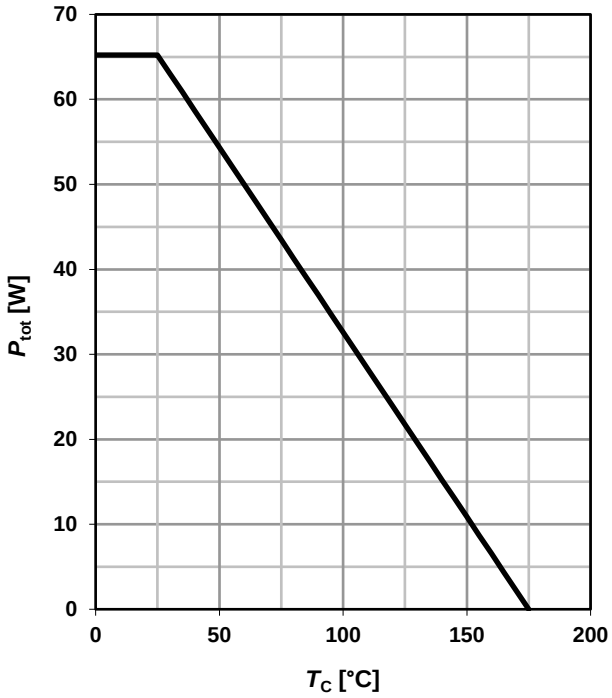
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4] Per channel

Downloaded from Arrow.com.

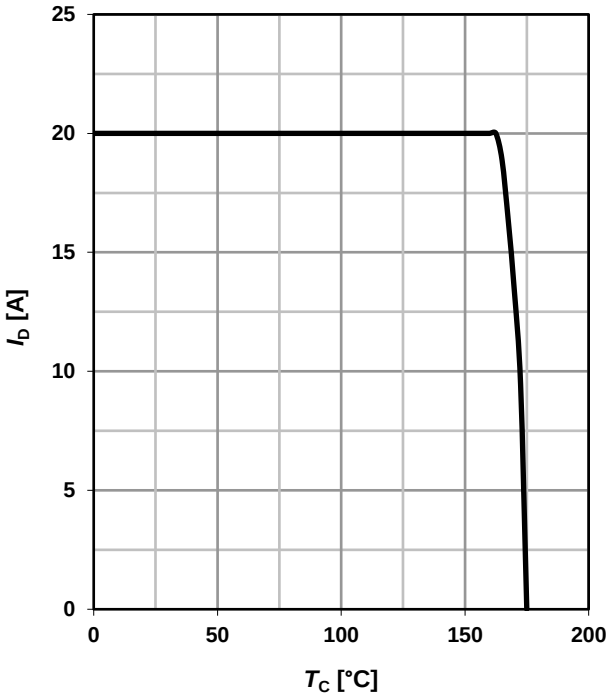
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



2 Drain current

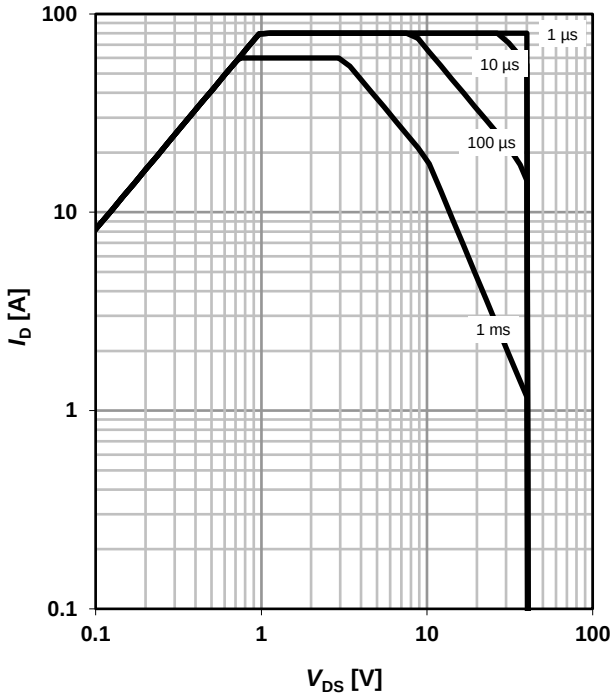
$I_D = f(T_C)$; $V_{GS} \geq 6$ V; one channel active



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$°C; $D = 0$; one channel active

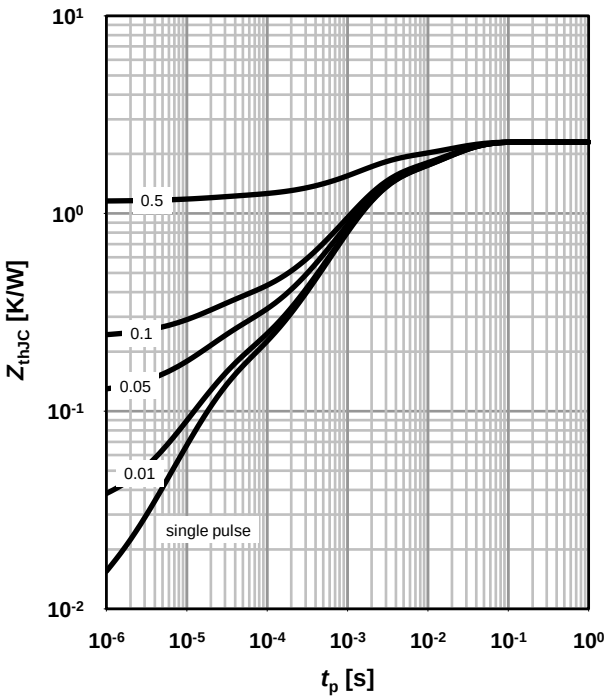
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

parameter: $D = t_p/T$

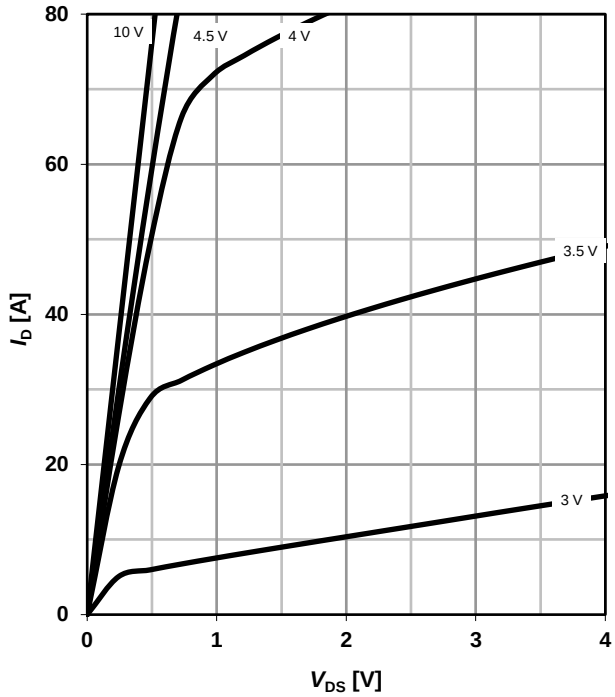


Downloaded from Arrow.com.

5 Typ. output characteristics[4)]

$I_D = f(V_{DS})$; $T_j = 25$ °C

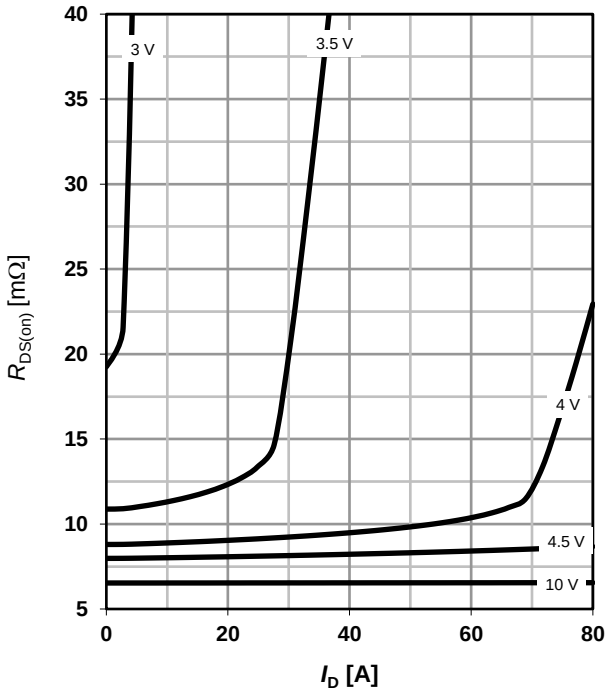
parameter: V_{GS}



6 Typ. drain-source on-state resistance[4)]

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

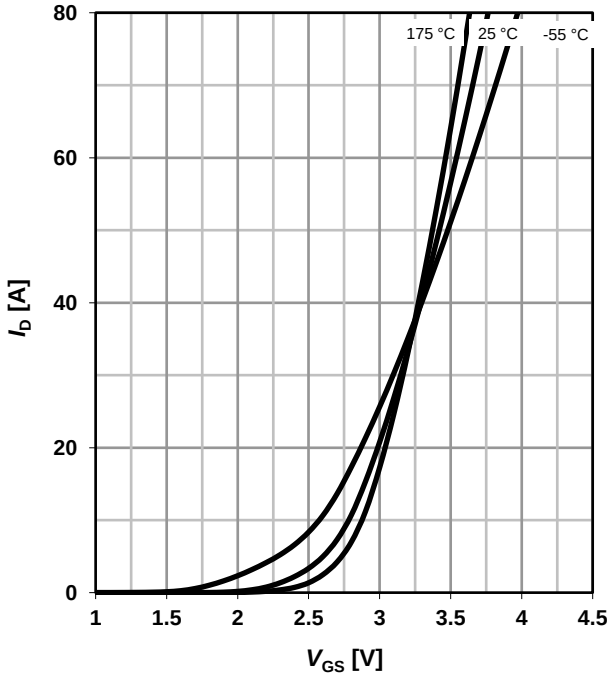
parameter: V_{GS}



7 Typ. transfer characteristics[4)]

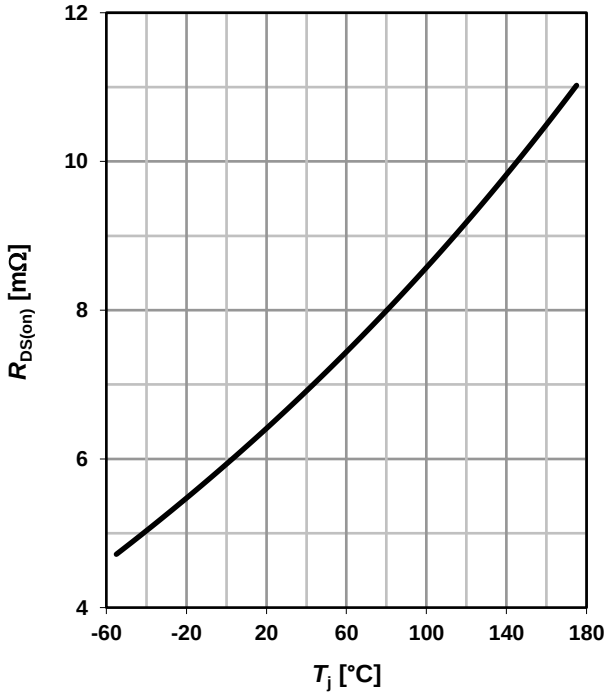
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance[4)]

$R_{DS(on)} = f(T_j)$; $I_D = 17$ A; $V_{GS} = 10$ V

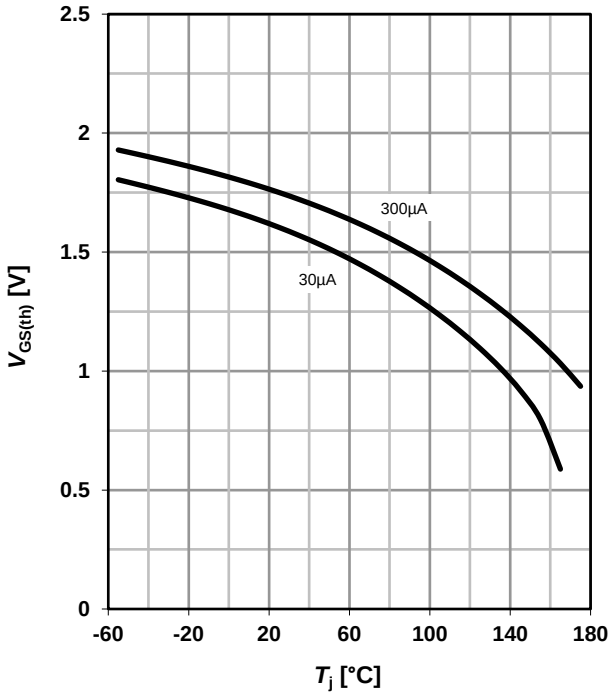


Downloaded from Arrow.com.

9 Typ. gate threshold voltage

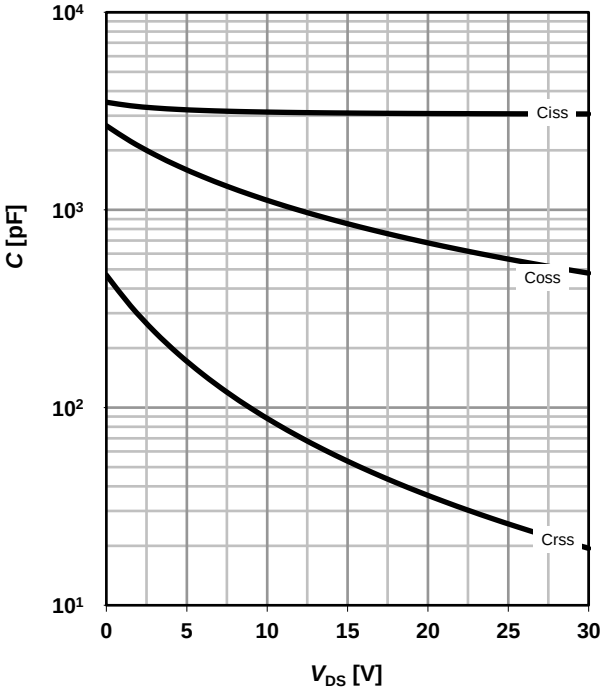
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances[4)]

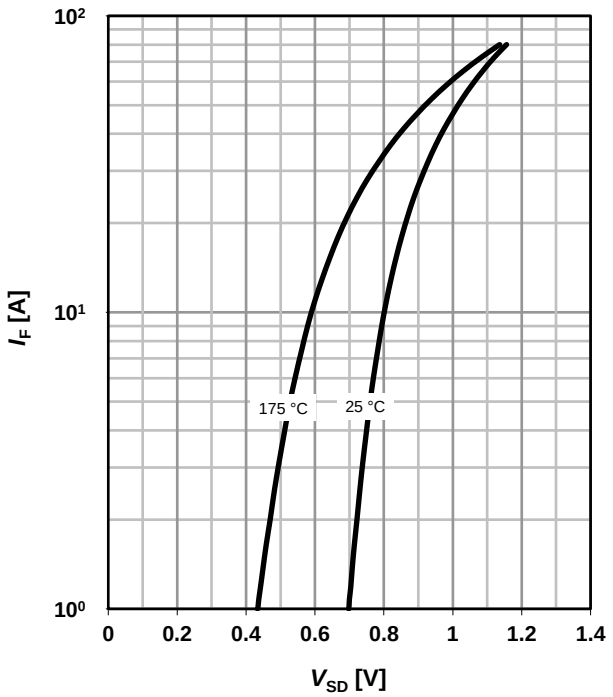
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristics[4)]

IF = f(V_{SD})

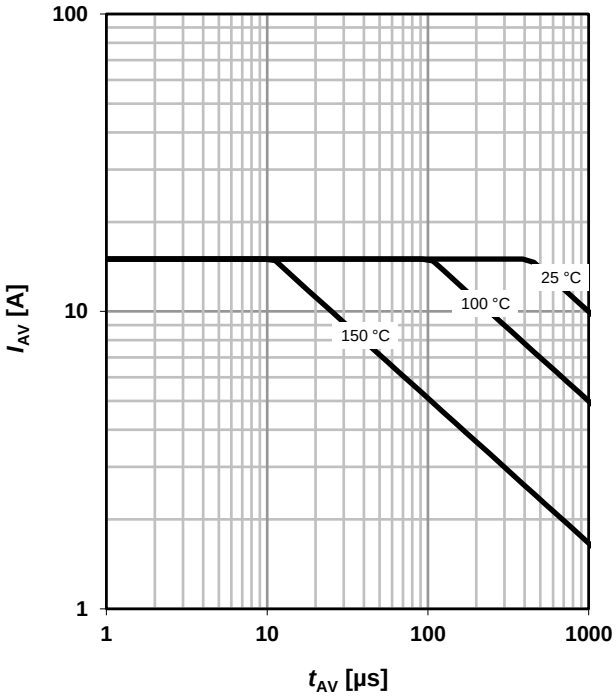
parameter: T_j



12 Avalanche characteristics[4)]

$I_{AS} = f(t_{AV})$

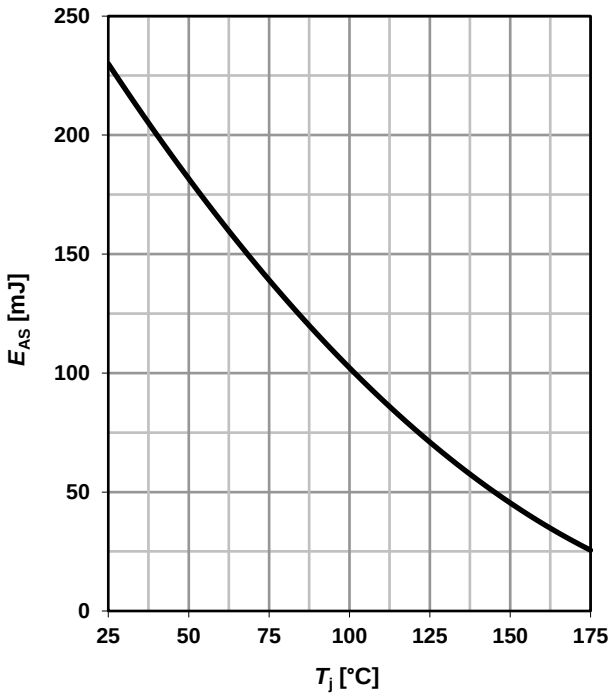
parameter: $T_{j(start)}$



Downloaded from Arrow.com.

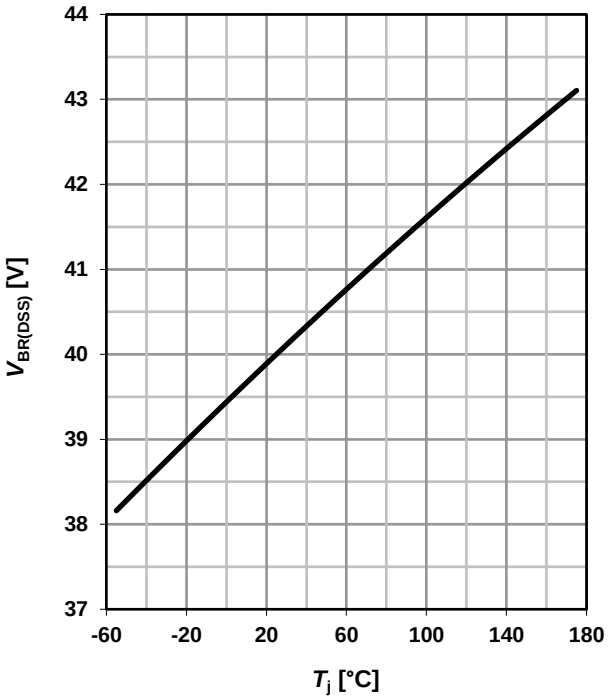
13 Avalanche energy[4)]

$E_{AS} = f(T_j)$, $I_D = 10A$



14 Drain-source breakdown voltage

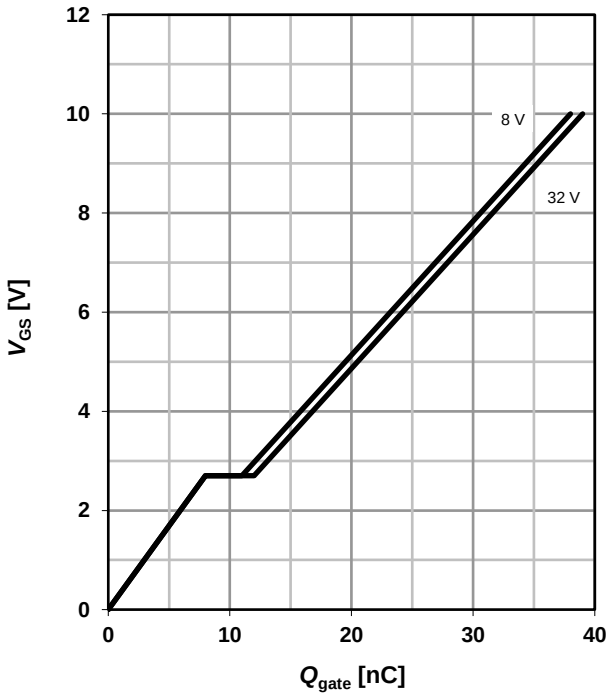
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



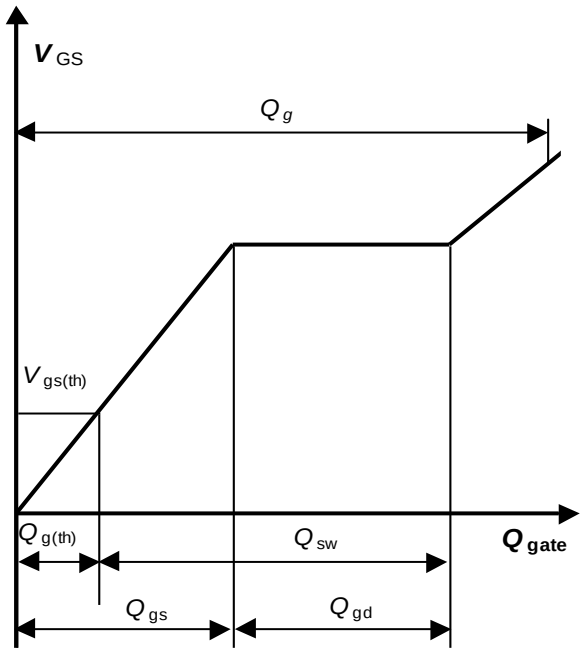
15 Typ. gate charge[4)]

$V_{GS} = f(Q_{gate})$; $I_D = 20$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



Downloaded from Arrow.com.

Published by
Infineon Technologies AG
81726 Munich, Germany

© Infineon Technologies AG 2024
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances.
For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Downloaded from Arrow.com.

Revision History

Version	Date	Changes
Revision 1.0	14.11.2012	Data Sheet revision 1.0
Revision 1.01	02.08.2024	Package naming updated

Downloaded from Arrow.com.