MPQ4253B

36V Buck Converter Supports One Type-A, One Type-C Dual USB Charging Ports and Passes Apple MFI, AEC-Q100 Qualified

DESCRIPTION

The MPQ4253B integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and charging port identification circuitry for each port. The MPQ4253B can achieve up to 6A of output current (I_{OUT}), with excellent load and line regulation across a wide input voltage (V_{IN}) range.

The USB outputs are fixed as one Type-A USB port and one Type-C USB port. Each USB switch is current-limited. The USB1 port supports USB Type-C 5V @ 3A DFP mode. The USB2 port supports DCP schemes for battery charging specification (BC1.2), Apple divider 3 mode, and 1.2V/1.2V mode, which eliminates the need for outside user interaction.

The MPQ4253B buck and USB2 output is always on if EN is high. If USB2 detects that a device is plugged in, then the USB1 port capability changes to 1.5A automatically.

The step-down converter uses peak current (I_{PEAK}) mode control to regulate I_{OUT}. Under light-load conditions, the part enters pulse-frequency modulation (PFM) mode to improve efficiency.

Full protection features include over-current protection (OCP) with hiccup mode, output over-voltage protection (OVP), and thermal shutdown. The device supports load-shedding mode for the USB1 port. When entering load-shedding, the Type-C advertised current capability changes to 1.5A.

The MPQ4253B requires a minimal number of readily available, standard external components, and is available in a QFN-26 (5mmx5mm) package.

FEATURES

- All-In-One Type-C + Type-A Solution
- Passes Apple MFI Certification Test
- Type-C Auto-Entry, 1.5A Load Capability when the Type-A Port Detects a Device Is Plugged In
- Default Frequency Spread Spectrum (FSS) at 480kHz (FREQ is Floating)
- Auto-PFM/PWM Mode
- Wide 6V to 36V Operating Input Voltage (V_{IN}) Range
- Selectable Output Voltage (V_{OUT}): 5.1V, 5.17V, or 5.3V
- 90mV Line-Drop Compensation
- Accurate USB1/USB2 Output Current Limit (I_{OUT_LIMIT})
- 18mΩ/15mΩ Internal, Low $R_{DS(ON)}$ Buck Power MOSFETs
- 18mΩ/18mΩ Internal, Low $R_{DS(ON)}$ USB1/USB2 Power MOSFETs
- 250kHz to 1MHz Adjustable Switching Frequency (f_{SW})
- Buck and USB Over-Current Protection (OCP) with Hiccup Mode
- Supports DCP Schemes for BC1.2, Apple Divider 3 Mode, and 1.2V/1.2V Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

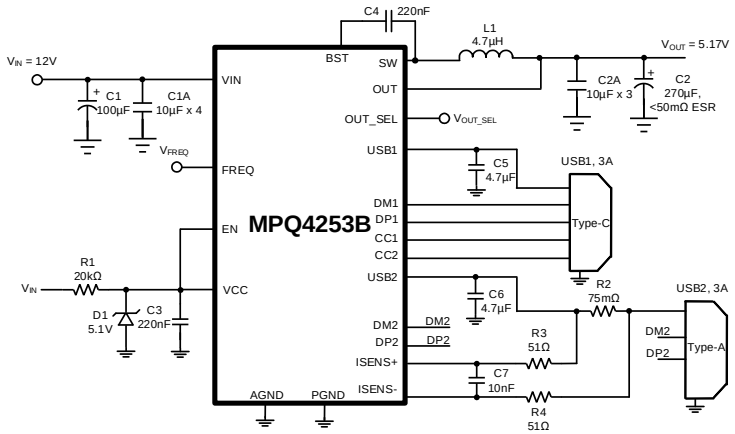
- USB Dedicated Charging Ports (DCPs)
- USB Type-C + Type-A Hybrid Charging Ports

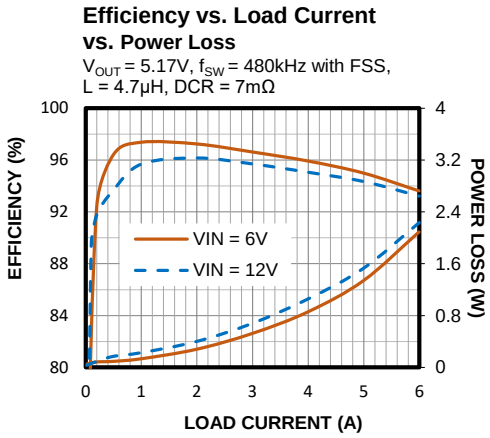
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

TYPICAL APPLICATION (1)





Note:

1) Add R1 and D1 to power VCC before the buck output (V_{OUT_BUCK}) ramps up.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4253BGU-AEC1	QFN-26 (5mmx5mm)	*See Below*	1

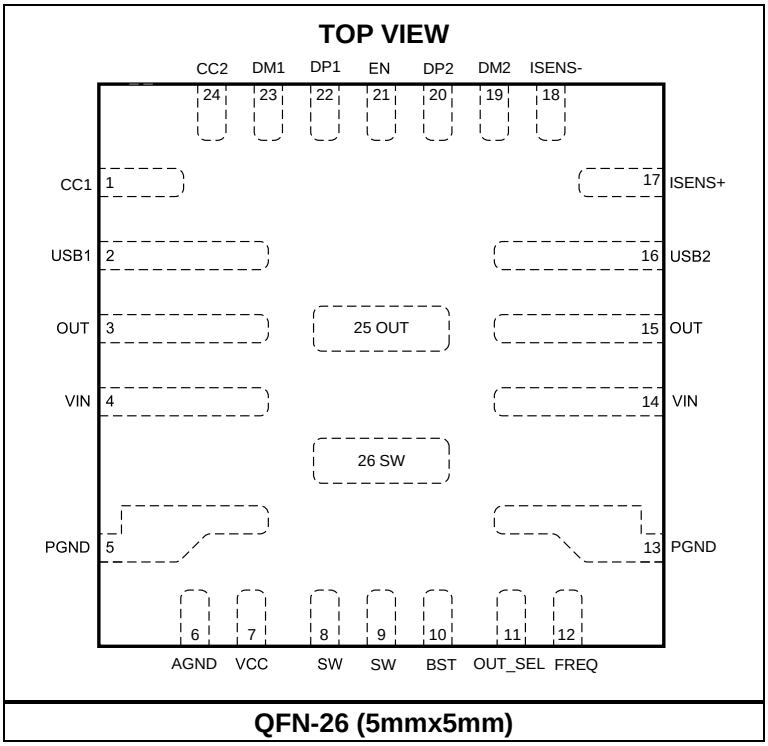
* For Tape & Reel, add suffix -Z (e.g. MPQ4253BGU-AEC1-Z).

TOP MARKING

MPSYYWW
MP4253B
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4253B: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



QFN-26 (5mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel 1.** The CC1 pin detects connections and configures the interface across the USB1 Type-C cables and connectors. Once a connection is established, CCx is reassigned to provide power across the plug's VCONN pin.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** The OUT pin is the input for the USB1 and USB2 pins.
4, 14	VIN	**Input voltage.** The VIN pin is the drain of the internal powered device, and provides the power supply for the entire chip. The MPQ4253B operates from a 6V to 36V input voltage (V_{IN}). A capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** The PGND pin is the reference ground of the regulated output voltage (V_{OUT}). PGND requires careful consideration during PCB layout. Use copper traces and vias to make the PGND connection.
6	AGND	**Analog ground.** Connect the AGND and PGND pins.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple the VCC pin using a 220nF decoupling capacitor. VCC requires an external power supply for initial start-up.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the SW connection.
10	BST	**Bootstrap.** Connect a 0.22µF capacitor between the SW and BST pins to form a floating supply across the high-side MSOFET (HS-FET) driver.
11	OUT_SEL	**Buck output voltage setting.** Pull the OUT_SEL pin low to set V_{OUT} 5.1V. Float OUT_SEL to set V_{OUT} to 5.17V. Pull OUT_SEL high to set V_{OUT} to 5.33V.
12	FREQ	**Switching frequency configuration input.** Connect a resistor between the FREQ pin and ground to set the switching frequency (f_{SW}). Float FREQ to set f_{SW} to 480kHz with frequency spread spectrum (FSS). Connect FREQ to ground to set f_{SW} to 250kHz internally.
16	USB2	**USB2 output.**
17	ISENS+	**Current-sense input positive terminal.** The ISENS+ and ISENS- pins are used to detect the USB2 output current (I_{OUT_USB2}) via an external resistor. Once I_{OUT_USB2} exceeds a certain level, the USB1 port's CCx pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source capability has changed to 1.5A.
18	ISENS-	**Current-sense input negative terminal.** The ISENS+ and ISENS- pins are used to detect the USB2 output current (I_{OUT_USB2}) via an external resistor. Once I_{OUT_USB2} exceeds a certain level, the USB1 port's CCx pin R_P changes to 22kΩ to indicate that its source capability has changed to 1.5A.
19	DM2	**D- data line to USB2 connector.** The DM2 pin is an input/output that is used to handshake with portable devices.
20	DP2	**D+ data line to USB2 connector.** The DP2 pin is an input/output that is used to handshake with portable devices.
21	EN	**On/off control input enable pin.** Pull EN high to turn the IC on; pull EN low to turn it off. Do not float EN.
22	DP1	**D+ data line to USB1 connector.** The DP1 pin is an input/output that is used to handshake with portable devices.
23	DM1	**D- data line to USB1 connector.** The DM1 pin is an input/output that is used to handshake with portable devices.
24	CC2	**Configuration channel 2.** The CC2 pin detects connections and configures the interface across the USB1 Type-C cables and connectors. Once a connection is established, CCx is reassigned to provide power across the plug's VCONN pin.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ABSOLUTE MAXIMUM RATINGS (2)

Input voltage (V_{IN}) .....-0.4V to +40V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} .....-0.3V to +10V (3)
V_{OUT}, V_{USBx} .....-0.3V to +6.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (4) (5)
QFN-26 (5mmx5mm) 4.8W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) (6):
CCx (7) .....±6KV
DPx, DMx, and USBx (7).....±8KV
All other pins .....±1.8KV
Charged device model (CDM) (8):
All pins .....±1KV

Recommended Operating Conditions (9)

Operating V_{IN} .....6V to 36V
USBx output current (I_{OUT_USBx}) 3A
Operating T_J..... -40°C to +125°C (5)

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (5mmx5mm)		
EVQ4253B-U-00A (10)	26	4 °C/W
JESD51-7 (11)	44	9 °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) See the Enable (EN) Control section on page 14 for more details.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Operating devices at >125°C junction temperatures is possible. Contact MPS for details.
6) Per JEDEC specification JESD22-A114. JEDEC document JEP155 states that a 500V human body model (HBM) allows for safe manufacturing with a standard ESD control process.
7) HBM with regard to ground (AGND and PGND are connected).
8) Per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP157 states that a 250V charged device model (CDM) allows for safe manufacturing with a standard ESD control process.
9) The device is not guaranteed to function outside of its operating conditions.
10) Measured on EVQ4253B-U-00A (50mmx50mm), 4-layer PCB.
11) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 is connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	I_{SD}	V_{EN} = 0V, V_{CC} = 0V			10	μA
Quiescent current	I_{Q1}	R_{CC1} = 5.1kΩ, V_{OUT_BUCK} = 5.4V, V_{EN} is high		540	1000	μA
	I_{Q2}	CC is floating, V_{OUT_BUCK} = 5.4V, EN is high		340	700	μA
EN rising threshold	V_{EN_RISING}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
Thermal shutdown (12)	T_{SD}			165		°C
Thermal hysteresis (12)	T_{SD_HYS}			20		°C
VCC enable threshold	V_{CC_EN}			2.3	3	V
VCC internal regulator voltage	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	$V_{CC_LOAD_REG}$	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		4.6	5	5.4	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			700		mV
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$			18	40	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$			15	30	mΩ
Output voltage	V_{OUT}	OUT_SEL is low	-2%	5.1	+2%	V
		OUT_SEL is floating, T_J = 25°C	-1%	5.17	+1%	V
		OUT_SEL is floating, T_J = -40°C to +125°C	-2%	5.17	+2%	V
		OUT_SEL is high	-2%	5.3	+2%	V
Output over-voltage protection (OVP) rising threshold	V_{OVP_RISING}		5.45	5.9	6.25	V
Output OVP falling threshold	$V_{OVP_FALLING}$		5.3	5.7	6.1	V
LS-FET current limit	I_{LIMIT_LS}			-2		A
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	μA
HS-FET current limit	I_{LIMIT_HS}	V_{OUT} = 0V	8	12	16	A
Switching frequency	f_{SW1}	R_{FREQ} is pulled to AGND	185	250	315	kHz
	f_{SW2}	R_{FREQ} = 66.5kΩ	250	350	450	kHz
Frequency spread spectrum (FSS) span	f_{SS}	R_{FREQ} is floating, f_{SW} = 480kHz		±10		%
Maximum duty cycle	D_{MAX}	f_{SW} = 480kHz	91	95	99	%
Minimum off time	t_{OFF_MIN}			110		ns
Minimum on time (12)	t_{ON_MIN}			130		ns
Soft-start time	t_{SS}	V_{OUT} is between 10% and 90%	0.5	1	1.7	ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 is connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Switch (USB1 and USB2)						
UVLO rising threshold	$V_{USB_UVLO_RISING}$		3.7	4	4.3	V
UVLO hysteresis	$V_{USB_UVLO_HYS}$			200		mV
MOSFET on resistance	$R_{DS(ON)_SW}$			18	35	mΩ
USB over-voltage (OV) clamp	V_{USB_OV}		5.5	5.8	6	V
Current limit	I_{LIMIT_USB1}	V_{OUT} drops to 10%, T_J = 25°C, Type-C mode (USB1)		5		A
	I_{LIMIT_USB2}	V_{OUT} drops 10%, T_J = 25°C Type-A mode (USB2)		4		A
Line drop compensation	V_{DROP_COMP}	I_{OUT} = 2.4A, V_{OUT} = 5.17V	40	90	140	mV
Bus voltage (V_{BUS1}) soft-start time	t_{SS1}	V_{OUT} is between 10% to 90%	1	2	3	ms
V_{BUS2} soft-start time	t_{SS2}	V_{OUT} is between 10% to 90%	0.5	1	1.5	ms
Hiccup mode on time	t_{HICCUP_ON}	OCP, V_{OUT} drops to 10%, T_J = 25°C	3.5	5	6.5	ms
		OCP, V_{OUT} drops to 10%, T_J = -40°C to +125°C	3	5	7	ms
Hiccup mode off time	t_{HICCUP_OFF}	V_{OUT} is connected to PGND	1	2	3	s
USB2 (Type-A Mode)						
ISENS± rising threshold	$V_{ISENS\pm_RISING}$		3.75	7.5	11.25	mV
ISENS± falling threshold	$V_{ISENS\pm_FALLING}$		1			mV
ISENS± falling voltage debounce timer	$t_{ISENS\pm_DEBOUNCE}$		2.4	3	3.6	s
BC1.2 DCP Mode						
DPx and DMx short resistance		V_{DPx} = 0.8V, I_{DMx} = 1mA, T_J = 25°C		85	155	Ω
		V_{DPx} = 0.8V, I_{DMx} = 1mA, T_J = -40°C to +125°C		85	160	Ω
Divider Mode						
DPx output voltage	$V_{DPx_DIVIDER}$		2.55	2.7	2.85	V
DMx output voltage	$V_{DMx_DIVIDER}$		2.55	2.7	2.85	V
DPx and DMx output impedance		T_J = 25°C	14	22	30	kΩ
		T_J = -40°C to +125°C	14	22	34	kΩ
1.2V/1.2V Mode						
DPx and DMx output voltage		V_{OUT} = 5V, T_J = 25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	V
DPx and DMx output impedance		T_J = 25°C	70	105	140	kΩ
		T_J = -40°C to +125°C	60	105	150	kΩ

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 is connected to ground via a 5.1kΩ resistor, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V @ 3A Mode (CC1 and CC2)						
CCx voltage to enable VCONN	V_{CCx_VCONN}				0.75	V
CCx voltage to enable V_{BUS}	V_{CCx_VBUS}		0.9		2.45	V
CCx detach threshold	V_{CCx_DETACH}		2.75			V
CCx falling voltage debounce time	$t_{CCx_FALLING_DEBOUNCE}$	V_{BUS} enable deglitch	100	144	200	ms
CCx rising voltage debounce time	$t_{CCx_RISING_DEBOUNCE}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	V_{CONN} comes from the buck output with some series resistance	100			mW

Note:

12) Guaranteed by engineering sample characterization.

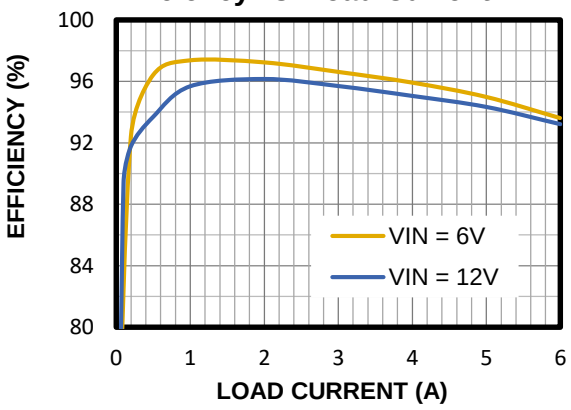
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

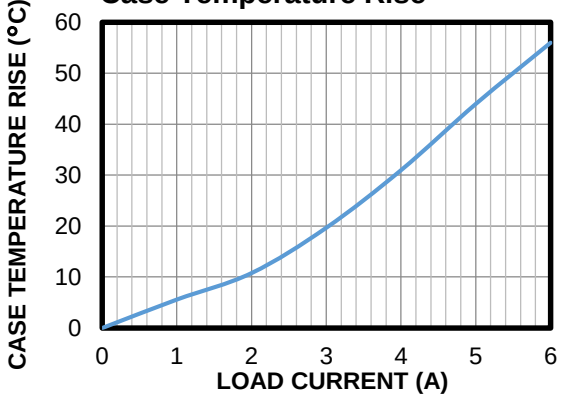
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 480kHz with FSS, L = 4.7µH, T_A = 25°C, CC1 is connected to ground via a 5.1kΩ resistor, unless otherwise noted.

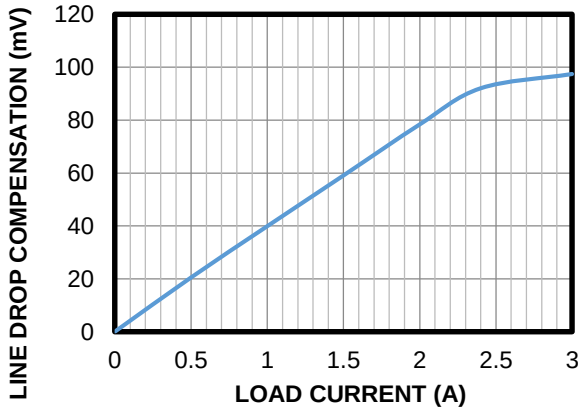
Efficiency vs. Load Current



Case Temperature Rise

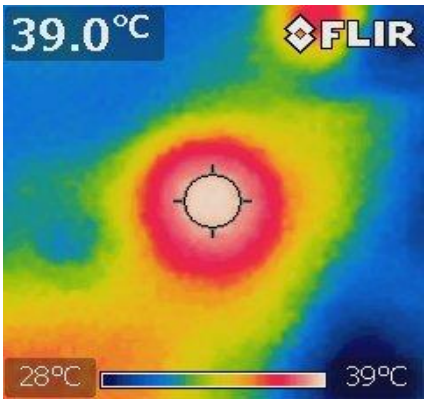


Line-Drop Compensation vs. Load Current



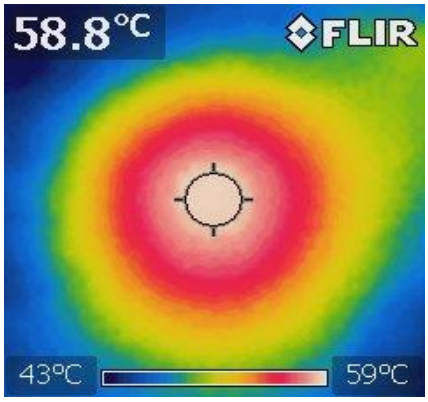
Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C, I_{OUT_USB1} = I_{OUT_USB2} = 1.5A



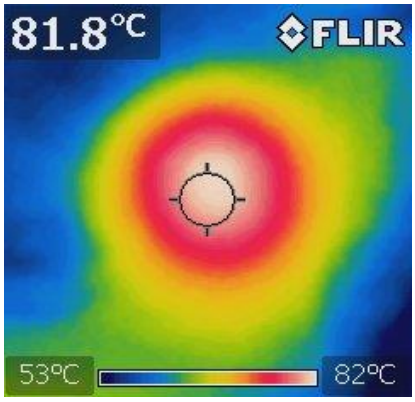
Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C, I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



Thermal Image

V_{IN} = 12V, V_{OUT} = 5.17V, T_A = 21°C, I_{OUT_USB1} = I_{OUT_USB2} = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

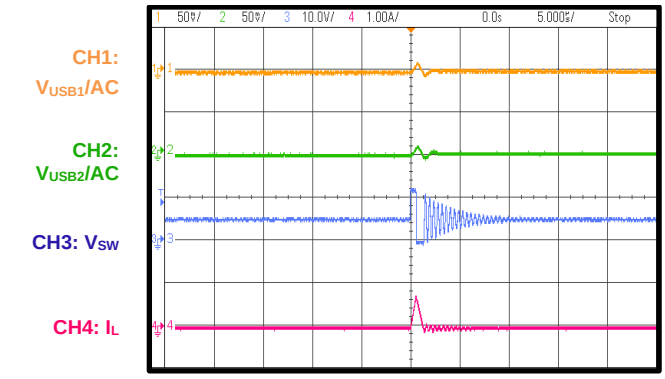
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 480kHz with FSS, L = 4.7µH, T_A = 25°C, CC1 is connected to ground via a 5.1kΩ resistor, unless otherwise noted.

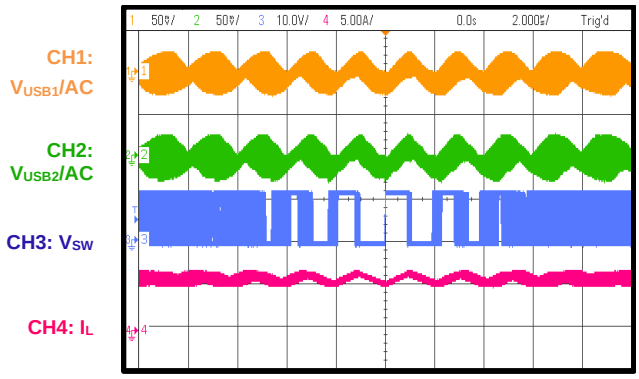
Steady State

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



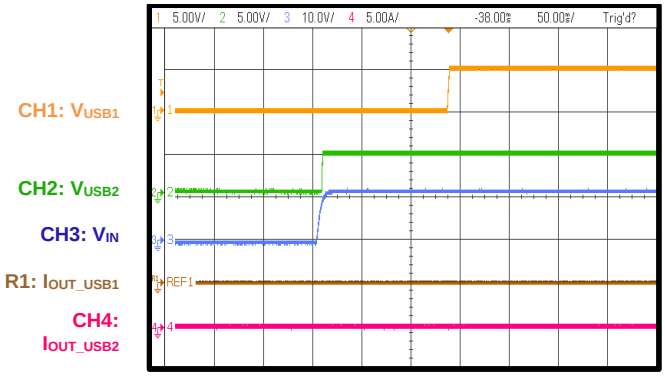
Steady State

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



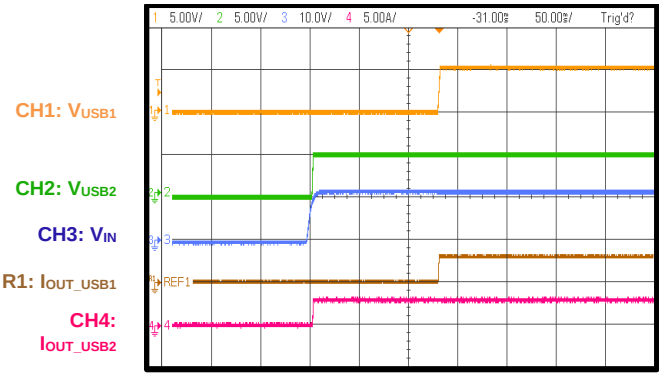
Start-Up through VIN

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



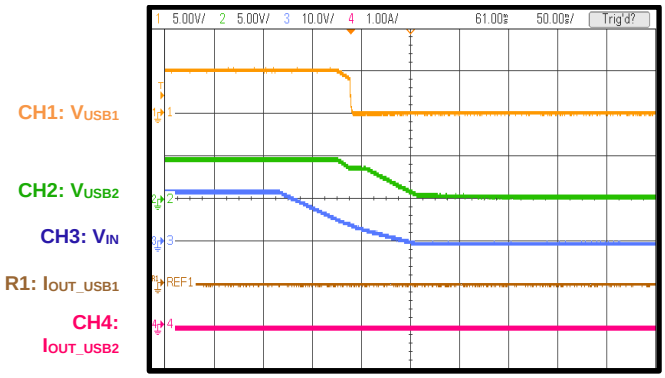
Start-Up through VIN

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



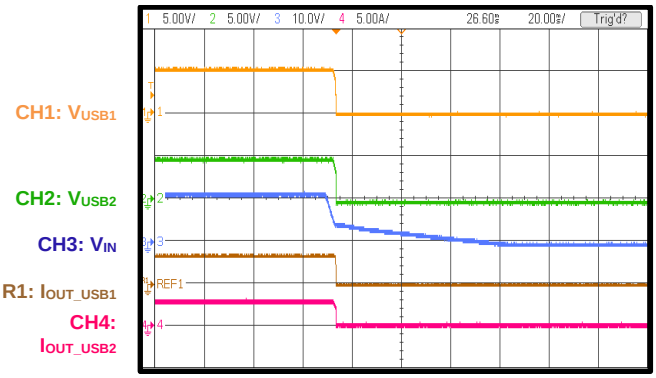
Shutdown through VIN

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



Shutdown through VIN

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

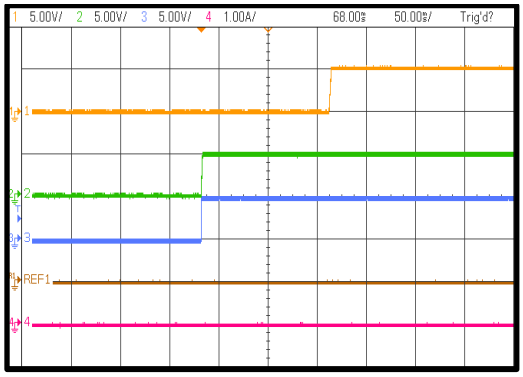
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 480kHz with FSS, L = 4.7µH, T_A = 25°C, CC1 is connected to ground via a 5.1kΩ resistor, unless otherwise noted.

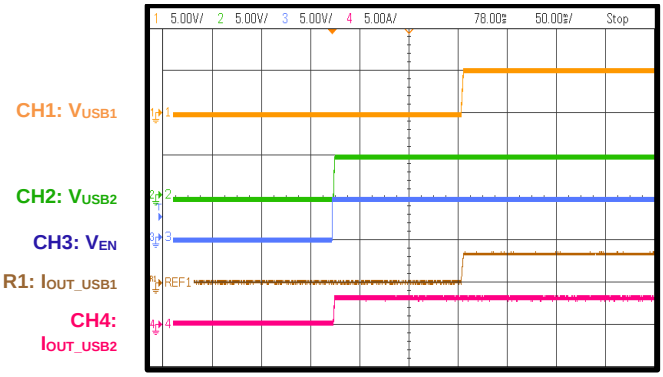
Start-Up through EN

EN pin is disconnected from VCC,
I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



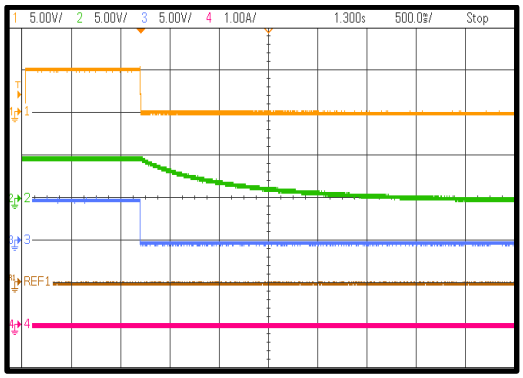
Start-Up through EN

EN pin is disconnected from VCC,
I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



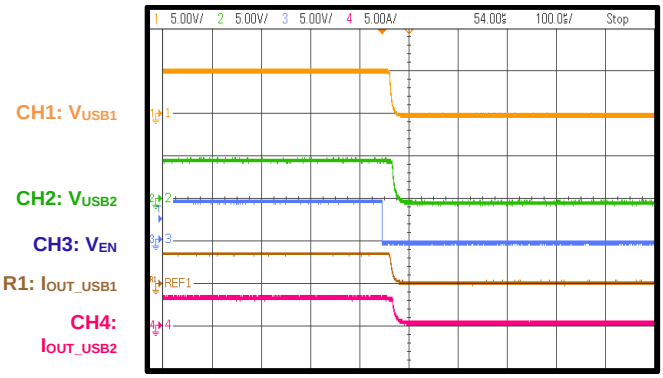
Shutdown through EN

EN pin is disconnected from VCC,
I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



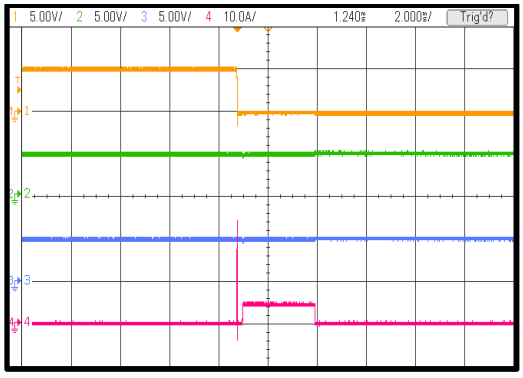
Shutdown through EN

EN pin is disconnected from VCC,
I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 3A



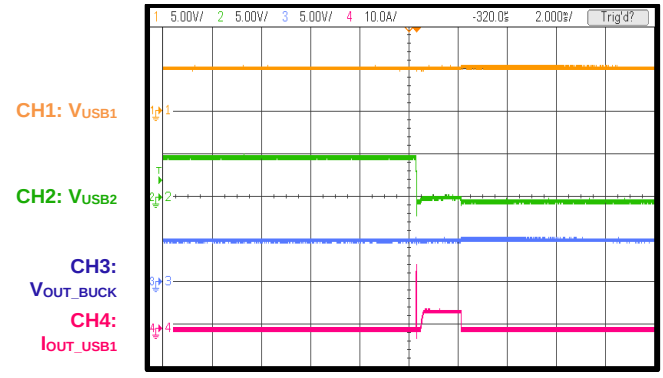
USB1 Short-to-Ground Entry

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



USB2 Short-to- Ground Entry

I_{OUT_USB1} = 1.5A, I_{OUT_USB2} = 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

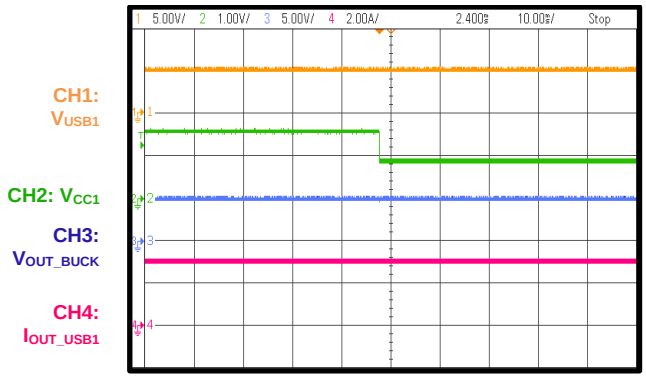
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, f_{SW} = 480kHz with FSS, L = 4.7µH, T_A = 25°C, CC1 is connected to ground via a 5.1kΩ resistor, unless otherwise noted.

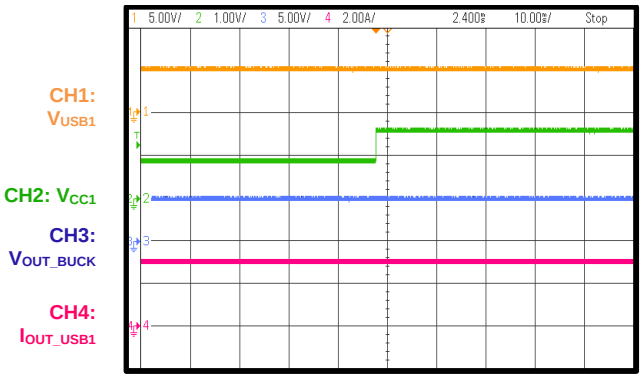
Load-Shedding Entry

USB1_I_{OUT} = 3A, USB2_I_{OUT} = 0A



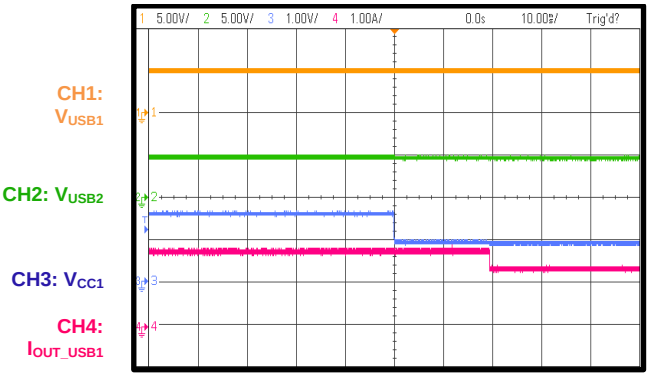
Load-Shedding Recovery

USB1_I_{OUT} = 3A, USB2_I_{OUT} = 0A



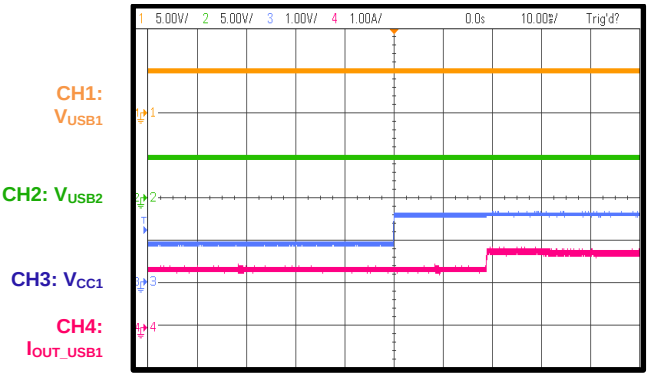
USB Type-C Entry

1.5A load capability, a 5.1kΩ resistor is connected between CC1 and ground, USB1 is connected to a mobile phone, USB2 is plugged into another mobile phone



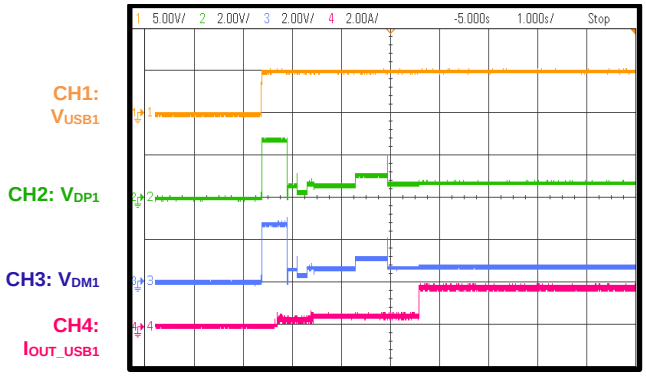
USB Type-C Exit

1.5A load capability, remove the a 5.1kΩ resistor is connected between CC1 and ground, USB1 is connected to a mobile phone, USB2 is disconnected from another mobile phone

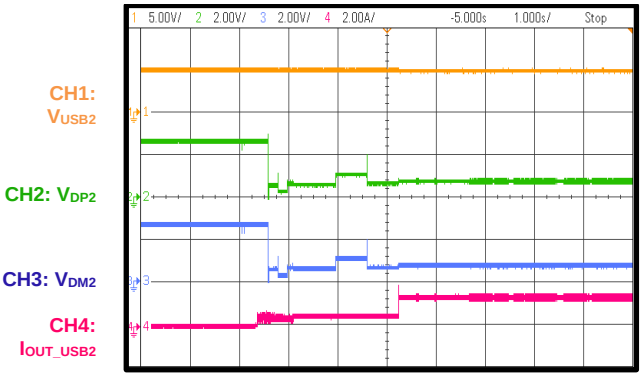


USB Type-C Device Charging Test

Remove the 5.1kΩ resistor connected between CC1 and ground



USB Type-A Device Charging Test



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

FUNCTIONAL BLOCK DIAGRAM

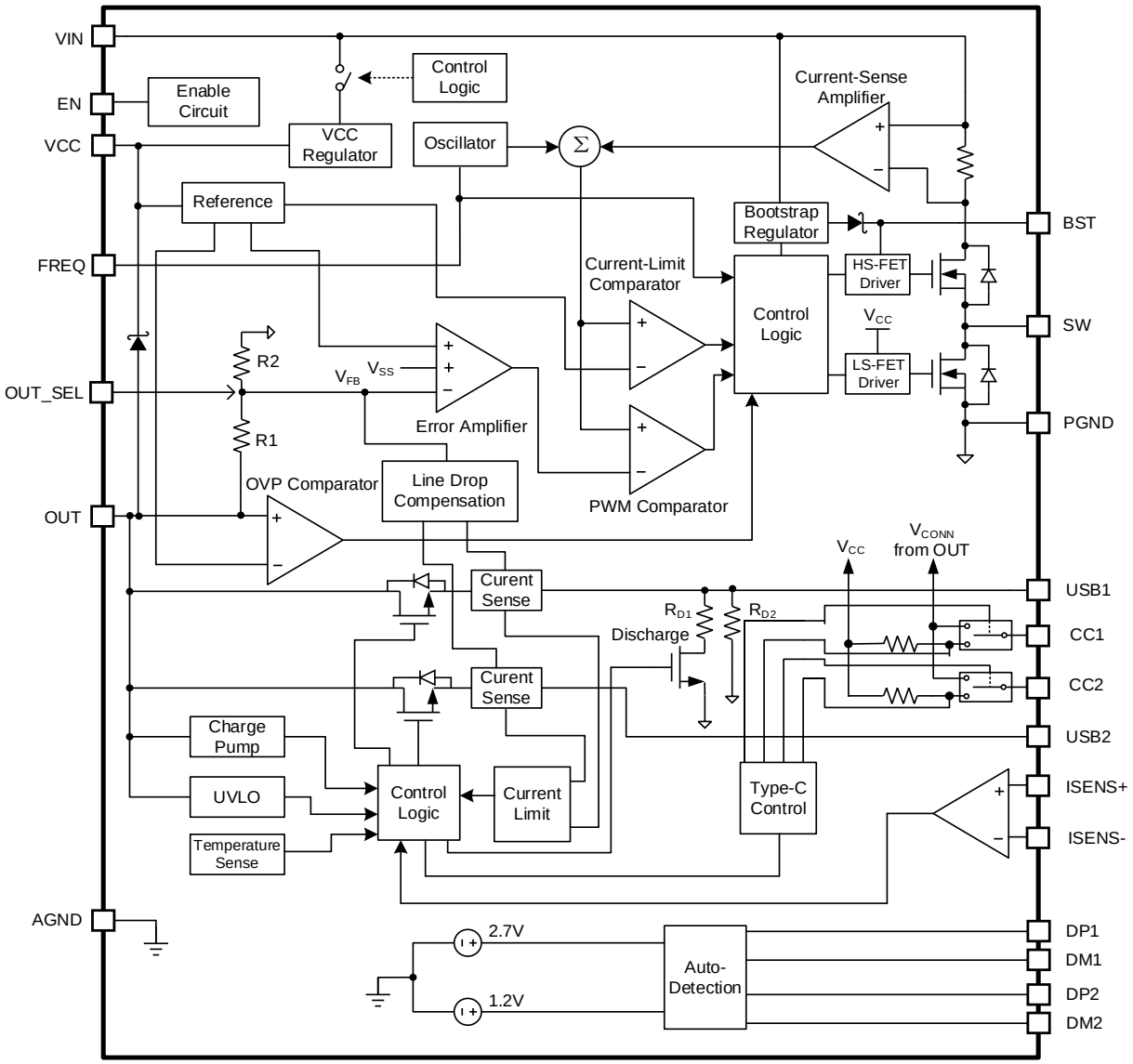


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

OPERATION

BUCK CONVERTER

The MPQ4253B integrates a monolithic, synchronous, rectified, step-down switch-mode converter with two USB current-limit switches and USB charging protocols. The MPQ4253B offers a compact solution that can achieve up to 6A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation.

The MPQ4253B operates with fixed-frequency, peak current (I_{PEAK}) mode control to regulate the output voltage (V_{OUT}). The internal clock initiates the pulse-width modulation (PWM) cycle, which turns the integrated high-side power MOSFET (HS-FET) on. The HS-FET remains on until its current (I_{HS}) reaches the value set by the COMP voltage (V_{COMP}). If the MOSFET turns off, then it remains off until the next clock cycle begins. If the duty cycle reaches 95% (480kHz switching frequency) in one PWM period, then I_{HS} does not reach the value set by V_{COMP}, and the power MOSFET turns off. Under light-load conditions, the device enters pulse-frequency modulation (PFM) mode to improve efficiency.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage (V_{FB}) and the internal reference (V_{REF}) to output V_{COMP}, which controls I_{HS}. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The MPQ4253B requires an external power supply connected to VCC to enable the chip before the converter turns on. This can be accomplished by connecting a resistor and a 5.1V Zener diode between VIN and AGND (see the Typical Application Circuit section on page 23). VCC is supplied by an external resistor and diode path. If VCC exceeds 2.3V, the internal VCC LDO regulator turns on. This regulator takes V_{IN} as the input and internally regulates the VCC voltage (V_{CC}) to 4.6V. VCC requires an external 220nF ceramic decoupling capacitor.

After the buck output starts up, the internal VCC LDO output is biased by the buck output via a Schottky diode.

Figure 2 shows the external VCC connection.

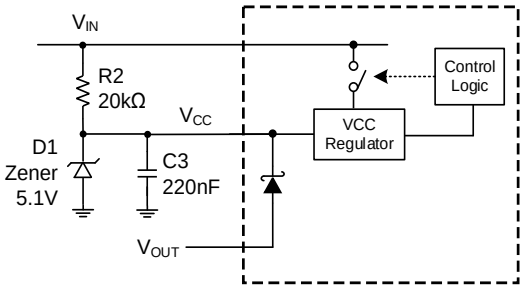


Figure 2: External VCC Connection

Enable (EN) Control

The MPQ4253B has an enable (EN) control pin. Pull EN high to turn the IC on; pull EN low to turn it off. The internal VCC LDO regulator and buck converter can also be turned off via EN. Do not float EN. Once the EN voltage (V_{EN}) is high, the buck output and USB2 are enabled.

V_{EN} is clamped internally via a 7.6V series Zener diode and the ESD cell's breakdown voltage (10V).

It is recommended to connect the EN and VCC pins. The IC starts up once V_{IN} exceeds the under-voltage lockout (UVLO) rising threshold. When selecting a pull-up resistor, ensure that it is large enough to limit the current flowing into EN below 100μA.

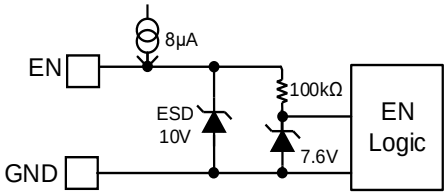


Figure 3: Zener Diode between EN and GND

Setting the Switching Frequency (f_{SW})

Connect a resistor between the FREQ pin and ground to set the switching frequency (f_{SW}) (see Table 1).

Table 1: Recommended Resistor Values for Typical Switching Frequencies

R_{FREQ} (kΩ)	f_{SW} (kHz)
0	250
66.5	350
Not connected	480 with FSS
22	1000

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

The FREQ resistor (R_{FREQ}) can be between 20kΩ and 80kΩ. f_{SW} can be estimated with Equation (1):

$$f_{SW}(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(k\Omega) + 53.7} \quad (1)$$

Figure 4 shows the relationship between f_{SW} and R_{FREQ}.

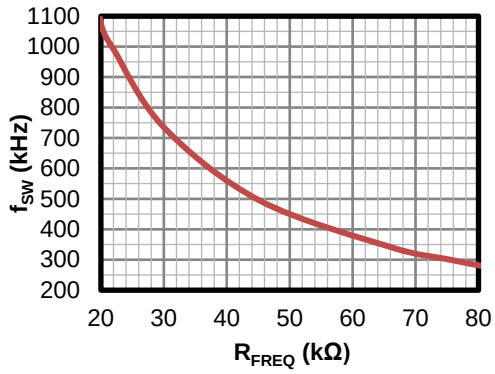


Figure 4: f_{SW} vs. R_{FREQ}

Two internal comparators monitor FREQ's logic voltage to enable FREQ, float FREQ, or short FREQ to ground. During start-up, there is another internal source current on FREQ. f_{SW} is set at 480kHz if the sensed FREQ voltage (V_{FREQ}) is >2V for longer than 8µs. f_{SW} is set at 250kHz if the sensed V_{FREQ} is <0.1V for longer than 8µs. Float FREQ for the default f_{SW} (480kHz). Short FREQ to ground to set f_{SW} at 250kHz (see Figure 5).

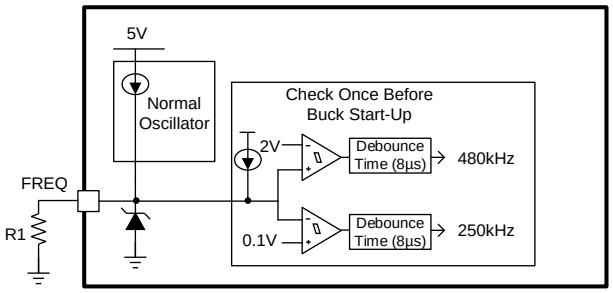


Figure 5: f_{SW} Functional Block Diagram

Frequency Spread Spectrum (FSS)

The purpose of the frequency spread spectrum (FSS) is to minimize the peak emissions at certain frequencies.

The MPQ4253B uses a 4kHz triangle wave (125µs rising, 125µs falling) to modulate the internal oscillator. The FSS span is ±10% f_{SW} (see Figure 6).

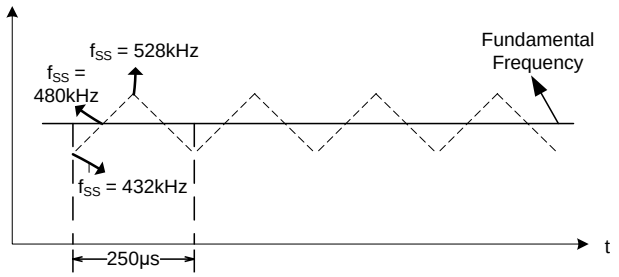


Figure 6: Frequency Spread Spectrum (FSS)

Float FREQ when using the FSS function. The part operates without FSS while FREQ is connected to an external resistor or shorted to ground.

Light-Load Operation

As the load decreases, the MPQ4253B enters discontinuous conduction mode (DCM), and maintains a fixed f_{SW} as the inductor current (I_L) approaches 0A.

If the load decreases further or if there is no load, then the part enters sleep mode. The IC consumes very low quiescent current (I_Q) to improve efficiency under light-load conditions. In sleep mode, the internal clock is blocked, and the MPQ4253B skips some pulses. If V_{FB} drops below the reference voltage (V_{REF}), then V_{COMP} ramps up until the peak I_L (I_{L_PEAK}) exceeds the advanced asynchronous modulation (AAM) threshold. Then the internal clock is reset, and the crossover time is used as the benchmark for the next clock. This control scheme achieves high efficiency by scaling down f_{SW} to reduce switching and gate driver losses.

V_{COMP} and f_{SW} increase as I_{OUT} increases from light load. If I_{OUT} exceeds the critical level set by V_{COMP}, then the MPQ4253B resumes fixed-frequency PWM control (see Figure 7).

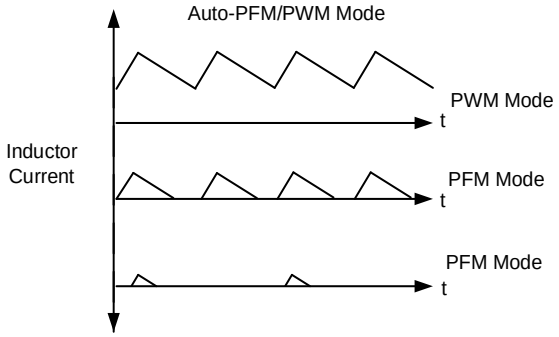


Figure 7: Auto-PFM/PWM Mode

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) protection protects the chip from operating at an insufficient supply voltage by monitoring V_{IN} via the UVLO comparator. The UVLO rising threshold is 5V, and the UVLO falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's output from overshooting during start-up. When the buck converter starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 5V. If V_{SS} is below V_{REF}, then the error amplifier (EA) uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

The soft-start time (t_{SS}) is set to 1ms internally. If the output is pre-biased to a certain voltage during start-up, then the IC turns off both the HS-FET and LS-FET until the voltage on the internal soft-start capacitor (C_{SS}) exceeds the internal V_{FB}.

Buck Over-Current Protection (OCP)

The MPQ4253B provides over-current protection (OCP) for the buck converter. There is a cycle-by-cycle over-current (OC) limit. If I_{L_PEAK} exceeds the current-limit threshold, and V_{FB} drops below the under-voltage protection (UVP) threshold (typically 50% below V_{REF}), then UVP is triggered, and the device enters hiccup mode to periodically restart the part. This protection mode is especially useful if the output is dead-shorted to ground. This reduces the average short-circuit (SC) current, alleviates thermal issues, and protects the regulator. The MPQ4253B exits hiccup mode once the OC fault is removed.

Buck Output Over-Voltage Protection (OVP)

The MPQ4253B provides output over-voltage protection (OVP) for the buck converter. If the output exceeds 5.9V, then the HS-FET turns off and the LS-FET turns on to discharge V_{OUT} until the it decreases to 5.7V. Once V_{OUT} drops below 5.7V, the part resumes normal operation.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C4) powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The BST voltage (V_{BST}) is regulated internally by VIN and VCC via D1, D2, M1, C4, L1, and C2 (see Figure 8).

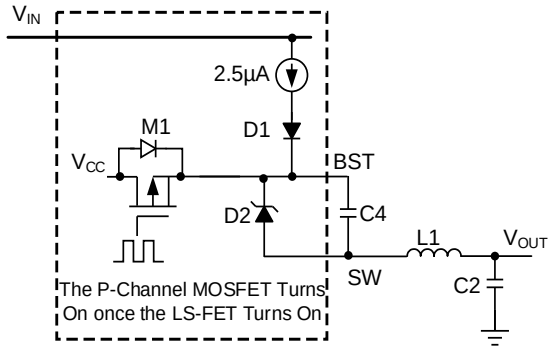


Figure 8: Internal BST Charging Circuit

V_{BST} is charged quickly by VCC via M1. If the LS-FET is not on, the input to the BST current source (2.5µA) can also charge V_{BST}.

Start-Up and Shutdown

If V_{IN} and V_{CC} exceed their respective thresholds, then the internal regulator starts up and provides a stable supply for the remaining circuitries. The buck converter and USB2 are active once EN starts up the part.

If V_{EN} or V_{IN} is pulled low, the part shuts down. During shutdown, the signaling path is blocked to avoid triggering any faults. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

USB CURRENT-LIMIT SWITCH

OCP with Hiccup Mode

The MPQ4253B integrates two USB current-limit switches. The MPQ4253B provides built-in soft-start circuitry that controls the rising slew rate of V_{OUT} to limit the inrush current and voltage surges.

If the load current (I_{LOAD}) reaches the current-limit threshold, then the USB power MOSFET operates in constant-current-limit mode.

If the OC limit condition lasts longer than 5ms (and V_{OUT} does not drop too low), then the corresponding USB channel enters hiccup mode with a 5ms on time (t_{ON}) and 2s off time (t_{OFF}). The other USB channel continues to operate normally.

Figure 9 on page 17 shows OCP.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

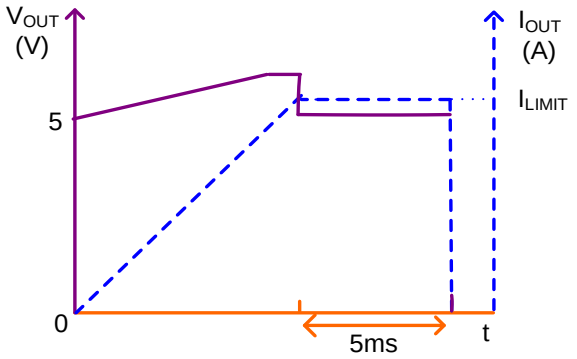


Figure 9: Over-Current Protection (OCP)

If the USB V_{OUT} is below 3.5V for longer than 50µs after soft start finishes, then the MPQ4253B enters hiccup mode without having to wait 5ms (see Figure 10).

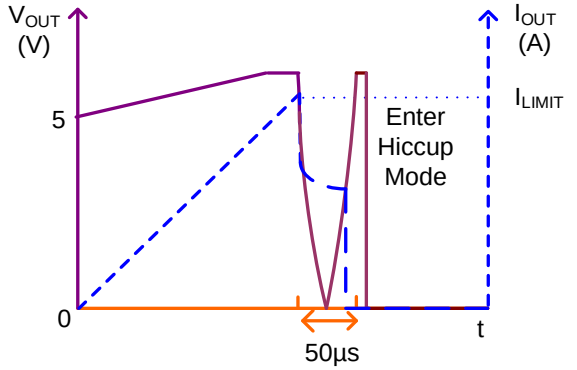


Figure 10: Over-Current Protection for CR Load

This prevents an abnormal thermal rise during a constant resistor (CR) load over-current case.

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 7A (for USB1) or 10.5A (for USB2) secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This helps limit I_{PEAK} through the switch, keeping the buck V_{OUT} from dropping too much and affecting another USB channel. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MPQ4253B regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MPQ4253B can compensate for a V_{OUT} drop, such as high impedance caused by a long trace, to maintain a fairly constant V_{OUT} at the load-side voltage.

The internal comparator compares the current-sense V_{OUT} of the two current-limit switches, and uses the larger current-sense V_{OUT} to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. It also has an upper limitation. At output currents above 2.4A, the line drop compensation is 90mV.

USB Output Over-Voltage (OV) Clamp

To protect the device at the cable terminal, the USB switch output has a fixed OVP threshold. If V_{IN} exceeds the OVP threshold, then V_{OUT} is clamped at its OVP threshold value.

USB Output Discharge and Impedance

The USB1 switch has a fast discharge path that can discharge the external output capacitor's energy quickly during power shutdown. This function is active when the CC pins are released or the part is disabled (V_{IN} is below the UVLO threshold or EN is off). The discharge path turns off when the USB V_{OUT} is discharged below 50mV. After the fast discharge path turns off, there is only a high-impedance resistor (typically 500kΩ) from USB1 to ground.

USB2 has no output discharge function.

USB Port State Detection

The MPQ4253B monitors the USB2 Type-A port's state through DP2/DM2 or through the USB2 I_{OUT} sensed by ISENS+ and ISENS-. If the DP2/DM2 voltage falls into the detection window or the voltage between ISENS+ and ISENS- exceeds 7.5mV, this means a Type-A device is attached. Then the USB1 port's CCx pin pull-up resistance (R_P) changes to 22kΩ to indicate that its source current capability is reduced to 1.5A.

1. The MPQ4253B returns to normal mode (R_P = 10kΩ) within 3 seconds once the MPQ4253B detects that there is not a device plugged into the Type-A port.
2. If the Type-C port or Type-A port is operating alone, it can provide up to 3A of current.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

Auto-Detection

The MPQ4253B integrates a USB dedicated charging port (DCP) auto-detection function. The USB outputs are fixed with one Type-C port for USB1 and one Type-A port for USB2. This function recognizes most mainstream portable devices and supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple divider 3 mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode (only for USB1)

The auto-detection function is a state machine that supports all of the DCP charging schemes listed above.

USB Type-C Mode and VCONN

For USB1 Type-C solutions, the CCx pins on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on the ability to detect terminations residing in the device being attached. To define the functional behavior of CCx, a pull-up and pull-down termination model is used based on a pull-up resistor (R_P) and a pull-down resistor (R_D = 5.1kΩ) (see Figure 11).

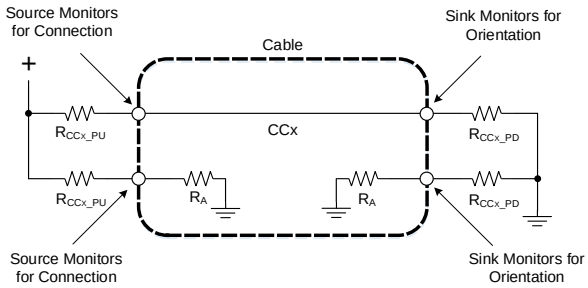


Figure 11: Current-Source and CCx Pull-Down Termination Model

A source exposes independent R_P terminations on its CCx pins, and a sink exposes independent R_D terminations on its CCx pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CCx for a voltage below its unterminated voltage. R_P is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to applying the VCONN voltage (V_{CONN}), a powered cable exposes R_A (typically 1kΩ) on its VCONN pin. R_A represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this may be a pure resistance. In other plugs, this may be the load.

The source should be able to differentiate between the presence of R_D and R_A to determine whether there is a sink attached, and where to apply V_{CONN}. A source is not required to supply V_{CONN}, unless R_A is detected.

There are two termination combinations on the CCx pins (as seen by a source) for directly attached accessory modes: R_A/R_A for audio adapter accessory mode, and R_D/R_D for debug accessory mode (see Table 2 on page 19). Figure 12 shows the functional block diagram of the CCx pins.

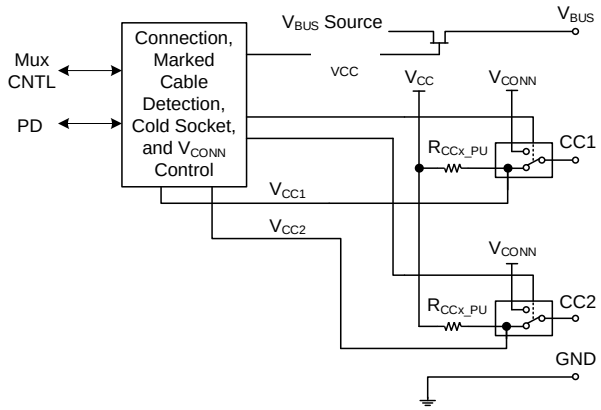


Figure 12: CCx Functional Block Diagram

A port that behaves as a source has the following functional characteristics:

1. The source uses a MOSFET to enable and disable power delivery (PD) across the bus voltage (V_{BUS}). The source disables V_{BUS} initially.
2. The source has two pull-up resistors (R_P) for the CCx pins. Both pull-up resistors are monitored to detect a sink. The presence of R_D on CCx indicates that a sink is attached. R_P indicates the initial USB Type-C current level supported by the host. The MPQ4253B's default R_P is 10kΩ, which indicates a 3A current level.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

3. The source uses R_D to detect and determine which CCx pin should supply V_{CONN} (once R_A is discovered).
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source can adjust the value of R_P dynamically to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures (or if USB2 detects a device is attached), R_P changes to 22kΩ to indicate a 1.5A current capability. The source continues to monitor the presence of R_D to detect whether a sink is detached. If a sink is detached, then the source is removed, and the process returns to step 2.

Load Shedding

The MPQ4253B monitors the die temperature, and changes the USB1 current capability dynamically. If the die temperature exceeds 125°C, then V_{OUT} remains unchanged. The USB1 port's R_P changes to 22kΩ to indicate a 1.5A source capability.

If the die temperature drops below 100°C for 16s, then the USB1 Type-C current capability returns to 3A (R_P = 10kΩ). The current-limit threshold is 5A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds the thermal shutdown threshold (165°C), then the USB switch shuts down. Once the temperature drops below about 145°C, the device resumes normal operation.

Table 2: CCx Logic Truth Table

EN	USB1 CCx	USB2 Port Status	Buck	VCONN (USB1)	USB1	USB2
0	-	-	Disabled	Disabled	Disabled	Disabled
1	Audio	Attached with device	Enabled	Disabled	Disabled	Enabled
	Debug		Enabled	Disabled	Disabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled (13)	Enabled
	Open		Enabled	Disabled	Disabled	Enabled
1	Audio	Unattached	Enabled	Disabled	Disabled	Enabled
	Debug		Enabled	Disabled	Disabled	Enabled
	R_D, R_A		Enabled	Enabled	Enabled	Enabled
	Open		Enabled	Disabled	Disabled	Enabled

Note:

13) R_P changes to 22kΩ to indicate that its source capability has changed to 1.5A.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% greater than the maximum I_{LOAD} (I_{LOAD_MAX}). Select an inductor with a small DC resistance to improve efficiency. For most designs, the inductance (L_1) can be calculated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose ΔI_L to be approximately 30% to 50% of the maximum load current. The maximum inductor current (I_{L_MAX}) can be calculated with Equation (3):

$$I_{L_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients. 100µF electrolytic and 40µF ceramic capacitors are recommended in automotive applications where f_{SW} = 480kHz.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (I_{C1}) can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose a C1 with an RMS current rating greater than half of I_{LOAD_MAX}.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic capacitors, place two additional high-quality ceramic capacitors as close to VIN as possible. The V_{IN} ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC V_{OUT}. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductance value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

A 100µF to 270µF capacitor with an ESR below 50mΩ (e.g. polymer or tantalum capacitors) and three 10µF ceramic capacitors are recommended in application (see Table 3).

Table 3: Recommended External Components

f_{SW} (kHz)	L (µH)	C1	C2
250	8	40µF ceramic capacitor + 100µF E-CAP	30µF ceramic capacitor + 270µF polymer capacitor
480	4.7	40µF ceramic capacitor + 100µF E-CAP	30µF ceramic capacitor + 270µF polymer capacitor

ESD Protection for the I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MPQ4253B features high ESD protection up to ±8kV human body model (HBM) on the DPx, DMx, and USBx pins. It features up to ±6kV HMB on the CCx pins. The ESD structures can withstand high ESD during both normal operation and while the device is off. Additional resistors and capacitors can be added

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

to further extend the DP and DM pins' ESD levels for complicated application environments

Figure 13 shows the recommended I/O pins ESD enhancements.

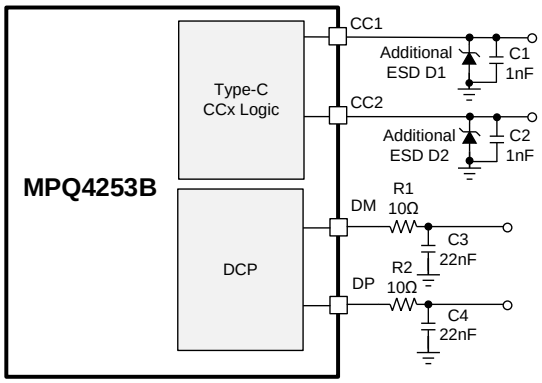


Figure 13: Recommended I/O Pins ESD Enhancement

Similar RC networks cannot be added on the CCx pins since the CCx line has to support a 200mA current and a 300kHz signaling. Additional ESD diodes can be added to CCx.

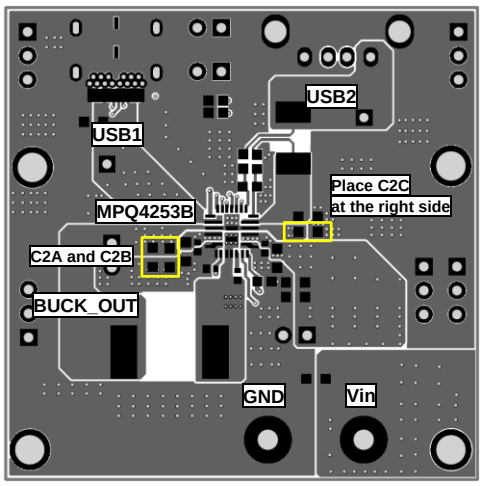
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

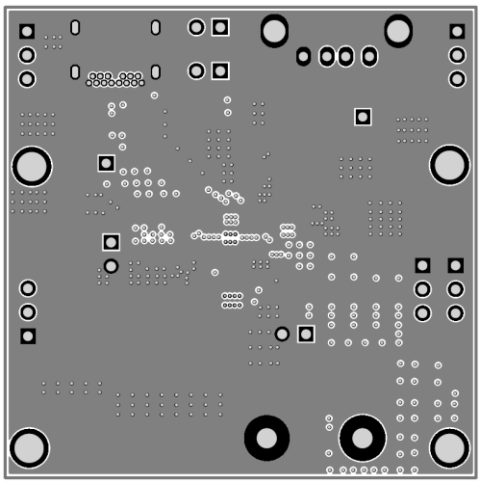
PCB Layout Guidelines (14)

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 14 and follow the guidelines below:

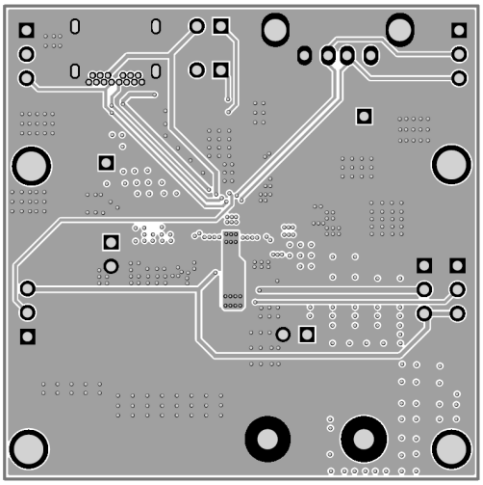
1. Connect OUT using short, direct, and wide traces.
2. Place multiple vias underneath the IC.
3. Route the OUT trace on both PCB layers.
4. Place the buck ceramic output capacitors C2A and C2B on the left side of the IC, and C2C on the right side of the IC.
5. Use a large copper plane for PGND, SW, USB1, and USB2 to reduce resistance.
6. Add multiple vias near IC to improve thermal dissipation.
7. Connect the AGND and PGND pins together.
8. Route the USB1 and USB2 traces on both PCB layers.
9. Place two ceramic input decoupling capacitors as close to VIN and PGND as possible to reduce EMI.
10. Place the symmetrical input capacitors on each side of the IC.
11. Place the BST capacitor close to the BST and SW pins.
12. Place the VCC decoupling capacitor as close to VCC as possible.



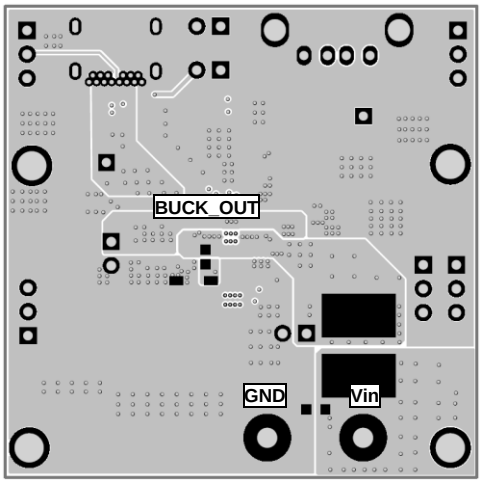
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 14: Recommended PCB Layout

Note:

14) The recommended PCB layout is based on Figure 15 on page 23.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

TYPICAL APPLICATION CIRCUIT

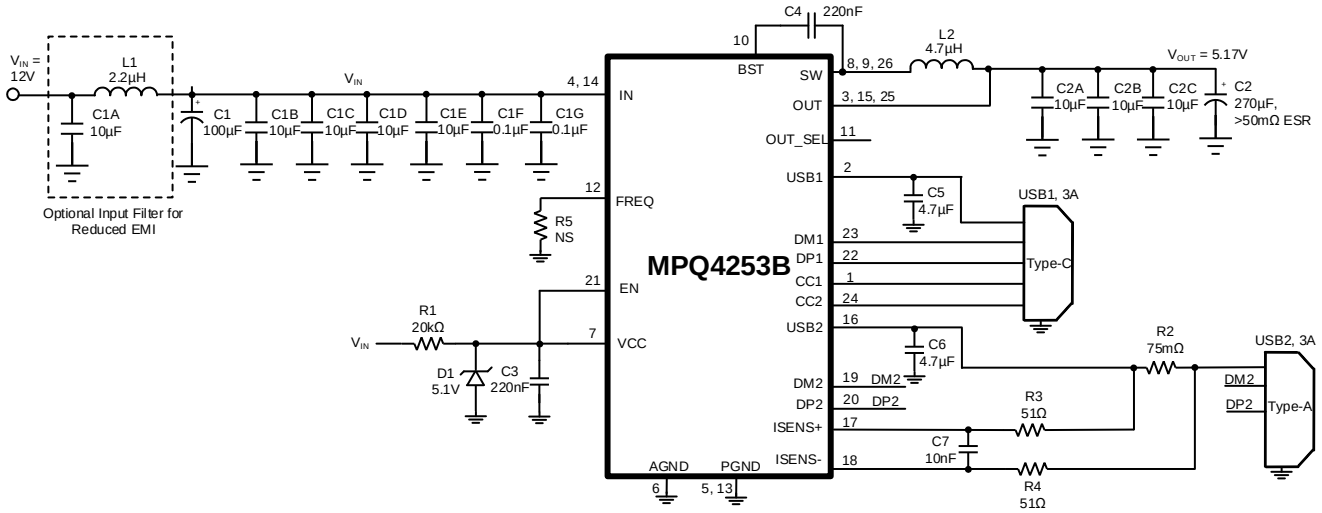


Figure 15: Typical Application Circuit (Type-C 5V/3A DFP Port + Type-A 5V/3A Port) (15)

Note:

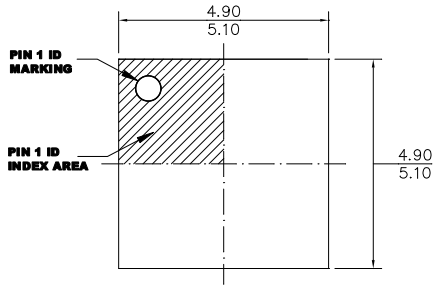
15) See Figure 13 for details on the I/O pins' ESD protections.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

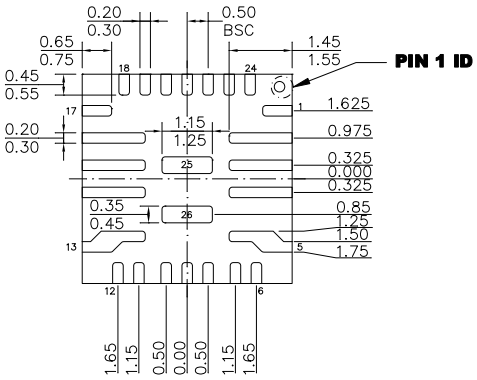
Downloaded from Arrow.com.

PACKAGE INFORMATION

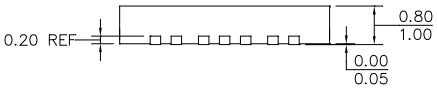
QFN-26 (5mmx5mm)



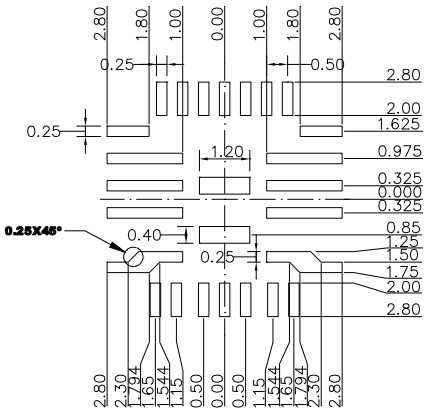
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

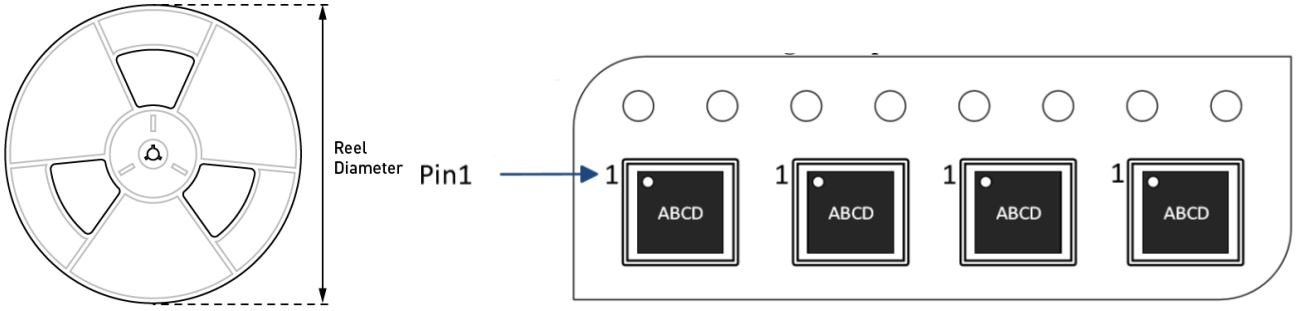
NOTE:

1) LAND PATTERNS OF PIN 2, PIN 3, PIN 4, PIN 14, PIN 15, AND PIN 16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN 13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITIES SHALL BE 0.1 MILLIMETERS MAX.
5) REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4253BGU-AEC1-Z	QFN-26 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/18/2022	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Downloaded from Arrow.com.