HMC624LFLP4E

v00.0511

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, 60 - 500 MHz

Typical Applications

The HMC624LFLP4E is ideal for:

- Cellular/3G Infrastructure
- Repeaters & Access Points
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF Applications

Features

0.5 dB LSB Steps to 31.5 dB

Power-Up State Selection

High Input IP3: +55 dBm

Low Insertion Loss: 1.2 dB

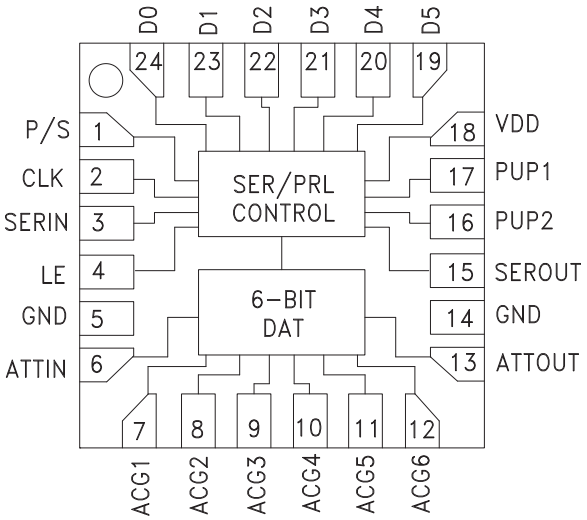
TTL/CMOS Compatible, Serial, Parallel or Latched Parallel Control

<0.1 dB Typical Step Error @ 300 MHz

Single +3V or +5V Supply

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

The HMC624LFLP4E is a 6-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator is suitable for a wide variety of IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC624LFLP4E also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC624LFLP4E is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, 50 Ohm System, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (MHz)	Min.	Typ.	Max.	Units
Insertion Loss	60 - 500 MHz		1.2	1.8	dB
Attenuation Range	60 - 500 MHz		31.5		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	60 - 500 MHz		20		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	60 - 300 MHz 300 - 400 MHz 400 - 500 MHz	± (0.20 + 1% of Atten. Setting) Max ± (0.20 + 2% of Atten. Setting) Max ± (0.20 + 2.5% of Atten. Setting) Max			dB dB dB
Input Power for 0.1 dB Compression	60 - 100 MHz 100 - 500 MHz		30 32		dBm
Input Third Order Intercept Point (Two-Tone Input Power = 10 dBm Each Tone)	60 - 100 MHz 100 - 500 MHz		50 55		dBm
Switching Speed tRise, tFall (10 / 90% RF) rON, tOFF (50% LE to 10 / 90% RF)	60 - 500 MHz		30 60		ns ns

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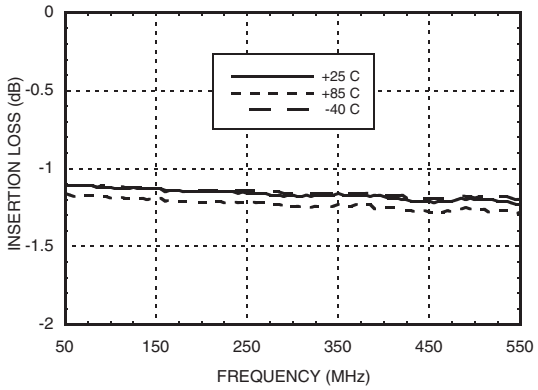
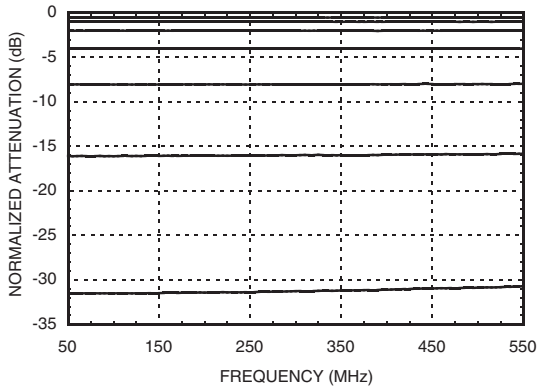
Insertion Loss vs. Temperature



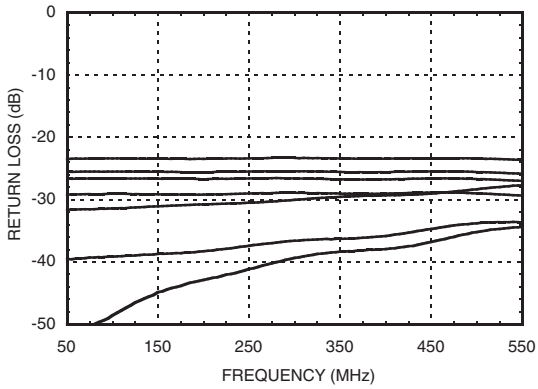
Normalized Attenuation

(Only Major States are Shown)



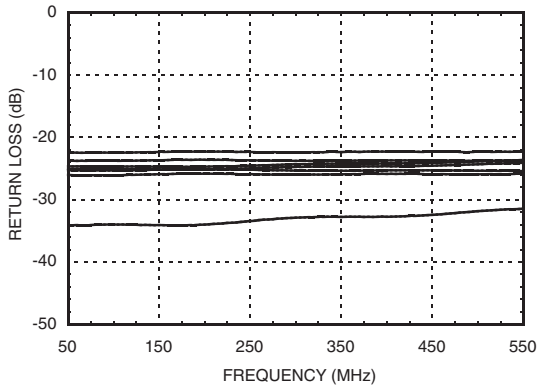
Input Return Loss

(Only Major States are Shown)

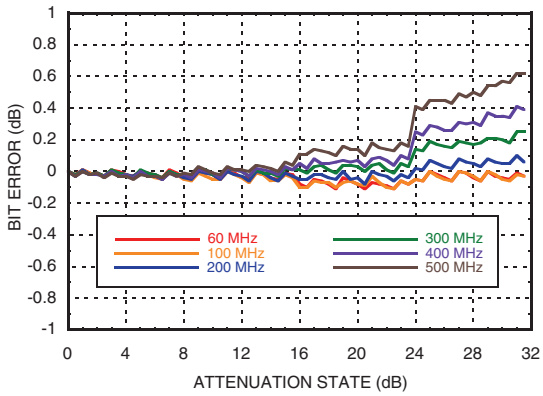


Output Return Loss

(Only Major States are Shown)

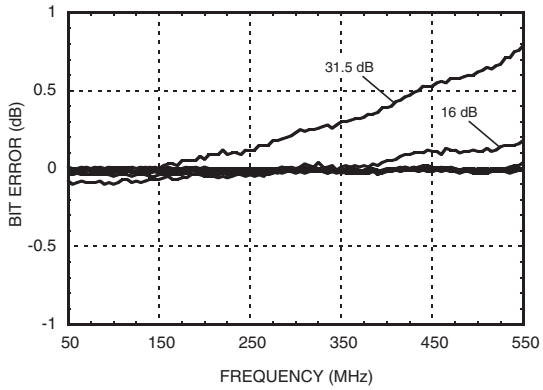


Bit Error vs. Attenuation State



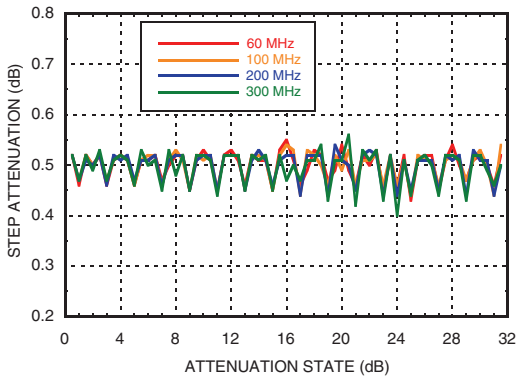
Bit Error vs. Frequency

(Only Major States are Shown)

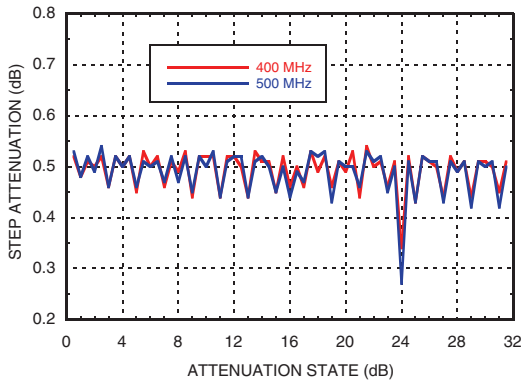


0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, 60 - 500 MHz

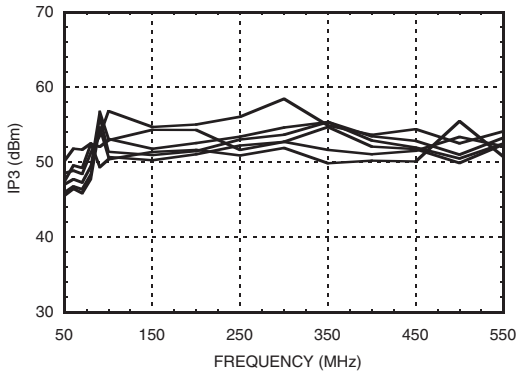
Step Attn vs. Attn State, 60 - 300 MHz



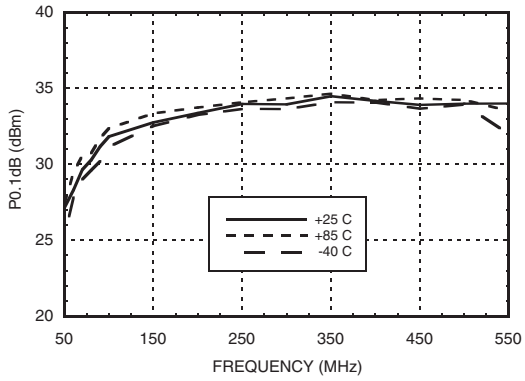
Step Attn vs. Attn State, 400-500 MHz



IP3 @ Major Attenuation States



P0.1dB vs. Temperature

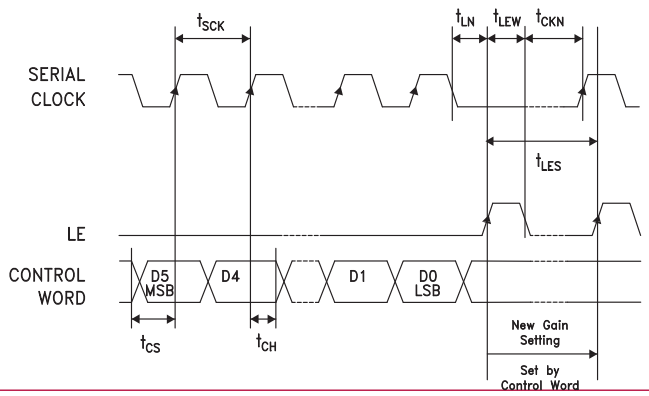


Serial Control Interface

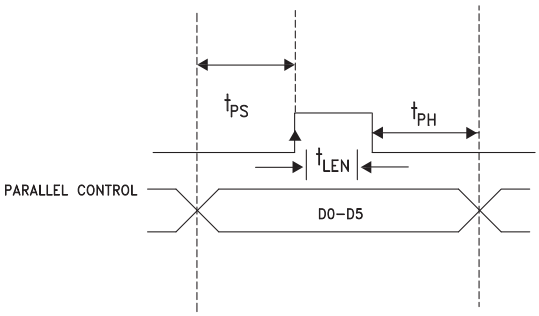
The HMC624LFLP4E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interface is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and the input register is loaded with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data changes the state of the part per truth table.

For all modes of operations, the state will stay constant while LE is kept low.



Timing Diagram (Latched Parallel Mode)



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Parallel Mode
(Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the control voltage inputs D0-D5 directly. The LE (Latch Enable) must be at a logic high at all times to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the control voltage inputs D0-D5 and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Bias Voltage Table

Vdd (V)	Idd (Typ.) (mA)
3	0.12
5	0.15

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

PUP Truth Table

LE	PUP1	PUP2	Relative Attenuation
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	0 to -31.5 dB

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Truth Table

Control Voltage Input						Reference Insertion Loss
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide an attenuation equal to the sum of the bits selected.						

HMC624LFLP4E

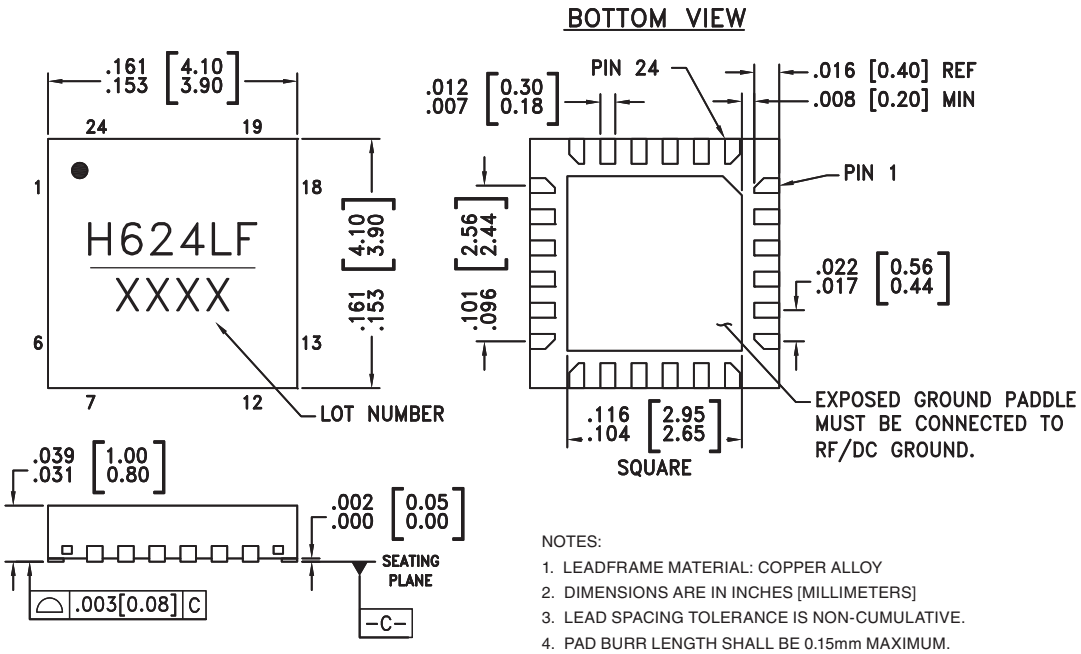
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, 60 - 500 MHz

Absolute Maximum Ratings

RF Input Power (60-500 MHz)	28 dBm (T = +85 °C)
Digital Inputs (P/S, CLK, SERIN, LE, PUP1, PUP2, D0-D5)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C)	0.635 W
Thermal Resistance	102 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

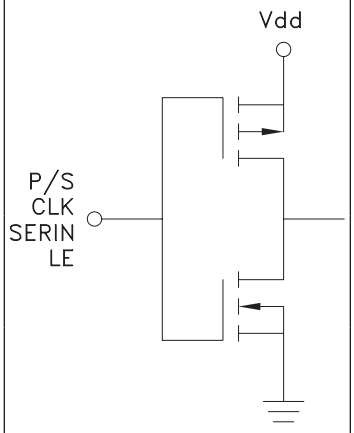
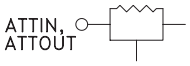
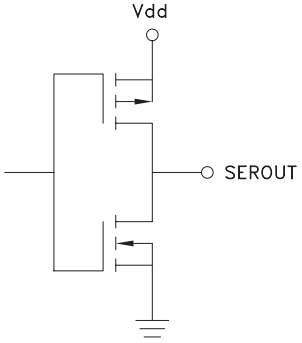
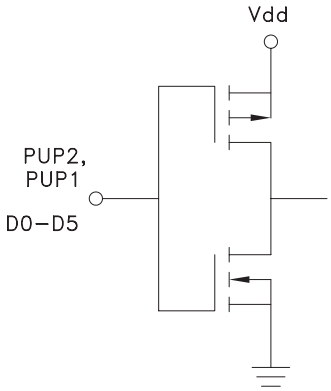
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

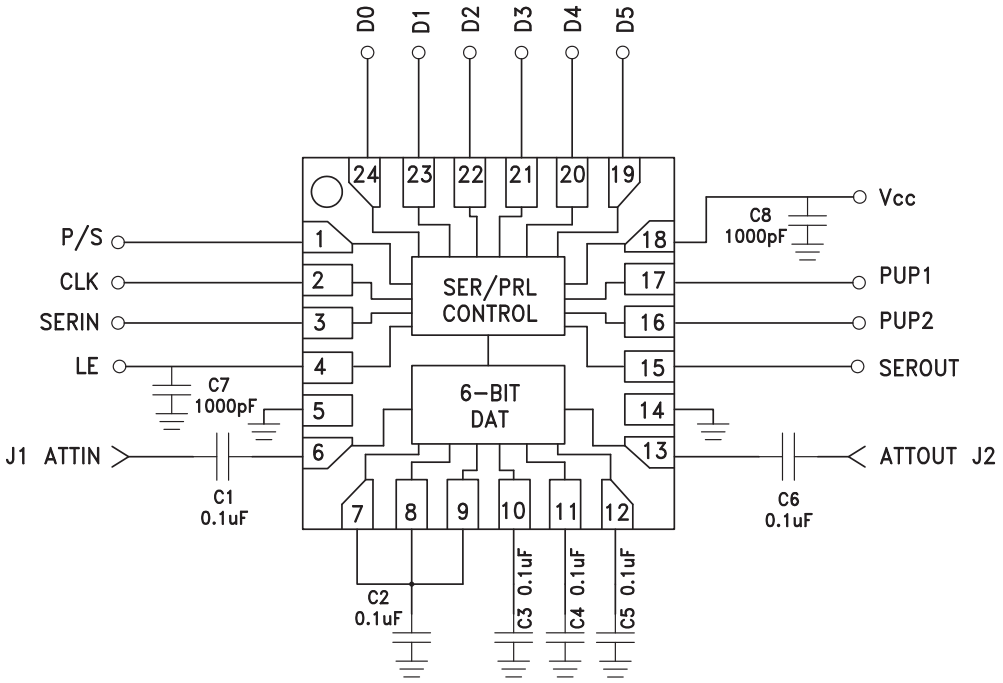
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC624LFLP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H624LF XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

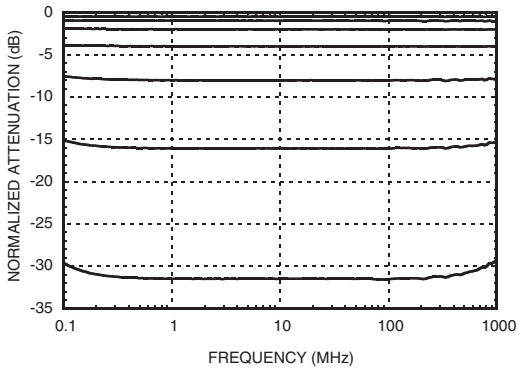
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	P/S	See truth table, control voltage table and timing diagram.	
2	CLK		
3	SERIN		
4	LE		
5, 14	GND	These pins and package bottom must be connected to RF/DC ground.	
6, 13	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
7 - 12	ACG1 - ACG6	External capacitors to ground are required. Select values for lowest frequency of operation. Place capacitors as close to pins as possible.	
15	SEROUT	Serial input data delayed by 6 clock cycles.	
16, 17 19 - 24	PUP2, PUP1 D5, D4, D3, D2, D1, D0	See truth table, control voltage table and timing diagram.	
18	Vdd	Supply voltage	

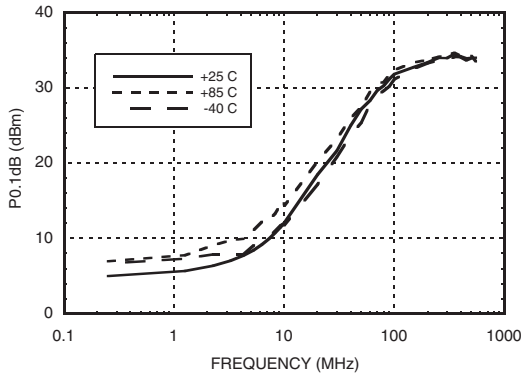
Application Circuit



Normalized Attenuation Wideband Performance



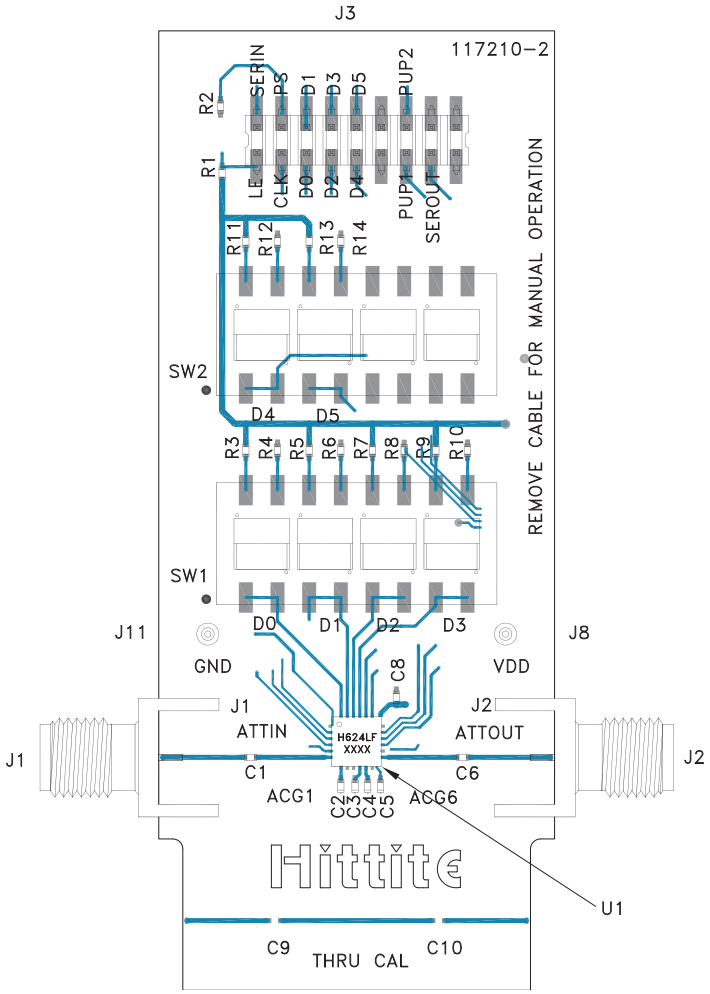
P0.1dB vs. Temperature Wideband Performance



Note: The capacitor value for C1-C6 shown in the standard Application Circuit as 0.1 uF will result in excellent wideband small signal performance from 200 kHz to 500 MHz. Small signal operation to frequencies lower than 200 kHz is possible through the proper selection of capacitors C1-C6. Contact Hittite Applications Group for proper selection of C1-C6 values for frequencies lower than 200 kHz.

Note: The 0.1 dB Input Compression Point degrades for low frequency operation. Typical 0.1 dB Input Compression Point at 60 MHz is +27 dBm tapering to +5 dBm at 250 kHz. The typical 0.1 dB Compression Point holds constant at +5 dBm for frequencies lower than 250 kHz. Hittite recommends that Absolute Maximum Input Power Levels be maintained to less than the 0.1 dB Compression point for reliable operation of the HMC624LFLP4E.

Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC624LFLP4E [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J8, J11	DC Pin
C1 - C6	0.1 uF Capacitor, 0402 Pkg.
C7 - C8	1000 pF Capacitor, 0402 Pkg.
R1 - R14	100 kOhm Resistor, 0402 Pkg.
SW1, SW2	SPDT 4 Position DIP Switch
U1	HMC624LFLP4E Digital Attenuator
PCB [2]	117210 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.