S-35720 A Series

CONVENIENCE TIMER

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AUTOMOTIVE, 125°C OPERATION, TIMER WITH INTERRUPT TIME SETTING PIN

The convenience timer is a CMOS timer IC which operates with low current consumption, and is suitable for the time management of the relative time.
The S-35720 Series compares the timer value and the value set to the SET0 pin and the SET1 pin, and outputs an interrupt signal when the values match each other.
The timer of the S-35720 Series is a 24-bit binary-up counter.
4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Alarm interrupt function: Settable interrupt time
- Low current consumption: 0.2 μA typ. (Quartz crystal: C_L = 6.0 pF, V_{DD} = 3.0 V, Ta = +25°C)
- Wide range of operation voltage: 1.8 V to 5.5 V
- Built-in 32.768 kHz crystal oscillation circuit
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

*1. Contact our sales representatives for details.

■ Application

- Time management of various systems during the sleep period

■ Package

- TMSOP-8

■ Block Diagram

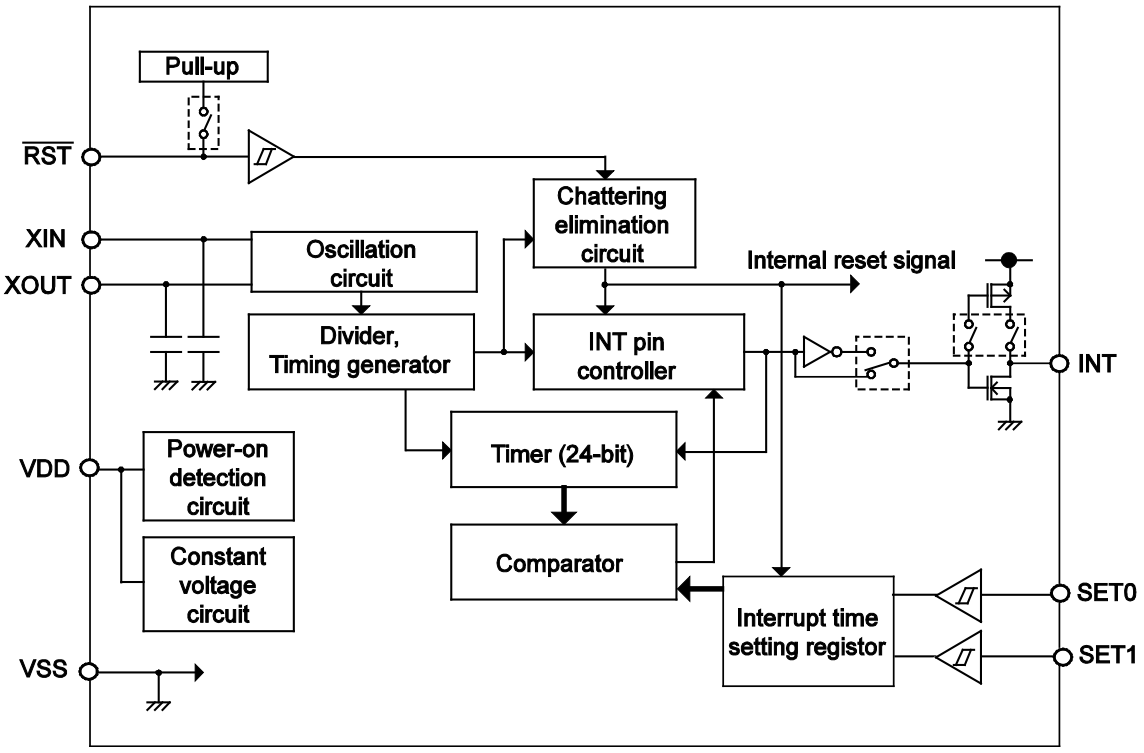


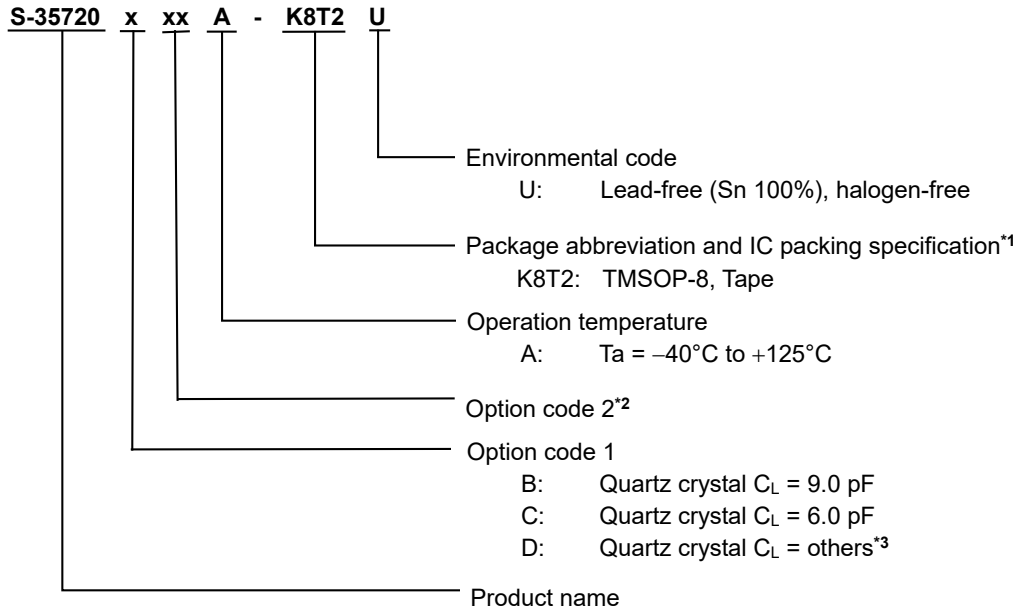
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** A sequence number added by the optional function that is user-selected.
***3.** Contact our sales representatives for details.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	$\overline{RST}$ Pin*1	INT Pin Output Form*2	Time-out Type*3	SET0 Pin, SET1 Pin Settings (SET0, SET1)			
				0, 0	0, 1	1, 0	1, 1
S-35720C01A-K8T2U	With pull-up resistor	Nch open-drain output	One-shot loop time-out (7.8 ms*4)	60 s	10 s	30 s	1 s
S-35720C02A-K8T2U	With pull-up resistor	CMOS output	One-shot loop time-out (125 ms*4)	60 s	10 s	30 s	1 s

***1.** The pin with / without pull-up resistor is selectable. Refer to "■ **Pin Functions**".
***2.** The pin of Nch open-drain output / CMOS output is selectable. Refer to "■ **Pin Functions**".
***3.** The type of one-shot loop time-out / handshake time-out / toggle operation is selectable. Refer to "■ **INT Pin Interrupt Signal Output**". Contact our sales representatives for the details of toggle operation.
***4.** Pulse widths when "one-shot loop time-out" is selected. Refer to "■ **INT Pin Interrupt Signal Output**".

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. TMSOP-8

Top view

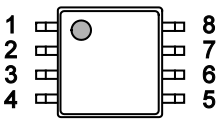


Figure 2

Table 3 List of Pins

Pin No.	Symbol	Description	I/O	Configuration
1	$\overline{\text{RST}}$	Input pin for reset signal	Input	CMOS input (With / without pull-up resistor is selectable)
2	XOUT	Connection pins for quartz crystal	–	–
3	XIN			
4	VSS	GND pin	–	–
5	INT	Output pin for interrupt signal	Output	Nch open-drain output / CMOS output is selectable
6	SET0	Input pins for interrupt time setting	Input	CMOS input
7	SET1			
8	VDD	Pin for positive power supply	–	–

■ Pin Functions

1. SET0, SET1 (Input for interrupt time setting) pins

These pins input the interrupt time setting signal. After the $\overline{RST}$ pin changes from "L" to "H", the S-35720 Series takes the values set to the SET0 pin and the SET1 pin. As a result, even if the SET0 pin and the SET1 pin settings are changed during timer count-up action, the interrupt time does not change.
In one-shot loop time-out and handshake time-out, 4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

2. $\overline{RST}$ (Input for reset signal) pin

This pin inputs the reset signal. The timer is reset when inputting "L" to the $\overline{RST}$ pin, and the timer starts the operation when inputting "H". The $\overline{RST}$ pin has a built-in chattering elimination circuit. Regarding the chattering elimination circuit, refer to "**■ Chattering Elimination of $\overline{RST}$ Pin**".
Also, the $\overline{RST}$ pin with / without pull-up resistor can be selected.

3. INT (Output for interrupt signal) pin

This pin outputs an interrupt signal. The interrupt signal is output when the time set to the SET0 pin and the SET1 pin comes. The interrupt signal output (time-out type) of one-shot loop time-out / handshake time-out / toggle operation*1 can be selected as the option. Regarding the operation of the interrupt signal output, refer to "**■ INT Pin Interrupt Signal Output**".
Also, the INT pin output form of Nch open-drain output / CMOS output can be selected.

***1.** Contact our sales representatives for the details of toggle operation.

4. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

5. VDD (Positive power supply) pin

Connect this pin with a positive power supply.
Regarding the values of voltage to be supplied, refer to "**■ Recommended Operation Conditions**".

6. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

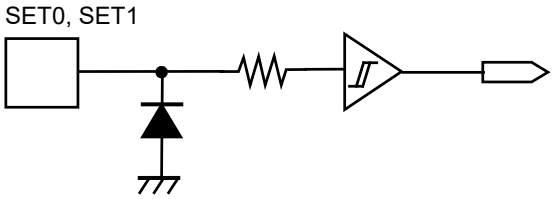


Figure 3 SET0 Pin, SET1 Pin

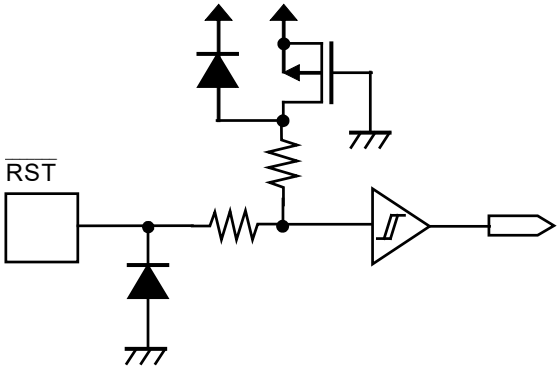


Figure 4 $\overline{\text{RST}}$ Pin (With Pull-up Resistor)

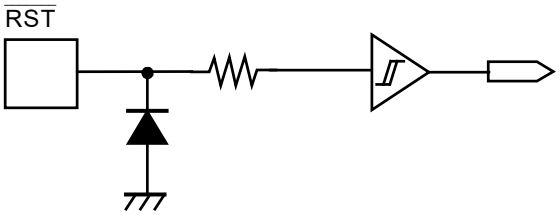


Figure 5 $\overline{\text{RST}}$ Pin (Without Pull-up Resistor)

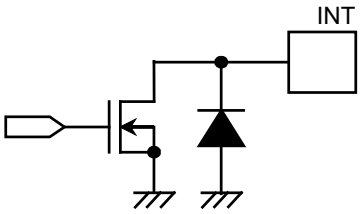


Figure 6 INT Pin (Nch Open-drain Output)

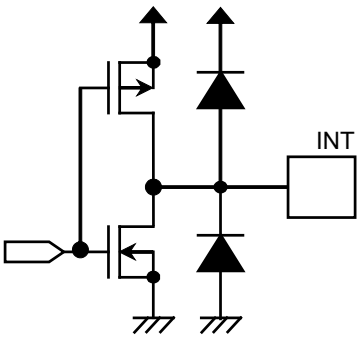


Figure 7 INT Pin (CMOS Output)

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	SET0, SET1, $\overline{RST}$*1	V_{SS} – 0.3 to V_{SS} + 6.5	V
		$\overline{RST}$*2	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Output voltage	V_{OUT}	INT*3	V_{SS} – 0.3 to V_{SS} + 6.5	V
		INT*4	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 6.5	V
Operation ambient temperature*5	T_{opr}	–	–40 to +125	°C
Storage temperature	T_{stg}	–	–55 to +150	°C

***1.** When a product without a pull-up resistor is selected.
***2.** When a product with a pull-up resistor is selected.
***3.** When an Nch open-drain output product is selected.
***4.** When a CMOS output product is selected.
***5.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Condition

Table 5

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V_{DD}	Ta = –40°C to +125°C	1.8	–	5.5	V

■ Oscillation Characteristics

Table 6

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.8	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–20	–	+20	ppm

***1.** Reference value

■ DC Electrical Characteristics

Table 7

(Ta = −40°C to +125°C, V_{SS} = 0 V unless otherwise specified)
(Quartz crystal (NX3215SD, C_L = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	V_{DD} = 3.0 V, Ta = −40°C to +85°C, $\overline{RST}$ pin = V_{DD}, INT pin = no load	–	0.2	0.35	µA
			V_{DD} = 3.0 V, Ta = +125°C, $\overline{RST}$ pin = V_{DD}, INT pin = no load	–	0.7	0.95	µA
High level input leakage current	I_{IZH}	SET0, SET1, $\overline{RST}$	V_{IN} = V_{DD}	−0.5	–	0.5	µA
Low level input leakage current	I_{IZL}	SET0, SET1, $\overline{RST}$*1	V_{IN} = V_{SS}	−0.5	–	0.5	µA
High level output leakage current	I_{OZH}	INT*2	V_{OUT} = V_{DD}	−0.5	–	0.5	µA
Low level output leakage current	I_{OZL}	INT*2	V_{OUT} = V_{SS}	−0.5	–	0.5	µA
High level input voltage	V_{IH}	SET0, SET1, $\overline{RST}$	–	0.7 × V_{DD}	–	V_{SS} + 5.5	V
Low level input voltage	V_{IL}	SET0, SET1, $\overline{RST}$	–	V_{SS} − 0.3	–	0.3 × V_{DD}	V
High level output voltage*3	V_{OH}	INT	I_{OH} = −0.4 mA	0.8 × V_{DD}	–	–	V
Low level output voltage	V_{OL}	INT	I_{OL} = 2.0 mA	–	–	0.4	V
Low level input current*4	I_{IL}	$\overline{RST}$	V_{DD} = 3.0 V, V_{IN} = V_{SS}	−100	−30	−5	µA

***1.** When a product without a pull-up resistor is selected.
***2.** When an Nch open-drain output product is selected.
***3.** When a CMOS output product is selected.
***4.** When a product with a pull-up resistor is selected.

■ INT Pin Interrupt Signal Output

The $\overline{RST}$ pin of the S-35720 Series has a built-in chattering elimination circuit. Therefore, after the $\overline{RST}$ pin changes from "L" to "H", a delay occurs until the timer starts the count-up action. Furthermore, an internal circuit delay occurs until the first interrupt signal occurs. Since the maximum delay time after the $\overline{RST}$ pin changes from "L" to "H" is approximately 700 ms, the timing for the occurrence of the first interrupt signal is delayed.
After the $\overline{RST}$ pin changes from "L" to "H", the S-35720 Series takes the values set to the SET0 pin and the SET1 pin. As a result, even if the SET0 pin and the SET1 pin settings are changed during timer count-up action, the interrupt time does not change.

The INT pin interrupt signal output (time-out type) can be selected from one of the following:

- One-shot loop time-out
- Handshake time-out
- Toggle operation*1

***1.** Contact our sales representatives for the details of toggle operation.

1. One-shot loop time-out

One-shot loop time-out is a type to output the "L" pulse interrupt signal repeatedly from the INT pin.
After the $\overline{RST}$ pin changes from "L" to "H", the timer starts the operation. Then, the INT pin outputs "L" pulse when the timer value matches the value set to the SET0 pin and the SET1 pin*1. After that, the S-35720 Series resets the timer automatically, and restarts a count-up action.
If "L" is input to the $\overline{RST}$ pin before the timer value matches the value set to the SET0 pin and the SET1 pin*1, the timer is reset.

***1.** 4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the INT pin output is the inverse logic of the Nch open-drain output product.

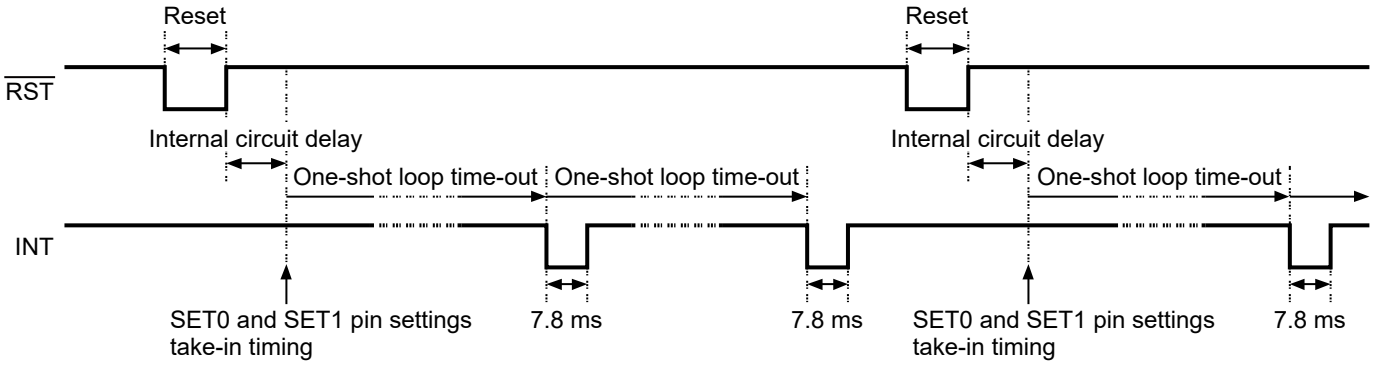


Figure 8 Output Timing of One-shot Loop Time-out (S-35720C01A / Nch Open-drain Output)

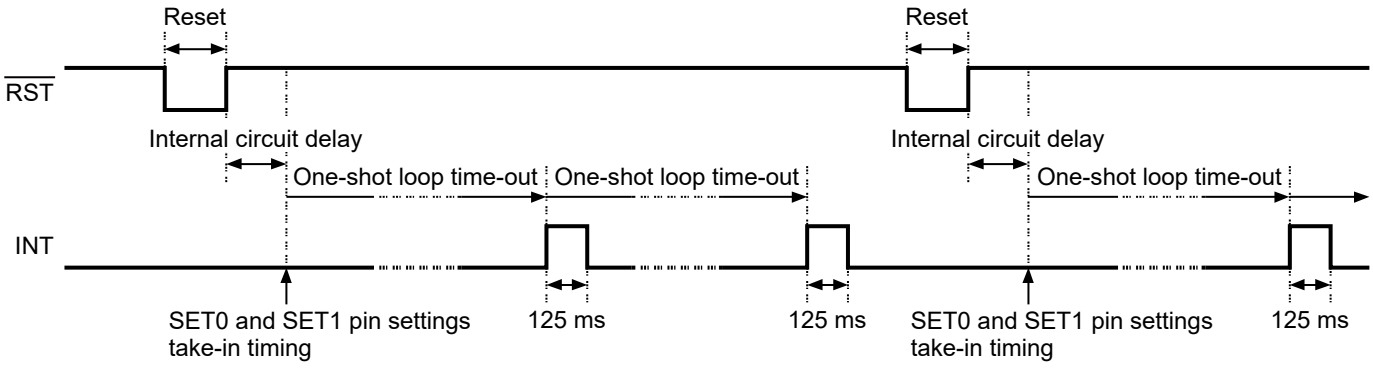


Figure 9 Output Timing of One-shot Loop Time-out (S-35720C02A / CMOS Output)

2. Handshake time-out

Handshake time-out is a type to output "L" level interrupt signal from the INT pin.
After the $\overline{RST}$ pin changes from "L" to "H", the timer starts the operation. Then, the INT pin outputs "L" level when the timer value matches the value set to the SET0 pin and the SET1 pin*1. When the INT pin outputs "L" level, the timer stops and maintains the timer value.
The timer is reset by inputting "L" to the $\overline{RST}$ pin. After that, if "H" is input to the $\overline{RST}$ pin, the INT pin is set to "H" and the timer restarts the count-up action.
If "L" is input to the $\overline{RST}$ pin before the timer value matches the value set to the SET0 pin and the SET1 pin*1, the timer is reset.

***1.** 4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

Remark The above description is the example of an Nch open-drain output product.
In a CMOS output product, the INT pin output is the inverse logic of the Nch open-drain output product.

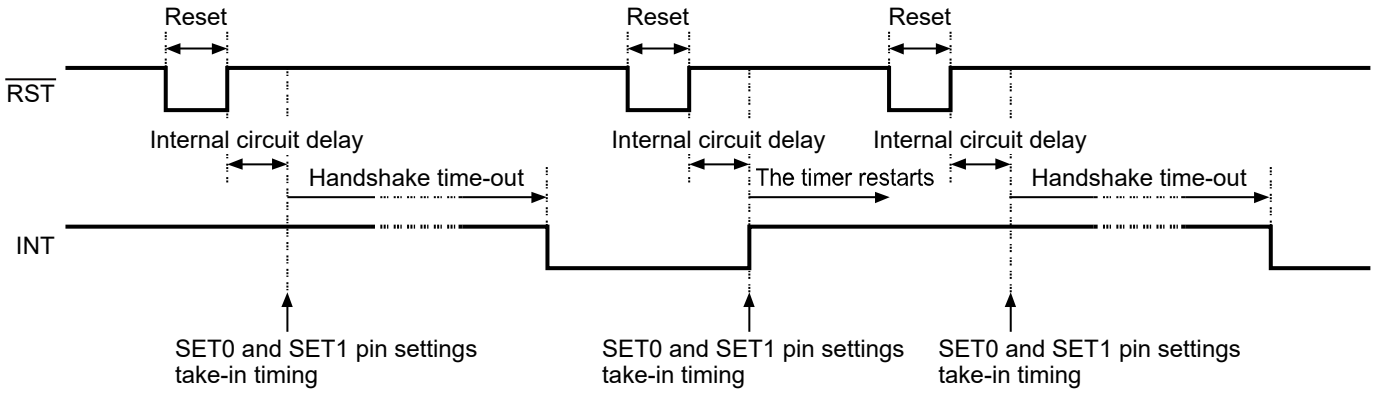


Figure 10 Output Timing of Handshake Time-out (Nch Open-drain Output)

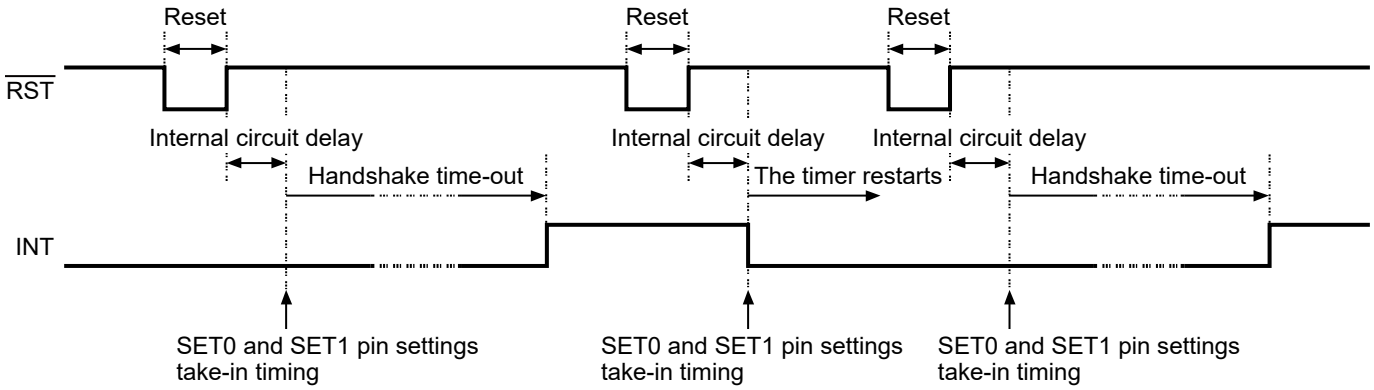
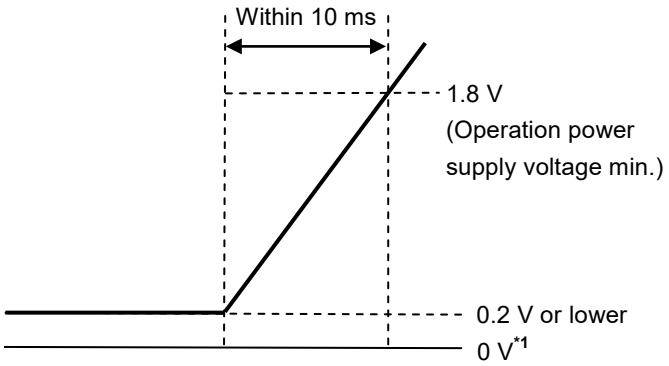


Figure 11 Output Timing of Handshake Time-out (CMOS Output)

■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 12**.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

Figure 12 How to Raise the Power Supply Voltage

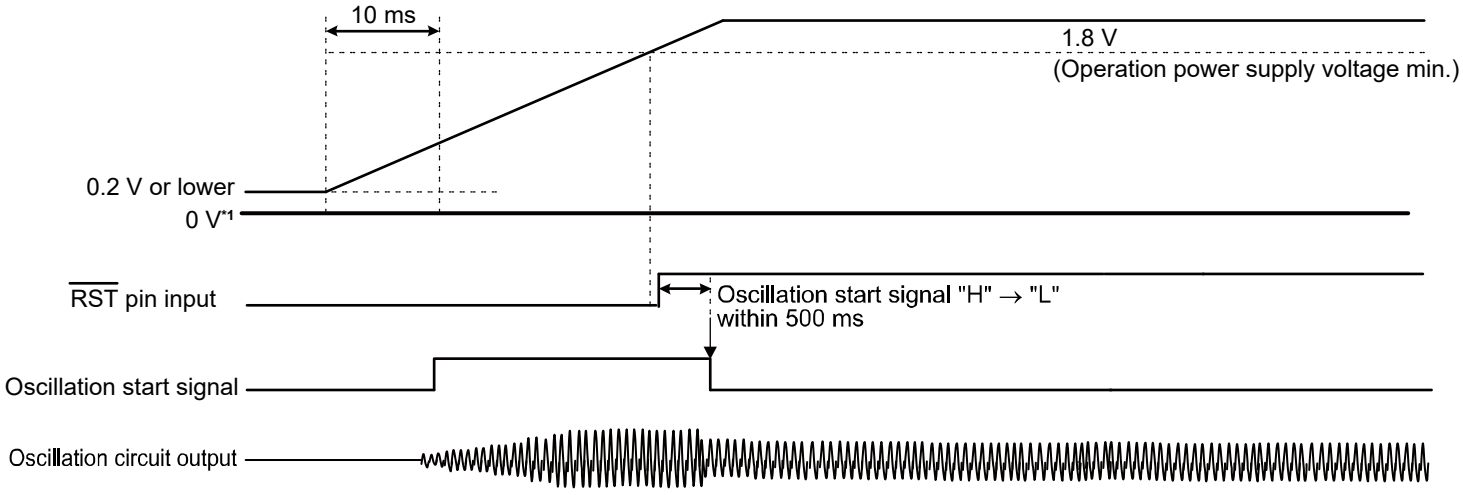
If the power supply voltage of the S-35720 Series cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start*1. In such case, perform the operations shown in "**1. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "L"** " and "**2. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "H"** ".

***1.** When one-shot loop time-out or handshake time-out is selected as the option.

1. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "L"

Set the $\overline{\text{RST}}$ pin to "L" until the power supply voltage reaches 1.8 V or higher. While the $\overline{\text{RST}}$ pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the $\overline{\text{RST}}$ pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.
The current consumption increases as mentioned below while the $\overline{\text{RST}}$ pin is set to "L".

- When a product without a pull-up resistor is selected: 1.7 μA typ.
- When a product with a pull-up resistor is selected: 30 μA typ.



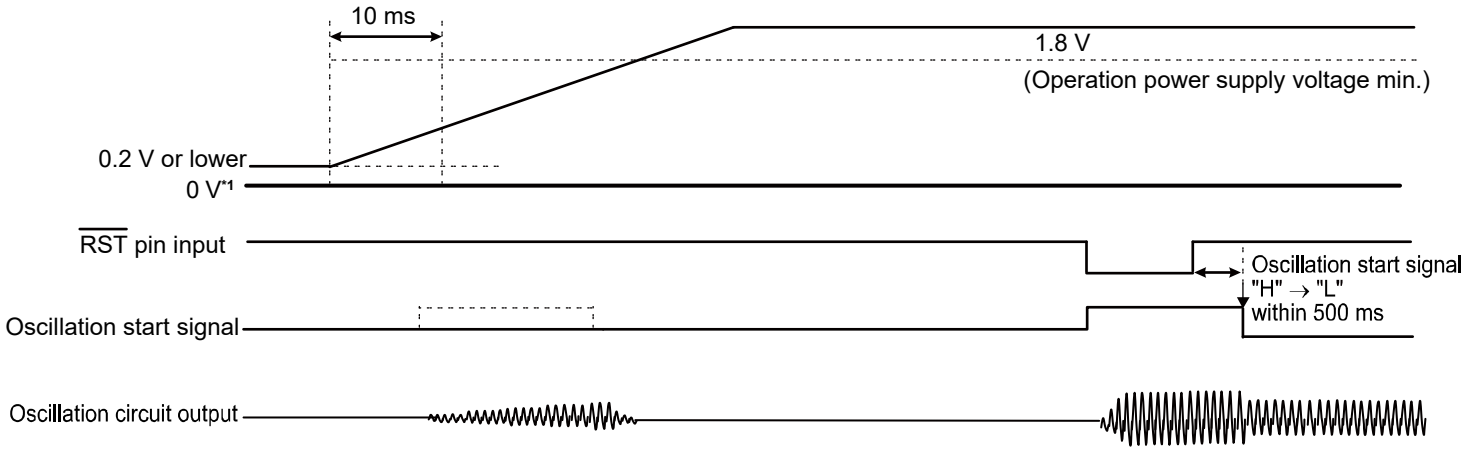
***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

Figure 13 When Power Supply Voltage is Raised at $\overline{\text{RST}}$ Pin = "L"

2. When power supply voltage is raised at $\overline{RST}$ pin = "H"

Set the $\overline{RST}$ pin to "L" after the power supply voltage reaches 1.8 V or higher. If the $\overline{RST}$ pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the $\overline{RST}$ pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained. The current consumption increases as mentioned below while the $\overline{RST}$ pin is set to "L".

- When a product without a pull-up resistor is selected: 1.7 μA typ.
- When a product with a pull-up resistor is selected: 30 μA typ.



***1.** 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

Figure 14 When Power Supply Voltage is Raised at $\overline{RST}$ Pin = "H"

The $\overline{RST}$ pin has a built-in chattering elimination circuit.
Regarding the chattering elimination of the $\overline{RST}$ pin, refer to "■ **Chattering Elimination of $\overline{RST}$ Pin**".

■ Chattering Elimination of $\overline{\text{RST}}$ Pin

The $\overline{\text{RST}}$ pin has a built-in chattering elimination circuit, and the output logic is active "L".
Sampling is carried out 3 times at a clock period of 8 Hz and the $\overline{\text{RST}}$ pin input signal is verified. If all of the sampling results are "L", the counter is reset, if all the results are "H", a count-up action is started.
The chattering elimination circuit can eliminate the pulse width of 2 periods (approximately 0.25 seconds) of the clock (8 Hz). To determine the $\overline{\text{RST}}$ pin "L" or "H" input, maintain the $\overline{\text{RST}}$ pin "L" or "H" input during the period longer than 3.5 periods (0.438 seconds) of clock (8 Hz). This is because, for example, if the $\overline{\text{RST}}$ pin "L" or "H" input is 0.375 seconds, the input may not be determined depending on the clock timing.

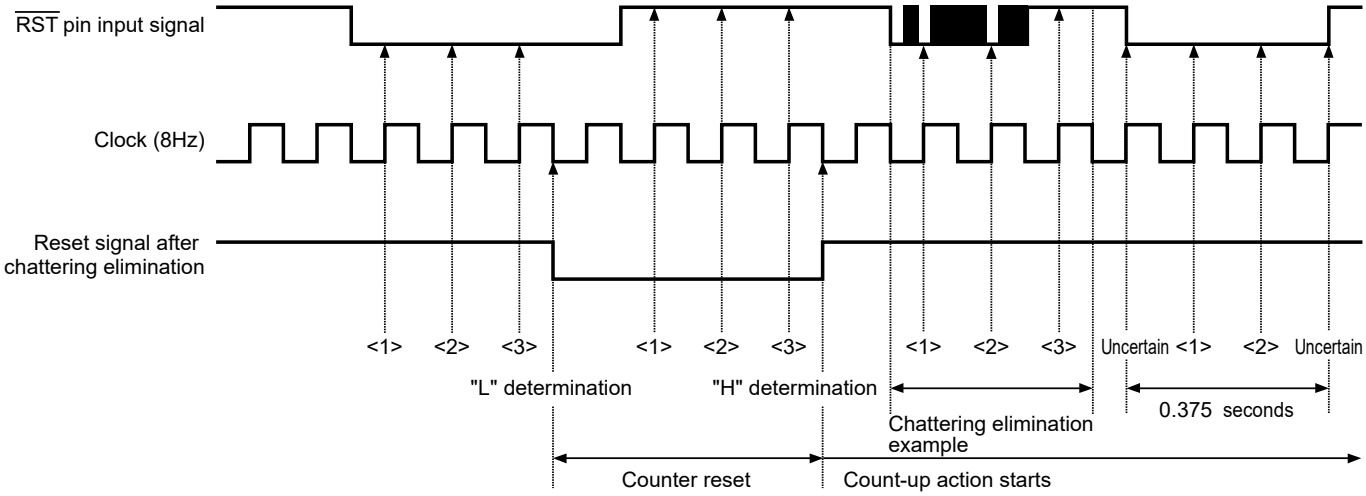
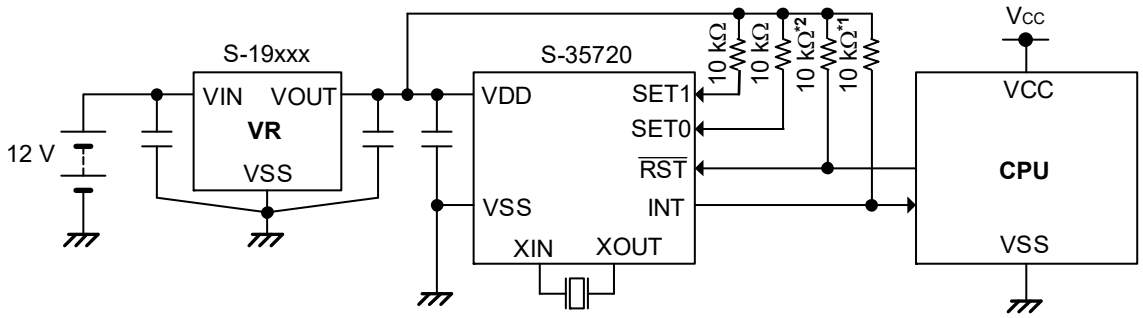


Figure 15 Example: Timing Chart of Chattering Elimination

■ Examples of Application Circuit



***1.** This resistor is unnecessary when a CMOS output product is selected.
***2.** This resistor is unnecessary when a product with a pull-up resistor is selected.

Figure 16

Caution **The above connection diagram does not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.**

■ Configuration of Crystal Oscillation Circuit

Since the S-35720 Series has built-in capacitors (C_g and C_d), adjustment of oscillation frequency is unnecessary. However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance (C_P), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35720 Series.
- Place the S-35720 Series and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.
  (In the case of a multi-layer board, only the layer farthest from the crystal oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

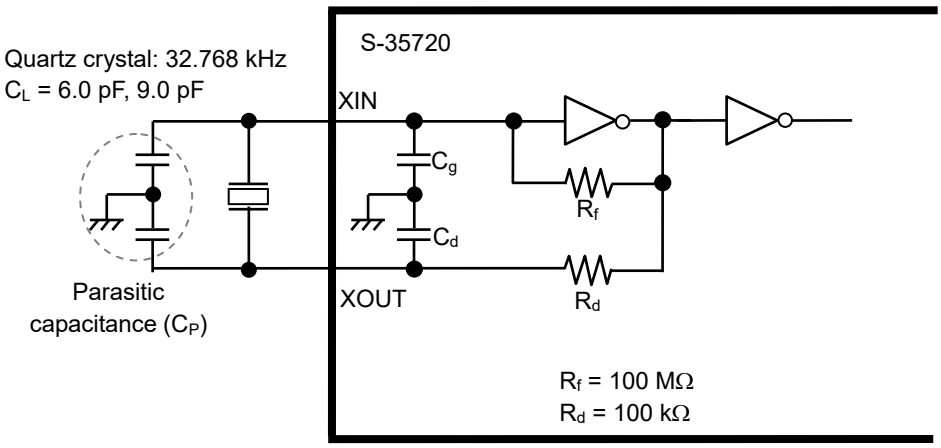


Figure 17 Configuration of Crystal Oscillation Circuit

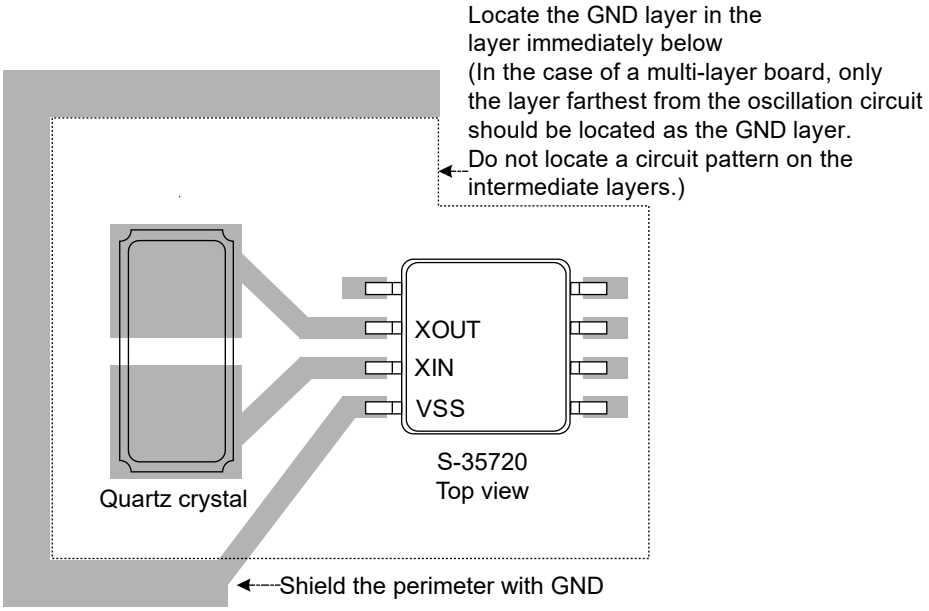


Figure 18 Example of Recommended Connection Pattern Diagram

Caution 1. Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal, and external capacitor. When configuring crystal oscillation circuit, pay sufficient attention for them.

2. When using the product in automobile equipment, select the components which can be automobile carried for each component such as quartz crystal, external capacitor, and board.

■ Cautions When Using Quartz Crystal

Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.
Refer to **Table 8** for recommended quartz crystal characteristics values. When using the product in an environment over Ta = +85°C, it is recommended to ensure the oscillation allowance shown in **Table 8** at room temperature.

Table 8 Quartz Crystal Characteristics

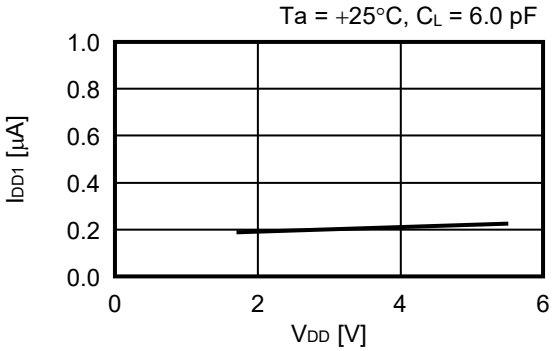
Quartz Crystal C_L Value (Load Capacitance)	R_1 Value (Equivalent Series Resistance)	Oscillation Allowance at Power-on
9.0 pF	80 kΩ max.	5 times or more
6.0 pF	80 kΩ max.	5 times or more

■ Precautions

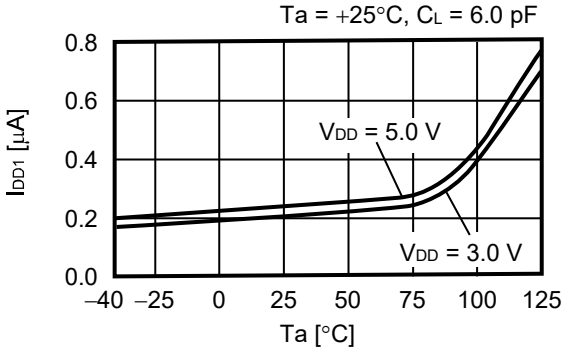
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

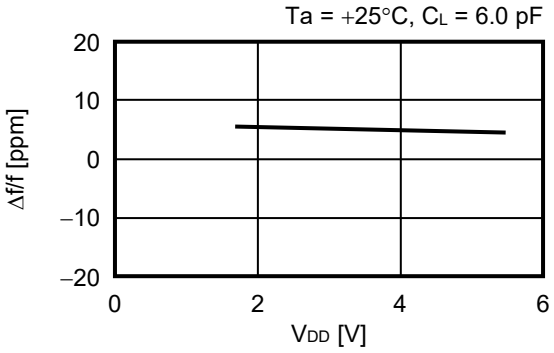
1. Current consumption 1 vs. Power supply voltage characteristics



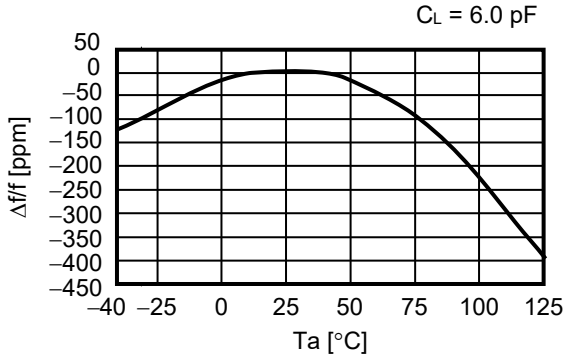
2. Current consumption 1 vs. Temperature characteristics



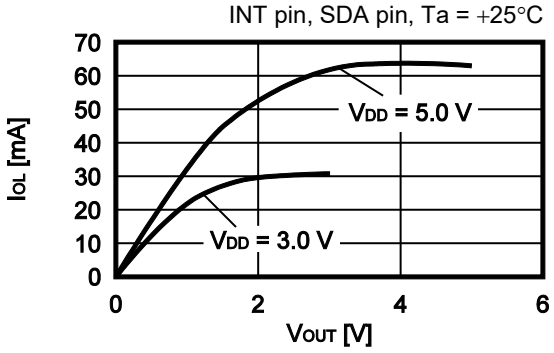
3. Oscillation frequency vs. Power supply voltage characteristics



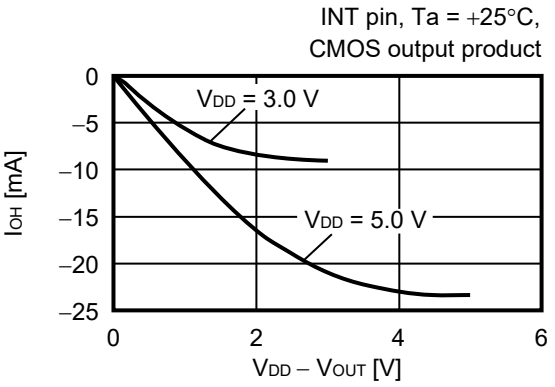
4. Oscillation frequency vs. Temperature characteristics



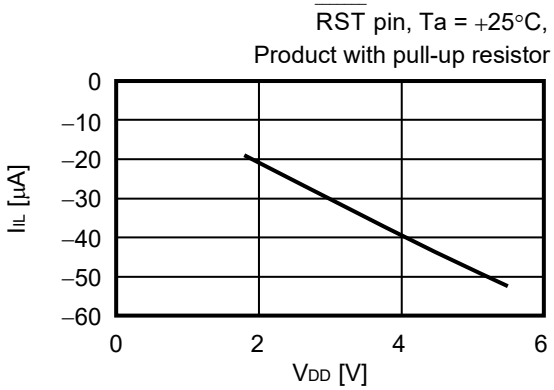
5. Low level output current vs. Output voltage characteristics

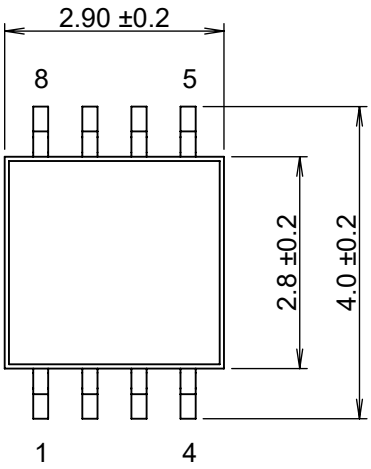


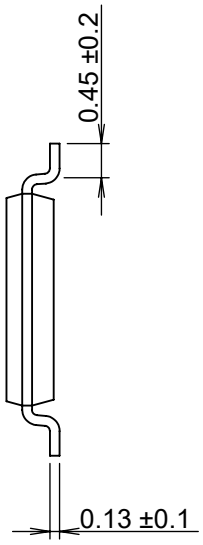
6. High level output current vs. V_{DD} – V_{OUT} characteristics

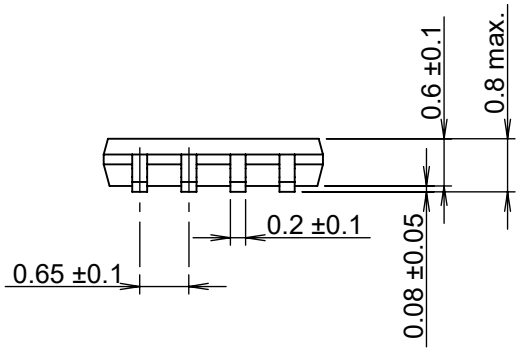


7. Low level input current vs. Power supply voltage characteristics



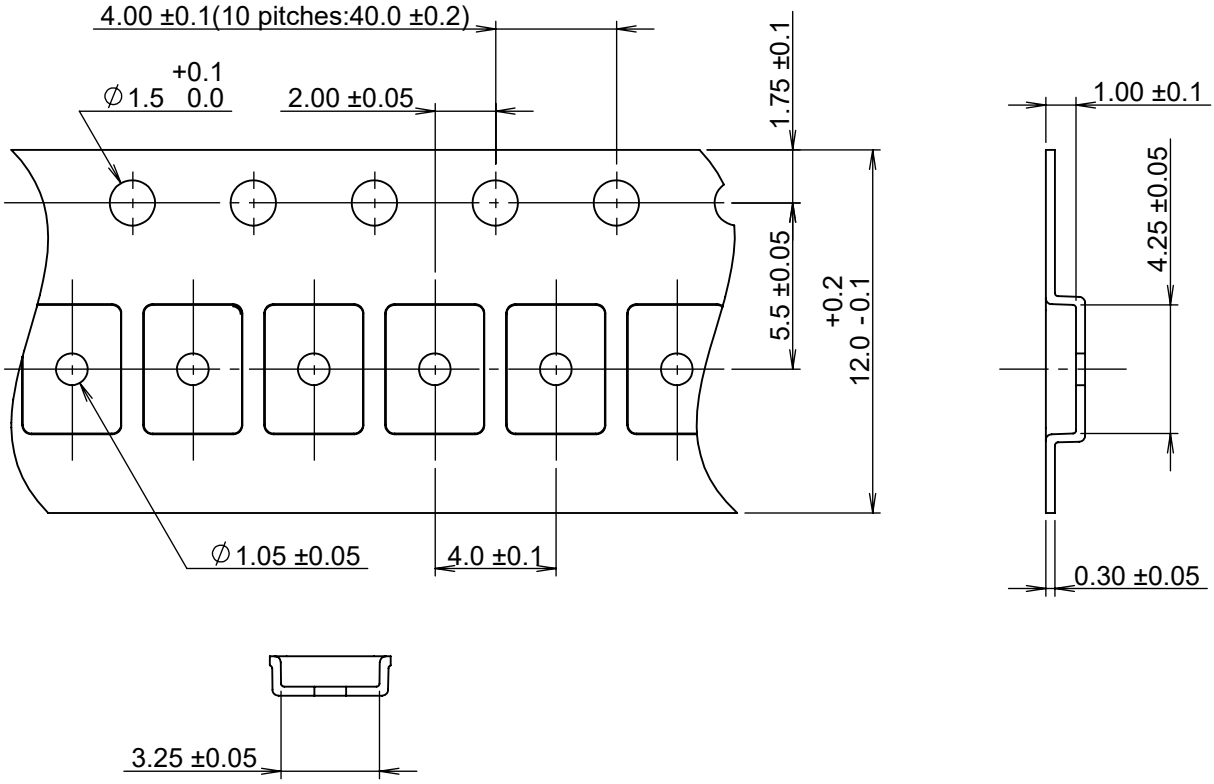


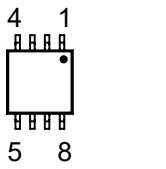


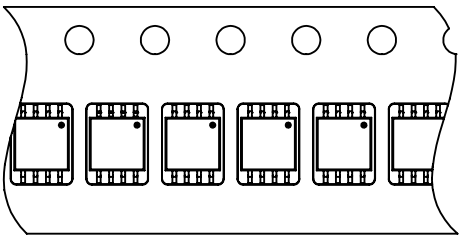


No.FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



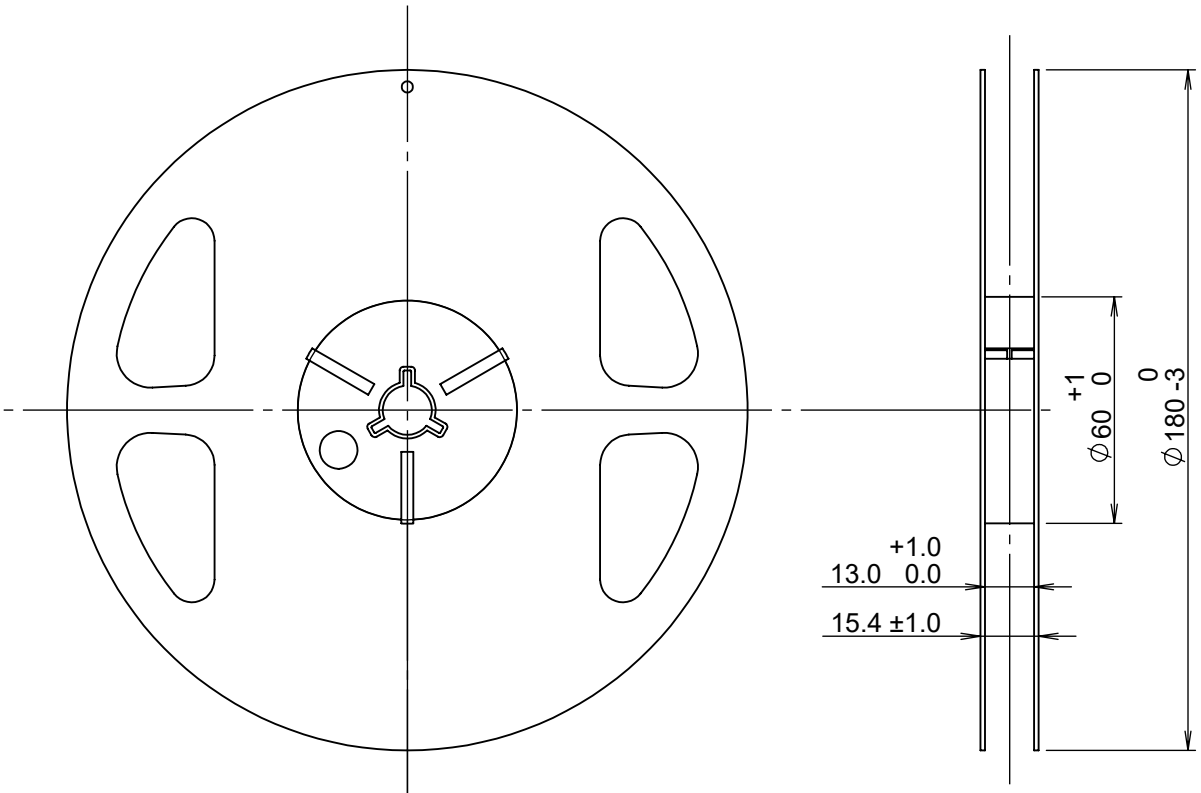




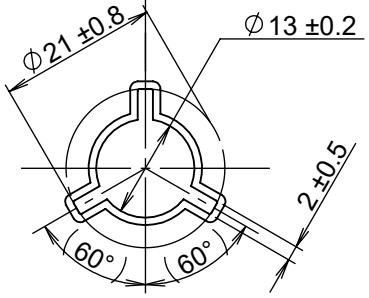
Feed direction

No. FM008-A-C-SD-3.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-3.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-2.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07