

MOSFET – N-Channel, QFET

400 V, 4.5 A, 1.0 mΩ**FQD6N40C****Description**

This N-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 4.5 A, 400 V, $R_{DS(on)}$ = 1.0 mΩ (Max.) @ V_{GS} = 10 V, I_D = 2.25 A
- Low Gate Charge (Typ. 16 nC)
- Low C_{RSS} (Typ. 15 pF)
- 100% Avalanche Tested

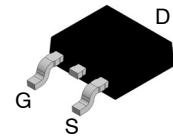
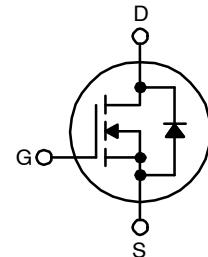
ABSOLUTE MAXIMUM RATINGS $(T_C = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-Source Voltage		400	V
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$)	4.5	A
		– Continuous ($T_C = 100^\circ\text{C}$)	2.7	A
I_{DM}	Drain Current	– Pulsed (Note 1)	18	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		270	mJ
I_{AR}	Avalanche Current (Note 1)		4.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		4.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W	
	Power Dissipation ($T_C = 25^\circ\text{C}$)	48	W	
	– Derate Above 25°C	0.38	W/ $^\circ\text{C}$	
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150	$^\circ\text{C}$	
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case, Max.	2.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

DPAK3 (TO-252 3 LD)
CASE 369AS

N-Channel MOSFET

MARKING DIAGRAM

&Z&3&K
FQD
6N40C
○

&Z = Assembly Plant Code
&3 = 3-Digit Date Code (Year and Week)
&K = 2-Digits Lot Run Traceability Code
FQD6N40C = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FQD6N40C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	400	–	–	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	–	0.54	–	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 400 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	–	–	1	μA
		$V_{\text{DS}} = 320 \text{ V}$, $T_C = 125^\circ\text{C}$	–	–	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -30 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	–	–	-100	nA
ON CHARACTERISTICS						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 250 \mu\text{A}$	2.0	–	4.0	V
$R_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 2.25 \text{ A}$	–	0.83	1	Ω
g_{FS}	Forward Transconductance	$V_{\text{DS}} = 40 \text{ V}$, $I_D = 2.25 \text{ A}$	–	4.7	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$, $f = 1.0 \text{ MHz}$	–	480	625	pF
C_{oss}	Output Capacitance		–	80	105	pF
C_{rss}	Reverse Transfer Capacitance		–	15	20	pF
SWITCHING CHARACTERISTICS						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}} = 200 \text{ V}$, $I_D = 6 \text{ A}$, $R_G = 25 \Omega$ (Note 4)	–	13	35	ns
t_r	Turn-On Rise Time		–	65	140	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		–	21	55	ns
t_f	Turn-Off Fall Time		–	38	85	ns
Q_g	Total Gate Charge	$V_{\text{DS}} = 320 \text{ V}$, $I_D = 6 \text{ A}$, $V_{\text{GS}} = 10 \text{ V}$ (Note 4)	–	16	20	nC
Q_{gs}	Gate-Source Charge		–	2.3	–	nC
Q_{gd}	Gate-Drain Charge		–	8.2	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

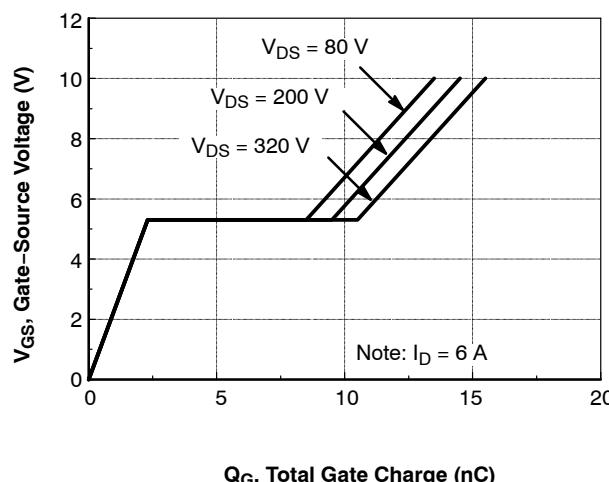
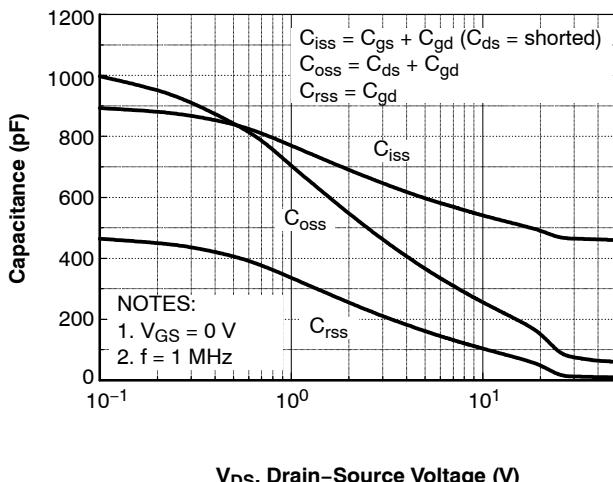
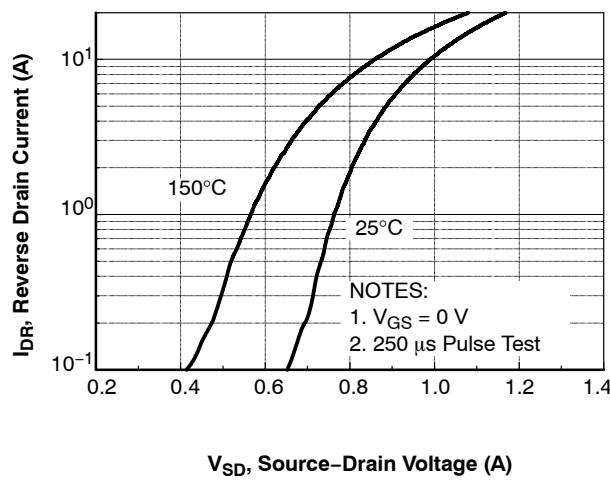
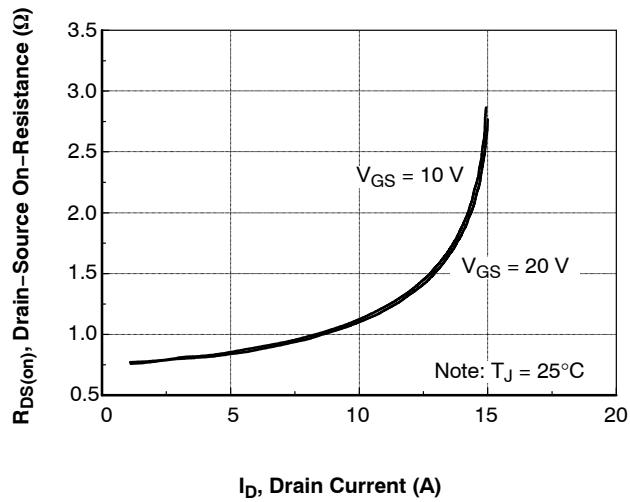
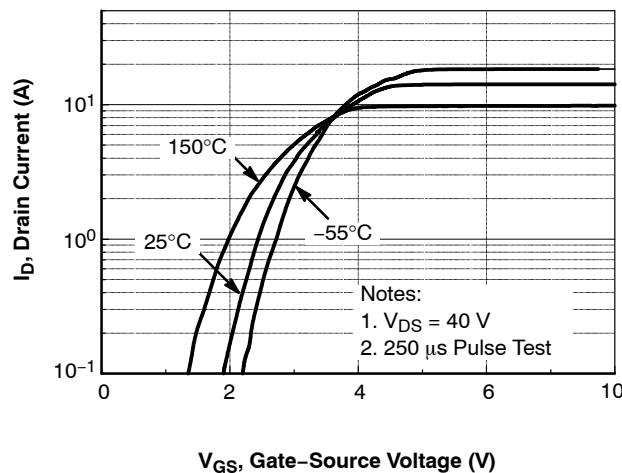
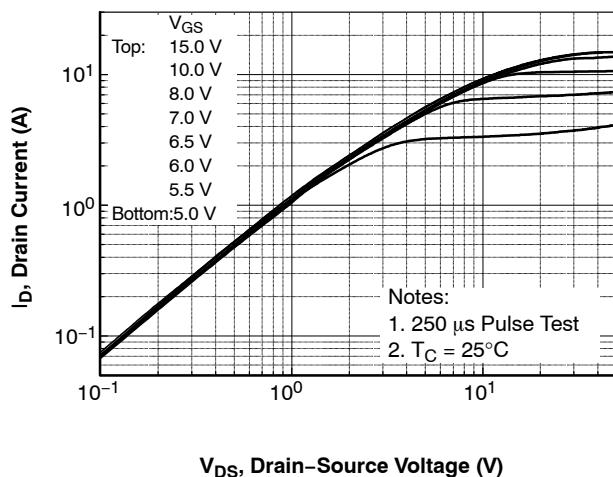
I_S	Maximum Continuous Drain-Source Diode Forward Current	–	–	4.5	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	–	–	18	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 4.5 \text{ A}$	–	–	1.4	V
t_{rr}	Reverse Recovery Time	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 6 \text{ A}$, $dI_F / dt = 100 \text{ A}/\mu\text{s}$	–	230	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.7	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2. $L = 13.7 \text{ mH}$, $I_{\text{AS}} = 6 \text{ A}$, $V_{\text{DD}} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{\text{SD}} \leq 6 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

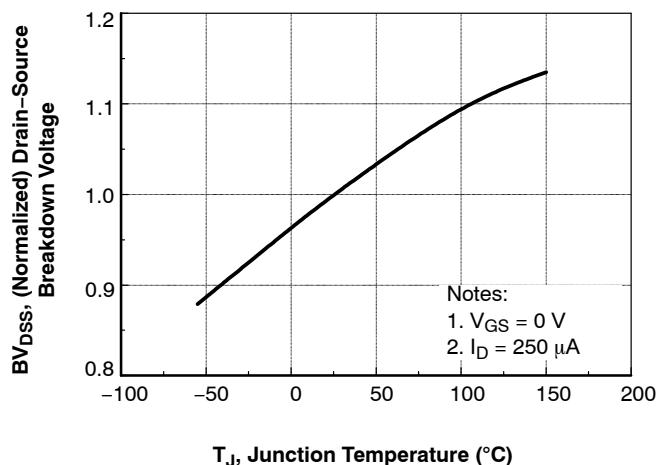


Figure 7. Breakdown Voltage Variation vs. Temperature

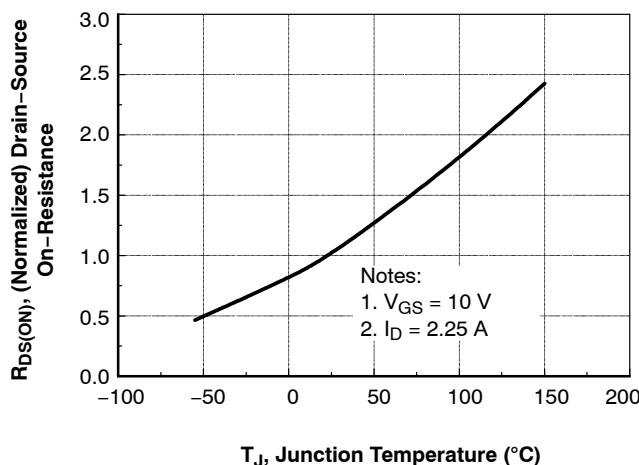


Figure 8. On-Resistance Variation vs. Temperature

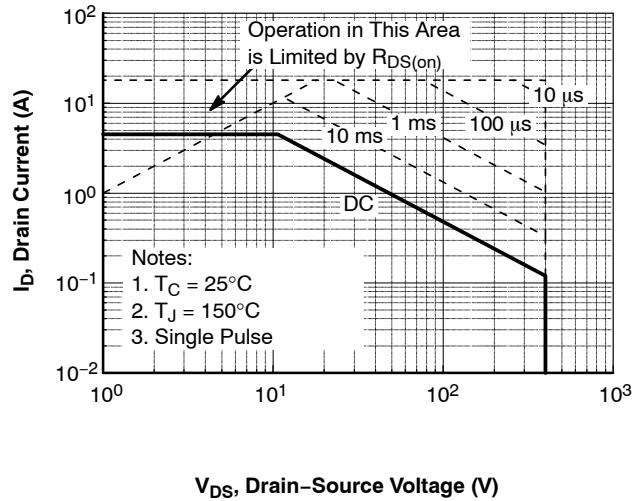


Figure 9. Maximum Safe Operating Area

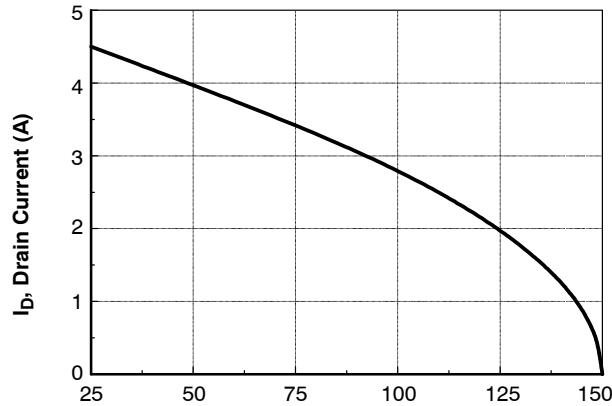


Figure 10. Maximum Drain Current vs. Case Temperature

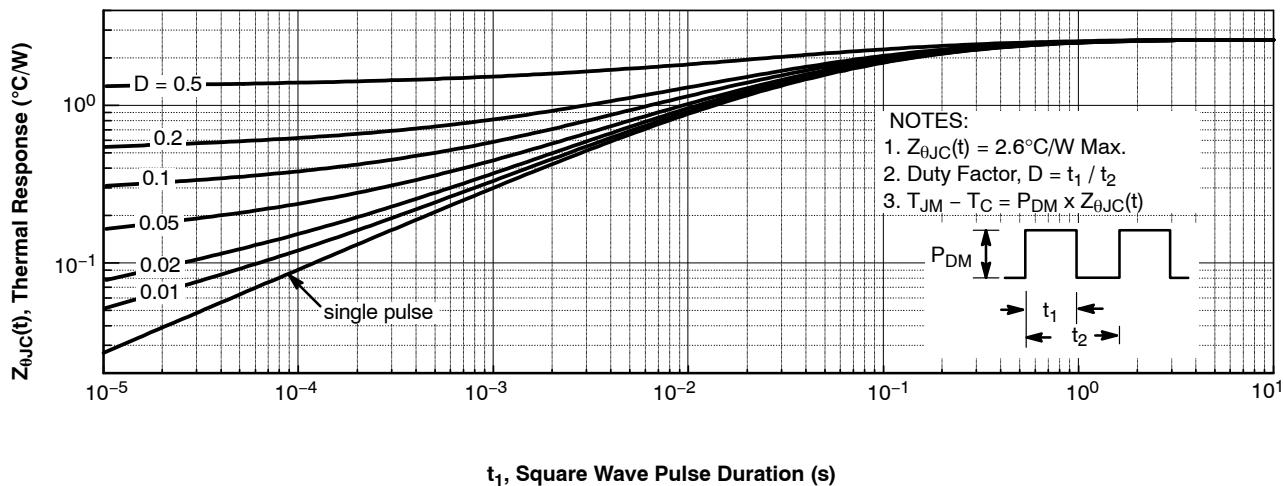


Figure 11. Transient Thermal Response Curve

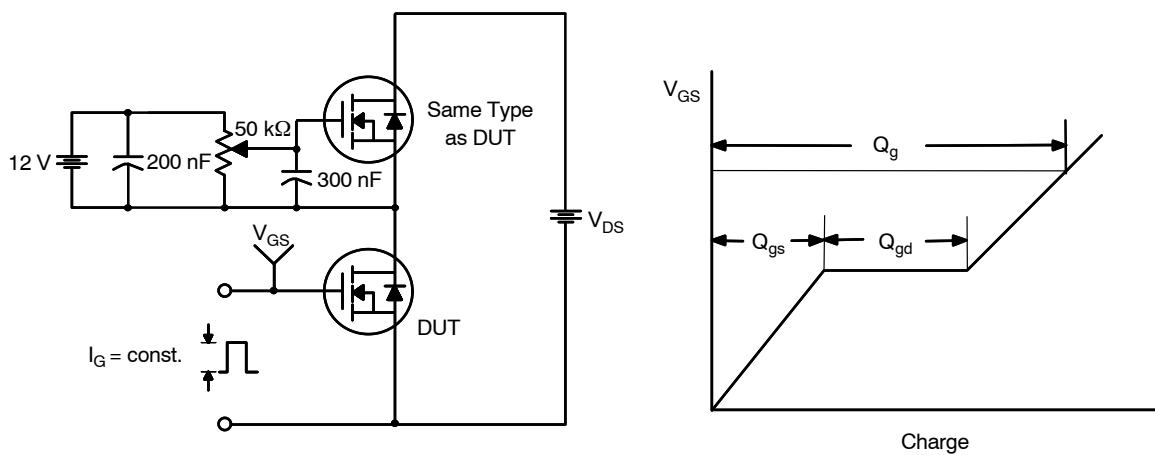


Figure 12. Gate Charge Test Circuit & Waveform

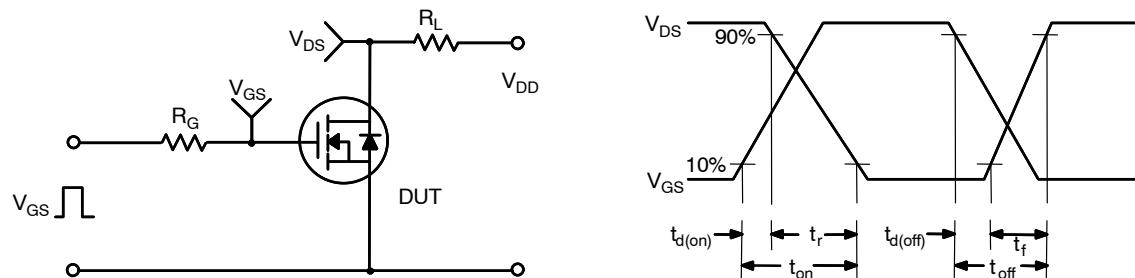


Figure 13. Resistive Switching Test Circuit & Waveforms

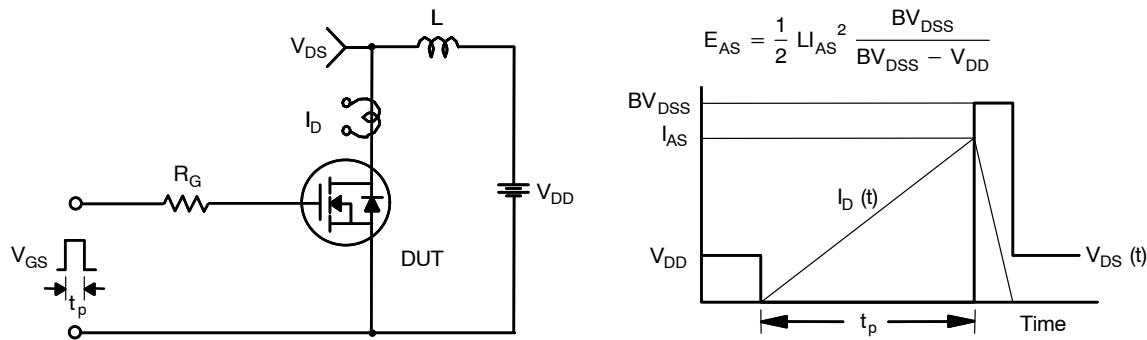


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FQD6N40C

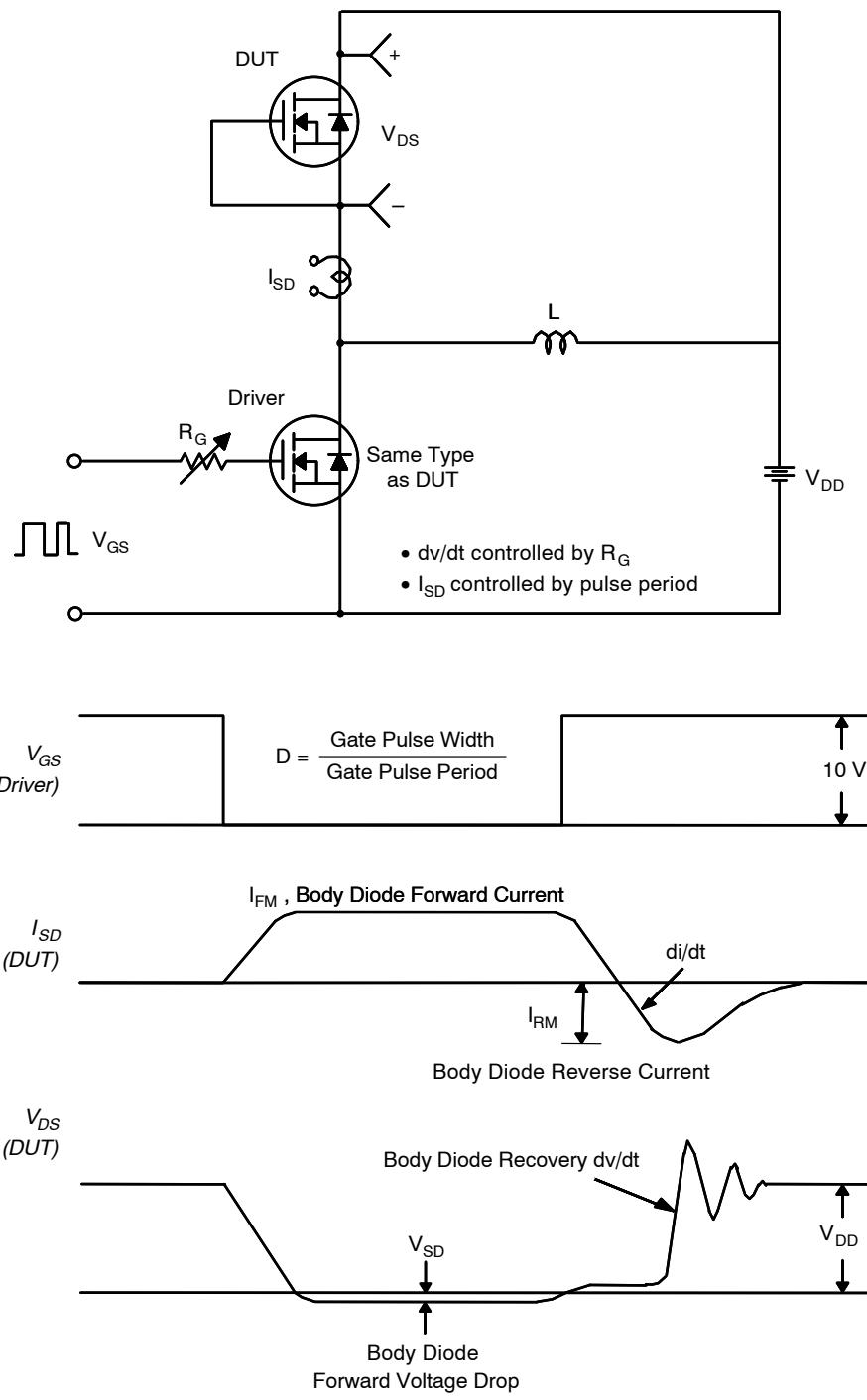
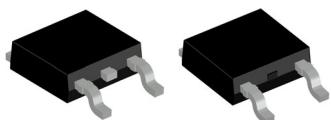


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

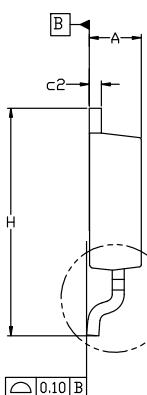
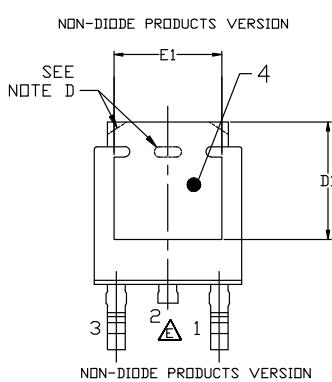
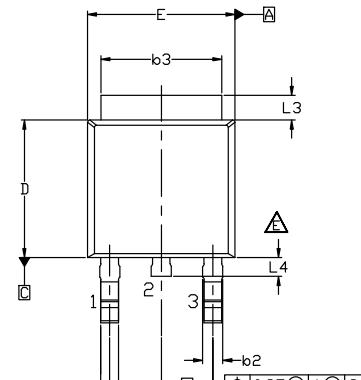
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FQD6N40CTM	FQD6N40C	DPAK3 (TO-252 3 LD)	330 mm	16 mm	2,500 / Tape & Reel

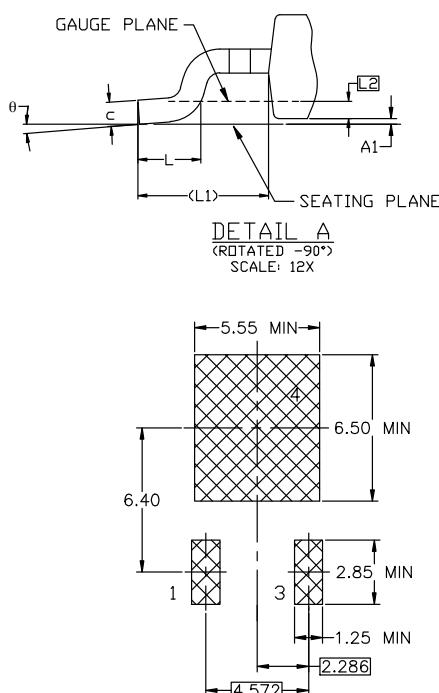
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TD-252,
ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY
STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD
TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	—	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286	BSC	
e1	4.572	BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	—	10°

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

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DESCRIPTION:	DPAK3 6.10x6.54x2.29, 4.57P	PAGE 1 OF 1

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