

N-Channel Power MOSFET

600V, 4.0A, 2.5Ω

FEATURES

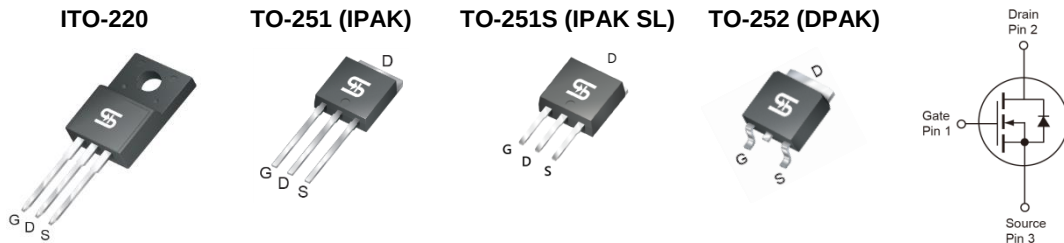
- 100% Avalanche Tested
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	2.5	Ω
Q_g	14.5	nC

APPLICATION

- Power Supply
- Lighting



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	UNIT
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current ^(Note 1)	I_D	4.0		A
		2.4		
Pulsed Drain Current ^(Note 2)	I_{DM}	16		A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	50	25	W
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	70		mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	4		A
Repetitive Avalanche Energy ^(Note 2)	E_{AR}	5		mJ
Peak Diode Recovery ^(Note 4)	dV/dt	4.5		V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	IPAK/DPAK	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.5	5	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	83	62.5	°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 5)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	600	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2.5	3.5	4.5	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V	I _{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 2.0A	R _{DS(on)}	--	2.2	2.5	Ω
Forward Transfer Conductance	V _{DS} = 40V, I _D = 2A	g _{fs}	--	2.6	--	S
Dynamic ^(Note 6)						
Total Gate Charge	V _{DS} = 480V, I _D = 4.0A, V _{GS} = 10V	Q _g	--	14.5	--	nC
Gate-Source Charge		Q _{gs}	--	3.4	--	
Gate-Drain Charge		Q _{gd}	--	7	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	500	--	pF
Output Capacitance		C _{oss}	--	53.2	--	
Reverse Transfer Capacitance		C _{rss}	--	7	--	
Switching ^(Note 7)						
Turn-On Delay Time	V _{DD} = 300V, R _{GEN} = 25Ω, I _D = 4.0A, V _{GS} = 10V,	t _{d(on)}	--	11	--	ns
Turn-On Rise Time		t _r	--	20	--	
Turn-Off Delay Time		t _{d(off)}	--	30	--	
Turn-Off Fall Time		t _f	--	19	--	
Source-Drain Diode ^(Note 5)						
Forward On Voltage	I _S = 4.0A, V _{GS} = 0V	V _{SD}	--	--	1.13	V
Reverse Recovery Time	V _{GS} =0V, I _S = 2A dI _F /dt = 100A/μs	t _{rr}	--	522	--	ns
Reverse Recovery Charge		Q _{rr}	--	1.6	--	μC
Source Current	Integral reverse diode in the MOSFET	I _S	--	--	4	A
Source Current (Pulse)		I _{SM}	--	--	16	A

Notes:

- Current limited by package.
- Pulse width limited by the maximum junction temperature.
- $L = 8mH, I_{AS} = 4.0A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
100% Eas Test Condition: $L = 8mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
- $I_{SD} \leq 4A, dI/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
- Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
- For DESIGN AID ONLY, not subject to production testing.
- Switching time is essentially independent of operating temperature.

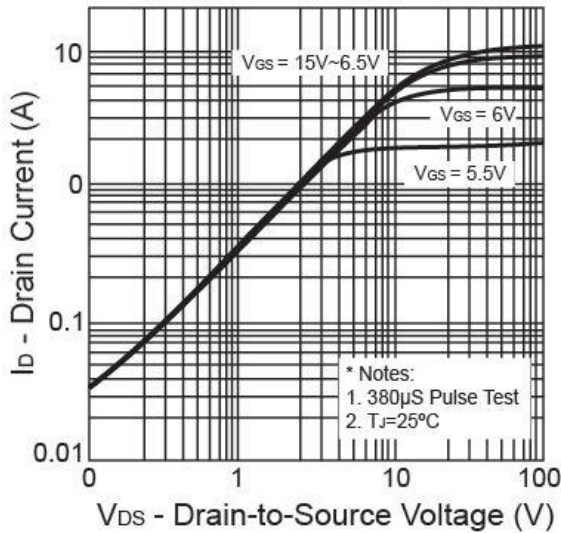
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM4NB60CI C0G	ITO-220	50pcs / Tube
TSM4NB60CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM4NB60CH X0G	TO-251S (IPAK SL)	75pcs / Tube
TSM4NB60CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

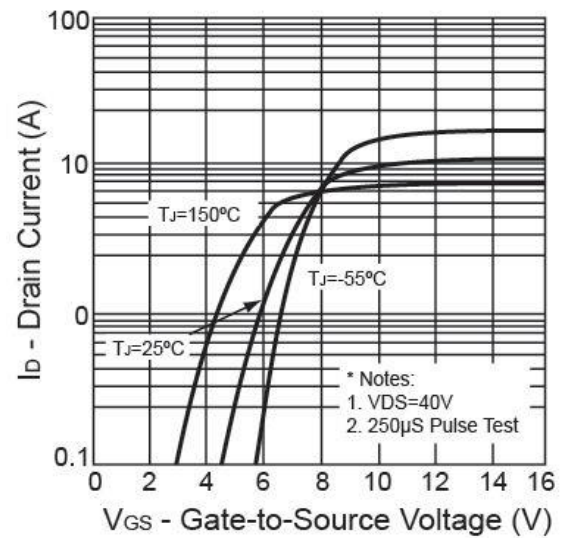
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

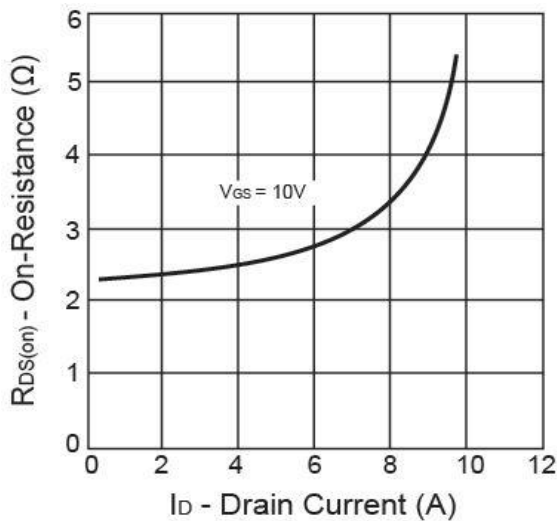
Output Characteristics



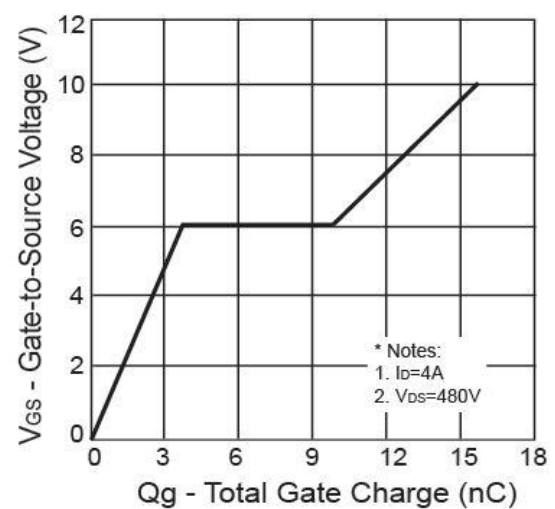
Transfer Characteristics



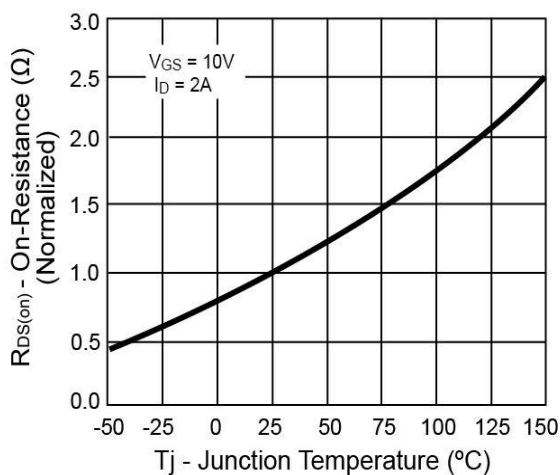
On-Resistance vs. Drain Current



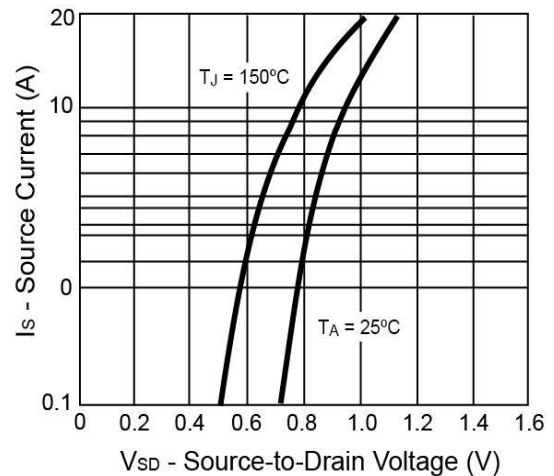
Gate Charge



On-Resistance vs. Junction Temperature



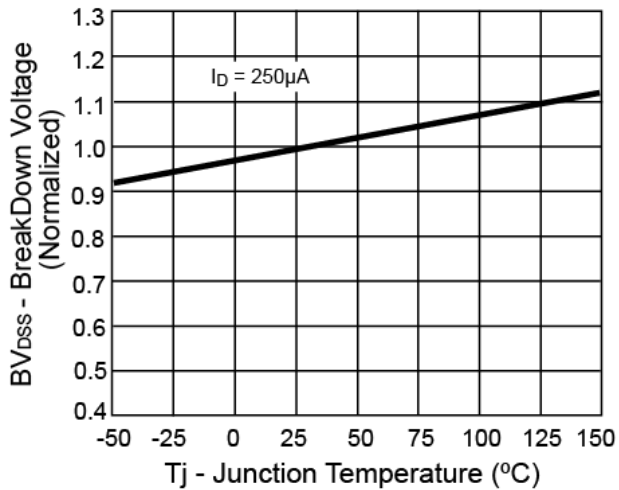
Source-Drain Diode Forward Voltage



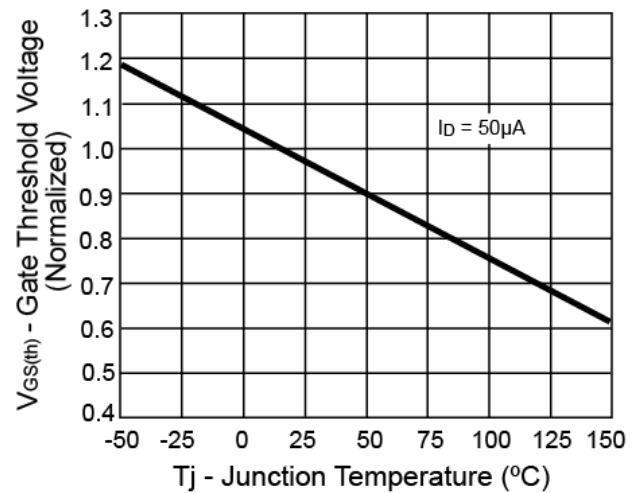
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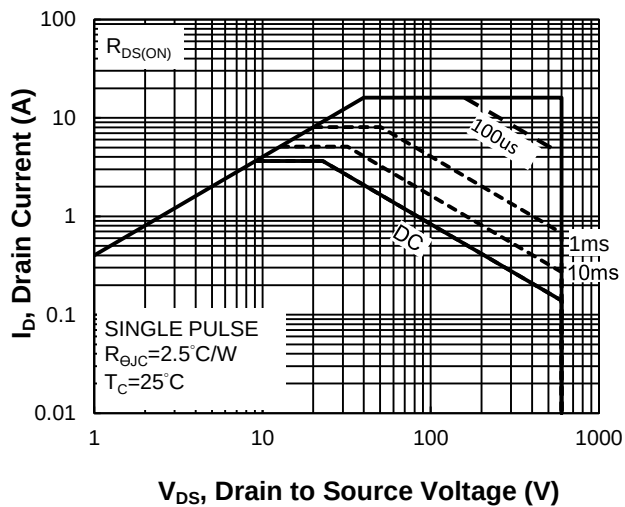
Breakdown Voltage vs. Temperature



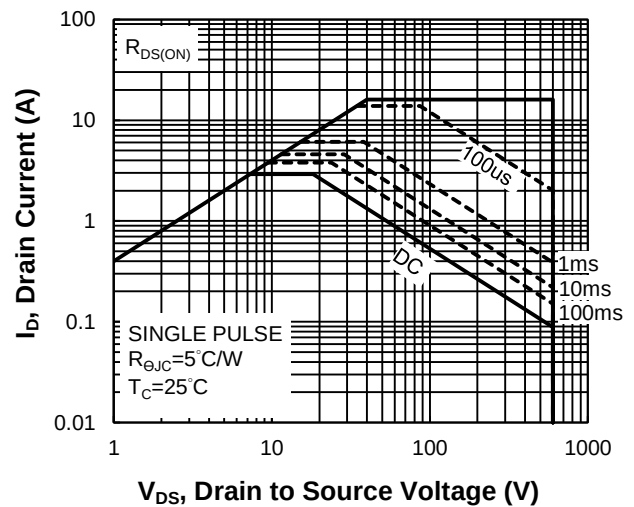
Threshold Voltage vs. Temperature



Maximum Safe Operating Area (IPAK/DPAK)

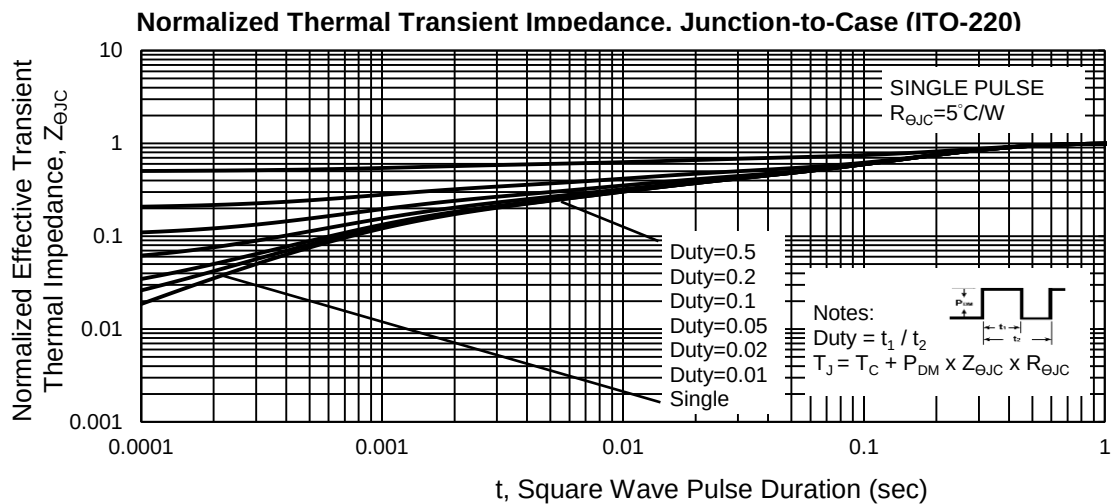
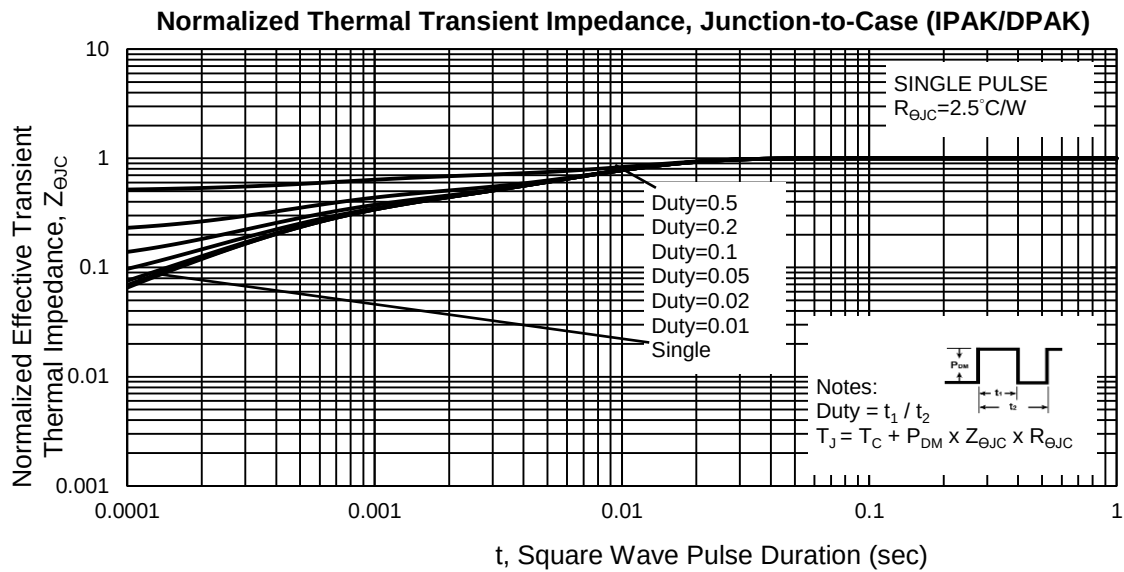


Maximum Safe Operating Area (ITO-220)

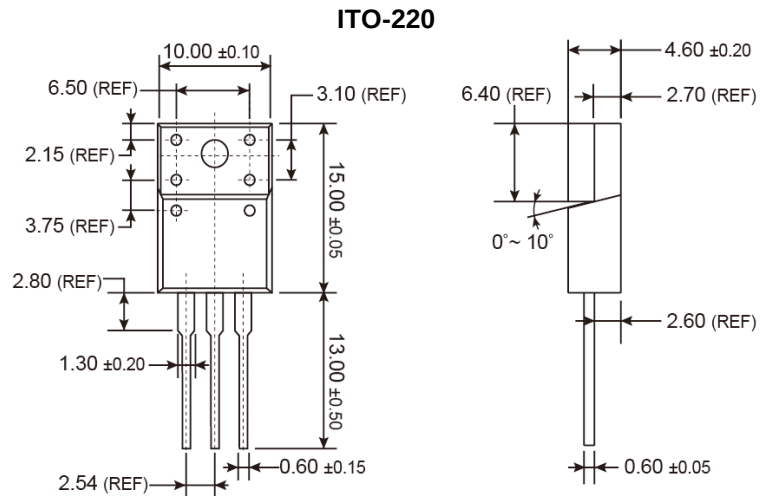


ELECTRICAL CHARACTERISTICS CURVES

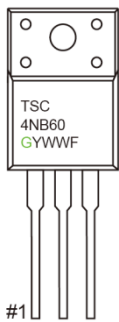
($T_C = 25^\circ\text{C}$ unless otherwise noted)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

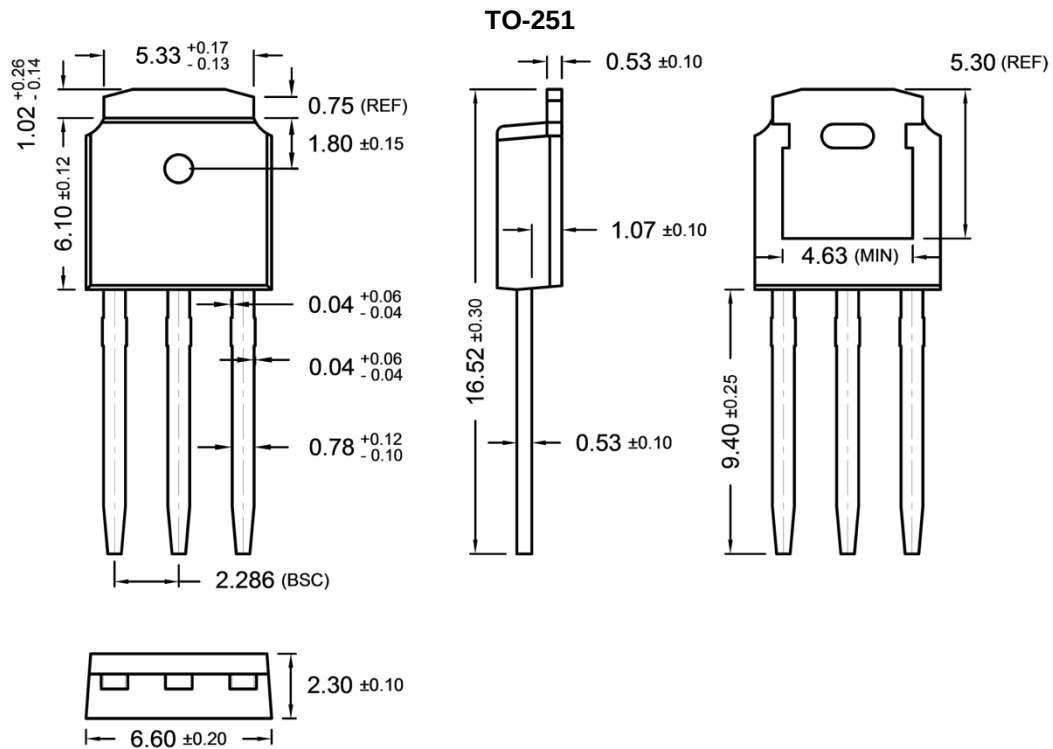


MARKING DIAGRAM

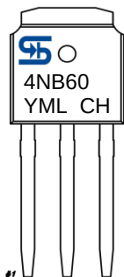


- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

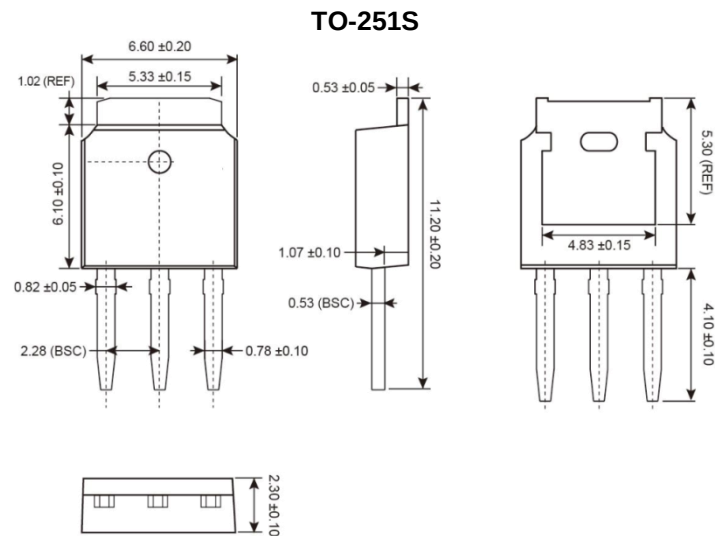


MARKING DIAGRAM

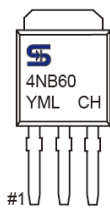


Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



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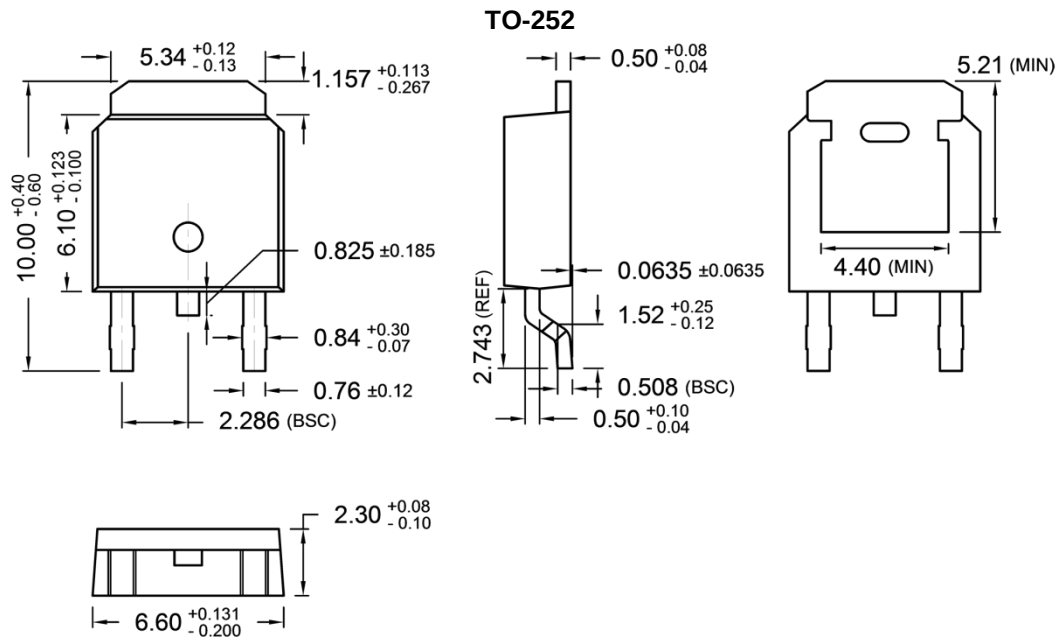
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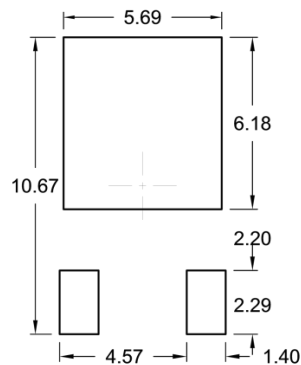
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PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



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