EiceDRIVER™ 2EDBx259K

Dual-channel isolated gate-driver ICs in LGA package

Description

EiceDRIVER™ 2EDBx259K is a family of dual-channel isolated gate driver ICs designed to drive Si MOSFETs. 2EDBx259K is available in a 13-pin LGA package with 3.4 mm input-to-output creepage and provide basic isolation by means of on-chip coreless transformer (CT) technology.

2EDBx259K offers optional shoot-through protection (STP) and dead-time control (DTC) functionality; this allows the operation as dual-channel low-side, dual-channel high-side or half-bridge gate driver with a configurable dead-time. With an excellent common-mode transient immunity (CMTI), low part-to-part skew and fast signal propagation, the products are best suited for use in fast-switching power conversion systems.

Features

- 2-channel isolated gate driver for Si MOSFETs
- 38 ns fast input-to-output propagation with excellent stability (+9/-5 ns)
- 5 A/9 A source/sink capability
- 1.2 V output clamping threshold
- < 2 µs fast UVLO recovery time
- 4 V and 8 V VDDA/B UVLO options
- > 150 V/ns CMTI
- Available in 13-pin LGA 5×5

Isolation and safety certificates

- UL1577 with V_{ISO} = 2500 V_{RMS} (*certification n. E311313*)
- CSA Component acceptance service notice no. 5A
- GB 4943.1-2022 (*certification n. CQC24001456819*)
- IEC 62368-1 (*certification n. CN70550-A1*)

Table 1 Portfolio

Part number	UVLO	V_{ISO}	Package
2EDB7259K	4 V	2.5 kV_{rms}	LGA 5×5
2EDB8259K	8 V	2.5 kV_{rms}	LGA 5×5

Potential applications

- Server, telecom SMPS
- EV off-board chargers
- Low voltage drives and power tools
- Solar micro inverter, solar optimizer
- Industrial power supply (SMPS, residential UPS)



Product validation

Fully qualified for industrial applications

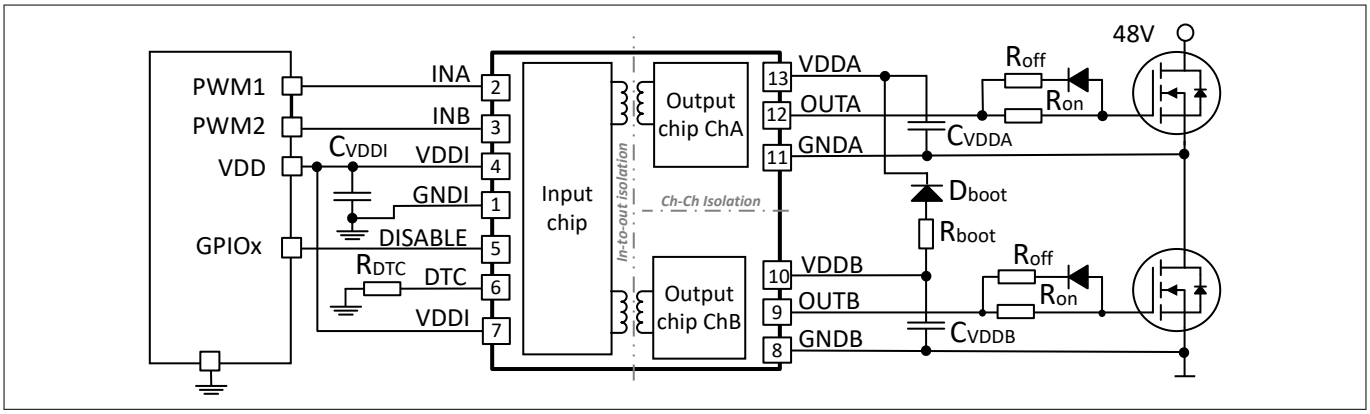


Figure 1 Application diagram

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Table of contents

Table of contents . . . 2
1 Pin configuration and description . . . 3
2 Functional description . . . 4
2.1 Block diagram . . . 4
2.2 Power supply and Undervoltage Lockout (UVLO) . . . 4
2.2.1 Input supply voltage . . . 4
2.2.2 Output supply voltage . . . 4
2.3 Input stage - INA, INB, DISABLE . . . 5
2.4 Shoot-through protection and configurable dead-time - STP/DTC . . . 6
2.5 Gate driver outputs . . . 7
2.6 Fast active output clamping in UVLO conditions . . . 7
2.7 CT communication and input to output data transmission . . . 7
3 Electrical characteristics . . . 8
3.1 Absolute maximum ratings . . . 8
3.2 Thermal characteristics . . . 9
3.3 Operating range . . . 10
3.4 Electrical characteristics . . . 10
3.5 Isolation specifications . . . 15
4 Timing diagrams . . . 17
5 Typical characteristics . . . 20
6 Package outline dimensions . . . 26
6.1 Device numbers and markings . . . 26
6.2 Package LGA5x5 . . . 26
7 Revision history . . . 29
Disclaimer . . . 30

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1 Pin configuration and description

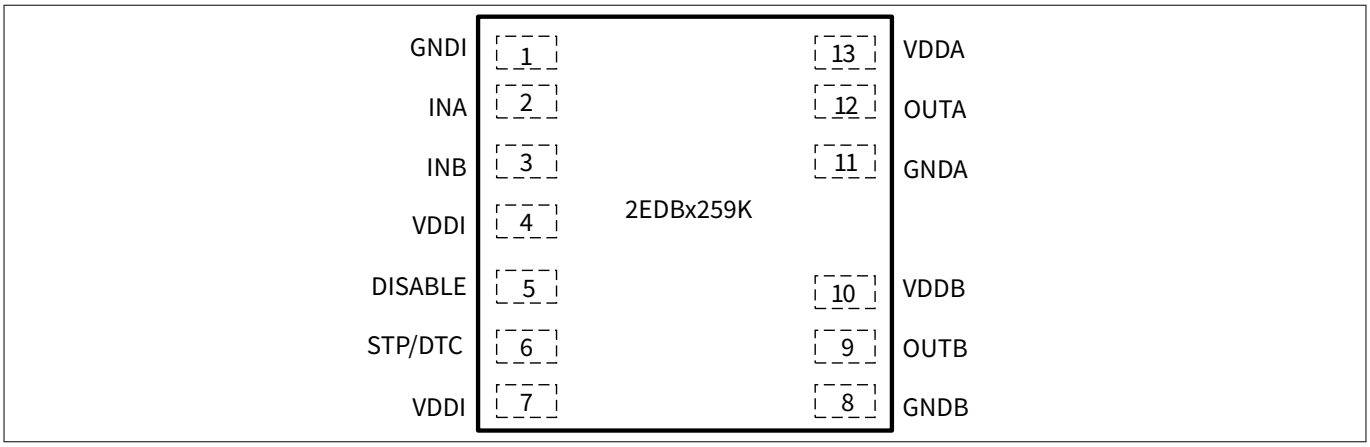


Figure 2 Pin configuration (top side view)

Table 2 Pin description

Pin	Symbol	Description
1	GNDI	**Ground primary-side**
2	INA	**Input signal channel A** Logic input with TTL compatible thresholds and internal pull-down resistor
3	INB	**Input signal channel B** Logic input with TTL compatible thresholds and internal pull-down resistor
4,7	VDDI	**Input-side supply voltage** (operating range: 3 V to 17 V)
5	DISABLE	**Disable input channel A and B** (active high) If DISABLE is low or left open, OUTA/OUTB are controlled by INA/INB DISABLE high causes OUTA/OUTB low
6	STP/DTC	**Shoot-through Protection (STP) and Dead-Time Control (DTC)** If STP/DTC is high or left open, OUTA and OUTB can overlap (SPT and DTC disabled). If STP/DTC is connected to GNDI with a resistance R_{DTC}, OUTA and OUTB cannot overlap and a “safe dead-time” can be configured: t_{dt} [ns] = 10 x R_{DTC} [kΩ] If STP/DTC is connected to GNDI, OUTA and OUTB cannot overlap (STP only enabled) Connecting capacitors to the DTC pin must be avoided.
8	GNDB	**Ground secondary-side channel B**
9	OUTB	**Output secondary-side channel B** Low-impedance output with source and sink capability
10	VDDB	**Supply secondary-side channel B** (operating range: UVLO to 20 V)
11	GNDA	**Ground secondary-side channel A**
12	OUTA	**Output secondary-side channel A** Low-impedance output with source and sink capability
13	VDDA	**Supply secondary-side channel A** (operating range: UVLO to 20 V)

For package drawing details see Chapter 6.

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2 Functional description

2.1 Block diagram

A simplified functional block diagram for EiceDRIVER™ 2EDBx259K is given in Figure 3.

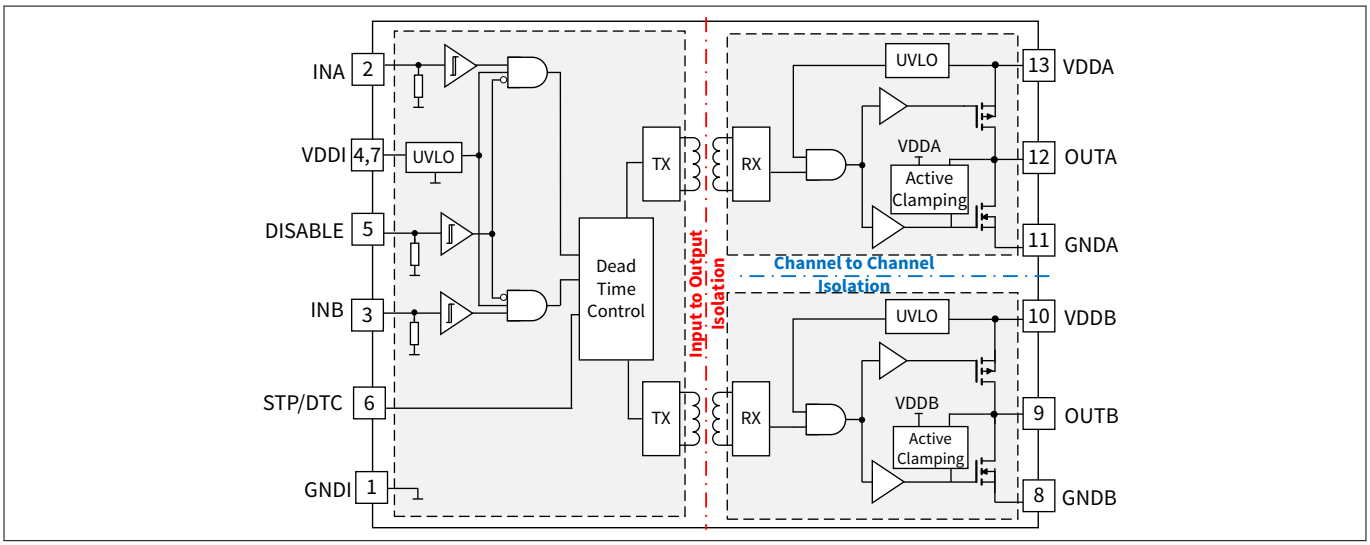


Figure 3 Block diagram

2.2 Power supply and Undervoltage Lockout (UVLO)

Due to the input-to-output and channel-to-channel isolation, three power domains with independent power management are required. Undervoltage Lockout (UVLO) functions for both input and output supplies ensure a defined startup and robust functionality under all operating conditions.

2.2.1 Input supply voltage

The input die is powered via VDDI and supports a wide supply voltage range from 3 V to 17 V. A ceramic bypass capacitor must be placed between VDDI and GNDI in close proximity to the device; a minimum bypass capacitance of 100 nF is recommended.

Power consumption to some extent, depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the coreless transformer. Due to the chosen robust encoding scheme the average repetition rate of these pulses and thus the average supply current depends on the switching frequency, f_{sw}. However, for f_{sw} < 500 kHz this effect is very small.

The Undervoltage Lockout function for the input supply V_{DDI} ensures that, as long as V_{DDI} is below UVLO (e.g. in startup), no data is transferred to the output side and the gate driver output is held low (safety Lock-down at startup). When V_{DDI} exceeds the UVLO level, the PWM input signal is transferred to the output side. If the output side is ready (not in UVLO condition), the output reacts according to the logic input.

2.2.2 Output supply voltage

The two output dies are powered via two independent supply voltages V_{DDA} and V_{DDB} (up to 20 V).

Two ceramic bypass capacitors must be placed between VDDA and GNDA and between VDDB and GNDB in close proximity to the device. A minimum capacitance of 20 x C_{iss} (MOSFET input capacitance) is recommended to ensure an acceptable ripple (5% of V_{DDO}) on the supply pin.

The minimum supply voltage is set by the Undervoltage Lockout (UVLO) function. The gate driver output can be switched only if the output supply voltage (V_{DDA}, V_{DDB}) exceeds the output-side UVLO. Thus, it can be guaranteed that the switch transistor is not operated if the driving voltage is too low to achieve a complete and fast transition to the "on" state. Low driving voltage, in fact, could cause the power MOSFET to enter its saturation (ohmic) region with potentially destructive power dissipation; the output UVLO ensures that the

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switch transistor always stays within its Safe Operating Area (SOA). Versions with 4 V and 8 V UVLO thresholds for the output supply are currently available; Table 3 shows the recommended UVLO levels for different Infineon power switch families.

Table 3 Recommended UVLO levels for typical use-cases

Inputs	Examples of part number	Recommended driver
Logic level OptiMOS™	BSC010N04LS6, BSZ070N08LS5, ..	2EDB7259K (4 V UVLO)
Normal level OptiMOS™	BSC040N10NS5, BSZ084N08NS5, ..	2EDB8259K (8 V UVLO)
CoolMOS™	IPP60R099C7, IPB60R600P6, ..	2EDB8259K (8 V UVLO)

2.3 Input stage - INA, INB, DISABLE

The inputs INA and INB control two independent PWM channels. The input signal is transferred non-inverted to the corresponding gate driver outputs OUTA and OUTB. All inputs are compatible with LV-TTL threshold levels and provide a hysteresis of typically 0.8 V. The hysteresis is independent of the supply voltage V_{DDI}.

The PWM inputs are internally pulled down to a logic low voltage level (GNDI). In case the PWM-controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off"-state (low).

If the DIS input is at high state, this unconditionally drives both channel outputs to low state regardless of the state of INA or INB.

Table 4 shows the INA, INB, DISABLE driver logic in case of sufficiently high supply voltage. Otherwise the outputs of the driver are determined by the Undervoltage Lockout (UVLO) and Output Active Clamping functionalities as shown in Table 7.

Table 4 Logic table in case of sufficient bias power - INA, INB, DIS

Inputs		DIS	Supplies	Outputs		Note
INA	**INB**		**V_{DDI}, V_{DDA}, V_{DDB}**	**OUTA**	**OUTB**	
L	L	L or left open	> $UVLO_{VDDx,on}$ (active)	L	L	–
L	H	L or left open		L	H	–
H	H	L or left open		H	H	DTC/STP pin tied to VDDI or left open
				L	L	DTC/STP pin tied to GNDI or tied to GNDI via R_{DTC}
Left open	Left open	L or left open		L	L	Input pins internally pulled down
x	x	H		L	L	Outputs disabled via DIS high

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2.4 Shoot-through protection and configurable dead-time - STP/DTC

The shoot-through protection pulls down the outputs OUTA and OUTB when both input signals INA, INB are at high state. Its activation is recommended when the driver is used as half-bridge driver to prevent dangerous shoot-through due to unwanted overlap of INA and INB. A dead-time can be ensured and configured via pin STP/DTC as shown in Table 5.

Table 5 STP/DTC logic table

Conditions on the STP/DTC pin	Shoot-through protection	Configurable dead-time
Tied to VDDI or left open	Disabled	Disabled
Connected to GNDI via resistor R_{DTC}	Enabled	Enabled with t_{dt} [ns] = 10 x R_{DTC} [kΩ]; allowed R_{DTC} range is 1.2kΩ to 100kΩ
Connected to GNDI	Enabled	Disabled

The driver dead-time logic is triggered during the falling edge of an input and delays the rising transition of the other input. The delay is only assigned if the driver configured dead-time is longer than the inputs signals' own dead-time.

The dead-time can be configured by changing the current fed into the STP/DTC pin via an external resistance according to the formula: t_{dt} [ns] = 10 x R_{DTC} [kΩ]. It is recommended to use resistors with 1% accuracy in the 1.2 kΩ to 100 kΩ range. Using a resistor outside this recommended range disables the shoot-through protection and dead-time control functionality. Connecting capacitors to the DTC pin must be avoided when the dead-time control functionality is used.

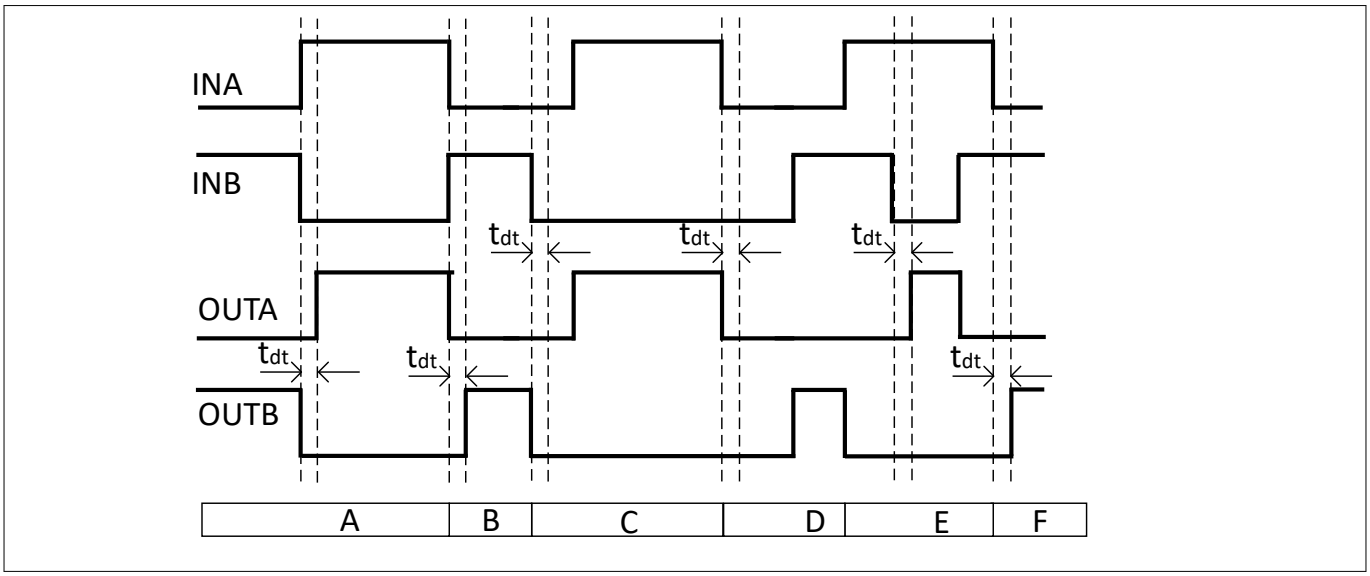


Figure 4 Logic for STP/DTC pin connected to GNDI via resistance R_{DTC}

Table 6 Logic for STP/DTC pin connected to GNDI via resistance R_{DTC}

Condition	STP/DTC logic
A, B	The driver logic assigns the configured dead-time since it is longer than the input signals' dead-time
C, D	The driver logic does not assign the configured dead-time since it is shorter than the input signals' dead-time

(table continues...)

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Table 6 (continued) Logic for STP/DTC pin connected to GNDI via resistance R_{DTC}

Condition	STP/DTC logic
E, F	The shoot-through protection pulls down the outputs OUTA, OUTB until one of the outputs goes low. At this point, after the configured driver dead-time, the other output is allowed to go high

2.5 Gate driver outputs

The rail-to-rail output stage realized with complementary MOS transistors is able to provide a typical 5 A sourcing and 9 A sinking peak current. The low on-resistance coming together with high driving current is particularly beneficial for fast switching of very large MOSFETs. With a R_{on} of ~1 Ω for the sourcing pMOS and ~0.5 Ω for the sinking nMOS transistor the driver can in most applications be considered as a nearly ideal switch. The p-channel sourcing transistor enables real rail-to-rail behavior without suffering from the voltage drop unavoidably associated with nMOS source follower stages.

In case of floating inputs or insufficient supply voltage not exceeding the UVLO thresholds, the driver outputs are actively clamped to the "low" level (GNDA, GNDB).

2.6 Fast active output clamping in UVLO conditions

The Undervoltage Lockout (UVLO) ensures that the gate driver output is not operated if the supplies are below the UVLO thresholds. However, this is not sufficient to guarantee that the output of the driver is kept low. Transients or noise in the power stage may pull-up the output node of the driver and the gate voltage causing an unwanted turn-on of the switch; this is particularly critical in system using bootstrapping since, during start-up, the supply of the high-side channel is delayed, while the low-side MOSFET is already switching. In resonant topologies (as LLC), the half-bridge switching node may be pulled up after the turn-off of the low-side switch. When the low-side MOSFET is turned on again, the high-side gate voltage increase induced by dV/dt event cannot be clamped by the driver $R_{DSON,sink}$ if the bootstrap supply is not yet available.

With a fast output clamping circuit in the output stage, the driver ensures safe operation against output induced overshoots in all UVLO situations. This structure allows fast reaction and effective clamping of the output pins (OUTA, OUTB). The exact reaction time depends on the output supply (V_{DDA}, V_{DDB}) and on the output voltage levels; however, already for very low supply levels (~1 V), the active output clamp is able to react in some tens of ns.

Undervoltage Lockout together with the output active clamping ensures that the outputs are actively held low in case of insufficient supply voltages.

Table 7 Logic table in case of insufficient bias power - INA, INB, DISABLE

Inputs		DIS	Supplies			Outputs	
INA	INB		V_{DDI}	V_{DDA}	V_{DDB}	OUTA	OUTB
x	x	x	< $UVLO_{VDDI,on}$	x	x	L	L
x	x	x	> $UVLO_{VDDI,on}$	< $UVLO_{VDDA,on}$	< $UVLO_{VDDB,on}$	L	L
x	x	x	> $UVLO_{VDDI,on}$	> $UVLO_{VDDA,on}$	< $UVLO_{VDDB,on}$	Follows INA	L
x	x	x	> $UVLO_{VDDI,on}$	< $UVLO_{VDDA,on}$	> $UVLO_{VDDB,on}$	L	Follows INB

2.7 CT communication and input to output data transmission

A coreless transformer (CT) based communication module is used for PWM signal transfer between input and output. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog timeout at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

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3 Electrical characteristics

The absolute maximum ratings are listed in Table 8. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 8 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	-0.3	–	18	V	–
Output supply voltage at pins VDDA, VDDB	V_{DDA}, V_{DDB}	-0.3	–	22 [1]	V	–
Voltage at pins INA, INB, DIS (DC)	V_{IN}	-0.3	–	18	V	–
Voltage at pins INA, INB, DIS (transient)	V_{IN}	-5	–	–	V	transient for 50 ns [3]
Voltage at pin DTC	V_{DTC}	[2]	–	V_{DDI} + 0.3	V	–
Voltage at pins OUTA, OUTB (DC)	V_{OUT}	-0.3	–	$V_{DDA/B}$ + 0.3	V	–
Voltage at pins OUTA, OUTB (transient)	V_{OUT}	-2	–	$V_{DDA/B}$ + 1.5	V	transient for 200 ns [3]
Reverse current peak at pins OUTA, OUTB	I_{SRC_rev}	-5	–	–	A_{pk}	transient for 500 ns [3]
Reverse current peak at pins OUTA, OUTB	I_{SNK_rev}	–	–	5	A_{pk}	transient for 500 ns [3]
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STG}	-65	–	150	°C	–
Soldering temperature	T_{SOL}	–	–	260	°C	reflow [4]
ESD capability	V_{ESD_CDM}	–	–	1	kV	Charged Device Model (CDM) [5]
ESD capability	V_{ESD_HBM}	–	–	2	kV	Human Body Model (HBM) [6]

1) Maximum positive supply voltage already complies with derating guidelines.
2) Minimum is given by internal regulation when DTC is operating (DTC pin connected to GND via resistance).
3) Not subject to production test - verified by design/characterization.
4) According to JEDEC-020E.
5) According to ANSI/ESDA/JEDEC JS-002.
6) According to ANSI/ESDA/JEDEC JS-001 (discharging 100 pF capacitor through 1.5 kΩ resistor).

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3.2 Thermal characteristics

Thermal characteristics are obtained from simulation with 65 mW applied to the driver input-side and 200 mW applied to any output channel.

Table 9 Thermal characteristics at T_A = 25°C

Parameter	Symbol	Value		Unit	Note or condition
		2s2p [1]	10-layer [2]		
Thermal resistance junction ambient [3]	R_{thJA25}	131	114	K/W	–
Thermal resistance junction-case (top) [4]	R_{thJC25}	56		K/W	–
Thermal resistance junction board [5]	R_{thJB25}	73	78	K/W	–
Characterization parameter junction-top [6]	Ψ_{thJT25}	10	9	K/W	–
Characterization parameter junction-board [6]	Ψ_{thJB25}	71	75	K/W	–

1) High-K board JEDEC-standard as specified in JESD51-7: four-layers board with 2-oz inner layers copper planes and with no thermal vias for cooling.

2) 10-layer board emulating typical application conditions: 3.2 mm thick board with 3-oz copper layers and 2 thermal vias connecting GNDA, GNDB to the inner layers.

3) Obtained by simulating the 2s2p JESD51-7 board or the 10-layer board in an environment described in JESD51-2a.

4) Obtained by simulating a cold plate test on the package top. No specific JEDEC standard exixts, but a close description can be found in the ANSI SEMI standard G30-88.

5) Obtained by simulating the 2s2p JESD51-7 board or the 10-layer board in an environment described in JESD51-8 with a ring cold plate fixture to control the PCB temperature.

6) Estimates the junction temperature in a real system and is extracted from the simulation data for obtaining RthJA, using a procedure described in JESD51-2a (sections 6 and 7).

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3.3 Operating range

Table 10 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage at pin VDDI	V_{DDI}	3	–	17	V	Min. defined by $UVLO_{VDDI}$
Output supply voltage at pin VDDA and VDDB	V_{DDA}, V_{DDB}	4.5	–	21 [1]	V	4 V UVLO option
Output supply voltage at pin VDDA and VDDB	V_{DDA}, V_{DDB}	8.5	–	21 [1]	V	8 V UVLO option
Input voltage at pins INA, INB, DISABLE	V_{IN}	0	–	17	V	–
Input voltage at pin DTC	V_{DTC}	[2]	–	V_{DDI}	V	–
Junction temperature	T_J	-40	–	150 [3]	°C	
Ambient temperature	T_A	-40	–	125	°C	–

1) Maximum positive supply voltage already complies with derating guidelines.
2) Minimum is given by internal regulation when DTC is operating (DTC pin connected to GND via resistance).
3) Continuous operation above 125°C may reduce lifetime.

3.4 Electrical characteristics

Unless otherwise noted, the electrical characteristics are given for V_{DDI} = 3.3 V, $V_{DDA/B}$ =12 V and no load. Typical values are given at T_J = 25°C whilst min. and max., instead, are the lower and upper limits, respectively, within the full operating range.

Table 11 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IVDDI quiescent current	I_{VDDIq}	–	1.67	2.12	mA	no switching
IVDDA/B quiescent current	$I_{VDDA/Bq}$	–	0.62	0.86	mA	OUT = low
IVDDA/B quiescent current	I_{VDDBq}	–	0.76	1.0	mA	OUT = high

Table 12 Undervoltage Lockout VDDI

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold VDDI	$UVLO_{VDDI,on}$	–	2.85	2.95	V	–

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Table 12 (continued) Undervoltage Lockout VDDI

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-off threshold VDDI	$UVLO_{VDDI,off}$	2.55	2.7	–	V	–
UVLO threshold hysteresis VDDI	$UVLO_{VDDI,hys}$	0.10	0.15	0.20	V	–

Table 13 Undervoltage Lockout VDDA, VDDB for 4 V UVLO option

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold VDDA, VDDB	$UVLO_{VDDA,on}$ $UVLO_{VDDB,on}$	–	4.2	4.4	V	–
Undervoltage Lockout (UVLO) turn-off threshold VDDA, VDDB	$UVLO_{VDDA,off}$ $UVLO_{VDDB,off}$	3.7	3.9	–	V	–
UVLO threshold hysteresis VDDA, VDDB	$UVLO_{VDDA,hys}$ $UVLO_{VDDB,hys}$	0.2	0.3	0.4	V	–

Table 14 Undervoltage Lockout VDDA, VDDB for 8 V UVLO option

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold VDDA, VDDB	$UVLO_{VDDA,on}$ $UVLO_{VDDB,on}$	–	8.0	8.5	V	–
Undervoltage Lockout (UVLO) turn-off threshold VDDA, VDDB	$UVLO_{VDDA,off}$ $UVLO_{VDDB,off}$	6.6	7.0	–	V	–
UVLO threshold hysteresis VDDA, VDDB	$UVLO_{VDDA,hys}$ $UVLO_{VDDB,hys}$	0.7	1	1.3	V	–

Table 15 Logic inputs INA, INB, DISABLE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	–	2.0	2.36	V	–
Input voltage threshold for transition HL	V_{INL}	0.9	1.2	–	V	–

(table continues...)

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Table 15 (continued) Logic inputs INA, INB, DISABLE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage threshold hysteresis	V_{IN_hys}	0.38	0.8	1.2	V	–
High-level input leakage current	I_{IN}	–	22	27	µA	INA/INB pin tied to VDDI
Input pull-down resistor	$R_{IN,PD}$	–	150	–	kΩ	–

Table 16 Dead-time control (DTC) and shoot-through protection (STP)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Dead-time	t_{dt}	85	100	115	ns	R_{DTC} = 10 kΩ
Dead-time	t_{dt}	255	300	345	ns	R_{DTC} = 30 kΩ
Dead-time	t_{dt}	800	950	1100	ns	R_{DTC} = 100 kΩ [1]
Channel-to-channel dead-time mismatch	$\Delta t_{dt,Ch\text{-}Ch}$	0	–	10	ns	R_{DTC} = 10 kΩ
Channel-to-channel dead-time mismatch	$\Delta t_{dt,Ch\text{-}Ch}$	0	–	14	ns	R_{DTC} = 30 kΩ
Channel-to-channel dead-time mismatch	$\Delta t_{dt,Ch\text{-}Ch}$	0	–	40	ns	R_{DTC} = 100 kΩ [1]
Part-to-part dead-time mismatch	$\Delta t_{dt,p\text{-}p}$	0	–	20	ns	R_{DTC} = 10 kΩ [2]
Part-to-part dead-time mismatch	$\Delta t_{dt,p\text{-}p}$	0	–	55	ns	R_{DTC} = 30 kΩ [2]
Part-to-part dead-time mismatch	$\Delta t_{dt,p\text{-}p}$	0	–	105	ns	R_{DTC} = 100 kΩ [1] [2]

1) Not subject to production test - verified by design/characterization.
2) The parameter gives the difference in the dead-time inserted from different samples under the same conditions, including same ambient temperature.

Table 17 Static output characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on_SRC}	0.6	1.0	1.6	Ω	I_{SRC} = 50 mA
Peak sourcing output current	I_{SRC_pk}	–	5	–	A	C_{LOAD} = 22 nF [1]
Low-level (sinking) output resistance	R_{on_SNK}	0.2	0.46	0.8	Ω	I_{SNK} = 50 mA

(table continues...)

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Table 17 (continued) Static output characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak sinking output current	I_{SNK_pk}		-9	–	A	C_{LOAD} = 22 nF 1)
Active output clamp	V_{clamp}	0.79	1.16	1.45	V	I_{SNK} = 10mA, V_{DDx} floating and unpowered

1) Not subject to production test - verified by design/characterization.

Table 18 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
INx to OUTx turn-on propagation delay	$t_{PDon,INx}$	33	38	47	ns	See Figure 5, Figure 6
INx to OUTx turn-off propagation delay	$t_{PDoff,INx}$	30	36	46	ns	See Figure 5, Figure 6
Part-to-part turn-on propagation delay mismatch	$\Delta t_{PDon,p-p}$	0	–	6	ns	1)
Part-to-part turn-off propagation delay mismatch	$\Delta t_{PDoff,p-p}$	0	–	8	ns	1)
Channel-to-channel turn-on propagation delay mismatch	$t_{PDon,ChA-ChB}$	-4	0	4	ns	See Figure 7 2)
Channel-to-channel turn-off propagation delay mismatch	$\Delta t_{PDoff,ChA-ChB}$	-5.5	-1	3	ns	See Figure 7 2)
Pulse width distortion	t_{PWD}	-5	2	5.5	ns	See Figure 8 3)
Channel turn-off to channel turn-on propagation delay mismatch	t_{DTD}	-5	-2	1	ns	See Figure 9 4) 5)
Rise time	t_{rise}	–	7.5	14	ns	C_{LOAD} = 1.8 nF, see Figure 10 6)
Fall time	t_{fall}	–	6	11	ns	C_{LOAD} = 1.8 nF, see Figure 10 6)
Minimum input pulse width that changes output state	t_{PW}	10	17	25	ns	See Figure 11
Input-side start-up time	$t_{START,VDDI}$	–	3.5	5	µs	See Figure 12 6)

(table continues...)

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Table 18 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input-side deactivation time	$t_{STOP,VDDI}$	600	750	–	ns	See Figure 12 6)
Output-side start-up time	$t_{START,VDDA/B}$	–	2.5	5	µs	See Figure 13 6)
Output-side deactivation time	$t_{STOP,VDDA/B}$	500	800	–	ns	See Figure 13 6)

1) The parameter gives the difference in the propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature; therefore, is an indication of the production spread. The limits given are valid for all channels combination: t_{PD_ChA} - t_{PD_ChA}, t_{PD_ChB} - t_{PD_ChB}, t_{PD_ChA} - t_{PD_ChB}, t_{PD_ChB} - t_{PD_ChA}.
2) The parameter gives the difference in the propagation delay of channel A and channel B switching in the same direction in the same sample.
3) The parameter gives the difference between ON and OFF propagation delay in the same channel (ChA or ChB), in the same sample at same ambient temperature.
4) The parameter gives the difference between the ON propagation delay of one channel and the OFF propagation delay of the other channel, in the same sample at same room temperature. This parameter represents the distortion of the inputs dead-time only when the driver DTC is not used or not enforced otherwise, please refer to "Dead-time and shoot-through protection" table.
5) Not subject to production test - verified by characterization.
6) Not subject to production test - verified by design/characterization.

Table 19 Thermal shutdown

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal shutdown rising threshold	T_{SHUT_RISE}	–	172	–	°C	1)
Thermal shutdown falling threshold	T_{SHUT_FALL}	–	149	–	°C	1)

1) Not subject to production test - specified by characterization.

Table 20 Common-Mode Transient Immunity (CMTI)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Static Common-Mode Transient Immunity	$\lvert CM_{Static,H} \rvert$	150	–	–	V/ns	V_{CM} = 1500 V; INA, INB tied to V_{DDI} (logic high inputs) 1)
Static Common-Mode Transient Immunity	$\lvert CM_{Static,L} \rvert$	150	–	–	V/ns	V_{CM} = 1500 V; INA, INB tied to GNDI (logic low inputs) 1)

1) Minimum slew rate of a common-mode voltage that is able to cause an incorrect output signal

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3.5 Isolation specifications

Table 21 Isolation specifications

Parameter	Symbol	Value	Unit	Note or condition
External input-to-output creepage [1]	CRP	3.4	mm	Shortest distance over package surface from any input pin to any output pin according to IEC 60664-1
External input-to-output clearance [1]	CLR	3.4	mm	Shortest distance in air from any input pin to any output pin according to IEC 60664-1
Comparative tracking index	CTI	> 400	V	According to DIN EN 60112 (VDE 0303-11)
Material group	–	II	–	According to IEC 60112
Pollution degree	–	II	–	According to IEC 60664-1
Overvoltage category (for basic isolation)	–	I - III	–	Rated mains voltage ≤ 150 V_{RMS}
	–	I - II	–	Rated mains voltage ≤ 300 V_{RMS}
	–	I	–	Rated mains voltage ≤ 600 V_{RMS}
Climatic category	–	40/125/21	–	
Input-to-output isolation according to UL1577 Ed.5 [2]				
Input-to-output isolation voltage	V_{ISO}	2500	V_{RMS}	$V_{TEST} = V_{ISO}$ for t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ for t = 1 s (100% productive tests)
Input-to-output isolation according to DIN VDE V0884-11 [3]				
Maximum rated transient isolation voltage	V_{IOTM}	3535	V_{pk}	$V_{TEST} = 1.2 \times V_{IOTM}$ for t_{ini} = 1s
Maximum rated repetitive isolation voltage	V_{IORM}	800	V_{pk}	According to Time Dependent Dielectric Breakdown (TDDB) Test
Apparent charge	q_{PD}	< 5	pC	Method (b1) [4] $V_{PD(ini)} = 1.2 \times V_{IOTM}$ for t_{ini} = 1s $V_{PD(m)} = 1.875 \times V_{IORM}$ for t_m = 1s
Maximum surge isolation voltage [5]	V_{IOSM}	5384	V_{pk}	$V_{IOSM_TEST} = 1.3 \times V_{IOSM}$
Isolation resistance input-to-output [6]	R_{IO}	10^{12}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 25°C
		10^{11}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 125°C
		10^{9}	Ω	V_{IO} = 500 V_{dc} for t = 60 s, T_A = 150°C
Capacitance input-to-output [6]	C_{IO}	2	pF	f = 1 MHz

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level.

2) See UL 1577 certificate n. E311313

3) Parameters provided according to VDE0884-11 specifications without safety certification

4) The partial discharge voltage VPD(m) is greater (1444 Vpk > 1.875 x VIORM) to include the F4 factor required by end equipment standards IEC 60664-1, IEC 62368-1, IEC 60950 (VPD(m) = F1 x F2 x F3 x F4 x VIORM = 1.875 x F4 x VIORM). The F3 factor (1.25) for reinforced isolation is also considered for further stress of the insulation.

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5) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier. The parameter is verified by design/characterization

6) The parameters apply to the product converted in a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together.

Table 22 Output channel-to-channel isolation specifications

Parameter	Symbol	Value	Unit	Note or condition
External channel-to-channel creepage [1)]	CRP_{Ch-Ch}	1.0	mm	Shortest distance over package surface between any output channel A pin and any output channel B pin

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level

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4 Timing diagrams

Figure 5 illustrates the input-to-output propagation delays as observed at the capacitively loaded output.

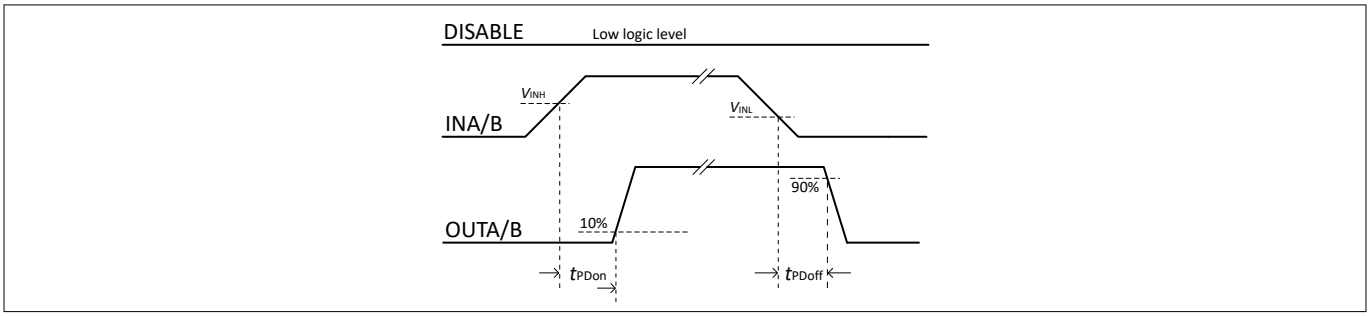


Figure 5 INx to OUTx propagation delays

Figure 6 illustrates the disable-to-output propagation delays as observed at the capacitively loaded output.

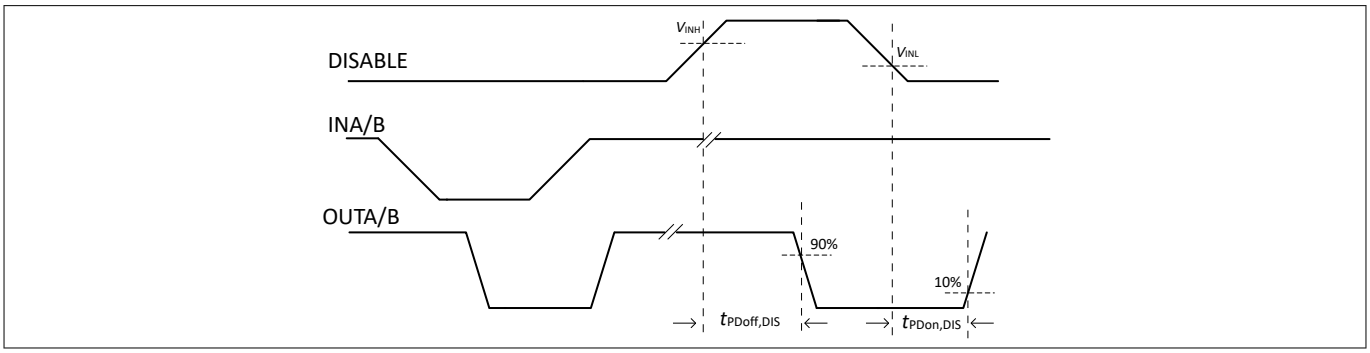


Figure 6 DISABLE to OUTx propagation delays

Figure 7 illustrates the channel-to-channel propagation delay mismatch at the unloaded outputs. This parameter is relevant when the channels drive parallel switches as it represents the delay in the two driving signals.

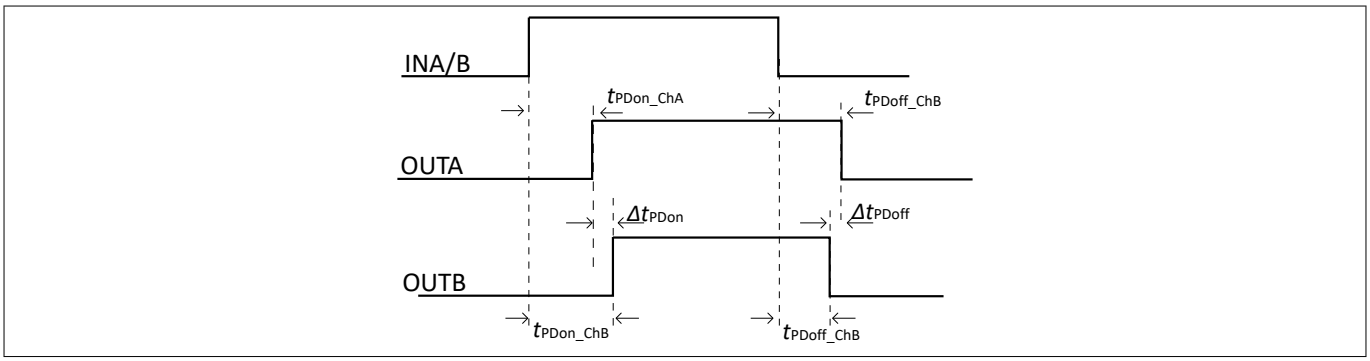


Figure 7 Channel-to-channel propagation delay mismatch

Figure 8 illustrates the pulse width distortion at the unloaded output. Ideally the width of the input pulse (t_{PW_INx}) equals the width of the output pulse (t_{PW_OUTx}); however, the driver introduces an output pulse distortion t_{PW} given by the difference between ON and OFF propagation delay.

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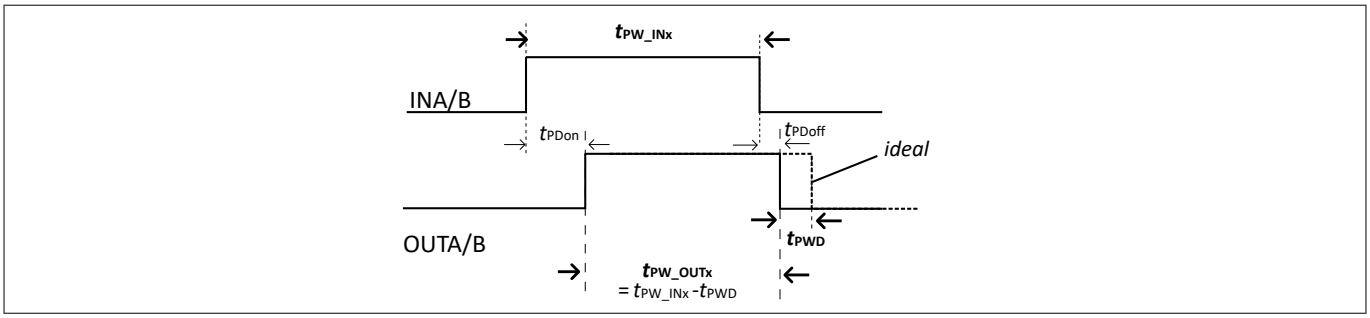


Figure 8 Pulse width distortion

Figure 9 illustrates the dead-time distortion at the unloaded outputs. This parameter is relevant in operation with complementary signals, as for the half-bridge driving when a certain dead-time t_{DT_INx} is set on the inputs INA, INB. Ideally the dead-time on the driver output (t_{DT_OUTx}) equals the input dead-time; however, the driver introduces a distortion t_{DTC} given by the difference between the OFF propagation delay of one channel and the ON propagation delay of the other channel.

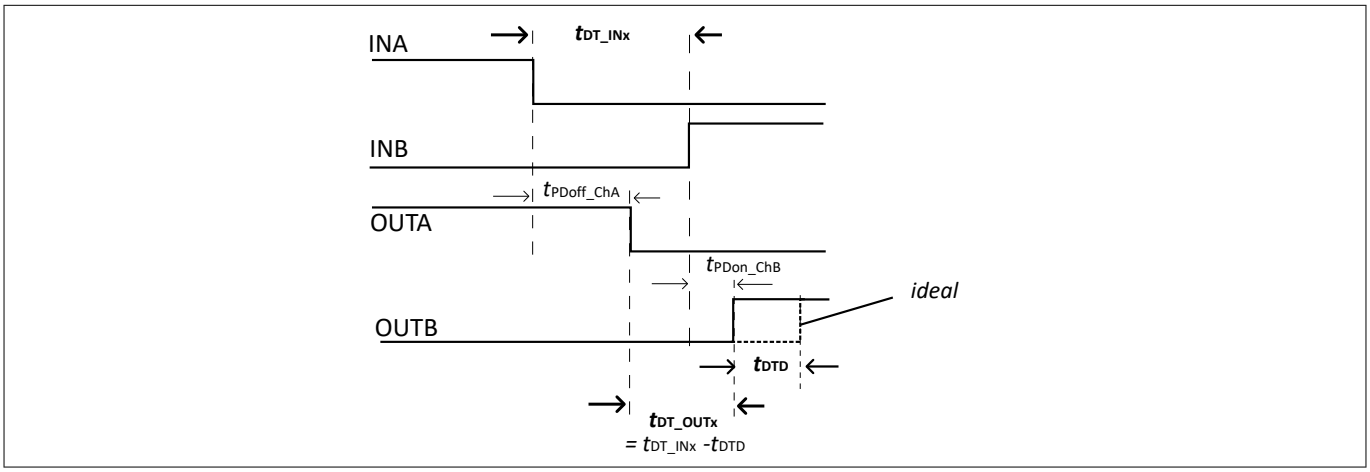


Figure 9 Channel turn-off to channel turn-on propagation delay mismatch

Figure 10 illustrates the rise and fall time as observed at the capacitively loaded output.

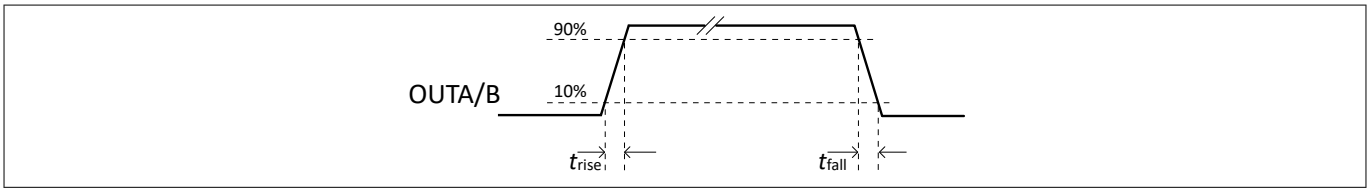


Figure 10 Rise and fall time

Figure 11 illustrates the behavior or the deglitch filter that filters spurios pulses on INA, INB with duration shorter than t_{PWmin}.

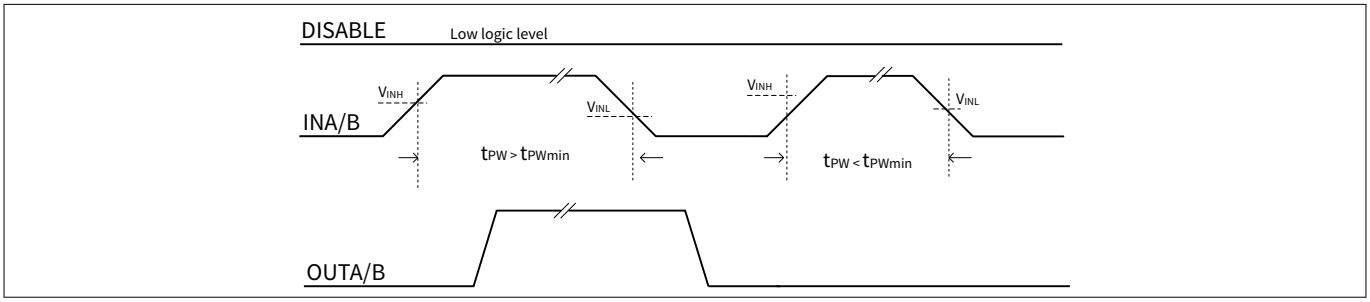


Figure 11 Minimum pulse that changes the output state

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4 Timing diagrams

Figure 12 illustrates the input-side supply UVLO behavior. It depicts the reaction time to UVLO events when V_{DDI} crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

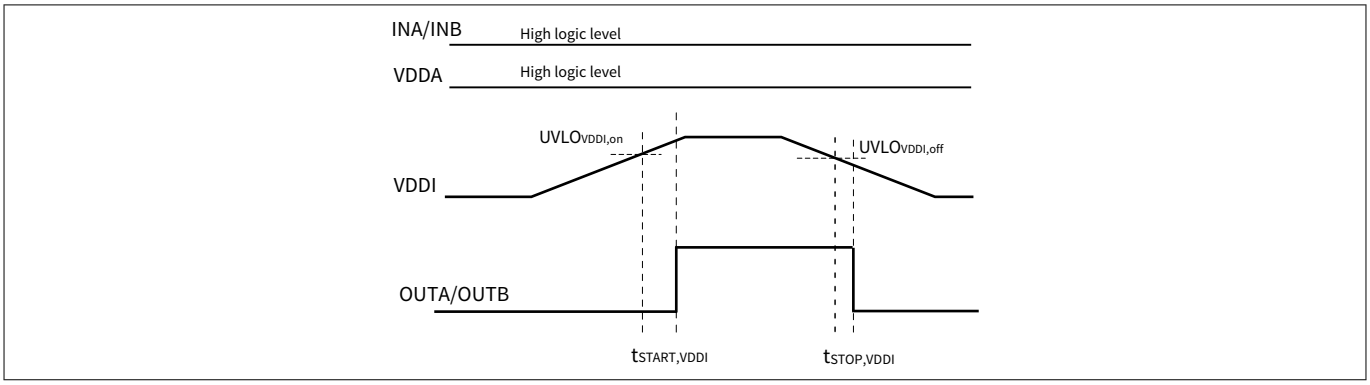


Figure 12 V_{DDI} UVLO behavior, start-up and deactivation time

Figure 13 illustrates the output-side supply UVLO behavior. It depicts the reaction time to UVLO events when $V_{DDA/B}$ crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

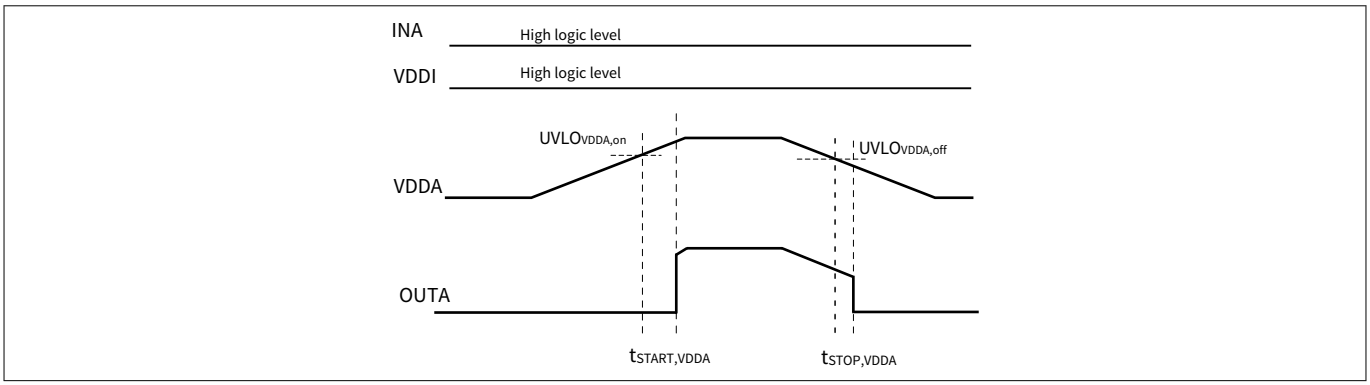


Figure 13 V_{DDA},V_{DDB} UVLO behavior, start-up and deactivation time

Figure 14 illustrates the shoot-through protection and dead-time logic. When enabled, the dead-time is added on top of the turn-off propagation delay if the driver dead-time is longer than the signals' own dead-time.

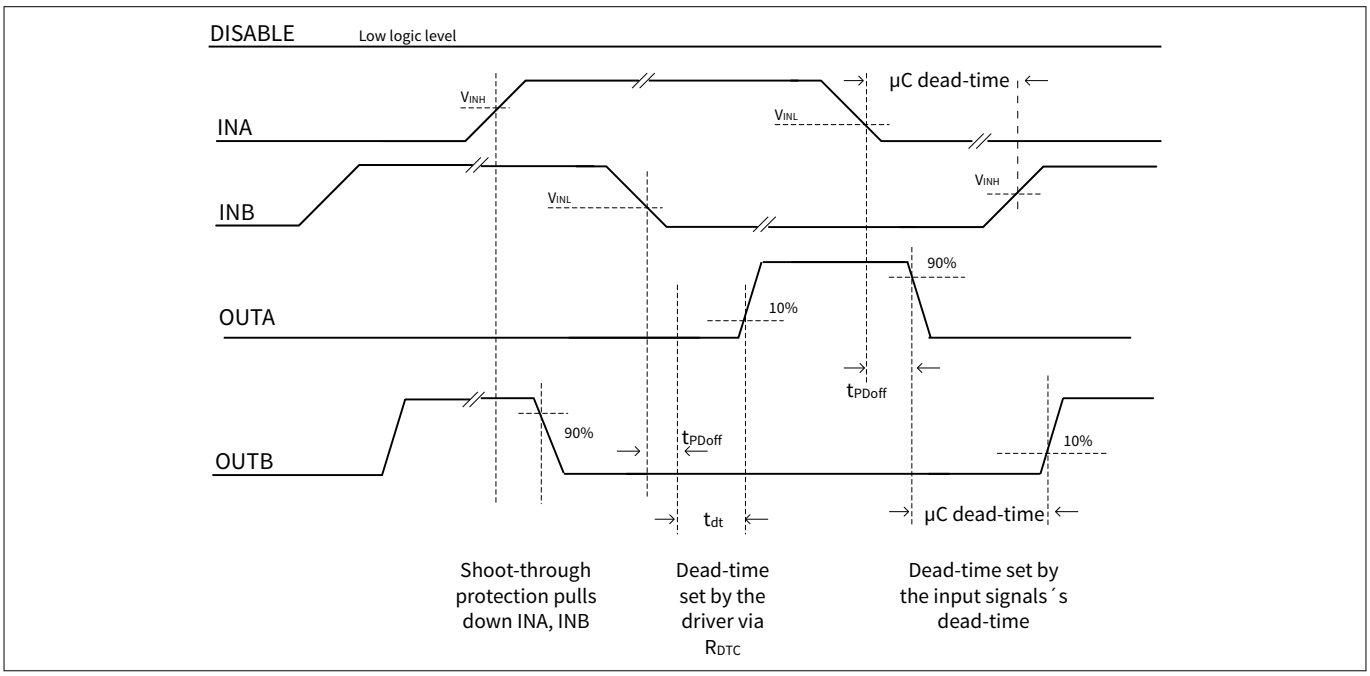
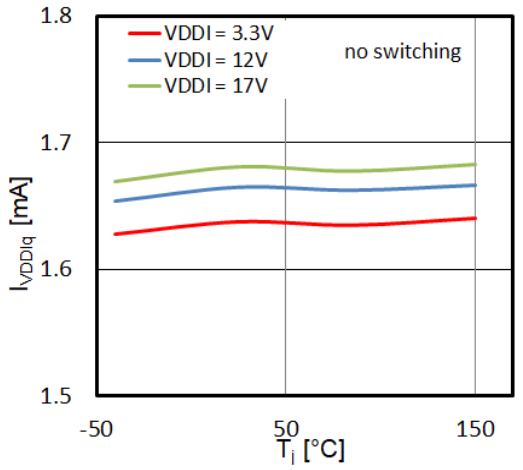


Figure 14 Shoot-through and configurable dead-time

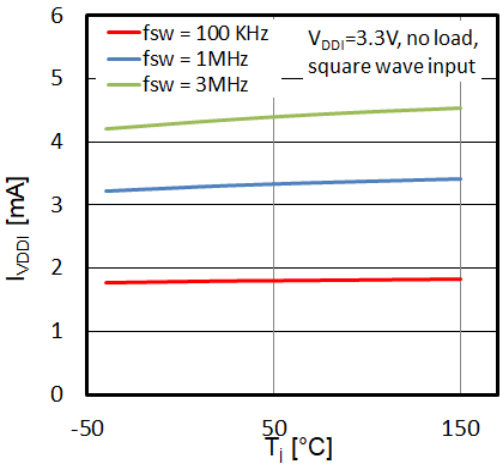
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5 Typical characteristics

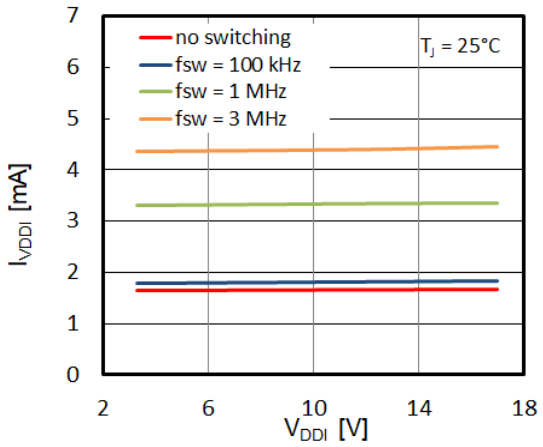
V_{DDI} = 3.3 V, $V_{DDA/B}$ = 12 V, T_A = 25°C, f_{sw} = 1 MHz, no load unless otherwise noted



Typical IVDDIq quiescent current vs. temperature



Typical IVDDIq switching current vs. temperature

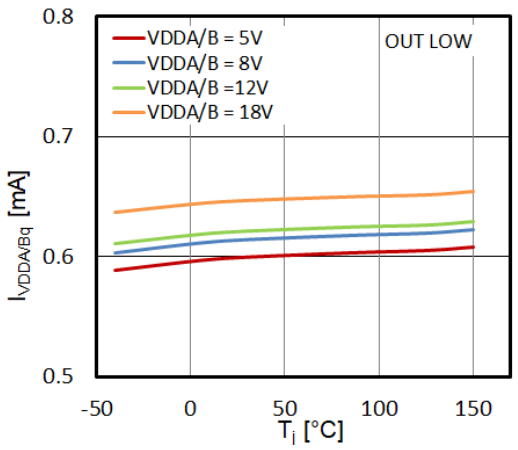


Typical IVDDI current vs. input-supply voltage V_{DDI}

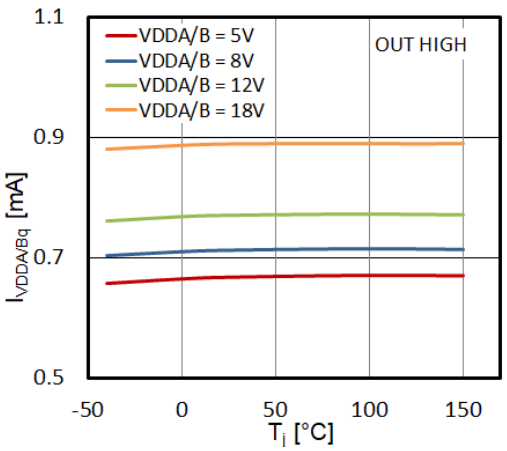
Figure 15 Input-side supply current

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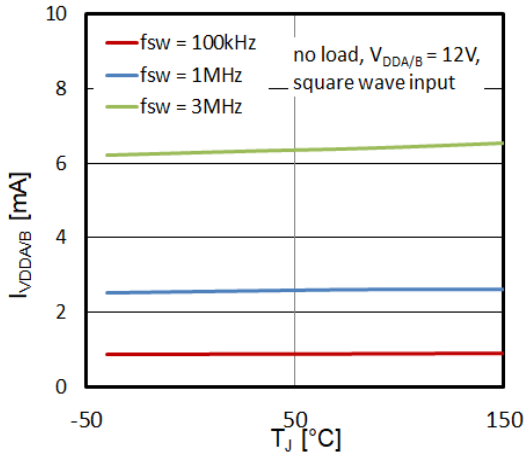
5 Typical characteristics



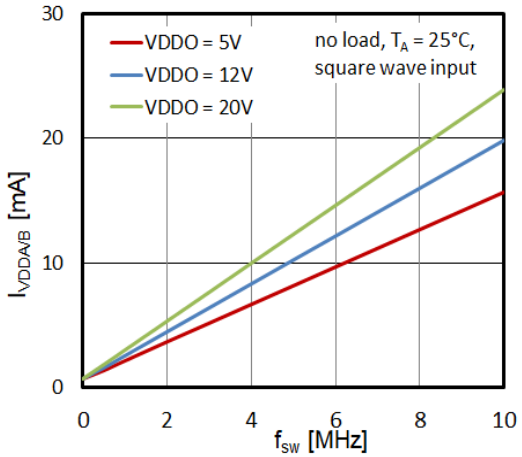
Typical $I_{VDDA/B}$ quiescent current (OUT low) vs. temperature



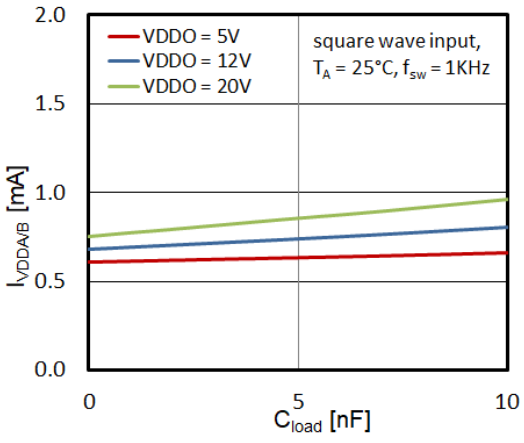
Typical $I_{VDDA/B}$ quiescent current (OUT high) vs. temperature



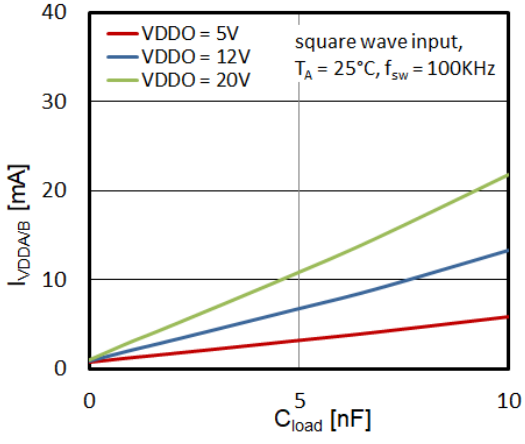
Typical $I_{VDDA/B}$ switching current vs. temperature



Typical $I_{VDDA/B}$ switching current vs. frequency



Typical $I_{VDDA/B}$ switching current vs. capacitive load (1 kHz frequency)

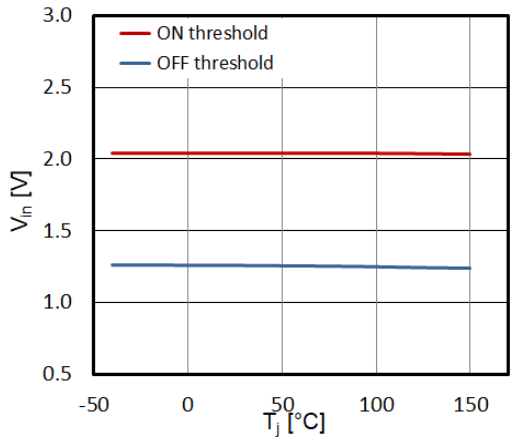


Typical $I_{VDDA/B}$ switching current vs. capacitive load (100 kHz frequency)

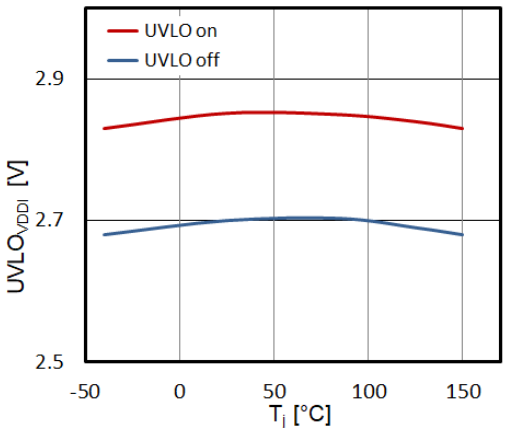
Figure 16 Output-side supply current

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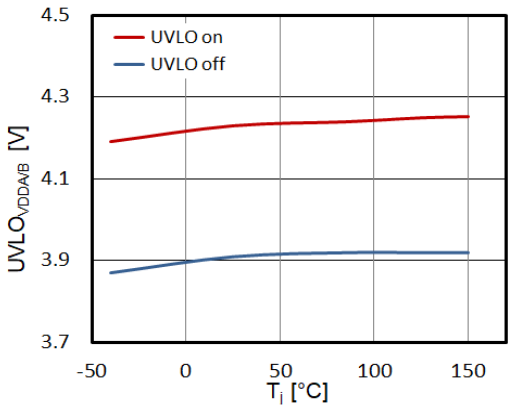
5 Typical characteristics



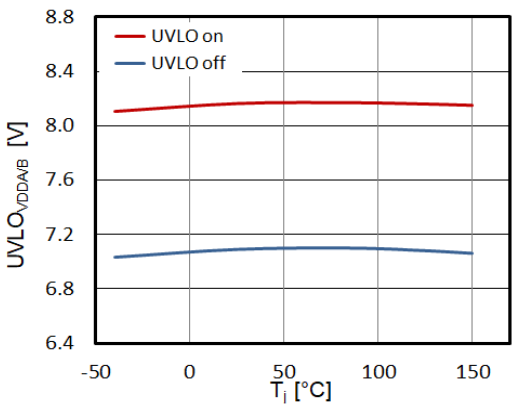
Typical input voltage thresholds vs. temperature



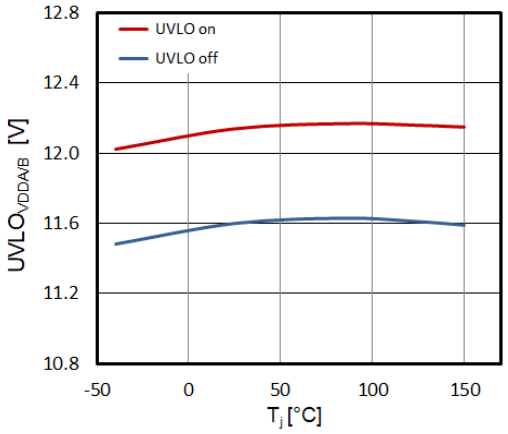
Typical Undervoltage Lockout thresholds VDDI vs. temperature



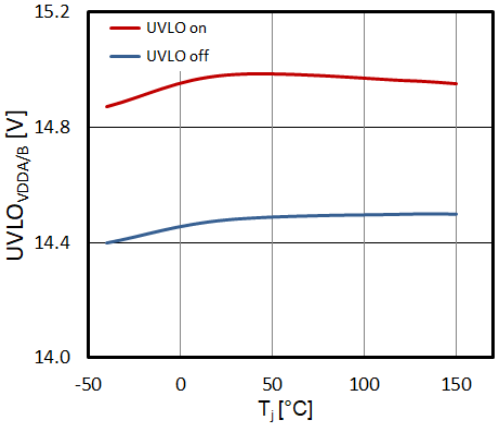
Typical Undervoltage Lockout VDDA/B thresholds vs. temperature (4 V version)



Typical Undervoltage Lockout VDDA/B thresholds vs. temperature (8 V version)



Typical Undervoltage Lockout VDDA/B thresholds vs. temperature (12 V version)

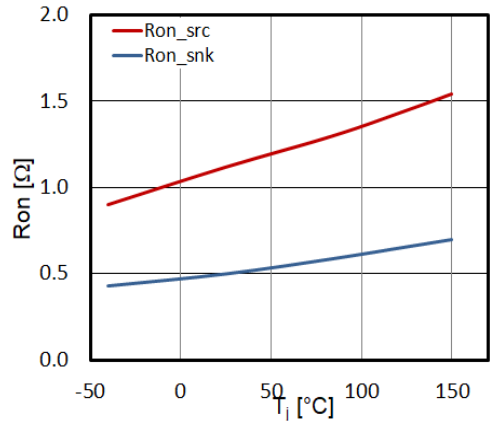


Typical Undervoltage Lockout VDDA/B thresholds vs. temperature (15 V version)

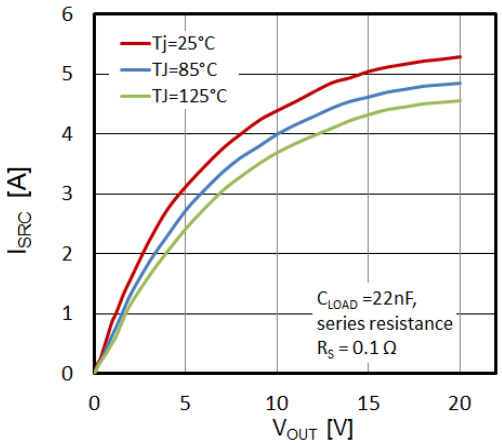
Figure 17 Input voltage thresholds and undervoltage lockout

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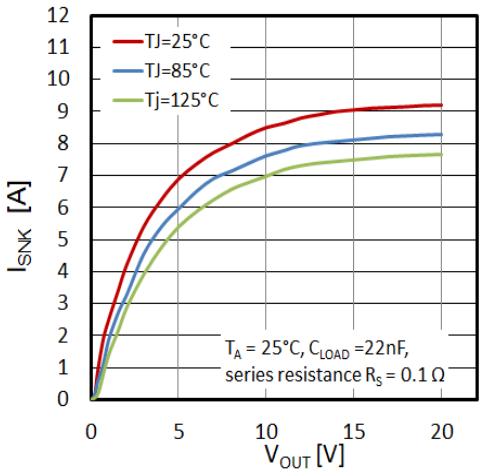
5 Typical characteristics



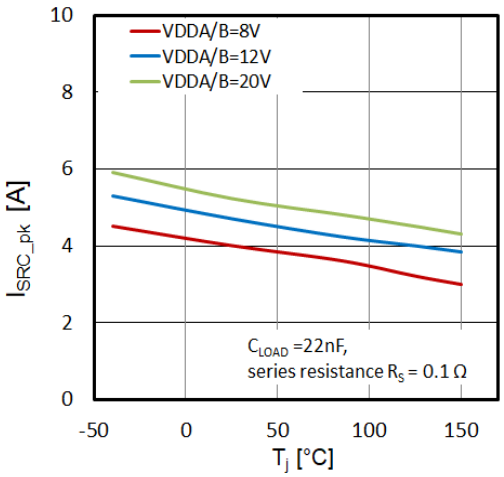
Typical output resistance
vs. temperature



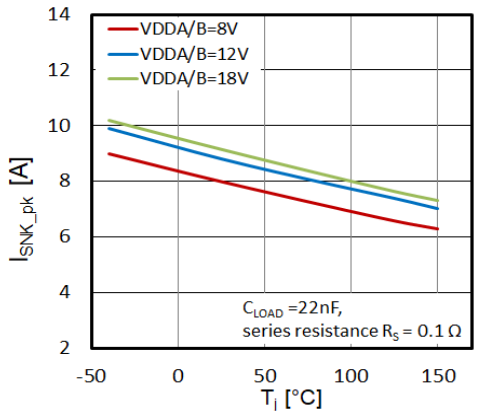
Typical sourcing output current
vs. output voltage



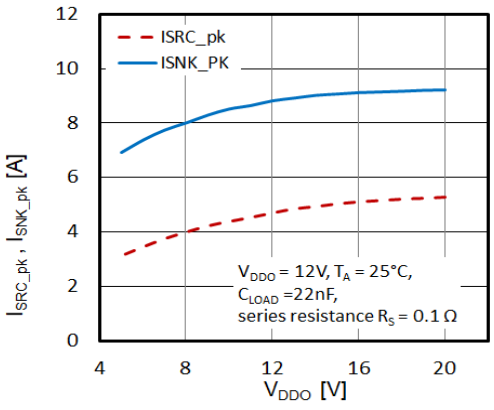
Typical sinking output current
vs. output voltage



Typical peak sourcing output current vs.
temperature



Typical peak sinking output current
vs. temperature

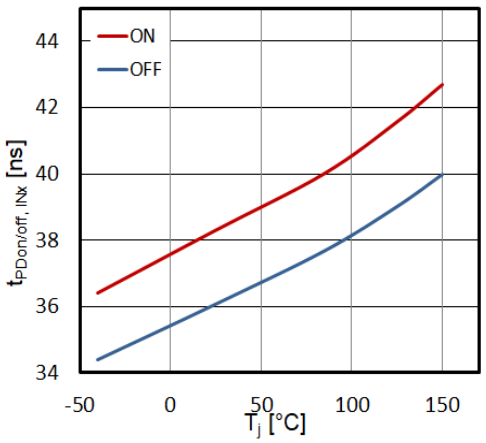


Typical peak output current vs.
supply voltage

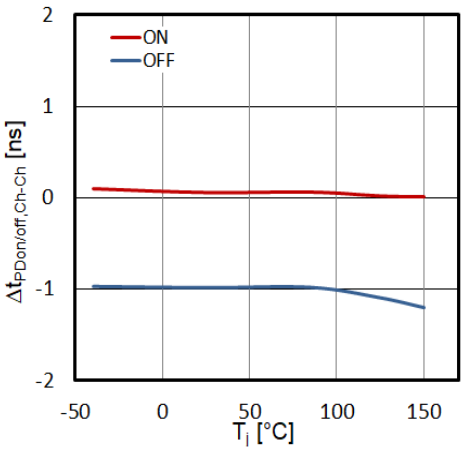
Figure 18 Typical output static characteristics

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5 Typical characteristics



Typical input-to-output propagation delay vs. temperature

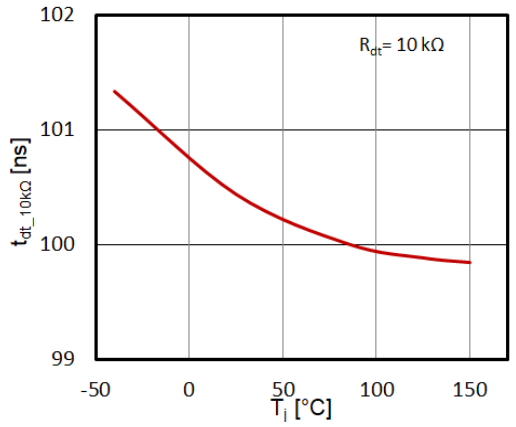


Typical channel-to-channel propagation delay mismatch vs. temperature

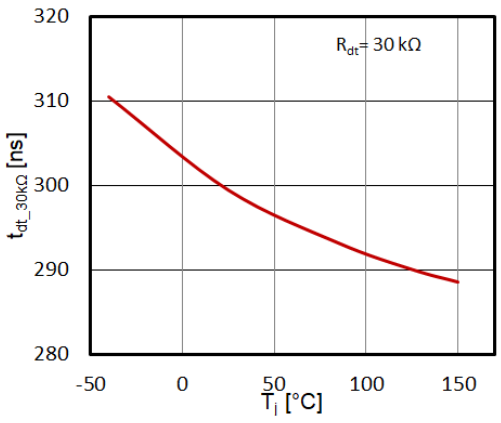
Figure 19 Typical propagation delays

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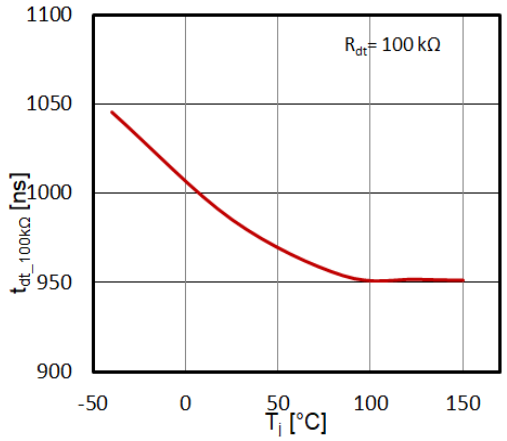
5 Typical characteristics



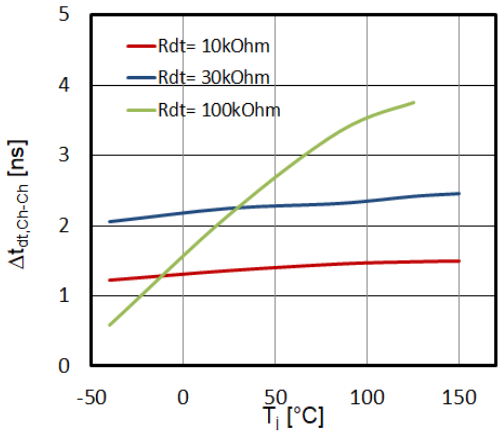
Typical Dead-time vs.
Temperature (R_{dt} = 10kΩ)



Typical Dead-time vs.
Temperature (R_{dt} = 30kΩ)



Typical Dead-time vs.
Temperature (R_{dt} = 100kΩ)



Typical channel-to-channel Dead-time
matching vs. Temperature

Figure 20 Typical Dead-time

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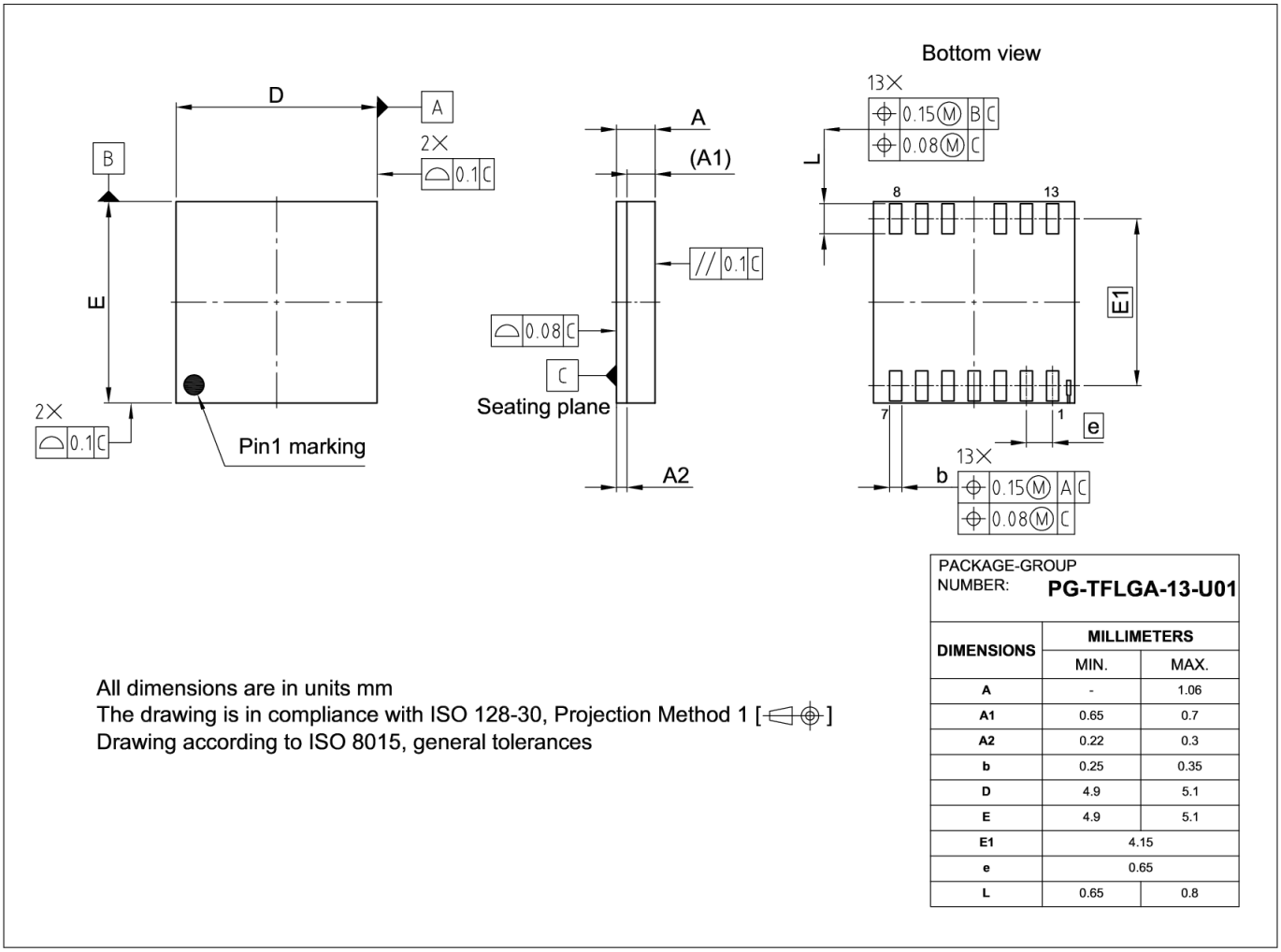
6 Package outline dimensions

6.1 Device numbers and markings

Table 23 Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
2EDB7259K	2EDB7259KXUMA1	2B7259B
2EDB8259K	2EDB8259KXUMA1	2B8259B

6.2 Package LGA5x5



PACKAGE-GROUP NUMBER: **PG-TFLGA-13-U01**

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	-	1.06
A1	0.65	0.7
A2	0.22	0.3
b	0.25	0.35
D	4.9	5.1
E	4.9	5.1
E1	4.15	
e	0.65	
L	0.65	0.8

Figure 21 LGA 5x5 package outline

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6 Package outline dimensions

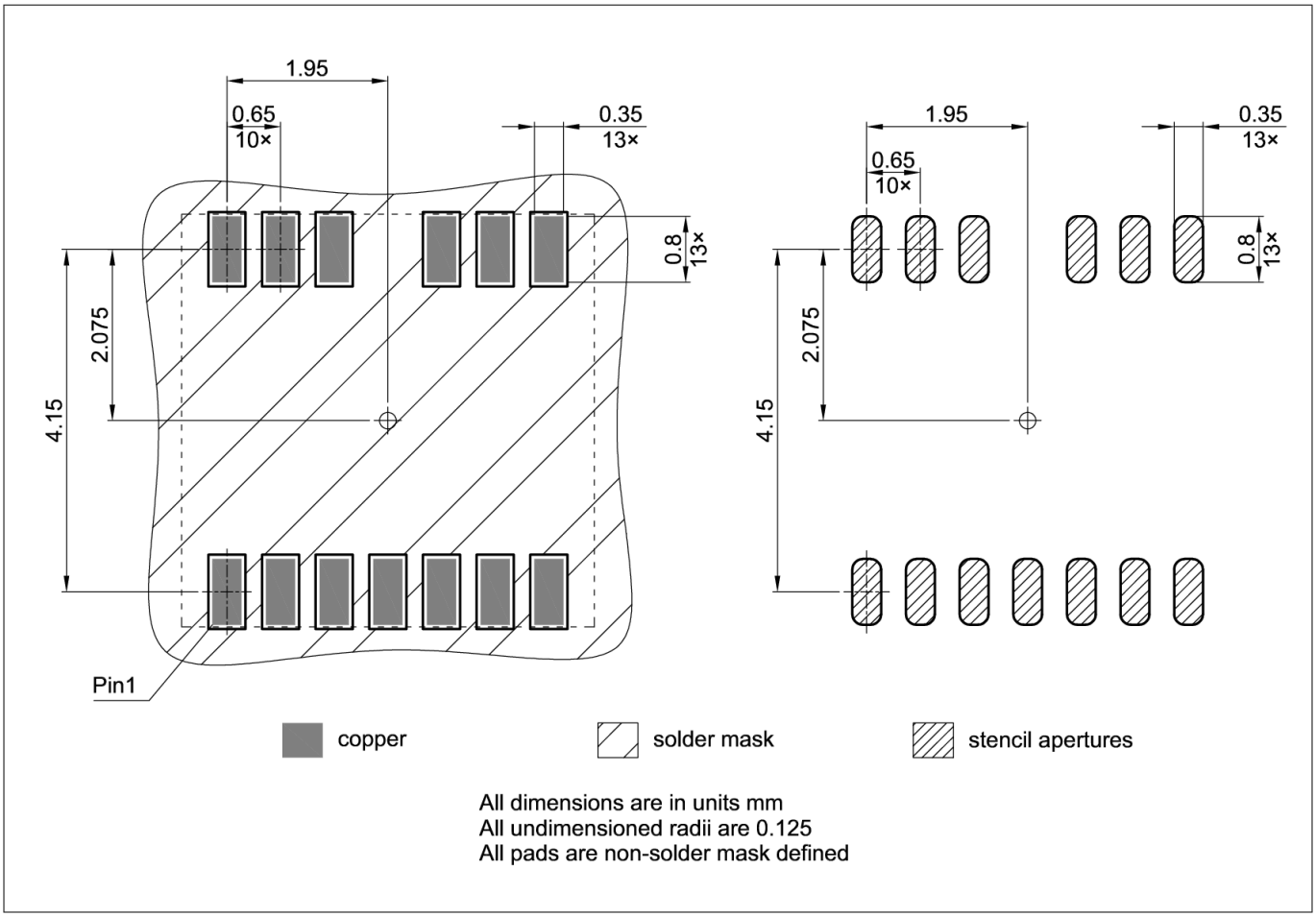


Figure 22 LGA5x5 footprint

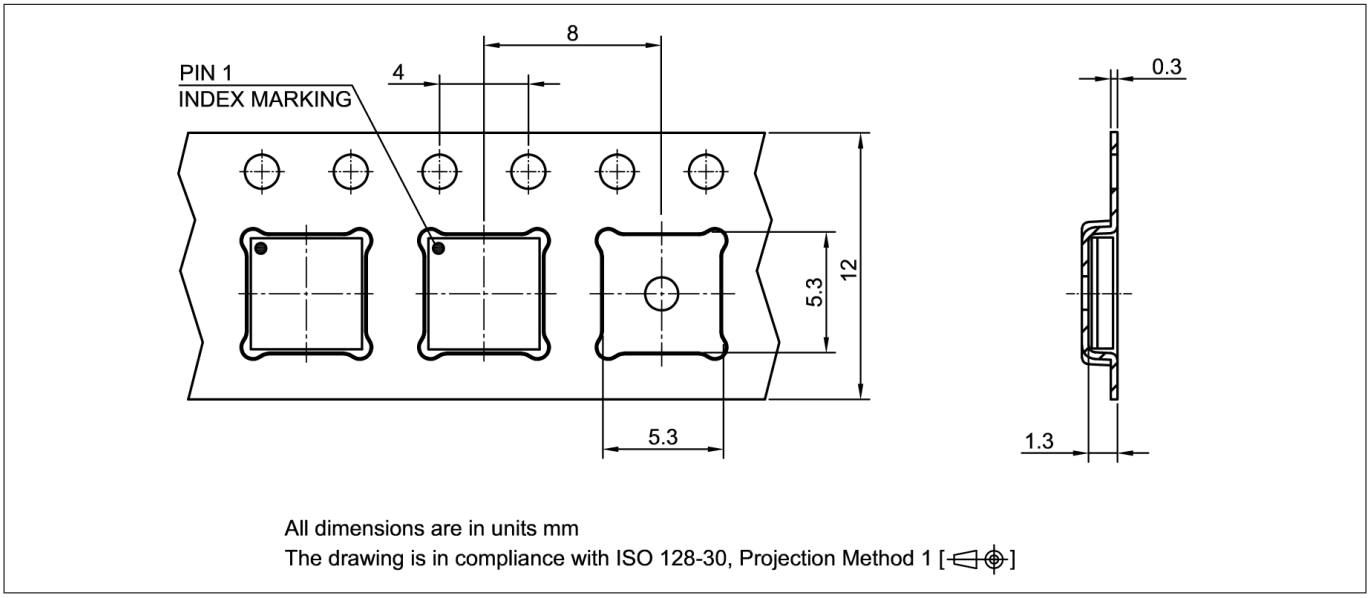


Figure 23 LGA5x5 packing

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-

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free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

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7 Revision history

Revision	Date	Description of changes
Rev 1.2	2026-04-09	Updated maximum operating voltage for V_{DDA} and V_{DDB} to 21 V in Operating range table
		Added typical value for $t_{PDon,ChA-ChB}$ and $t_{PDoff,Cha-ChB}$ in dynamic characteristics table and added active output clamp parameter in static output characteristics table
		Removed note or condition for the climatic category in isolation specifications table
		Added certification number for GB 4943.1-2022 and IEC 62368-1, added CSA component acceptance service notice no. 5A and modified features in the cover page
		Updated STP/DTC feature description
		Added thermal shutdown parameters in Electrical characteristics table
Rev 1.1	2024-03-21	Updated device marking and application drawing
		Updated typical characteristic curves
		Updated ESD CDM rating
		Updated thermal characteristics table (RthJC25_top and ΨthJT25_top) for LGA 5x5
		Removed LGA 4x4
Rev 1.0	2023-05-04	Initial release

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