AP54RHC420

Radiation-Hardened Dual Quad-SR Latch

with **cold sparing** and **Schmitt trigger inputs**

1 GENERAL DESCRIPTION

The **AP54RHC420** is a radiation-hardened by design dual quad-SR latch that is ideally suited for commercial space and other applications demanding radiation tolerance and high reliability. It delivers high resiliency to single-event effects (SEE) and to a total ionizing dose (TID).

The AP54RHC420 features Schmitt-triggered inputs. The inputs and/or outputs can be cross-strapped with no impact to operation or leakage current, which simplifies cold-sparing implementation. The redundant output stage has high drive capability with low static power loss.

Ordering information may be found in Table 10 on Page 15.

1.1 DEVICE INFORMATION

PART NUMBER	GRADE	Package
AP54RHC420ANT(1)	A-Grade Flight (LEO)	TSSOP-20 Plastic mass 74 mg
AP54RHC420BNT(1)	B-Grade Flight (LEO)	
AP54RHC420CNT(1)	C-Grade Flight (LEO)	
AP54RHC420ENT	E-Grade (Evaluation)	

(1) Release in June 2026.

1.2 APPLICATIONS

- System-level glitch latching
- Power supply transient detection
- FDIR: Fault Detection, Isolation, and Recovery
- Single-bit latching
- Discrete state machines
- SEE fault detection in non-rad hard components

1.3 FEATURES

- 5 ns transient detection at V_{CC} > 3 V
- SEL/SEFI/SET immune to LET of 75 MeV-cm^2/mg
- 1.4 V to 5.5 V operation
- Schmitt triggers on inputs
- Cold sparing Inputs and Outputs
- Single-supply Level Translation
- TID RLAT 30 krad (Si) at 5.5 V
- Operating temperature range -55 °C to +125 °C
- Meets NASA's ASTM E595 outgassing specification
- Moisture Sensitivity Level 1 (Unlimited)

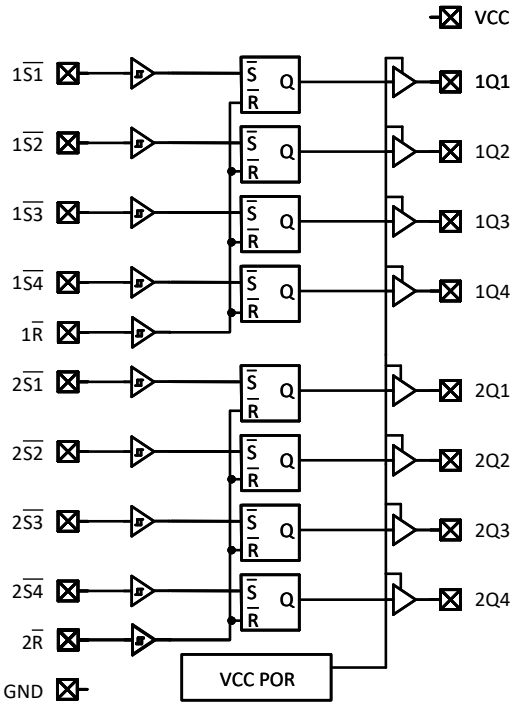


Figure 1: AP54RHC420 Logic Diagram

† See detailed note.

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2 ACRONYMS AND ABBREVIATIONS

ESD	Electrostatic Discharge
POR	Power On Reset
RHA	Radiation Hardness Assurance
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
CDM	Charged-device Model
HBM	Human-body Model

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3 LOGIC DATA

3.1 TRUTH TABLE

The AP54RHC420 truth table is found in Table 1. **H** indicates HIGH logic level and **L** indicates LOW logic level.

Table 1: AP54RHC420 Device Truth Table

Input		Output
$\overline{S}$	$\overline{R}$	Q
L	L	H
L	H	H
H	L	L
H	H	No Change

4 PIN CONFIGURATION

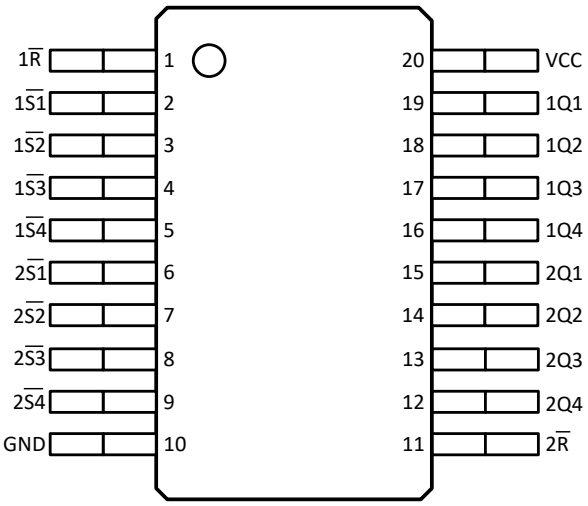


Figure 2: AP54RHC420 Device Pinout

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Table 2: AP54RHC420 Device Pinout

PIN NAME(S)	PIN NUMBER(S)	DESCRIPTION
$1\overline{S1}$	2	Active-Low Set Inputs
$1\overline{S2}$	3	
$1\overline{S3}$	4	
$1\overline{S4}$	5	
$2\overline{S1}$	6	
$2\overline{S2}$	7	
$2\overline{S3}$	8	
$2\overline{S4}$	9	
$1\overline{R}$	1	Active-Low Reset Inputs
$2\overline{R}$	11	
1Q1	19	Outputs
1Q2	18	
1Q3	17	
1Q4	16	
2Q1	15	
2Q2	14	
2Q3	13	
2Q4	12	
V_{CC}	20	Positive Voltage Supply
GND	10	Ground

5 ELECTRICAL CHARACTERISTICS

The sign convention for current follows JEDEC standards with negative values representing current sourced from the device and positive values representing current sunk into the device.

5.1 ABSOLUTE MAXIMUM RATINGS

Excursions beyond the values listed in Table 3 may cause permanent damage to the device. Proper function of the device cannot be guaranteed if these values are exceeded, and long-term device reliability may be affected. Functionality of the device at these values, or beyond those listed in Recommended Operating Conditions (Table 4) is not guaranteed.

All parameters are specified across the entire operating temperature range unless otherwise specified.

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Table 3: Absolute Maximum Ratings

SYMBOL	PARAMETER		VALUE	UNITS
V_{CC}	Supply Voltage		-0.5 to +5.5	V
V_I	Input voltage range		-0.5 to +5.5	V
V_O	Output voltage range		-0.5 to +5.5	V
I_{IK} (V_I < 0)	Input clamp current		100	mA
I_O	Continuous output current (per pin)		100	mA
I_{CC}	Maximum supply current		100	mA
V_{ESD}	ESD Voltage	HBM	1000	V
		CDM	500	V
T_J	Operating junction temperature range		-55 to +150	°C
T_{STG}	Storage temperature range		-65 to +150	°C

5.2 RECOMMENDED OPERATING CONDITIONS

All parameters are specified across the entire operating temperature range unless otherwise specified. For A-grade flight and B-grade flight parts, all parameters are specified over the entire recommended voltage range of 1.4 V to 5.5 V. For C-grade flight and E-grade Evaluation parts, all parameters are specified over the voltage range of 1.65 V to 5.5 V.

Table 4: Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage (A-grade flight, B-grade flight)		1.4	-	5.5	V
V_{CC}	Supply voltage (C-grade flight, E-grade Evaluation)		1.65	-	5.5	V
V_I	Input voltage range		0	-	5.5	V
V_O	Output voltage range		0	-	V_{CC}	V
I_{OH}	HIGH-level output current	V_{CC} = 1.4 to 1.6 V	-	-	-2	mA
		V_{CC} = 1.65 to 1.95 V	-	-	-4	
		V_{CC} = 2.3 to 2.7 V	-	-	-8	
		V_{CC} = 3.0 to 3.6 V	-	-	-16	
		V_{CC} = 4.5 to 5.5 V	-	-	-24	
I_{OL}	LOW-level output current	V_{CC} = 1.4 to 1.6 V	-	-	2	mA
		V_{CC} = 1.65 to 1.95 V	-	-	4	
		V_{CC} = 2.3 to 2.7 V	-	-	8	
		V_{CC} = 3.0 to 3.6 V	-	-	16	
		V_{CC} = 4.5 to 5.5 V	-	-	24	

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Table 4: Recommended Operating Conditions continued

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
t_{pw_rst} (1)	Minimum Pulse Width for Reset	V_{CC} = 1.4 to 1.6 V	-	15	19	ns
		V_{CC} = 1.65 to 1.95 V	-	11	18	
		V_{CC} = 2.3 to 2.7 V	-	7	16	
		V_{CC} = 3.0 to 3.6 V	-	5	14	
		V_{CC} = 4.5 to 5.5 V	-	4.5	9	
t_{pw_set} (1)	Minimum Pulse Width for Set	V_{CC} = 1.4 to 1.6 V	-	14	24	ns
		V_{CC} = 1.65 to 1.95 V	-	9.5	23	
		V_{CC} = 2.3 to 2.7 V	-	6	20	
		V_{CC} = 3.0 to 3.6 V	-	4.5	17	
		V_{CC} = 4.5 to 5.5 V	-	4.3	11	
t_{d_rst} (1) (2)	Delay after set for reset to avoid ambiguity for overlapping pulses	V_{CC} = 1.4 to 1.6 V	5.0	-	-	ns
		V_{CC} = 1.65 to 1.95 V	4.7	-	-	
		V_{CC} = 2.3 to 2.7 V	4.1	-	-	
		V_{CC} = 3.0 to 3.6 V	3.4	-	-	
		V_{CC} = 4.5 to 5.5 V	2.0	-	-	
t_{d_set} (1) (3)	Delay after reset for set to avoid ambiguity for overlapping pulses	V_{CC} = 1.4 to 1.6 V	7.9	-	-	ns
		V_{CC} = 1.65 to 1.95 V	7.5	-	-	
		V_{CC} = 2.3 to 2.7 V	6.4	-	-	
		V_{CC} = 3.0 to 3.6 V	5.2	-	-	
		V_{CC} = 4.5 to 5.5 V	2.7	-	-	

(1) guaranteed by design

(2) For t_{d_rst}, refer to Figure 7 (Detailed Description).

(3) For t_{d_set}, refer to Figure 8 (Detailed Description).

Table 5: Thermal Information

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_J	Operating junction temperature	-55	-	+125	°C
$R_{\theta JA}$	Junction to ambient thermal resistance	-	100	-	°C/W

5.3 STATIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified. For A-grade flight and B-grade flight parts, all parameters are specified over the entire recommended voltage range of 1.4 V to 5.5 V. For C-grade flight and E-grade Evaluation parts, all parameters are specified over the voltage range of 1.65 V to 5.5 V.

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Table 6: DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC}	MIN	TYP	MAX	UNITS
V_{OL}	LOW-Level Output Voltage	I_O = 100 µA	1.4 to 5.5 V	-	0.02	0.05	V
		I_O = 1 mA	1.4 to 5.5 V	-	0.05	0.15	V
		I_O = 4 mA	1.65 V	-	0.27	0.8	V
			2.3 V	-	0.3	0.6	V
			3.0 V	-	0.2	0.4	V
			4.5 V	-	0.2	0.4	V
		I_O = 8 mA	2.3 V	-	0.6	1.0	V
			3.0 V	-	0.4	0.8	V
			4.5 V	-	0.3	0.6	V
		I_O = 16 mA	3.0 V	-	1.0	1.4	V
			4.5 V	-	1.1	1.2	V
		I_O = 24 mA	4.5 V	-	1.1	1.5	V
V_{OH}	HIGH-Level Output Voltage	I_O = -100 µA	1.4 to 5.5 V	V_{CC} - 0.1	V_{CC} - 0.02	-	V
		I_O = -1 mA	1.4 to 5.5 V	V_{CC} - 0.15	V_{CC} - 0.08	-	V
		I_O = -4 mA	1.65 V	1	1.35	-	V
			2.3 V	1.8	2.0	-	V
			3.0 V	2.6	2.8	-	V
			4.5 V	4.2	4.4	-	V
		I_O = -8 mA	2.3 V	1.4	1.7	-	V
			3.0 V	2.2	2.5	-	V
			4.5 V	3.9	4.1	-	V
		I_O = -16 mA	3.0 V	1.5	2.0	-	V
			4.5 V	3.3	3.8	-	V
		I_O = -24 mA	4.5 V	3.0	3.5	-	V
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND I_O = 0 mA	1.6 V	-	43	75	µA
			1.95 V	-	48	85	µA
			3.6 V	-	125	195	µA
			5.5 V	-	247	400	µA
		V_I = V_{CC} or GND I_O = 0 mA T_a = 25°C, Post TID	5.5 V	-	527	564	µA
I_I	Input current	V_I = V_{CC} or GND	1.4 to 5.5 V	-1	-	1	µA
I_{OFF}	Powerdown leakage current(1)	V_I = V_{CC} or GND	OFF(2)	-	-	5	µA

(1) into any input or output port
(2) V_{CC} is at GND potential

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Table 7: DC Electrical Transfer Characteristics

SYMBOL	PARAMETER	V_{CC}	MIN	TYP	MAX	UNITS
V_{T+} (1)	Positive-going threshold voltage	1.40 V	0.80	0.99	1.10	V
		1.65 V	0.99	1.12	1.21	V
		2.30 V	1.35	1.54	1.65	V
		3.00 V	1.72	1.97	2.10	V
		4.50 V	2.60	2.88	3.06	V
		5.50 V	3.01	3.48	3.68	V
V_{T-}	Negative-going threshold voltage	1.40 V	0.45	0.55	0.60	V
		1.65 V	0.53	0.62	0.80	V
		2.30 V	0.76	0.87	1.10	V
		3.00 V	1.00	1.16	1.45	V
		4.50 V	1.53	1.79	2.10	V
		5.50 V	1.95	2.22	2.50	V
ΔV_T (1)	Input hysteresis (V_{T+} - V_{T-})	1.40 V	0.20	0.44	0.60	V
		1.65 V	0.32	0.50	0.62	V
		2.30 V	0.45	0.67	0.80	V
		3.00 V	0.60	0.82	1.00	V
		4.50 V	0.80	1.10	1.25	V
		5.50 V	0.95	1.26	1.42	V

(1) Tested on Set, guaranteed by similarity on Reset.

5.4 DYNAMIC CHARACTERISTICS

All parameters are specified across the entire operating temperature range unless otherwise specified. For A-grade flight and B-grade flight parts, all parameters are specified over the entire recommended voltage range of 1.4 V to 5.5 V. For C-grade flight and E-grade Evaluation parts, all parameters are specified over 1.65 V to 5.5 V.

Table 8: AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	V_{CC}	MIN	TYP	MAX	UNITS
t_{pd} (1)	Propagation Delay (Falling edge $\overline{\mathbf{S}}_\mathbf{n}$ to output **Q**)	C_L = 50 pF	4.5 to 5.5 V	-	12	16	ns
			3.0 to 3.6 V	-	20	28	ns
			2.3 to 2.7 V	-	24	34	ns
			1.65 to 1.95 V	-	27	39	ns
			1.4 to 1.6 V	-	28	41	ns
t_{pd} (1)	Propagation Delay (Falling edge $\overline{\mathbf{R}}_\mathbf{n}$ to output **Q**)	C_L = 50 pF	4.5 to 5.5 V	-	10	14	ns
			3.0 to 3.6 V	-	16	25	ns
			2.3 to 2.7 V	-	19	29	ns
			1.65 to 1.95 V	-	22	34	ns
			1.4 to 1.6 V	-	23	35	ns
C_{in}	Input Capacitance(1)	V_I = V_{CC} or GND	1.4 to 5.5 V	-	2	4	pF
C_{pd}	Power Dissipation Capacitance(1)	I_O = 0 mA f = 1 MHz	5.5 V	-	40	-	pF

(1) guaranteed by design

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5.5 RADIATION RESILIENCE

For detailed radiation testing reports, please contact Apogee Semiconductor at sales@apogeesemi.com.

Table 9: Radiation Resilience Characteristics

PARAMETER	CONDITIONS	VALUE	UNITS
Total Ionizing Dose (TID)	Please contact Apogee Semiconductor for test report.	30	krad (Si)
SEL Onset LET Threshold	Please contact Apogee Semiconductor for test report.	≥75	MeV-cm^2/mg

5.6 CHARACTERISTICS MEASUREMENT INFORMATION

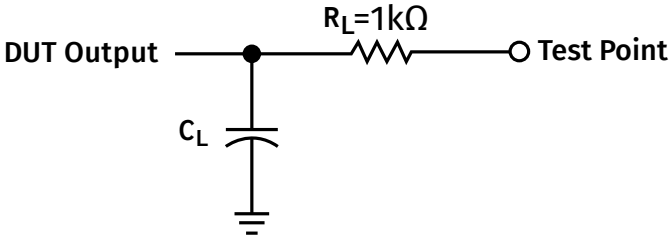


Figure 3: Load Circuit

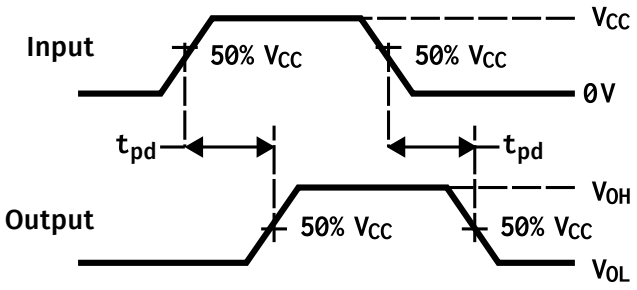


Figure 4: Propagation Delay Measurement

6 DETAILED DESCRIPTION

The AP54RHC420 is an dual quad-SR latch intended to latch short duration active low transient events. Designed to operate from a wide supply voltage of 1.4 to 5.5 V, it has fully redundant input and output stages and internal states providing for superior resiliency to single event effects, including single event upsets (SEU).

The eight SR latches are implemented as two units, each containing four individual active low set inputs, one common active low reset input and four separate outputs. The set inputs are dominant, which means that if set and reset are both active at the same time, set will prevail over reset.

Note that if the Power On Reset is active, the outputs will be tristate. On leaving POR, if both SET and RESET inputs are high , i.e. inactive, the state of the SR latches will initially be indeterminate, i.e. the Q outputs could be high or low.

A typical application for this part might be to monitor "power good" signals from PMICs, LDOs or other devices: if one of these signals transitions low for a short period, these latches can capture that event and present it for detection at the inputs of an Apogee Semiconductor APIO16 GPIO expander, which can in turn alert the control system that a transient event has been detected.

The output and input stages are constructed with transient-activated clamps (Figure 5, Figure 6) that prevent inadvertent biasing of the V_{CC} power rail through parasitic diodes inherent to conventional input, output, and ESD circuits. The IC also incorporates an internal power-on reset (POR) circuit that prevents the output from driving erroneous results during power-on, and guarantees correct operation at power supply voltages as low as 1.4 V. While the supply is ramping, the POR holds the output buffers in tri-state, a feature that prevents unwanted DC current during cold sparing on input and output pins.

The AP54RHC family's I/O protection circuitry allows for cold sparing configurations as it avoids a leakage current penalty on inputs and outputs while in a power-down state. This can result in considerable power savings in

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systems where multiple-path redundancy is employed. The ESD clamp circuits for this logic family are designed to support Class 1C ESD levels of 1 kV HBM and 500 V CDM.

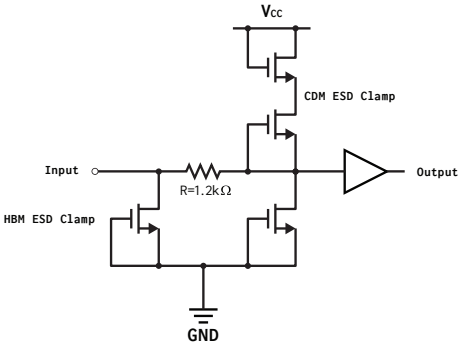


Figure 5: Input Pin Structure

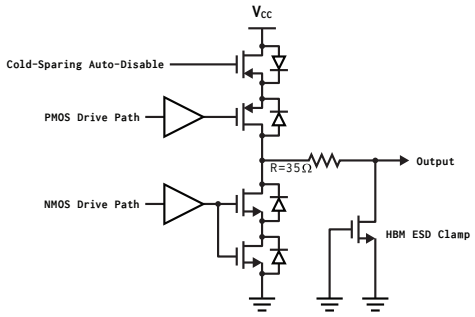


Figure 6: Output Pin Structure

6.1 OVERLAPPING $\overline{S}$ AND $\overline{R}$ PULSES

When the active-low pulses on $\overline{S}$ and $\overline{R}$ overlap, a minimum separation between their de-asserting (rising) edges is required so that the latch does not resolve to an indeterminate output state. If $\overline{S}$ de-asserts first, $\overline{R}$ must remain low for at least t_{d_rst} after $\overline{S}$ rises (Figure 7). If $\overline{R}$ de-asserts first, $\overline{S}$ must remain low for at least t_{d_set} after $\overline{R}$ rises (Figure 8).

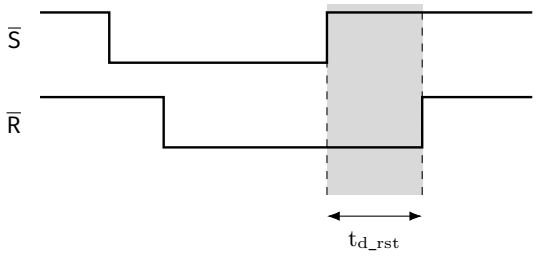


Figure 7: Overlapping pulses with long set

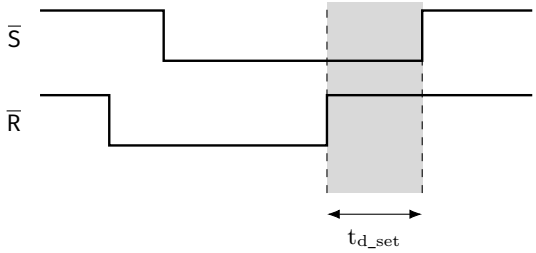


Figure 8: Overlapping pulses with long reset

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7 APPLICATIONS INFORMATION

The Schmitt trigger operation of this gate allows for it to be used in applications where input signals with slow ramps or additive noise exist. Slow rising input signals into CMOS inputs may cause “shoot-through” to occur on conventional input gates, but is resolved by the Schmitt trigger operation of the AP54RHC420 and its input hystersis that results in no input rise or fall time limitations. Additionally, the Schmitt trigger operation and level conversion offered by this IC will guarantee that gate outputs exhibit clean and fast transitions at the appropriate V_{CC} level(s).

7.1 USE IN COLD-SPARING CONFIGURATION

As the AP54RHC family is radiation-hardened by design and includes internal TMR, it can be utilized in high-reliablity applications without additional supporting circuitry or devices. Nonetheless, some application requirements call for fully-redundant designs, where an “A” and a “B” device are required, often on separate power rails.

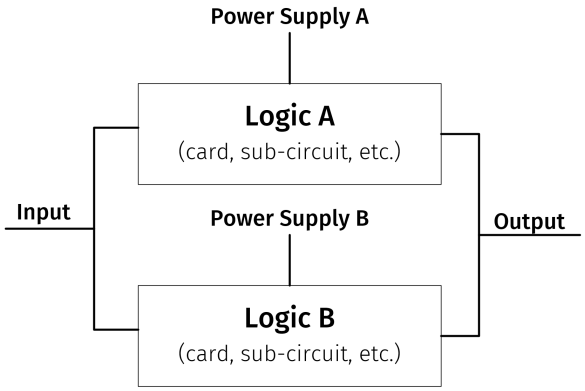


Figure 9: Two-Path Cold-Sparing Configuration

With the cold sparing capability of the AP54RHC family, fully redundant “A” and “B” functions may be placed in parallel (as seen in Figure 9) running off redundant power supplies. The inputs and outputs on each one of these functions are assumed to be based on the AP54RHC family, allowing for direct parallel connection without unwanted leakage current paths during cold sparing. In the event of a failure in power supply A or within function A, the system can simply shut power supply A off and switch on power supply B, without requiring additional input or output switching or configuration changes.

7.2 PMIC POWER GOOD LATCHING

A typical application for this part might be to monitor “power good” signals from PMICs, LDOs or other devices: if one of these signals transitions low for a short period, these latches can capture that event and present it for detection at the inputs of an Apogee Semiconductor APIO16 GPIO expander, which can in turn alert the control system that a transient event has been detected.

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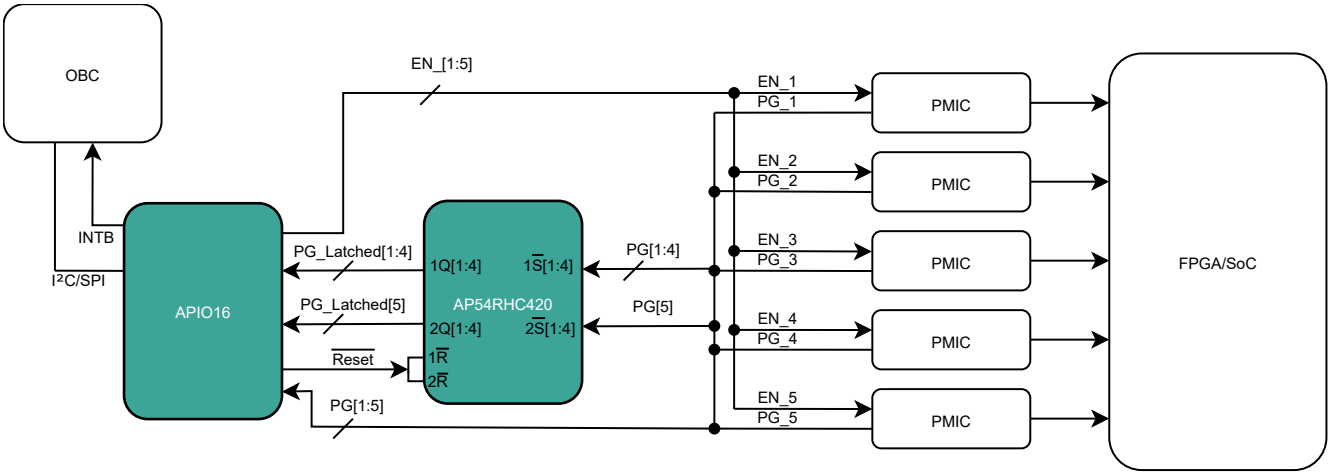


Figure 10: Latched and Unlatched PMIC Fault Detection

Figure 10 shows the AP54RHC420 used to latch the power good (PG) signals from five separate PMICs. As with the application described above, the device can capture any low transients on the PG signals so that transient faults are not missed. The diagram illustrates the AP54RHC420 interfacing with an APIO16 I/O expander, which enables the controller (OBC in the diagram) to detect faults on multiple PMICs without consuming many I/Os. The change of state of the APIO16 can trigger an interrupt to the OBC to initiate reading the APIO16.

Also shown in Figure 10 is the PG signals from the PMICs connected directly to the APIO16 through the bottom-most trace. This enables the APIO16 to monitor both the latched signals and the current value of the PG signals, so that it can diagnose both a fault and the current state of the PMICs. In the event this level of monitoring is not needed a single AP54RHC420 can be used to latch the PG signals of up to eight PMICs as shown in Figure 11.

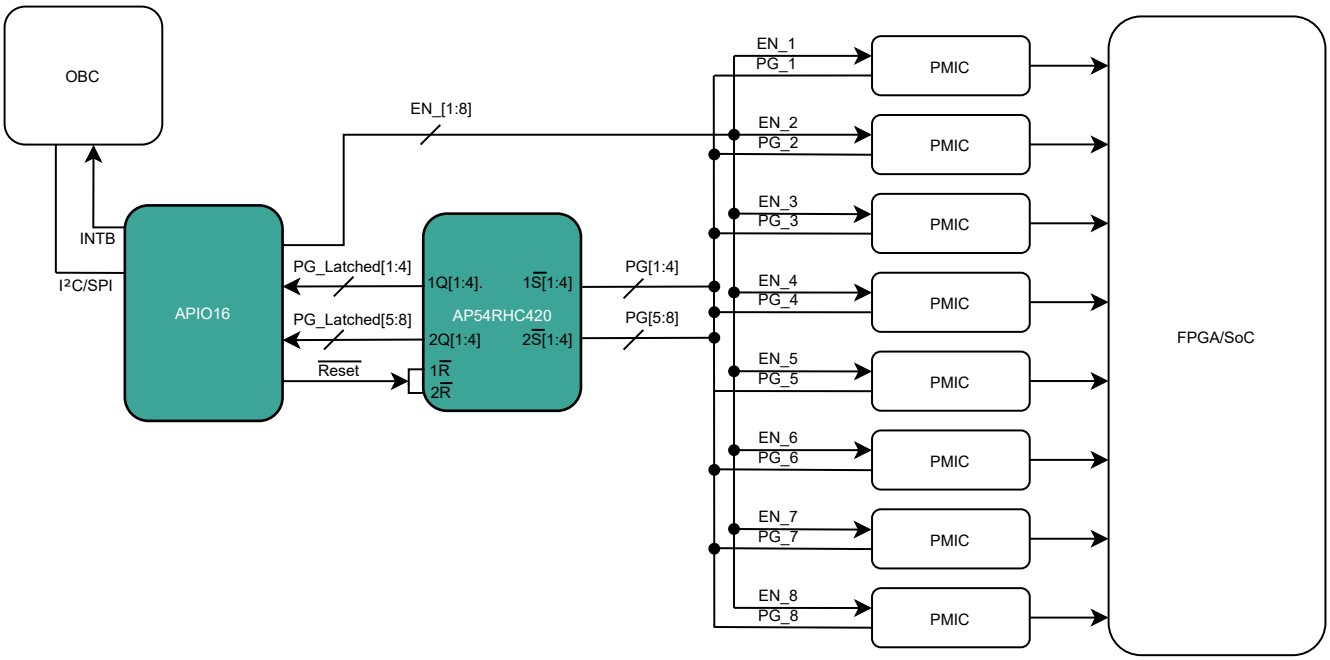


Figure 11: Latched PMIC Fault Detection

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Some systems may desire to capture transients that do not fully drive an open-drain network below the standard V_{IL} threshold at that voltage node. A solution may exist by operating the AP54RHC420 at a higher V_{CC} than the PMIC in order to scale the minimum V_{T-} to a higher value. Additionally, adjusting the pull-up rail voltage on the open-drain network must ensure that the voltage seen when the signal is high impedance is above the V_{T+} threshold.

7.3 POWER SUPPLY RECOMMENDATIONS

This device can operate at any voltage within the range specified in Table 4 Recommended Operating Conditions.

At a minimum, a 16 VDC (or higher), X7R-rated 0.1 µF ceramic decoupling capacitor should be placed near (within 1 cm) the V_{CC} pin of the device.

7.4 APPLICATION TIPS

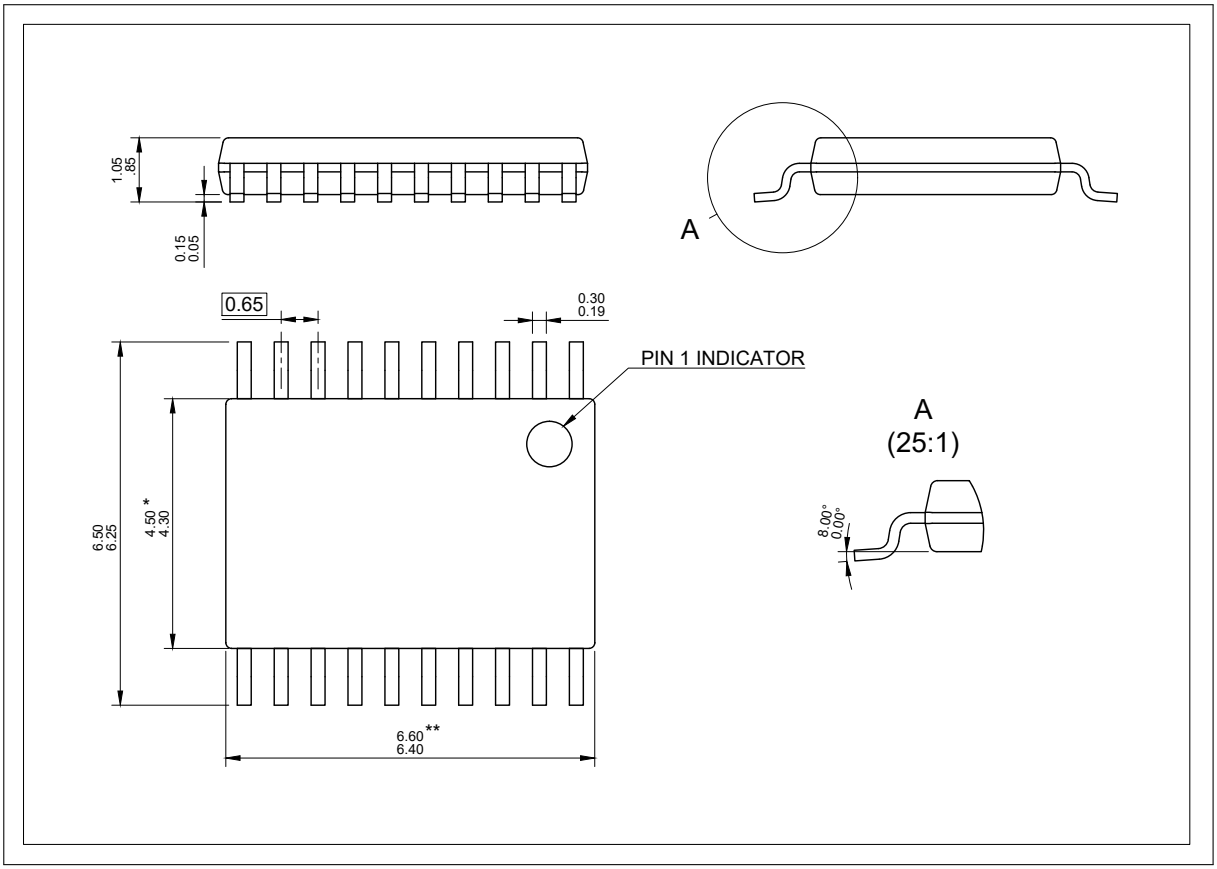
Unused **inputs** must **not** be left floating. They may be connected to either a low (GND) or high (V_{CC}) bias to provide a known state at the input of the device. Resistors may be used to tie off unused inputs. In the event of a design change, such resistors can be removed, thereby allowing use of the inputs without having to cut traces on the PCB.

An unused **output** may be left floating. It is suggested that it be routed to a test point or similar accessible structure in case the gate needs to be utilized as part of a design revision.

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8 PACKAGING INFORMATION



Notes:
1. All linear dimensions are in millimeters. Dimensioning and tolerancing are as per ISO/TS 128-71:2010
2. The part is compliant with JEDEC MO-153 specifications.

* Body width does **not** include interlead flash. Interlead flash shall not exceed 0.25 mm each side.
** Body length does **not** include mold flash, protrusion, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 mm on each side.

Figure 12: 20-NT - Package Mechanical Drawing (NiPdAu)

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9 ORDERING INFORMATION

Example part numbers for the AP54RHC420 are listed in Table 10. The full list of options for this part can be found in Figure 13. For a detailed description of product grades, please refer to Product Grades and Quality Flows document. Please contact Apogee Semiconductor sales at sales@apogeesemi.com for further information on sampling, lead time and purchasing on specific part numbers.

Table 10: AP54RHC420 Ordering Information

DEVICE	DESCRIPTION	PACK-AGING	PACKAGE	LEAD FINISH	STATUS
AP54RHC420ANT-R	Rad-Hard Dual Quad-SR Latch (A-Grade Flight)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC420BNT-R	Rad-Hard Dual Quad-SR Latch (B-Grade Flight)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC420CNT-R	Rad-Hard Dual Quad-SR Latch (C-Grade Flight)	Reel	TSSOP-20	NiPdAu	Plan Rls JUN-2026
AP54RHC420ENT-R	Rad-Hard Dual Quad-SR Latch (E-Grade for Evaluation)	Reel	TSSOP-20	NiPdAu	Available

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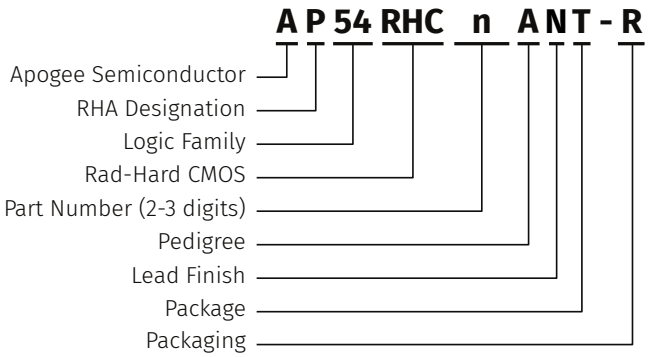


Figure 13: Part Number Decoder

1. RHA Designation
   - **P** 30 krad (Si)
   - **F** 300 krad (Si)
2. Part Number
   - **_** 420 (Dual Quad-SR Latch)
3. Pedigree
   - **A** -55 to +125 °C (Burn-in)
   - **B** -55 to +125 °C (No burn-in)
   - **C** 25 °C (No burn-in)
   - **E** 25 °C Functional Test Only (Evaluation)
4. Lead Finish
   - **N** Nickel-Palladium-Gold (NiPdAu)
5. Package
   - **T** 20-pin Thin Shrink Small Outline Package (TSSOP-20)
6. Packaging
   - **R** Tape and Reel[(1)]

(1) Contact us for custom reel quantities. Orders less than full reel quantities may be shipped as cut tape.

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10 REVISION HISTORY

REVISION	DESCRIPTION	DATE
B00	Initial Release.	2026-May-06

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11 LEGAL

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