

### General Description

- Trench Power AlphaSGT™ technology
- Low  $R_{DS(ON)}$
- Low Gate Charge
- ESD protected

### Applications

- High efficiency power supply
- Secondary synchronus rectifier

### Product Summary

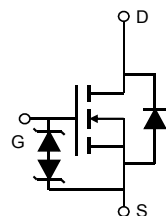
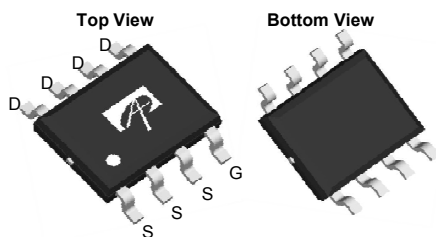
$V_{DS}$	60V
$I_D$ (at $V_{GS}=10V$ )	16.5A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 6.5mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 8.5mΩ

Typical ESD protection **HBM Class 2**

100% UIS Tested  
100% Rg Tested



SOIC-8



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AO4262E	SO-8	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	16.5	A
	$T_A=70^\circ\text{C}$	13.0	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	65	A
Avalanche Current <sup>C</sup>	$I_{AS}$	23	A
Avalanche energy $L=0.3\text{mH}$ <sup>C</sup>	$E_{AS}$	79	mJ
$V_{DS}$ Spike <sup>G</sup>	$V_{SPIKE}$	72	V
	$10\mu\text{s}$		
Power Dissipation <sup>B</sup>	$P_D$	3.1	W
	$T_A=70^\circ\text{C}$	2.0	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		59	75	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

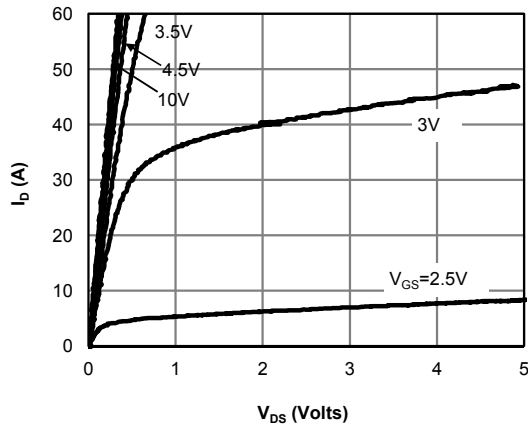
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.65	2.2	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =16.5A T <sub>J</sub> =125°C		5.2 8.3	6.5 10.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =14.5A		6.6	8.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =16.5A		70		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz		1652		pF
C <sub>oss</sub>	Output Capacitance			520		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			52		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.6	1.3	2.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =16.5A		30	45	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			15	25	nC
Q <sub>gs</sub>	Gate Source Charge			3.5		nC
Q <sub>gd</sub>	Gate Drain Charge			6.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =1.8Ω, R <sub>GEN</sub> =3Ω		6		ns
t <sub>r</sub>	Turn-On Rise Time			5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			29		ns
t <sub>f</sub>	Turn-Off Fall Time			7		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =16.5A, di/dt=500A/μs		19		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =16.5A, di/dt=500A/μs		60		nC

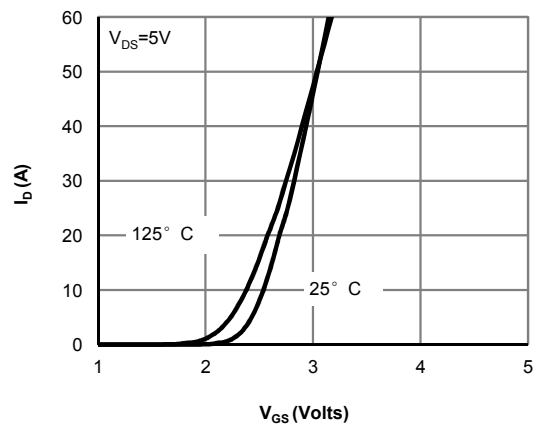
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.
- G. The spike duty cycle 5% max, limited by junction temperature T<sub>J(MAX)</sub>=125° C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

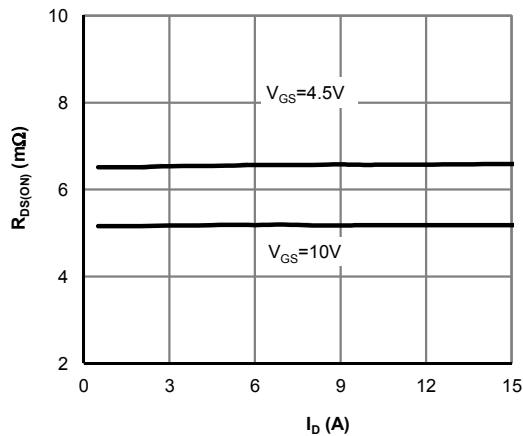
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



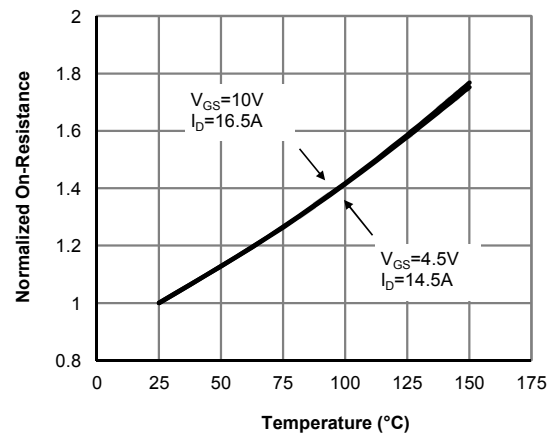
**Figure 1: On-Region Characteristics (Note E)**



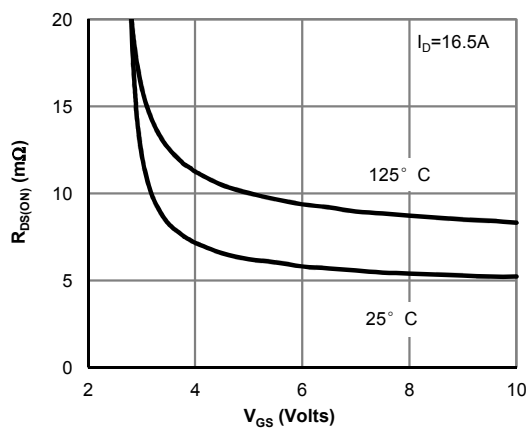
**Figure 2: Transfer Characteristics (Note E)**



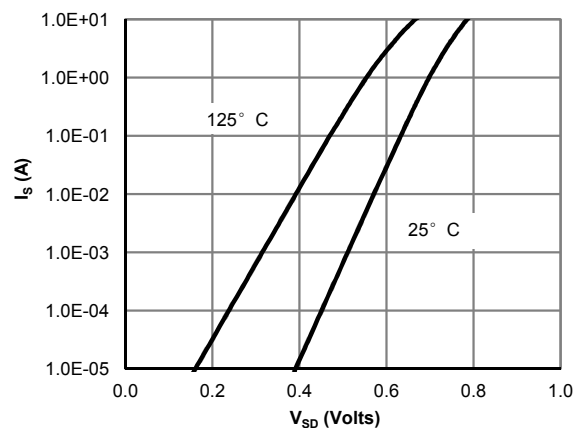
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

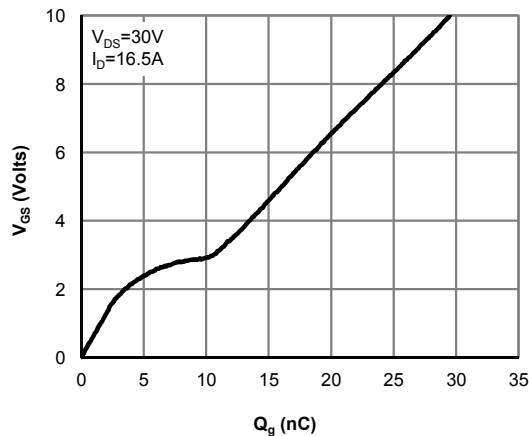


Figure 7: Gate-Charge Characteristics

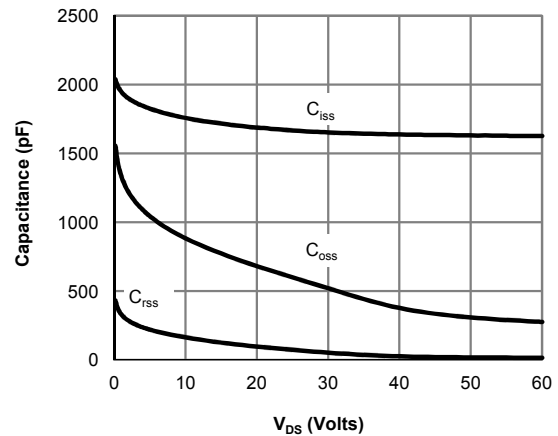


Figure 8: Capacitance Characteristics

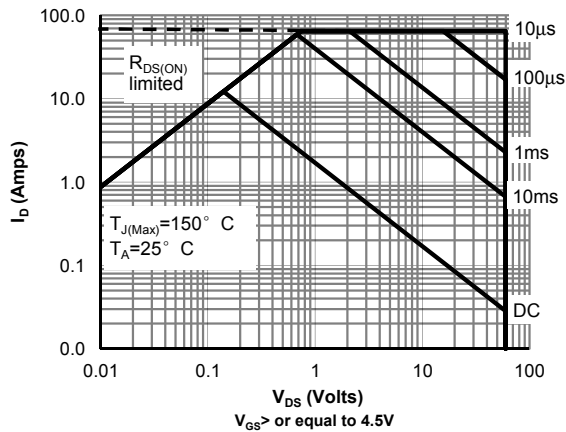


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

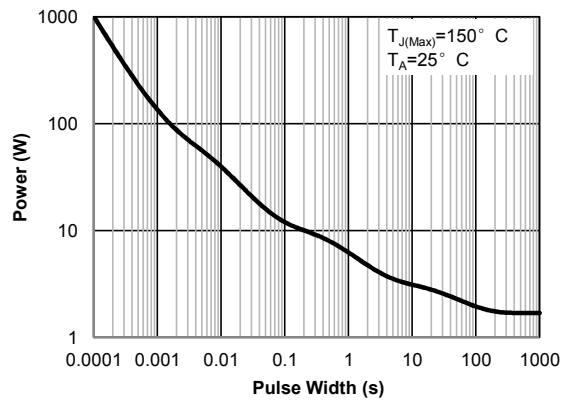


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

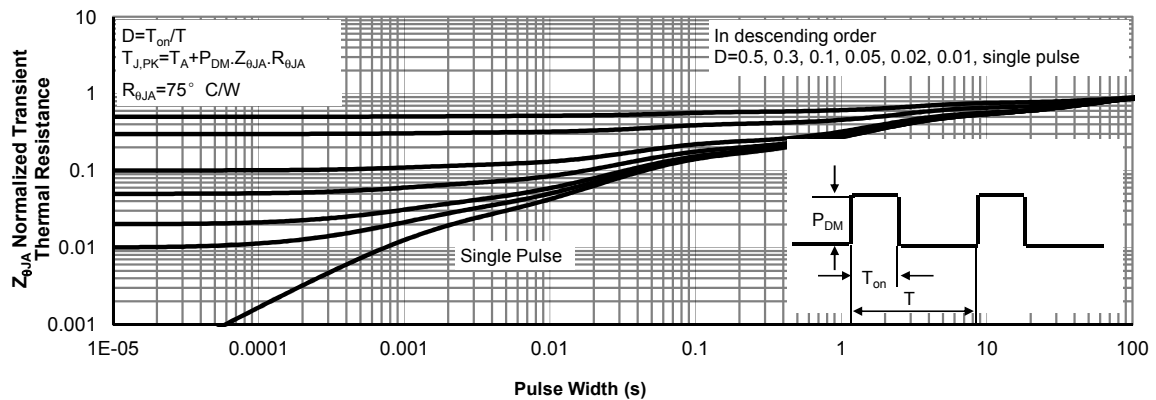


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

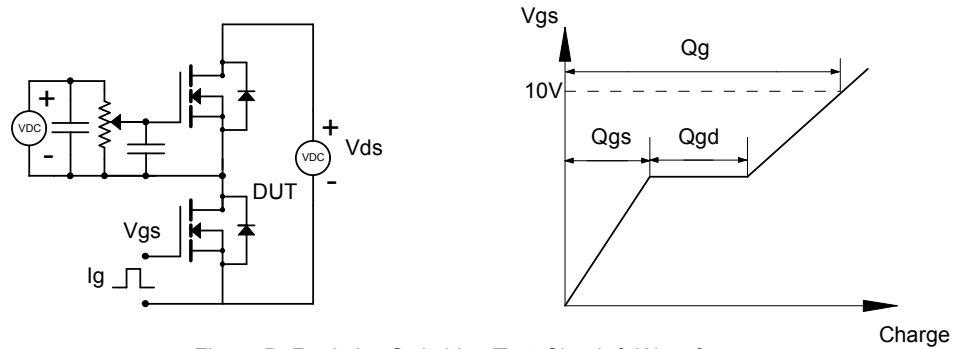


Figure B: Resistive Switching Test Circuit & Waveforms

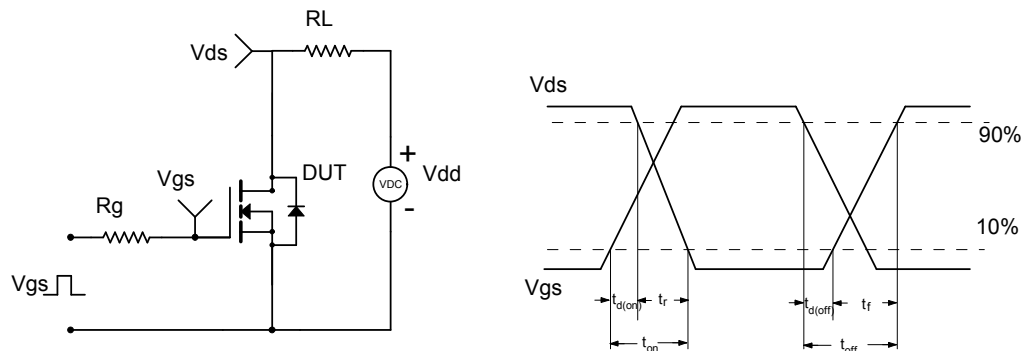


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

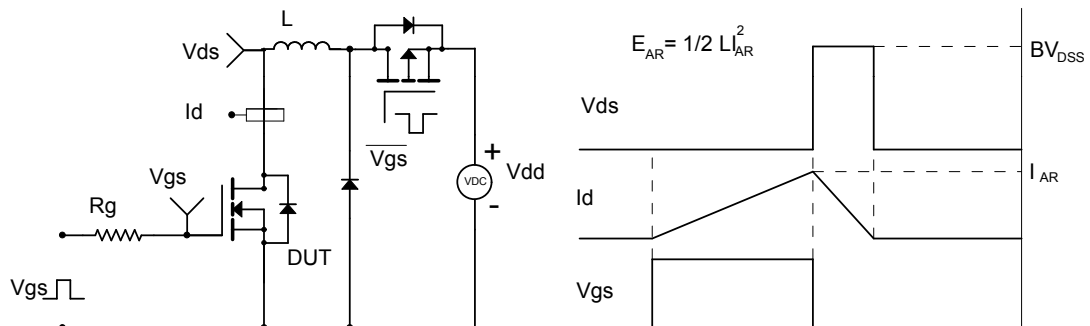


Figure D: Diode Recovery Test Circuit & Waveforms

