PI3HDMI621

2:1 Active HDMI™1.4 Sink-side Switch with Integrated ARC and Fast Switching Support

Features

- HDMI 1.4 compliant
- Operation up to 3.4 Gbps per lane(340 MHz pixel clock) to support 4K x 2K @24Hz (297 MHz) and 3D video format (1080p, 1080i and 720p)
- Support up to 48-bit per pixel Deep Color™
- Integrated ARC(Audio Return Channel) and Rx Sense function
- Fast switching between two HDMI input ports
- Programmable equalizer, emphasis and amplitude settings to achieve optimized HDMI signal integrity
- Each input can be AC coupled or DC coupled, while the output will maintain TMDS compliance DC coupled, current steering signals
- Idle clock detection function for output squelch and auto standby
- Integrated ESD protection on I/O pins to connector
  - 8 KV contact per IEC61000-4-2, level 4
  - 8 KV HBM
- Industrial temperature coverage
- Packaging (Pb-free & Green): 48-contact LQFP (FB)

Description

PI3HDMI621 is 2:1 active switch that supports HDMI 1.4 specification with data rate up to 3.4 Gbps.

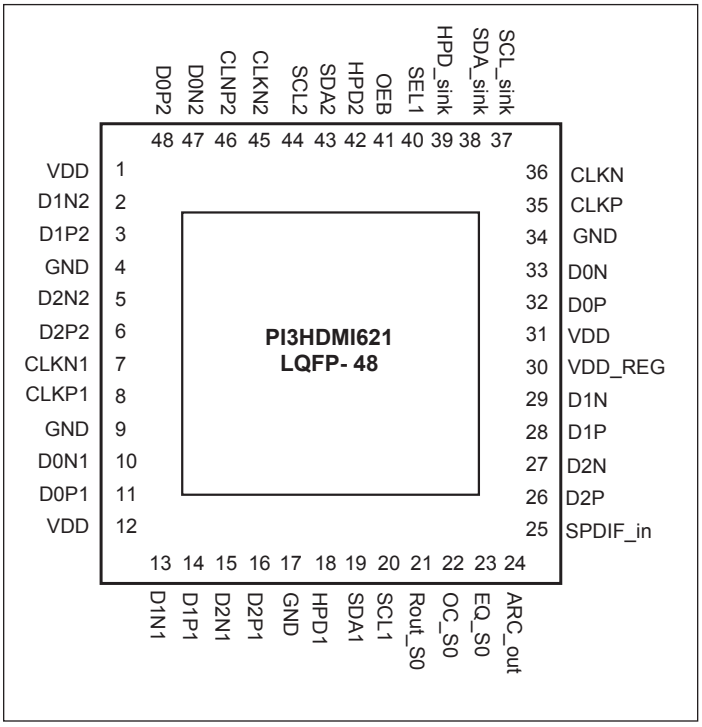
The I^2C configuration function with multiple system control signal integration of DDC channel MUX, Hot Plug Detection DEMUX, cable plug-unplug detection and HDMI 1.4 ARC transmitter help to save the extra requirement of GPIO control pins or control chip and provide optimized trace routing and component reduction.

Programmable termination settings at TMDS input help to avoid the compatibility issue caused by non standard HDMI source to determine the connection status of TMDS channel with proper termination voltage setting. The programmable output termination setting supports double termination option between PI3HDMI621 and the HDMI receiver chip to ease the reflection effect caused by improper impedance matching design and reducing jittery signals.

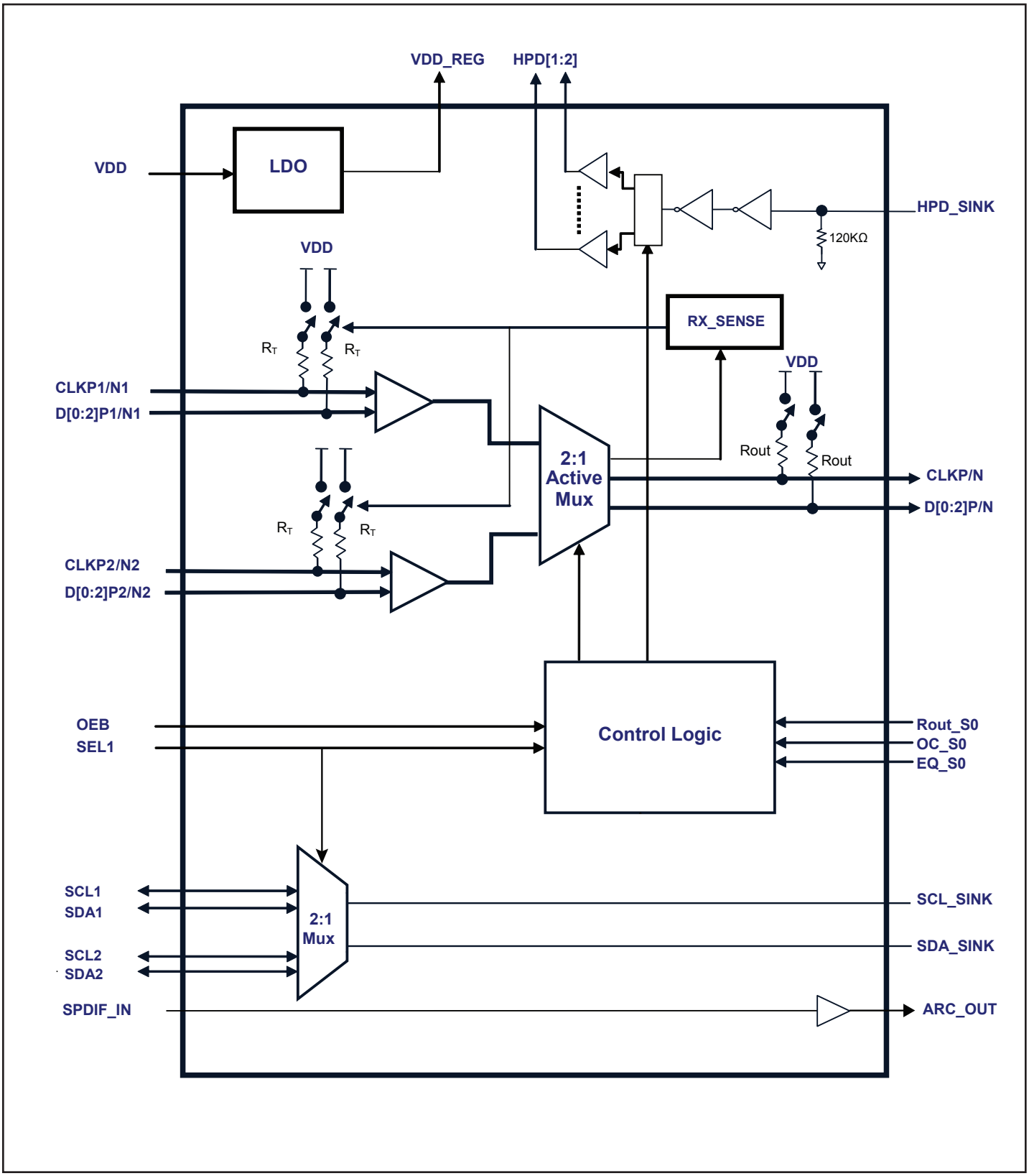
PI3HDMI621 integrates ARC and supports video fast switching among HDMI ports.

The device is fully compatible with HDMI 1.4 and supports backward compatibility to the DVI 1.0 standard.

Pin Configuration



Functional Block Diagram



Pin Description

Pin #	Pin Name	Type [1]	Description
39	HPD_SINK	I	Sink side hot plug detector input; internal pull-down at 120K ohm.
18	HPD1	O	Port 1 HPD output
42	HPD2	O	Port 2 HPD output
7 8 10 11 13 14 15 16	CLKN1 CLKP1 D0N1 D0P1 D1N1 D1P1 D2N1 D2P1	I	Port 1 TMDS inputs. Rt=50 Ohm
45 46 47 48 2 3 5 6	CLKN2 CLKP2 D0N2 D0P2 D1N2 D1P2 D2N2 D2P2	I	Port 2 TMDS inputs. Rt=50 Ohm
36 35 33 32 29 28 27 26	CLKN CLKP D0N D0P D1N D1P D2N D2P	O	TMDS outputs. Rout=50 Ohm when Rout_S0=High
20	SCL1	IO	Port 1 DDC Clock
44	SCL2	IO	Port 2 DDC Clock
19	SDA1	IO	Port 1 DDC Data
43	SDA2	IO	Port 2 DDC Data
37	SCL_SINK	IO	Sink side DDC Clock
38	SDA_SINK	IO	Sink side DDC Data
21	Rout_S0	I	TMDS output termination selection. If HIGH or floating, then 50 Ohm is present on TMDS output pins. if LOW, then 50 Ohm is not present on TMDS output pins. This pin has internal 100 KOhm pull-up
41	OEB	I	Output Enable control. Active low. Internal 100 KOhm pull-down. See truth table for functionality.
22	OC_S0	I	TMDS output pre-emphasis selection. See OC_S0 truth table for functionality. This pin has internal 100 KOhm pull-up

Pin Description

Pin #	Pin Name	Type [1]	Description
23	EQ_S0	I	TMDS input equalization selection. If LOW or floating , EQ is set at 9 dB for all TMDS data inputs If HIGH, EQ is set at 15 dB for all TMDS data inputs (please note, TMDS clock inputs are always set to 3 dB eq). This pin has an internal 100 KOhm pull-low
40	SEL1	I	PORT1 or PORT2 selection. Please see truth table for functionality This pin has an internal 100K Ohm pull-up
25	SPDIF_IN	I	Single mode ARC signal input
24	ARC_OUT	O	Single mode ARC signal output
1, 12, 31	VDD	P	3.3V power supply
30	VDD_REG	P	LDO output for internal core power supplier. External capacitor 2.2 to 4.7 µF should be added to GND.
4, 9, 17, 34	GND	G	Supply Ground

Note

1. I = Input, O = Output, IO = Bidirectional, P = Power, G = Ground.

Description of Operation

Squelch function:

Squelch control is using low frequency clock signal detection method. When TMDS input clock frequency is less than 10 MHz or less than 50 mV, power-down mode will initiate to save power.

Rx-SENSE detector:

This device searches for 50 Ohm termination present in the other side of HDMI Receiver. If the 50 Ohm is not present in the other side, the device determine no valid HDMI receiver chip is connected. Then, this device will turn off 50 Ohm input termination resistors for all TMDS data and clock pairs and enter into the power-down mode.

OC_S0 Truth Table (Swing setting 500 mV as default)

TMDS output pre-emphasis setting		Setting Value	
Rout_S0 (internal pull-up)	OC_S0 (internal pull-up)	Single-end Vswing (mV)	Pre-emphasis (dB)
0	0	500	0 (open drain)
0	1	500	2.5 (open drain)
1	0	500	0 (double termination)
1	1	500	2.5 (double termination)

Note

1. open drain (Rout off); double termination (Rout on).
2. TMDS CLK pre-emphasis value is fixed to 0 dB.

Port Selection Truth Table

OEB (Internal pull-down)	SEL1	TMDS port	DDC port	HPD port
0	1	CLKN/P1, D0N/P1, D1N/P1,D2N/P1	SCL1/SDA1	HPD1
0	0	CLKN/P2, D0N/P2, D1N/P2,D2N/P2	SCL2/SDA2	HPD2
1	X	OFF	Follow SEL1	Follow SEL1

EQ_S0 Truth Table

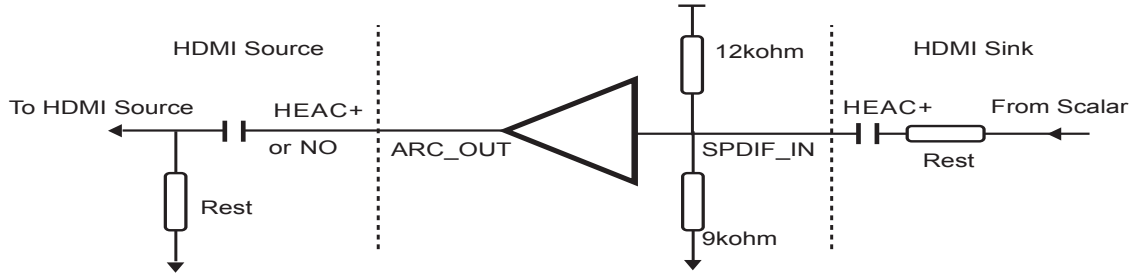
EQ_S0 (Internal pull-down)	Operation
0	9 dB
1	15 dB

Note

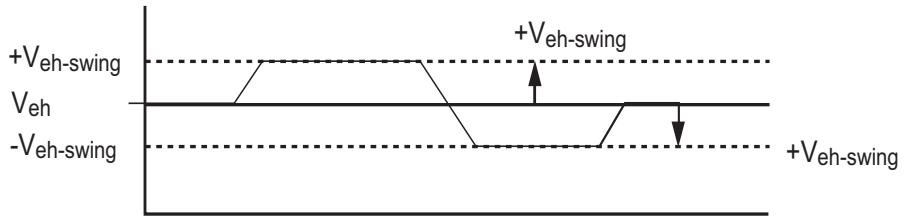
1. For TMDS CLK channels, the EQ value is fixed to 3dB.

Audio Return Channel(ARC):

There are two ARC input modes, common mode and single mode input. This device can supports "single mode input" only.

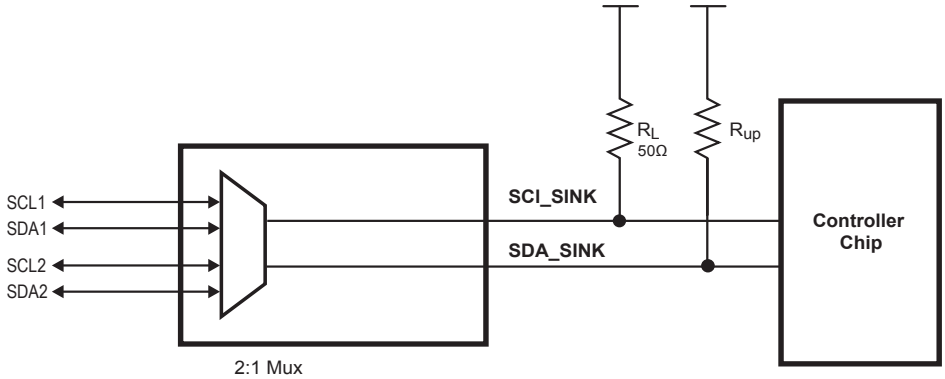


ARC single mode input and output



V_{eh} = 0~5V
$+V_{eh\text{-}swing}$ = 250mV
$-V_{eh\text{-}swing}$ = 250mV

ARC single mode signal output waveform



DDC Channel Application Diagram

Absolute Maximum Ratings

Item	Rating
Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Note: Stress beyond those lists under "Absolute Maximum Ratings" may cause permanent damage to the device

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		85	°C
Power Supply Voltage (measured in respect to GND)	3.0		3.6	V

DC Specification (V_{DD} = 3.3 ± 10%)

Parameter	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	VDD Supply Current	Output Enable (open drain 500 mV single-ended 0 dB pre-emphasis)		120	150	mA
		Output Enable (double termination, 500 mV single-ended 0 dB pre-emphasis)		190	230	mA
Idd_Squelch	Supply Current in squelch mode	Input TMDS signal is not valid		11	13	mA
Idd_Rx sense	Supply current when no 50ohm detected in Rx	Input TMDS is valid, 50 Ohm Rx is not detected		4	5	mA
I_{stb}	Standby mode	V_{DD} = 3.6V, HPD_x = 0, Arc_out = 0, OEB = High		4	5	mA
V_{OL_HPD}	Open Drain Output Low Voltage	I_{OL} = 4 mA	0		0.4	V
I_{OFF_HPD}	Off leakage current	V_{DD} = 0, V_{IN} = 3.6V			20	µA
		V_{DD} = 0, V_{IN} = 5.5V			40	
I_{OZ_HPD}	Open drain Output leakage current	V_{DD} = 3.6, V_{IN} = 3.6V			20	
		V_{DD} = 3.6, V_{IN} = 5.5V			40	

HPD_SINK

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level digital input current	V_{IH} = VDD	25		40	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage	V_{DD} = 3.3V	2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V

Control Pin (OEB)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	High level digital input current	V_{IH} =VDD	30		45	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-10		10	µA
V_{IH}	High level digital input voltage		2.0			V
V_{IL}	Low level digital input voltage		0		0.8	V

DDC Channel Block

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LK}	Input leakage current	DDC switch is off	-10		40	µA
C_{IO}	Input/Output capacitance	V_I peak-peak = 1V, 100 KHz		10		pF
R_{ON}	On resistance	I_O = 3mA, V_O = 0.4V		25	50	Ω
V_{pass}	Switch Output voltage	V_I=3.3V, I_I=100uA V_{DD}=3.3V	1.5	2.0	2.5	V
V_{OH_DDC} (source/sink)	DDC Switch Output High Voltage	V_{IN}=3.3V. External pull-up Rup to V_{DD} from 1.5 KΩ to 5 KΩ	V_{DD} - 1			V

SPDIF & ARC Pins, See ARC single mode waveform

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH_SPDIF}	High level input current	Vdd=3.6V, V_{IH} =3.6V		500		µA
I_{IL_SPDIF}	Low level input current	Vdd=3.6V, V_{IL} = GND		-350		µA
Vel	Single mode input/output Vel DC voltage level		0		5.0	V
Vel swing SPDIF	Single mode input swing		0.2		0.6	V
Vel swing ARC_ OUT	Single mode ARC output swing		0.4	0.5	0.6	V
R_O	Output resistance of ARC output stage			55		Ω
t_r	ARC output rise time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz)			25	ns
t_f	ARC output fall time (10% to 90%)	< 0.4UI (f_{clock} = 6.144MHz)			25	ns
T_{Jpp}	ARC signal peak to peak jitter	< 0.4UI (f_{clock} = 6.144MHz)			3	ns
I_{OZ}	Leakage current with Hi-Z I/O	V_{DD} = 3.6V			10	µA

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Single-ended high level output voltage	V_{DD} = 3.3V, Rout=50Ω	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended low level output voltage		V_{DD}-600		V_{DD}-400	mV
V_{swing}	Single-ended output swing voltage		400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage (1)				180	mV
$V_{OD(U)}$	Undershoot of output differential voltage (2)				200	mV
$V_{OD(U)}$	Change in steady-state common-mode output voltage between logic				5	mV
I_{OS}	Short Circuit output current		-12		12	mA
	Short Circuit output current at double termination mode		-24		24	mA
$V_{I(open)}$	Single-ended input voltage under high impedance input or open	I_I = 10uA	V_{DD}-10		V_{DD}+10	mV
R_T	Input termination resistance	V_{IN} = 2.9V	45	50	55	Ω

Note:

1. Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%
2. Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

AC Characteristics (Over recommended operating conditions unless otherwise noted)

TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
tpd	Propagation delay	V_{DD} = 3.3V, Rout = 50 Ohm			2000	ps
t_r	Differential output signal rise time (20% - 80%)				190	
t_f	Differential output signal fall time (20% - 80%)				190	
$t_{sk(p)}$	Pulse skew			10	50	
$t_{sk(D)}$	Intra-pair differential skew			23	50	
$t_{sk(o)}$	Inter-pair differential skew				100	
$t_{jit(pp)}$	Peak-to-peak output jitter CLK residual jitter	CLK Input = 165 MHz clock		15	30	
$t_{jit(pp)}$	Peak-to-peak output jitter DATA Residual Jitter			18	50	
t_{SX}	Select to switch output				10	
t_{en}	Enable time				1000	ns
t_{dis}	Disable time				10	ns

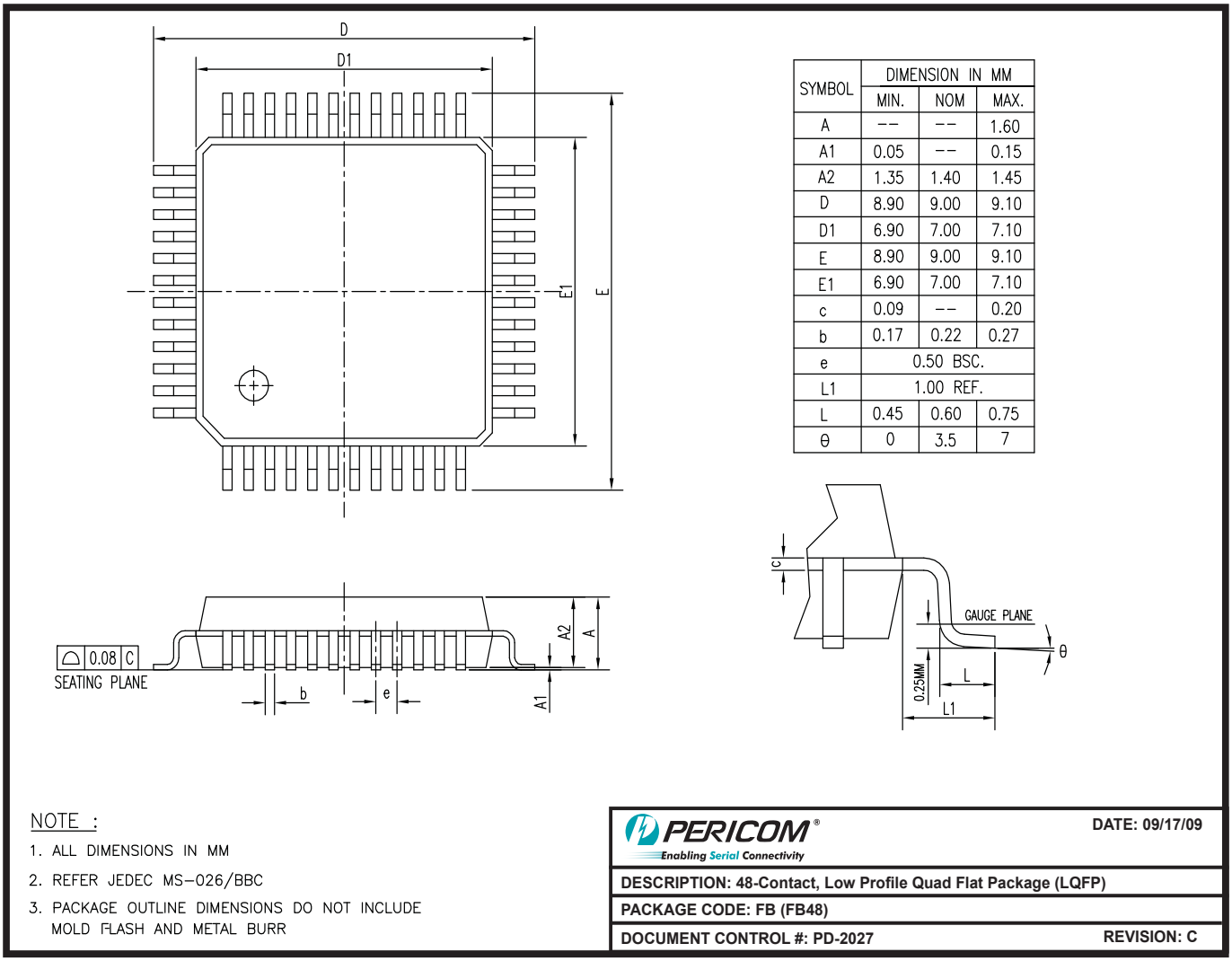
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd(DDC)}$	Propagation Delay	C_L = 10pF		0.4	2.5	ns

Control and Status Pins (HPD_SINK, HPD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd(HPD)}$	Propagation Delay	C_L = 10pF, Pull-up resistor=1 KOhm Open drain output		10		ns
$t_{sx(HPD)}$	Select to switch output			10		ns

Packaging Mechanical: 48-Contact LQFP (FB)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.90	7.00	7.10
c	0.09	--	0.20
b	0.17	0.22	0.27
e	0.50 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
θ	0	3.5	7

NOTE :

1. ALL DIMENSIONS IN MM
2. REFER JEDEC MS-026/BBC
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR

PERICOM Enabling Serial Connectivity

DATE: 09/17/09

DESCRIPTION: 48-Contact, Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FB (FB48)

DOCUMENT CONTROL #: PD-2027 REVISION: C

09-0012

Please check for the latest package information on the Pericom web site at www.pericom.com/packaging/

Related Products

Part Number	Product Description
PI3EQXDP1201	DisplayPort 1.2 Re-driver with built-in AUX listener
PI3VDP1430	Dual Mode DisplayPort to HDMI Level Shifter and Re-driver
PI3HDMI511	3.4Gbps HDMI 1.4 Re-driver for Source-side application, supporting Dual Mode DisplayPort
PI3HDMI611	3.4Gbps HDMI 1.4 Re-driver for Sink-side application, supporting Dual Mode DisplayPort
PI3VDP3212	2-Lane DisplayPort 1.2 Compliant Switch
PI3VDP12412	4-Lane DisplayPort 1.2 Compliant Switch
PI3HDMI412AD	1:2 Active 3.4Gbps HDMI 1.4 compliant Splitter/Re-driver
PI3HDMI521	2:1 Active 3.4Gbps HDMI 1.4 Switch with built-in ARC and Fast Switching support for Source-side Application
PI3HDMI336	3:1 Active 3.4Gbps HDMI 1.4 Switch/Re-driver with I^2C control and ARC Transmitter

Reference Information

Document	Description
VESA	VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010 VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012 VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
HDMI	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDMI621FBE	FB	Pb-free & Green 48-Contact LQFP

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**

Revision History

Date	Changes