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3 MHz, 1.6 A, PWM Synchronous Buck Converter

High Efficiency, PWM Only, Low Ripple, Fixed Output Voltage

NCV6323F-xx

NCV6323F is a synchronous Buck converter optimized to supply different sub−systems from a pre−regulator supply rail in the 2.8 V to 5.5 V range. The device is able to deliver up to 1.6 A DC (85°C ambient temperature) on a fixed output voltage. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Technology and internal structure allows the IC to operate from a wide input voltage range. Synchronous rectification offers improved system efficiency and integrated feedback network allows very simple and straightforward implementation to power supply designers with only a few components to select.

The NCV6323F is housed in in a space saving Wettable flank DFN8, 2x2 mm (0.8 mm thickness), 0.5 mm pitch package.

Features

- 2.8 V to 5.5 V Input Voltage Range
- Fixed Output Voltage
- Up to 1.6 A DC Output Current (85°C Ambient Temperature)
- Up to 1.2 A DC Output Current (105°C Ambient Temperature)
- 3 MHz Switching Frequency
- Synchronous Rectification
- Soft Start / Over Current Protection
- Thermal Shutdown Protection
- Output Active Discharge (Disabled)
- Enable Input / Power Good (PG) Option
- WDFNW8, 2x2 mm, 0.5 mm Pitch Package
- Maximum 0.8 mm Thickness
- AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Automotive Advanced Driver−Assistance System (ADAS)
  - Front Camera – Rear View Camera
  - Surround View
  - Blind Spot Monitoring
- Automotive Telematics Clusters − Camera
- Automotive Space−Optimized Systems
- Point Of Load

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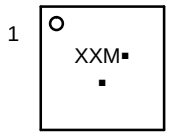
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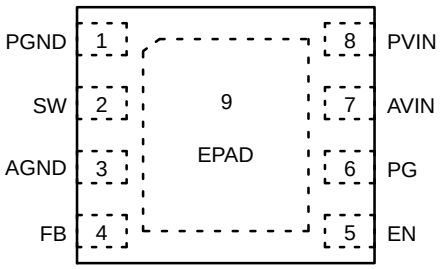
WDFNW8 2x2, 0.5P
CASE 511CL

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Package Top View)
8−pin, 2x2 mm, 0.5mm Pitch

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

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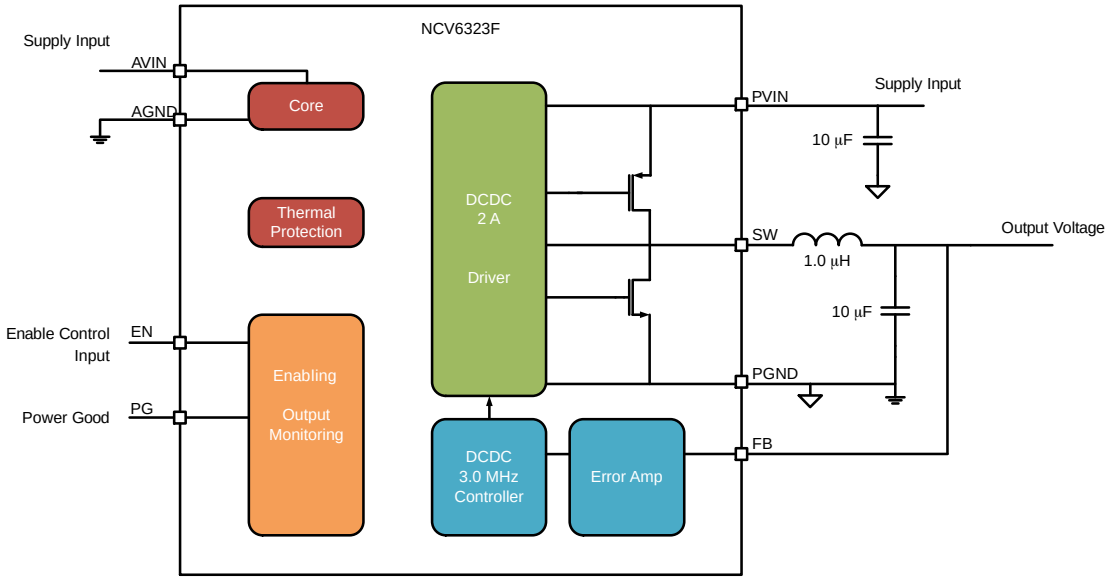


Figure 1. Application Schematic

FUNCTIONAL BLOCK DIAGRAM

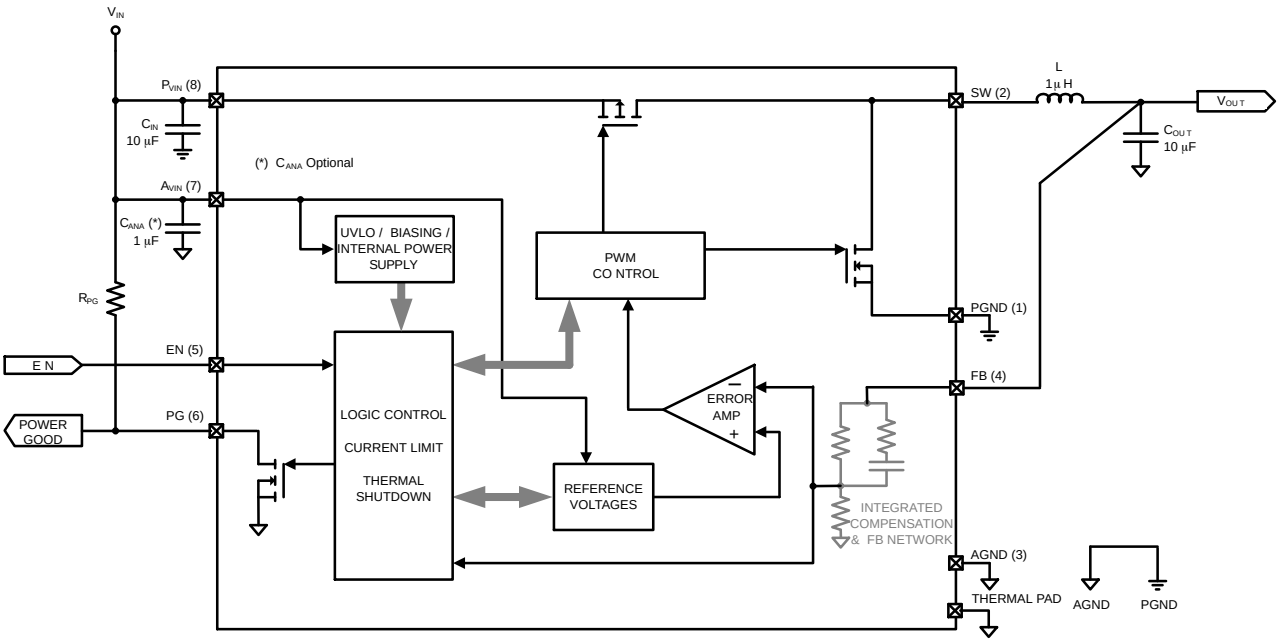


Figure 2. Functional Block Diagram

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PIN OUT DESCRIPTION

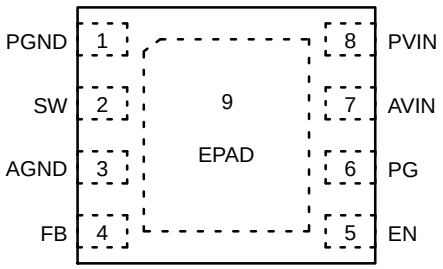


Figure 3. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Name	Type	Description
1	PGND	Power Ground	*Switch Ground.* This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane that connects all PGND terminals together is recommended. Analog and power grounds should only be connected together in one location with a trace.
2	SW	Power Output	*Switch Node.* This pin supplies drive power to the inductor. Typical application uses 1.0 μH inductor; refer to application section for more information. This pin must be connected with short large PCB connections.
3	AGND	Analog Ground	*Analog Ground.* Analog and digital modules ground. Must be connected to the system ground.
4	FB	Analog Input	*Feedback* Voltage from the buck converter output. This is the input for the internal regulation loop. Connect this pin directly to the output voltage rail, preferably as close as possible to positive terminal of the output capacitor. It is recommended to follow as much as possible PCB layout recommendation in the application section to avoid noise on this input.
5	EN	Digital Input	*Enable Input.* High level at this pin enables the device. Low level at this pin disables the device.
6	PG	Open Drain	*Power Good.* It is open drain output. Low level at this pin indicates the device is out of regulation, while high impedance at this pin indicates the device output voltage is within expected range. If not used this pin can be left unconnected.
7	AVIN	Analog Input	*Analog Supply.* This pin is the device analog and digital supply. Can be connected directly to the V_{IN} plane with an optional 1 μF or 4.7 μF ceramic capacitor
8	PVIN	Analog Input	*Power Supply.* This pin is the power supply of the device. A 10 μF or larger ceramic capacitor must bypass this input to the ground. This capacitor should be placed as close as possible to pin. This pin must be connected with short large PCB connections.
9	EPAD	Analog Ground	*Exposed Thermal Pad.* Must be soldered to system Ground plane to achieve power dissipation performances. This pin is internally connected to AGND

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MAXIMUM RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{A-DC}	Analog Pins DC Non Switching: AVIN, FB (Note 1)	− 0.3	−	6.0	V
V_{P-DC}	Power Pin DC Non Switching: PVIN, SW (Note 1)	− 0.3	−	6.0	V
V_{P-TR}	Between PVIN−PGND Pins, Transient 3 ns – 3 MHz (Note 1)	− 0.3	−	7.5	V
V_{DG}	Digital Pins Voltage: EN, PG	−0.3	−	V_{A-DC}	V
HBM	Human Body Model (HBM) ESD Rating (Note 2)	−	−	2000	V
CDM	Charged Device Model (CDM) ESD Rating (Note 2)	−	−	500	V
I_{LU}	Latch Up Current (Note 3)	−	100	−	mA
T_{STG}	Storage Temperature Range	− 55	−	150	°C
T_{JMAX}	Junction Temperature Range	− 40	−	TSD	°C
MSL	Moisture Sensitivity (Note 4)	−	Level1	−	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Charged Device Model (CDM) ±500 V per JEDEC standard: JESD22−C101 Class IV.
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
AV_{INR}	Analog Input Supply	2.8	−	5.5	V
PV_{INR}	Power Input Supply	2.8	−	5.5	V
T_J	Operating Junction Temperature Range (Note 6)	− 40	25	+125	°C
L_{OUT}	Inductor for DC to DC Converter (Note 5)	0.67	1.0	1.3	μH
C_{OUT}	Output Capacitor for DC to DC Converter NCV6323FxL Version (Note 5, 7)	6.4	10	100	μF
	Output Capacitor for DC to DC Converter NCV6323FxH Version (Note 5, 7)	50	150	250	
C_{AVIN}	Optional Input Capacitor for Analog Supply (Note 5)	0.47	1.0	−	μF
C_{PVIN}	Input Capacitor for Power Supply (Note 5)	4.7	10	−	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Including de−ratings (Refer to the Application Information section of this document for further details)
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
7. NCV632F compensation network is integrated. Special care should be taken with the capacitive load (refer to the application information)

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THERMAL INFORMATION

Symbol	Parameter	JEDEC JESD51−3 (Calculated)	Demo Board (Measured)	Unit
θ_{JCTOP}	Thermal Resistance Junction to Case Top (Note 8)	135	−	°C/W
θ_{JCBOT}	Thermal Resistance Junction to Case Bottom (Exposed Pad) (Note 9)	43	−	°C/W
θ_{JA}	Thermal Resistance Junction to Ambient. (Note 10)	121	40	°C/W
Ψ_{CTOP}	Thermal Characterization Parameter Junction to Case Top (Note 11)	−	15	°C/W
Ψ_{JB}	Thermal Characterization Parameter Junction to Board. Measured on the AGND Footprint (Note 11)	−	20	°C/W
CC_{105}	Current Capability ($T_A \le 105°$) (Note 12)	−	1.2	A
CC_{85}	Current Capability ($T_A \le 85°$) (Note 12)	−	1.6	A

8. Calculated with infinite heatsink affixed to case top without any board present
9. Calculated with infinite heatsink affixed to case bottom without any board present.
10. Rθ_{JA} is dependent on the PCB heat dissipation. Refer to AND8215/D (AND8215−D.PDF)
11. The thermal characterization parameters are measured on the Demo Board
12. The current capability (CC) is dependent on input voltage, PCB stack up and layout, as well as the external components selected. Filled with $AV_{IN} = PV_{IN} = 5.0$ V $V_{OUT} = 1.8$ V

ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.
Min and Max Limits apply for T_J = −40°C to +125°C, $A_{VIN} = P_{VIN} = 3.3$ V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, $C_{IN} = C_{OUT}$ = 10 μF and default configuration, unless otherwise specified.
Typical values are referenced to T_J = + 25°C, $A_{VIN} = P_{VIN} = 3.3$ V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, $C_{IN} = C_{OUT}$ = 10 μF and default configuration, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE AND CURRENT (APPLIES TO A_{VIN} / P_{VIN} PIN)					
V_{IN}	Input Voltage Range (Note 13)	2.8 or V_{OUT} + 0.5 V	−	5.5	V
I_Q	V_{IN} Quiescent Supply Current · No Load · $V_{OUT} \le 1.8$ V	−	5.7	9	mA
I_{Q33}	V_{IN} Quiescent Supply Current · No Load · $V_{OUT} > 1.8$ V	−	7.8	12	mA
I_{SD}	V_{IN} Shutdown Current · EN Pin LOW · $A_{VIN} = P_{VIN} = 5.5$ V	−	1	6	μA
OUTPUT VOLTAGE					
ΔV_{OUT}	Output Voltage DC Error − NCV6323F−x · V_{IN} = 2.8 V (10, 11, 12, 18 versions) or V_{OUT} + 0.5 V (33 version) ≤ $V_{IN} \le 5.5$ V · 0 mA ≤ $I_{OUT} \le 1$ A (Note 14)	−2	−	+2	%
V_{OUT18_200mA}	Output Voltage NCV6323F−18 · V_{IN} = 3.3 V, I_{OUT} = 200 mA (Note 14)	1.773	1.8	1.827	V
V_{OUT12_200mA}	Output Voltage NCV6323F−12 · V_{IN} = 3.3 V, I_{OUT} = 200 mA (Note 14)	1.182	1.2	1.218	V
V_{OUT11_200mA}	Output Voltage NCV6323F−11 · V_{IN} = 3.3 V, I_{OUT} = 200 mA (Note 14)	1.083	1.1	1.117	V
V_{OUT10_200mA}	Output Voltage NCV6323F−10 · V_{IN} = 3.3 V, I_{OUT} = 200 mA (Note 14)	0.985	1.0	1.015	V
V_{OUT33_200mA}	Output Voltage NCV6323F−33 · V_{IN} = 5.0 V, I_{OUT} = 200 mA (Note 14)	3.25	3.3	3.35	V
V_{OUT_LOAD}	Output Voltage in Load Regulation · V_{IN} = 3.3 V (10, 11, 12, 18 Versions) or 5.0 V (33 Version) · $V_{FB} = V_{OUT}$ · I_{OUT} from 200 mA to I_{OUT_MAX}	−	±0.5	−	%/A

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ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.
Min and Max Limits apply for T_J = −40°C to +125°C, A_{VIN} = P_{VIN} = 3.3 V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, C_{IN} = C_{OUT} = 10 μF and default configuration, unless otherwise specified.
Typical values are referenced to T_J = + 25°C, A_{VIN} = P_{VIN} = 3.3 V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, C_{IN} = C_{OUT} = 10 μF and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
OUTPUT VOLTAGE					
V_{OUT_LINE}	Output Voltage in Line Regulation · I_{OUT} = 200 mA, · V_{FB} = V_{OUT} · V_{IN} from V_{IN_MIN} 2.8 V (10, 11, 12, 18 Versions) or V_{OUT} + 0.5 V (33 Version) to 5.5 V	−	0	−	%
D_{MAX}	Duty Cycle	−	−	100	%
OUTPUT CURRENT					
I_{OUT_MAX105}	DC Output Current Capability · T_A = 105°C (Note 15, 16)	1.2	−	−	A
I_{OUT_MAX85}	DC Output Current Capability · T_A = 85°C (Note 15, 16)	1.6	−	−	A
I_{LIM_P}	Output Peak Current Limit – High Side Switch (P−MOS) (Note 18)	2.3	2.8	3.3	A
I_{LIM_N}	Output Peak Current Limit – Low Side Switch (N−MOS) (Note 17, 18)	−	−0.8	−	A
VOLTAGE MONITOR					
V_{INUVLO_FALL}	V_{IN} UVLO Falling Threshold	−	−	2.62	V
V_{INUVLO_RISE}	V_{IN} UVLO Rising Threshold	−	−	2.8	V
V_{INHYS}	V_{IN} UVLO Hysteresis · UVLO Released for V_{IN} = V_{INUVLO_FALL} + V_{INHYS}	60	150	250	mV
V_{PGL}	Power Good Low Threshold · V_{OUT} drops until Threshold (Percentage of FB Voltage)	87	90	92.5	%
V_{PGHYS}	Power Good Hysteresis · V_{OUT} Rises up to the Threshold (Percentage of Power Good Low (V_{PLG}) Threshold)	0	2.5	5	%
TD_{PGH1}	Power Good High Delay at Start Up · From EN Rising Edge to PG L to H Transition	−	1.1	−	ms
TD_{PGL1}	Power Good Low Delay at Shut Down · From EN Falling Edge to PG Going Low	−	4	−	μs
TD_{PGH}	Power Good High Delay in Regulation · From V_{FB} Going Higher than 95% Nominal Level to PG Going High. Does Not Apply to First Start Up.	−	11	−	μs
TD_{PGL}	Power Good Low Delay in Regulation · From V_{FB} Going Lower than 90% Nominal Level to PG Going Low.	−	8	−	μs
V_{PG_L}	Power Good Pin Low Voltage · Voltage at PG Pin with 5 mA Sink Current	−	−	0.3	V
I_{PG_LK}	Power Good Pin Leakage Current · 3.3 V at PG Pin when Power Good Valid	−	−	100	nA
INTEGRATED MOSFET					
R_{ON_HSP3}	High−Side MOSFET ON Resistance · V_{IN} = 3.3 V (10, 11, 12, 18 Versions) (Note 19)	120	170	250	mΩ
R_{ON_HSP5}	High−Side MOSFET ON Resistance · V_{IN} = 5.0 V	90	135	200	mΩ
R_{ON_LSN3}	Low−Side MOSFET ON Resistance · V_{IN} = 3.3 V (10, 11, 12, 18 Versions) (Note 19)	60	115	180	mΩ
R_{ON_LSN5}	Low−Side MOSFET ON Resistance · V_{IN} = 5.0 V	60	95	150	mΩ

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ELECTRICAL CHARACTERISTICS (Refer to the Application Information section of this data sheet for more details.
Min and Max Limits apply for T_J = −40°C to +125°C, A_{VIN} = P_{VIN} = 3.3 V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, C_{IN} = C_{OUT} = 10 μF and default configuration, unless otherwise specified.
Typical values are referenced to T_J = + 25°C, A_{VIN} = P_{VIN} = 3.3 V (10, 11, 12, 18 Versions) or 5.0 V (33 Versions), L = 1 μH, C_{IN} = C_{OUT} = 10 μF and default configuration, unless otherwise specified.) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
SWITCHING FREQUENCY					
F_{SW}	Normal Operation Frequency	2.7	3.0	3.3	MHz
START UP					
T_{START_E}	Start Up Time: Applies to NCV6323FE−xx Version · Time from EN to 90% of Output Voltage Target	0.3	0.51	0.75	ms
T_{SS_E}	Soft Start time: Applies to NCV6323FE−xx Version · Time from 50 mV to 90% of Output Voltage Target	0.2	0.42	0.68	ms
CONTROL LOGIC					
V_{EN_H}	EN Input High Voltage	1.1	−	−	V
V_{EN_L}	EN Input Low Voltage	−	−	0.4	V
I_{EN_BIAS}	EN Input Bias Current	−	0.1	1	μA
T_{ENFTR}	Digital Input EN Filter: Rising and Falling (Note 20)	−	4	8	μs
MISCELLANEOUS					
R_{DIS}	Internal Output Discharge Resistance	390	490	600	Ω
T_{SD}	Thermal Shutdown Threshold	−	150	−	°C
T_{SD_HYST}	Thermal Shutdown Hysteresis	−	25	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
13. Operation above 5.5 V input voltage for extended period of time may affect device reliability
14. $V_{IN} \geq V_{OUT}$ + 0.5 V or 2.8 V
15. Junction temperature must be maintained below 125°C. Output load current capability depends on the application thermal capability.
16. Characterized and not tested in Production
17. Limit for reverse current from SW to GND
18. The Output Peak Current Limit does not operate when V_{OUT} < 300 mA
19. Maximum values apply for T_J = 125°C
20. Covered by Scan

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TYPICAL OPERATING CHARACTERISTICS

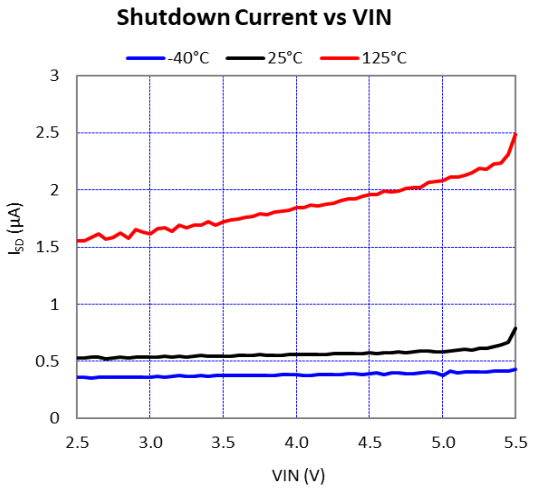


Figure 4. Shutdown Current vs. Input Voltage (EN = Low, No Load)

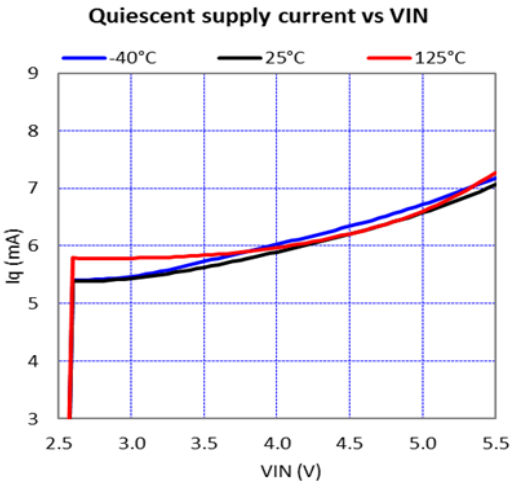


Figure 5. Quiescent Current vs. Input Voltage (EN = High, V_{OUT} = 1.0 V, No Load)

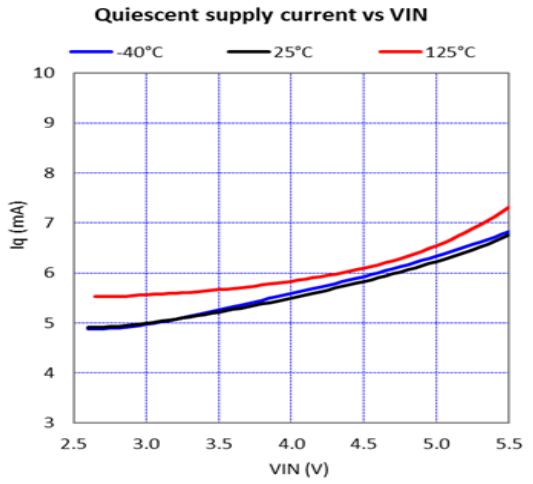


Figure 6. Quiescent Current vs. Input Voltage (EN = High, V_{OUT} = 1.1 V, No Load)

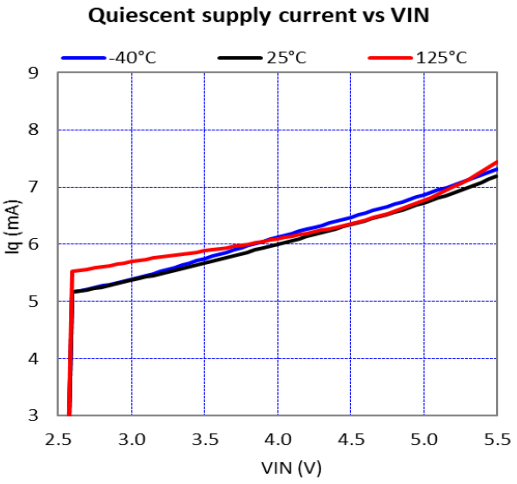


Figure 7. Quiescent Current vs. Input Voltage (EN = High, V_{OUT} = 1.2 V, No Load)

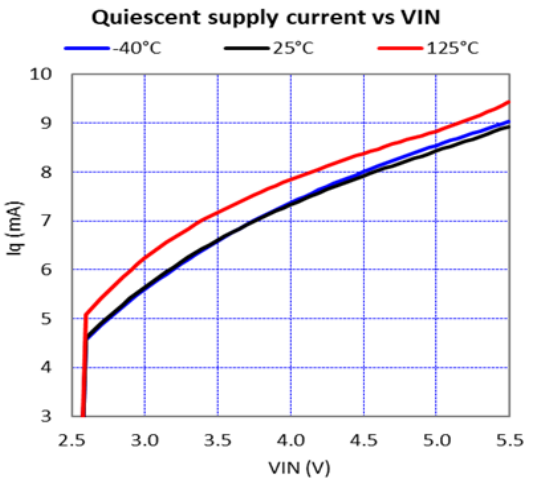


Figure 8. Quiescent Current vs. Input Voltage (EN = High, V_{OUT} = 1.8 V, No Load)

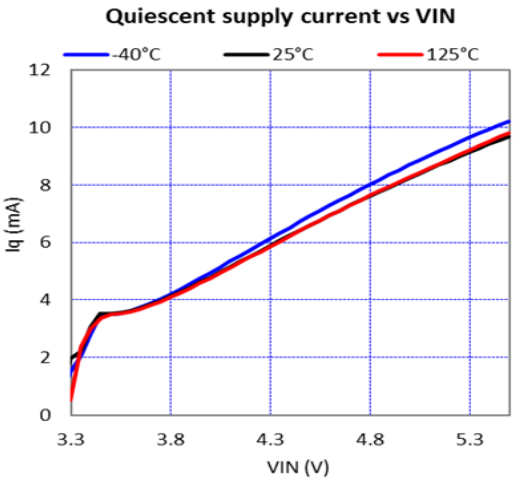


Figure 9. Quiescent Current vs. Input Voltage (EN = High, V_{OUT} = 3.3 V, No Load)

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TYPICAL OPERATING CHARACTERISTICS (continued)

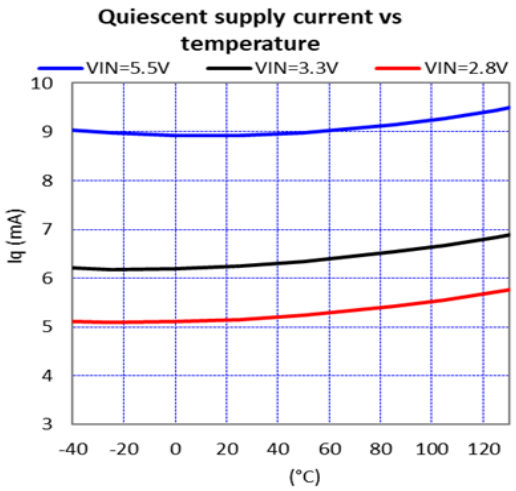


Figure 10. Quiescent Current vs. Temperature (EN = High, V_{OUT} = 1.8 V, No Load)

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TYPICAL OPERATING CHARACTERISTICS (continued)

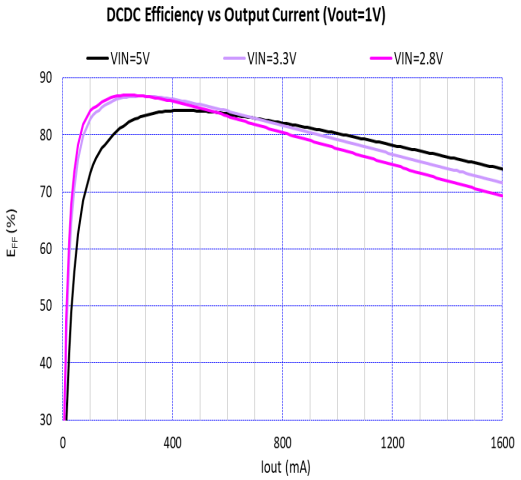


Figure 11. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.0 V, T_A = 25°C, L = FDSD0420−H−1R0M)

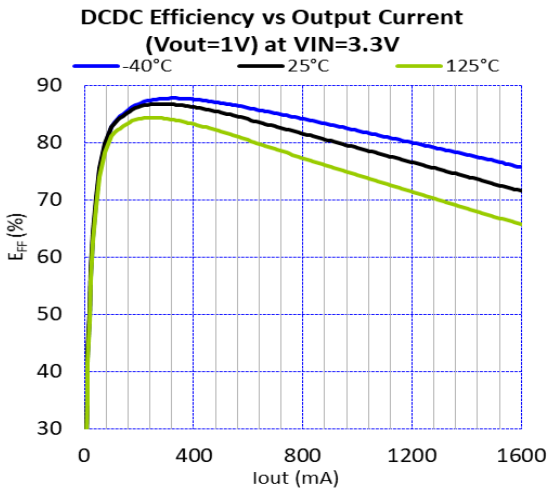


Figure 12. Efficiency vs. Output Current and Temperature at V_{IN} = 3.3 V (V_{OUT} = 1.0 V, L = FDSD0420−H−1R0M)

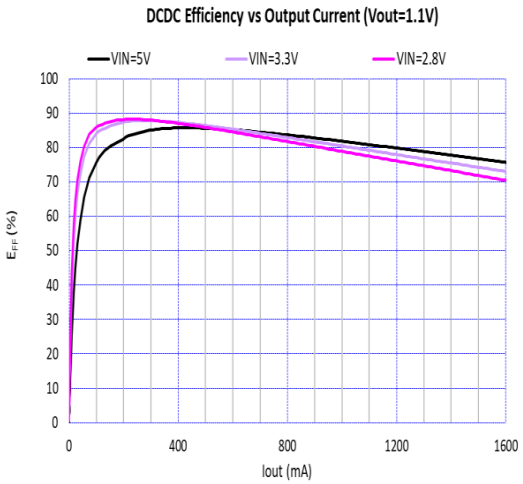


Figure 13. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.1 V, T_A = 25°C, L = FDSD0420−H−1R0M)

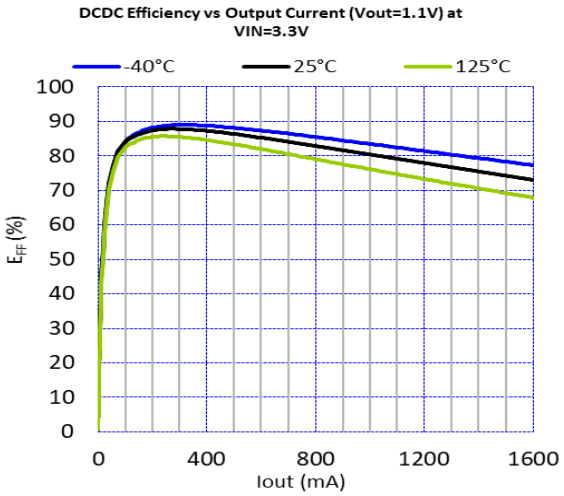


Figure 14. Efficiency vs. Output Current and Temperature at V_{IN} = 3.3 V (V_{OUT} = 1.1 V, L = FDSD0420−H−1R0M)

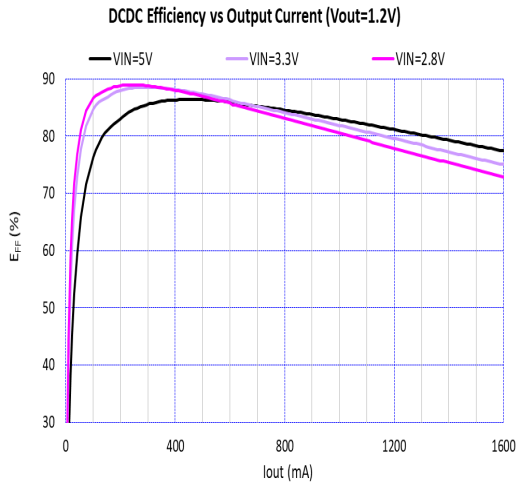


Figure 15. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.2 V, T_A = 25°C, L = FDSD0420−H−1R0M)

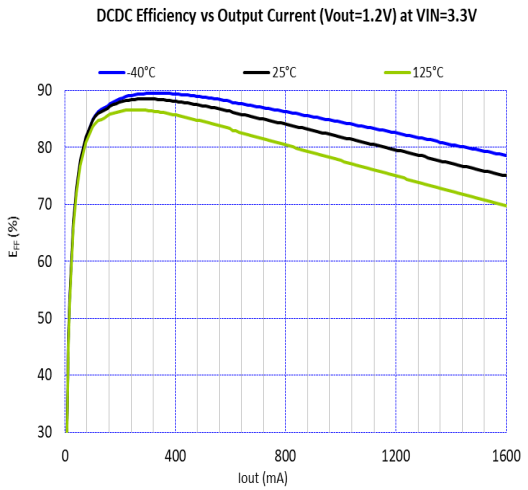


Figure 16. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.2 V, T_A = 25°C, L = FDSD0420−H−1R0M)

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TYPICAL OPERATING CHARACTERISTICS (continued)

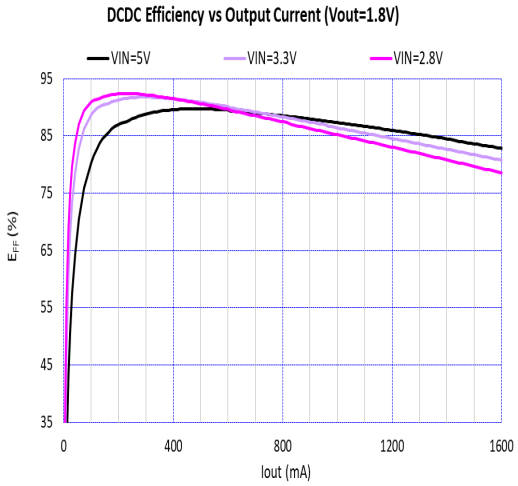


Figure 17. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 1.8 V, T_A = 25°C, L = FDSD0420−H−1R0M)

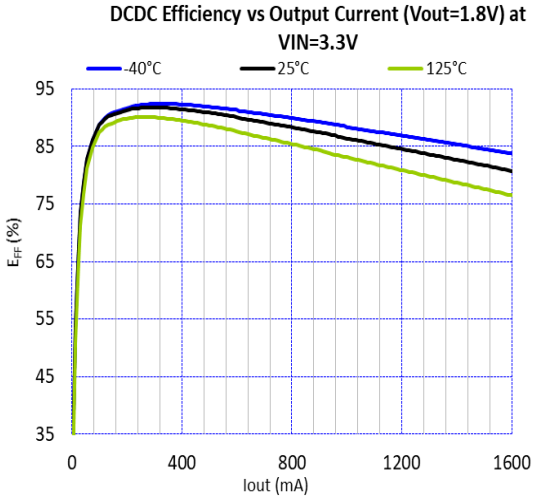


Figure 18. Efficiency vs. Output Current and Temperature at V_{IN} = 3.3 V (V_{OUT} = 1.8 V, L = FDSD0420−H−1R0M)

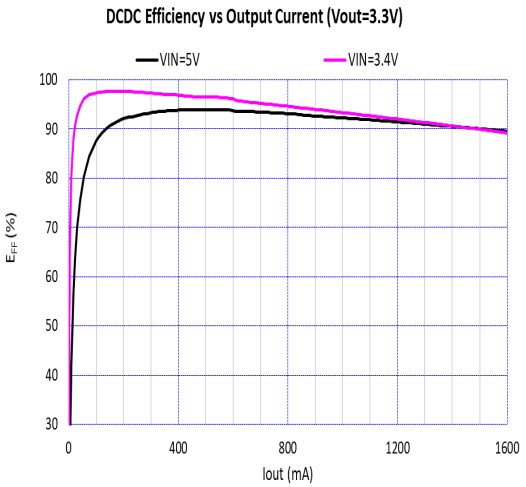


Figure 19. Efficiency vs. Output Current and Input Voltage (V_{OUT} = 3.3 V, T_A = 25°C, L = FDSD0420−H−1R0M)

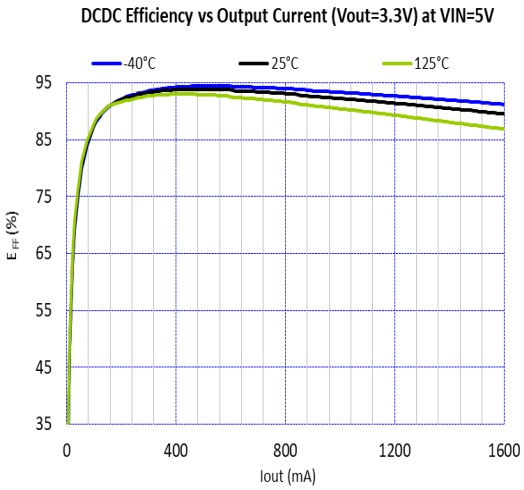


Figure 20. Efficiency vs. Output Current and Temperature at V_{IN} = 5.0 V (V_{OUT} = 3.3 V, L = FDSD0420−H−1R0M)

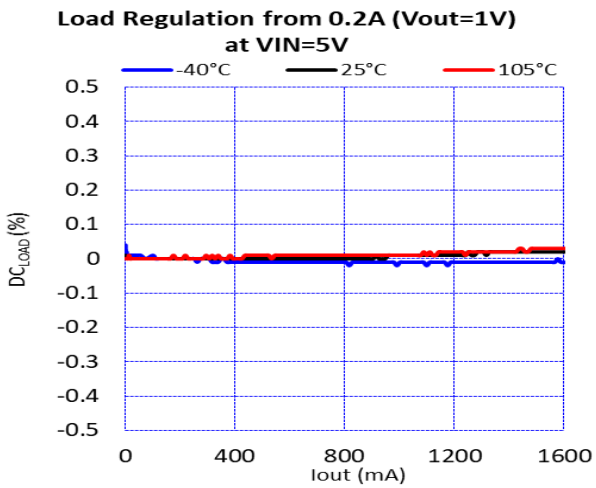


Figure 21. Load Regulation (V_{IN} = 5.0 V, V_{OUT} = 1.0 V)

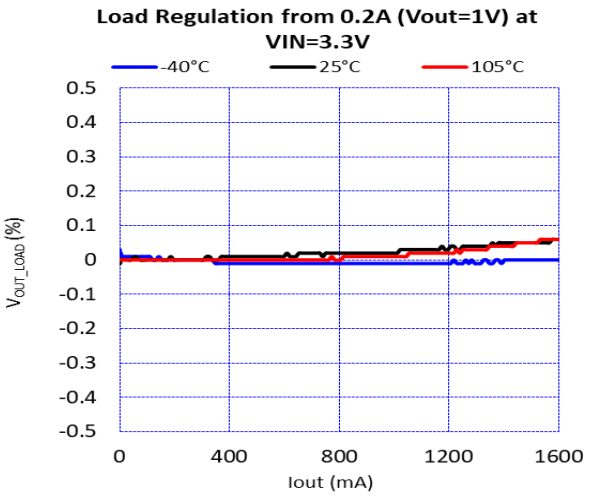


Figure 22. Load Regulation (V_{IN} = 3.3 V, V_{OUT} = 1.0 V)

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TYPICAL OPERATING CHARACTERISTICS (continued)

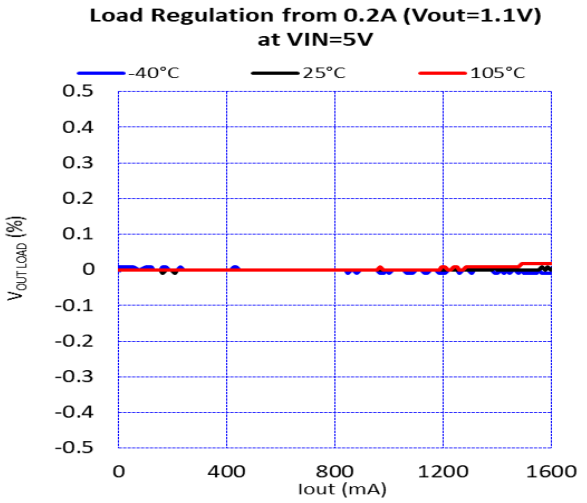


Figure 23. Load Regulation (V_{IN} = 5.0 V, V_{OUT} = 1.1 V)

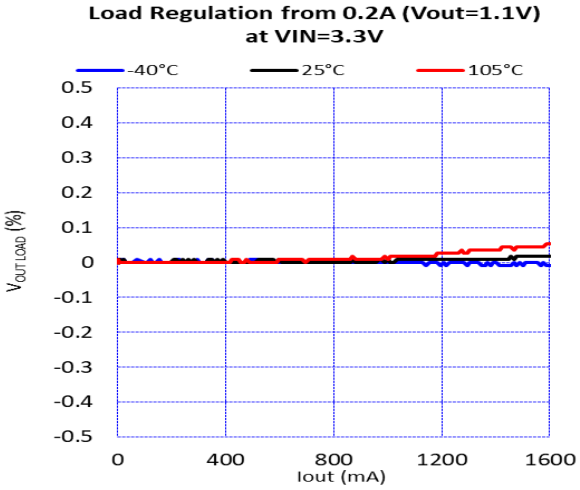


Figure 24. Load Regulation (V_{IN} = 3.3 V, V_{OUT} = 1.1 V)

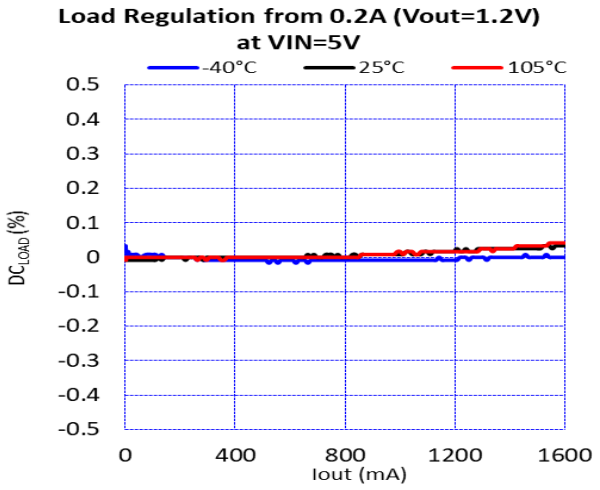


Figure 25. Load Regulation (V_{IN} = 5.0 V, V_{OUT} = 1.2 V)

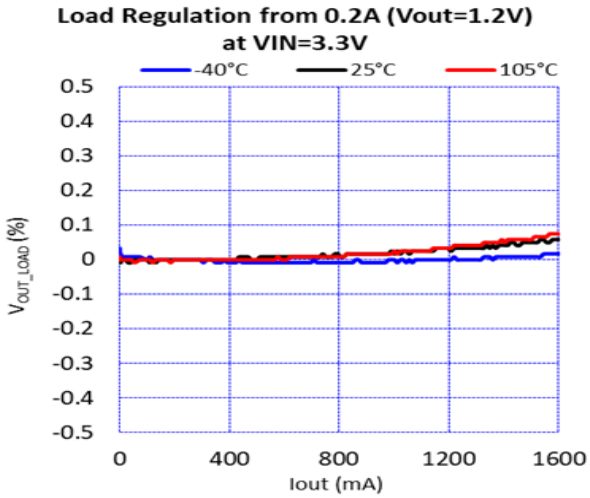


Figure 26. Load Regulation (V_{IN} = 3.3 V, V_{OUT} = 1.2 V)

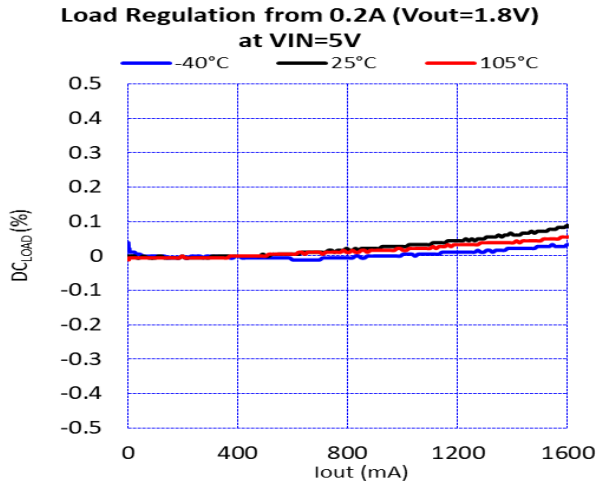


Figure 27. Load Regulation (V_{IN} = 5.0 V, V_{OUT} = 1.8 V)

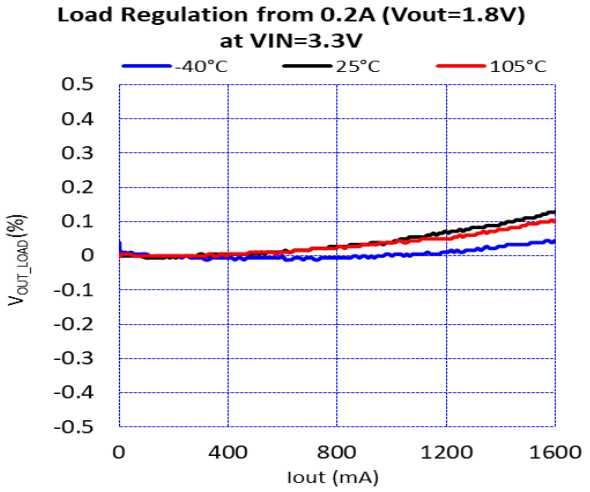


Figure 28. Load Regulation (V_{IN} = 3.3 V, V_{OUT} = 1.8 V)

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TYPICAL OPERATING CHARACTERISTICS (continued)

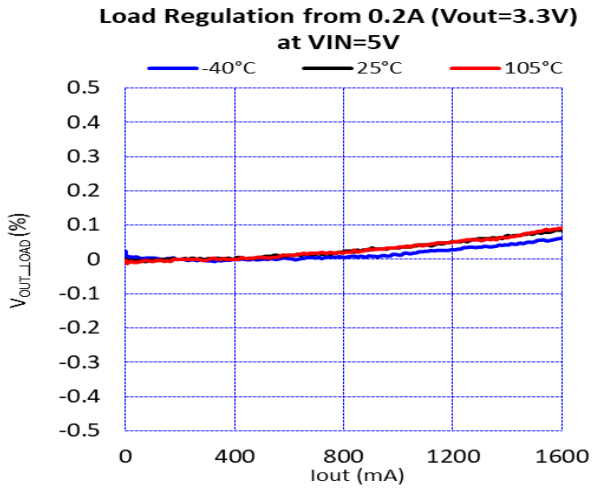


Figure 29. Load Regulation (V_{IN} = 5.0 V, V_{OUT} = 3.3 V)

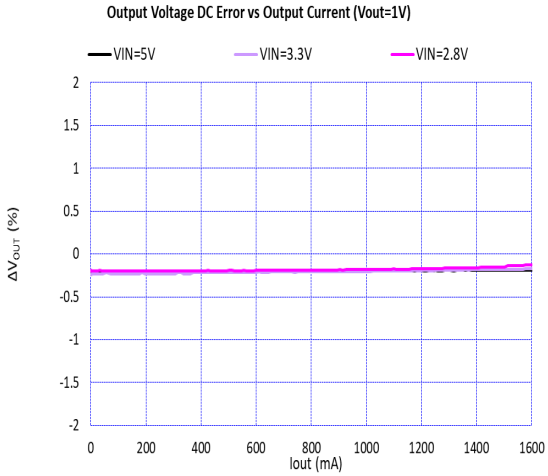


Figure 30. Output Voltage DC Error vs Output Current (V_{OUT} = 1.0 V, T_A = 25°C)

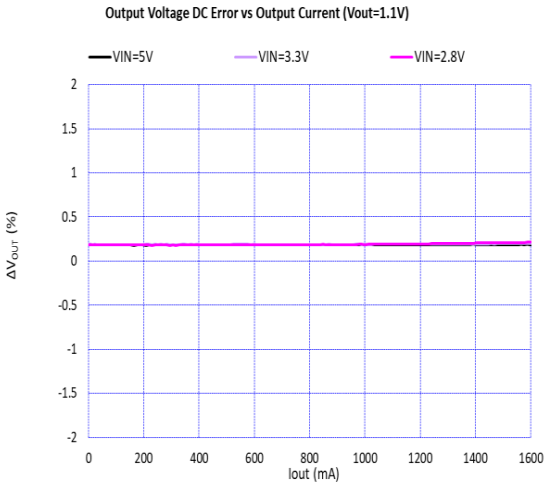


Figure 31. Output Voltage DC Error vs Output Current (V_{OUT} = 1.1 V, T_A = 25°C)

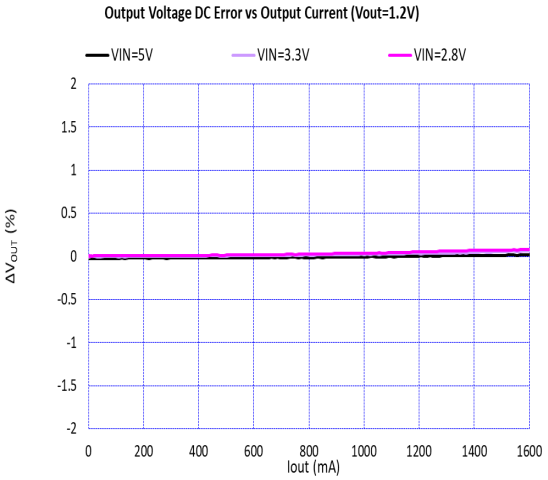


Figure 32. Output Voltage DC Error vs Output Current (V_{OUT} = 1.2 V, T_A = 25°C)

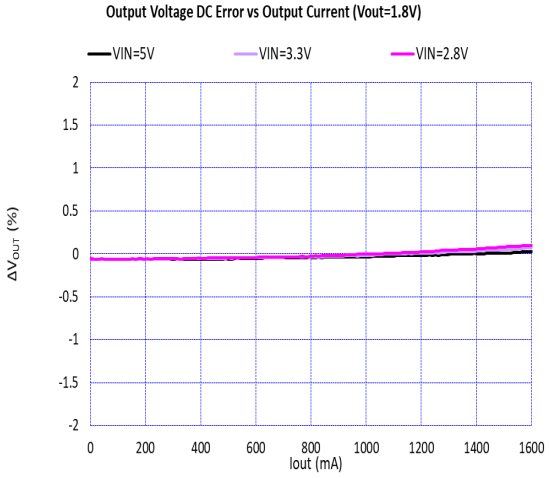


Figure 33. Output Voltage DC Error vs Output Current (V_{OUT} = 1.8 V, T_A = 25°C)

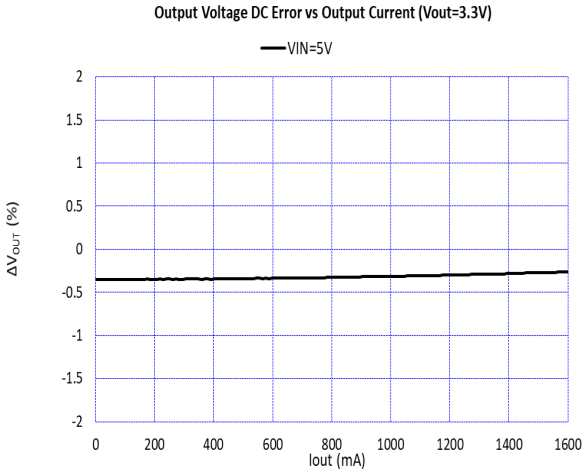


Figure 34. Output Voltage DC Error vs Output Current (V_{OUT} = 3.3 V, T_A = 25°C)

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TYPICAL OPERATING CHARACTERISTICS (continued)

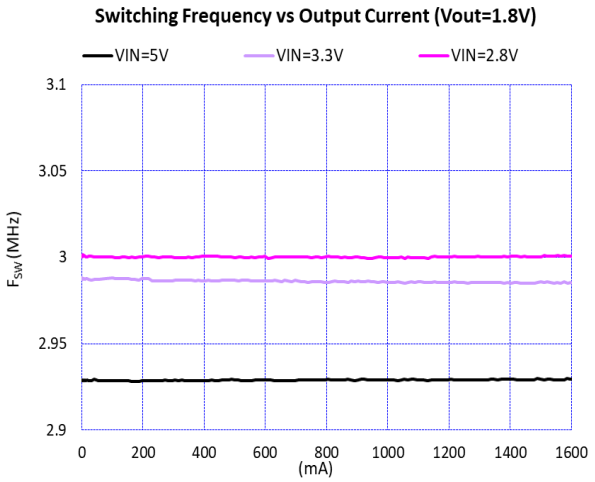


Figure 35. Switching Frequency vs Output Current (V_{OUT} = 1.8 V, T_A = 25°C)

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TYPICAL OPERATING CHARACTERISTICS (continued)

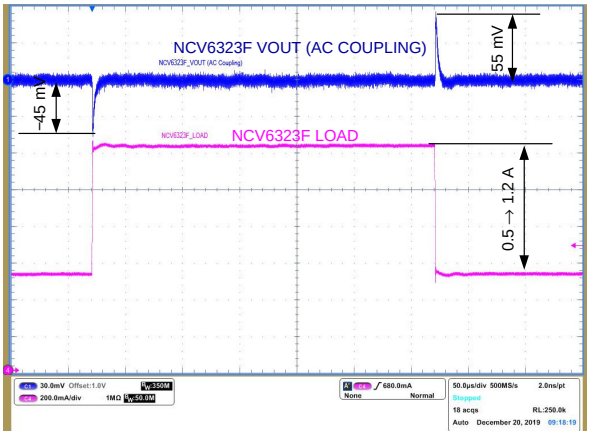


Figure 36. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.0 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 500 mA → 1.2 A → 500 mA

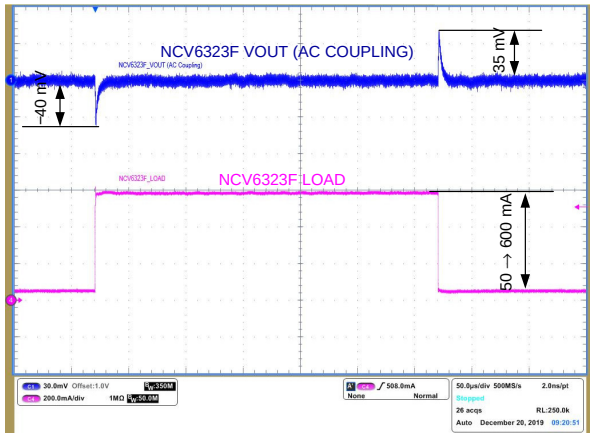


Figure 37. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.0 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 50 mA → 600 mA → 50 mA

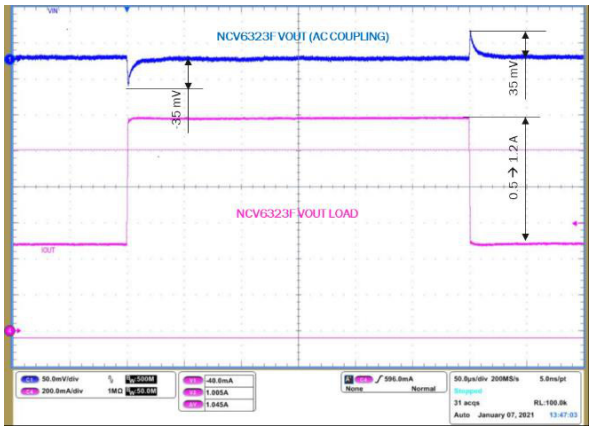


Figure 38. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.1 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 500 mA → 1.2 A → 500 mA

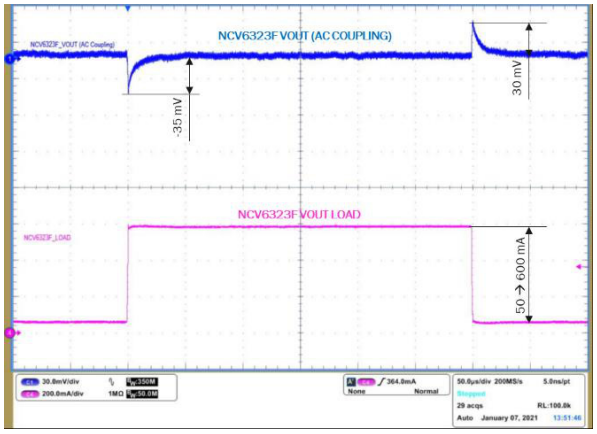


Figure 39. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.1 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 50 mA → 600 mA → 50 mA

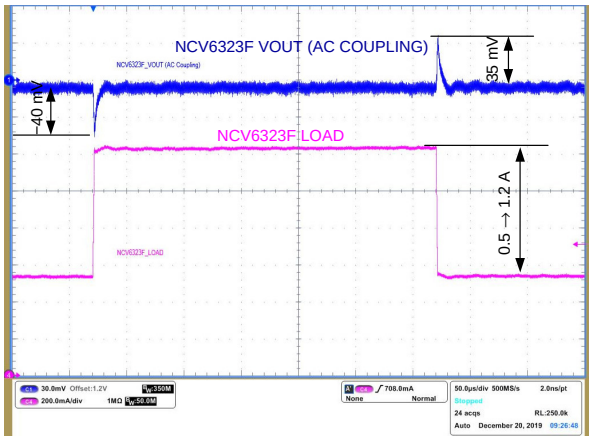


Figure 40. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.2 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 500 mA → 1.2 A → 500 mA

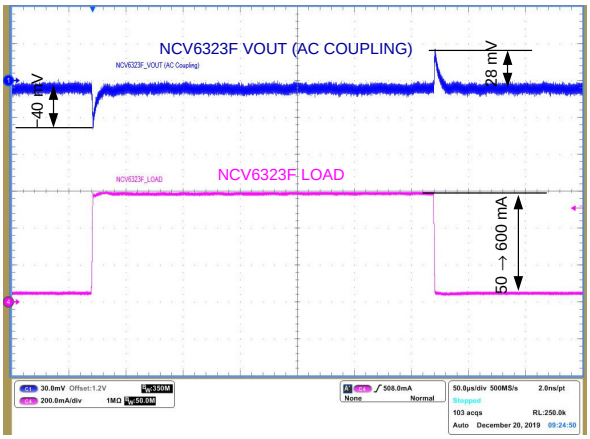


Figure 41. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.2 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 50 mA → 600 mA → 50 mA

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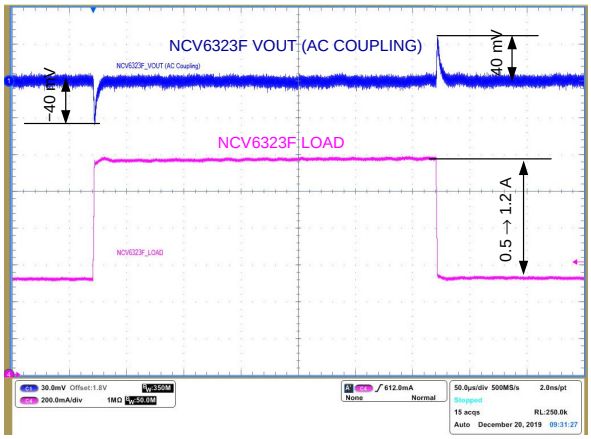


Figure 42. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.8 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 500 mA → 1.2 A → 500 mA

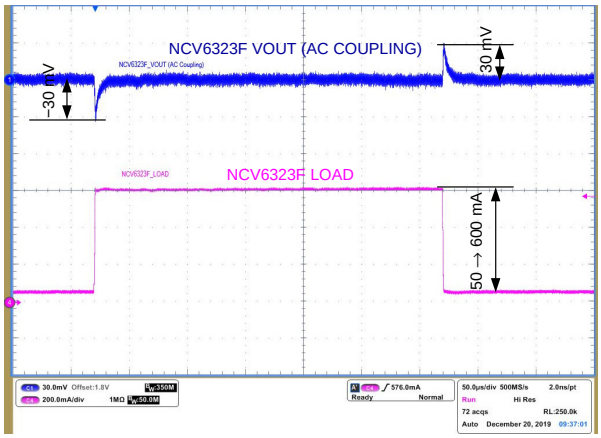


Figure 43. Load Transient (V_{IN} = 3.3 V, V_{OUT} = 1.8 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 50 mA → 600 mA → 50 mA

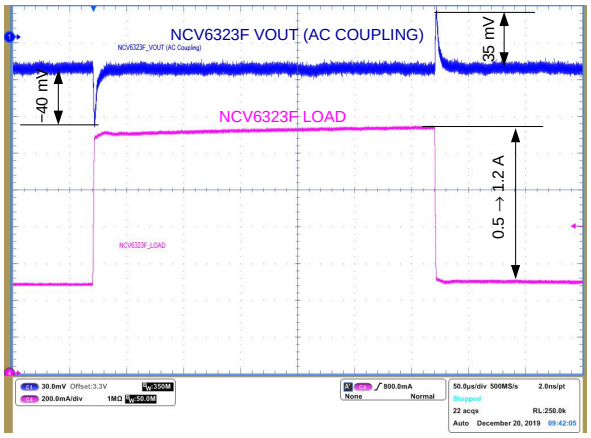


Figure 44. Load Transient (V_{IN} = 5.0 V, V_{OUT} = 3.3 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 500 mA → 1.2 A → 500 mA

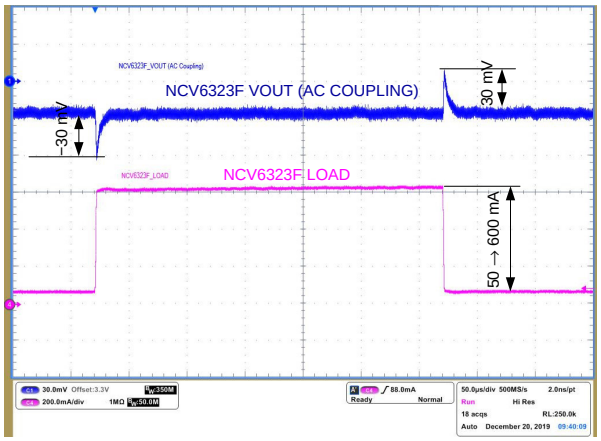


Figure 45. Load Transient (V_{IN} = 5.0 V, V_{OUT} = 3.3 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M) 50 mA → 600 mA → 50 mA

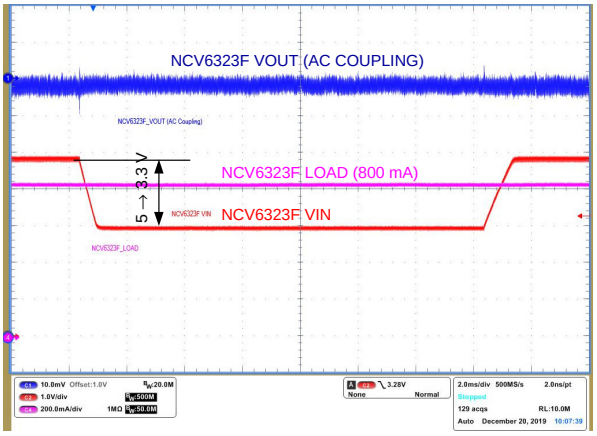


Figure 46. Line Transient (V_{OUT} = 1.0 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

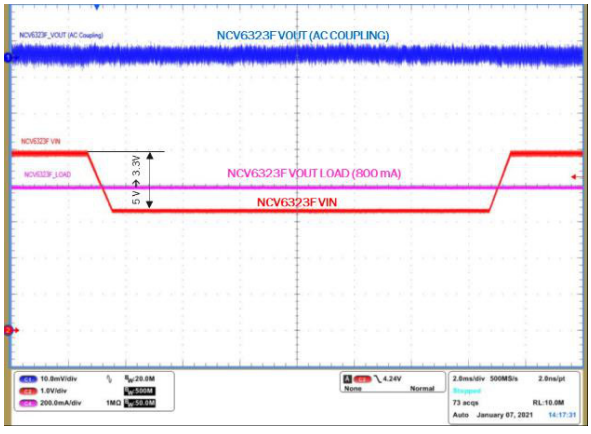


Figure 47. Line Transient (V_{OUT} = 1.1 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

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TYPICAL OPERATING CHARACTERISTICS (continued)

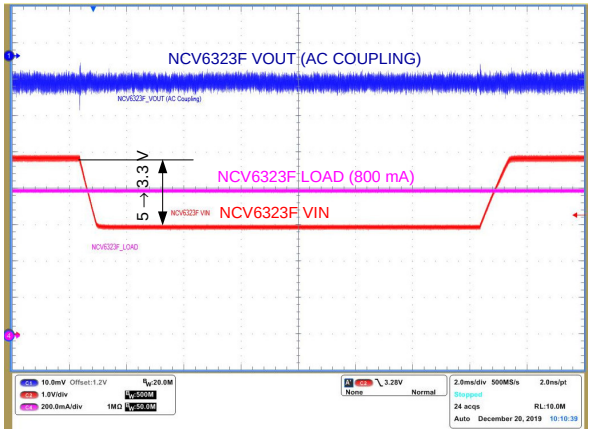


Figure 48. Line Transient (V_{OUT} = 1.2 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

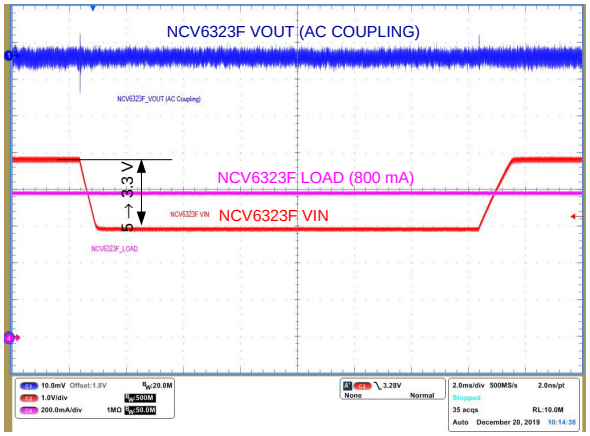


Figure 49. Line Transient (V_{OUT} = 1.8 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

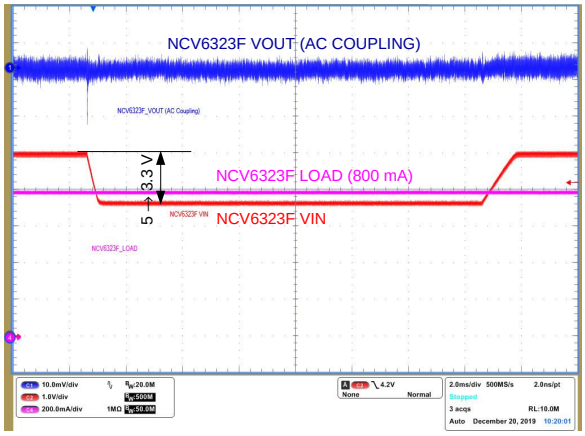


Figure 50. Line Transient (V_{OUT} = 3.3 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

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TYPICAL OPERATING CHARACTERISTICS (continued)

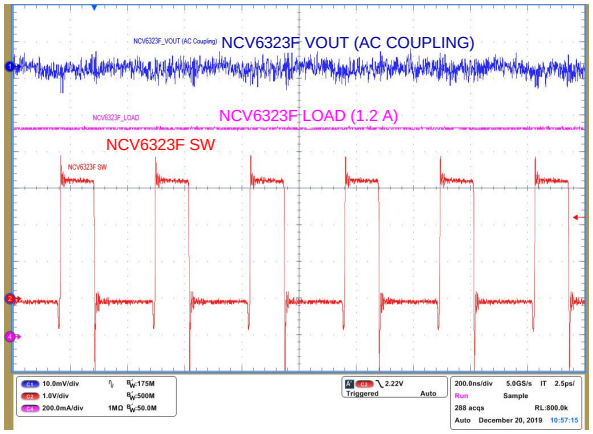


Figure 51. Output Voltage Ripple (V_{IN} = 3.3 V, V_{OUT} = 1.0 V, C_{OUT} = GCM21BR70J106KE22, I_{OUT} = 500 mA)

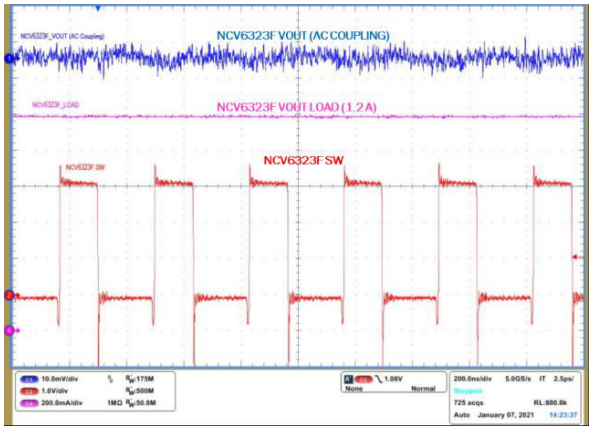


Figure 52. Output Voltage Ripple (V_{IN} = 3.3 V, V_{OUT} = 1.1 V, C_{OUT} = GCM21BR70J106KE22, I_{OUT} = 500 mA)

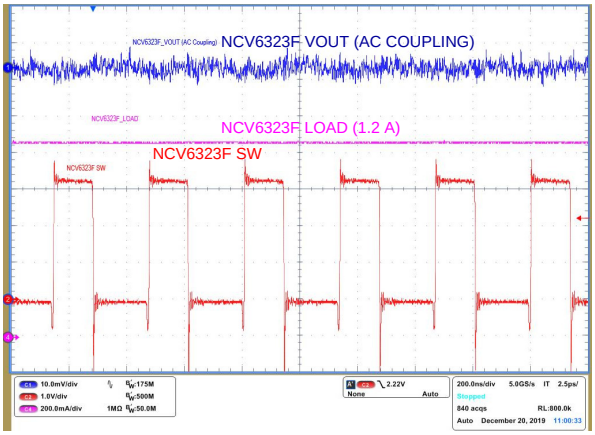


Figure 53. Output Voltage Ripple (V_{IN} = 3.3 V, V_{OUT} = 1.2 V, C_{OUT} = GCM21BR70J106KE22, I_{OUT} = 500 mA)

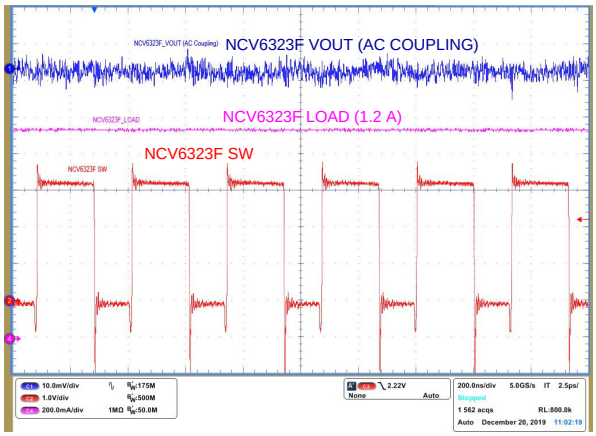


Figure 54. Output Voltage Ripple (V_{IN} = 3.3 V, V_{OUT} = 1.8 V, C_{OUT} = GCM21BR70J106KE22, I_{OUT} = 500 mA)

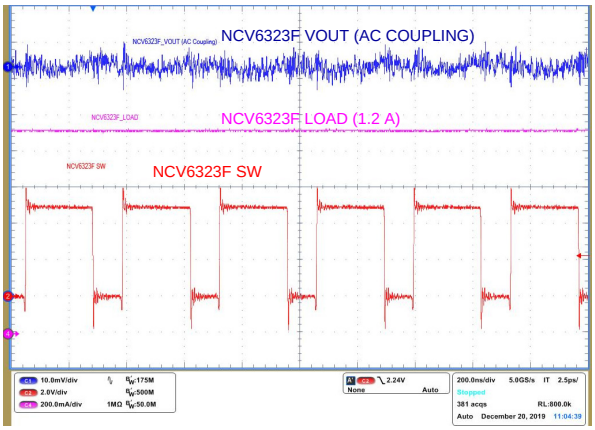


Figure 55. Output Voltage Ripple (V_{IN} = 5.0 V, V_{OUT} = 3.3 V, C_{OUT} = GCM21BR70J106KE22, I_{OUT} = 500 mA)

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TYPICAL OPERATING CHARACTERISTICS (continued)

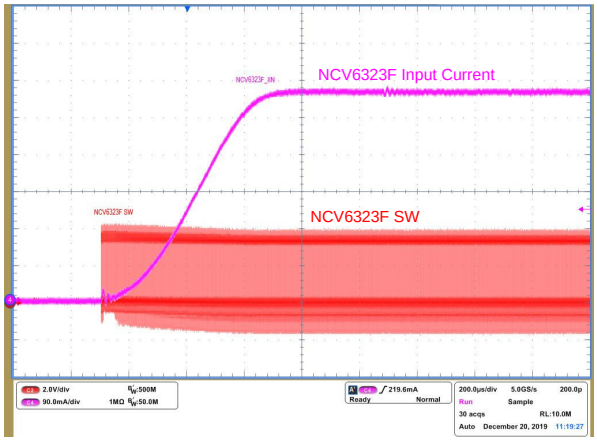


Figure 56. Inrush Current (V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 800 mA, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

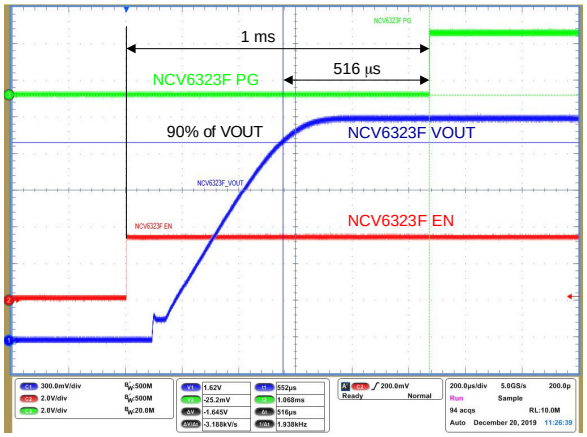


Figure 57. PG Delay after Start Up – NCV6323F−E (V_{IN} = 3.3 V, V_{OUT} = 1.8 V, C_{OUT} = GCM21BR70J106KE22, L = FDSD0420−H−1R0M)

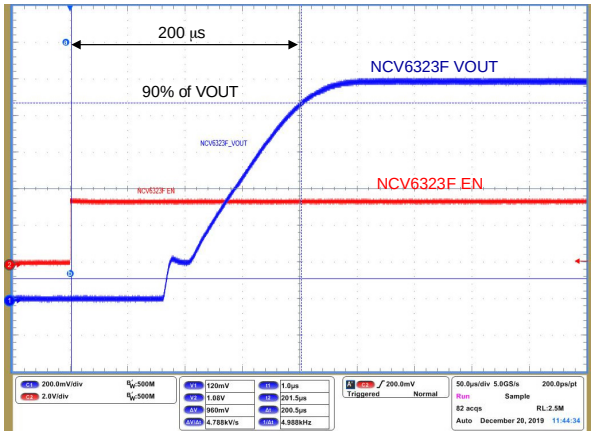


Figure 58. Startup Time T_{START} (NCV6323FCLMTW12, C_{OUT} = 10 µF)

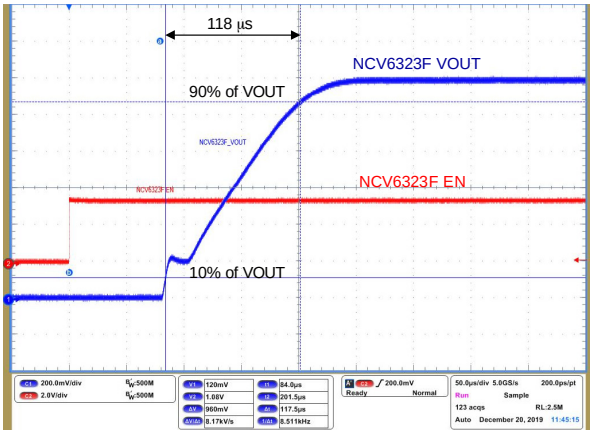


Figure 59. Soft Start Time T_{SS} (NCV6323FCLMTW12, C_{OUT} = 10 µF)

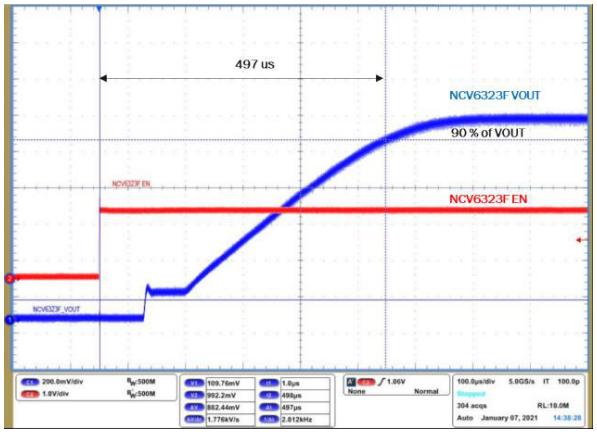


Figure 60. Startup Time T_{START} (NCV6323FELMTW11, C_{OUT} = 10 µF)

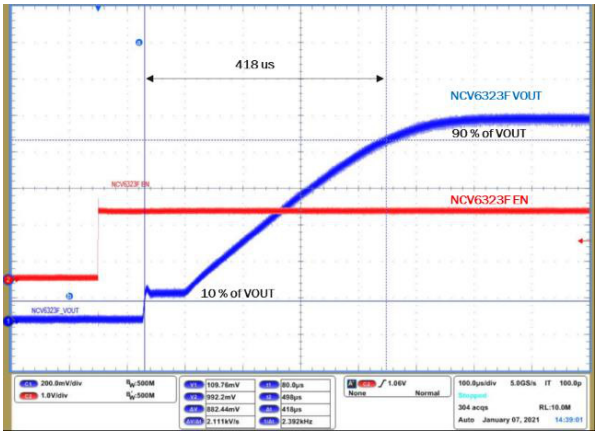


Figure 61. Soft Start Time T_{SS} (NCV6323FELMTW11, C_{OUT} = 10 µF)

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TYPICAL OPERATING CHARACTERISTICS (continued)

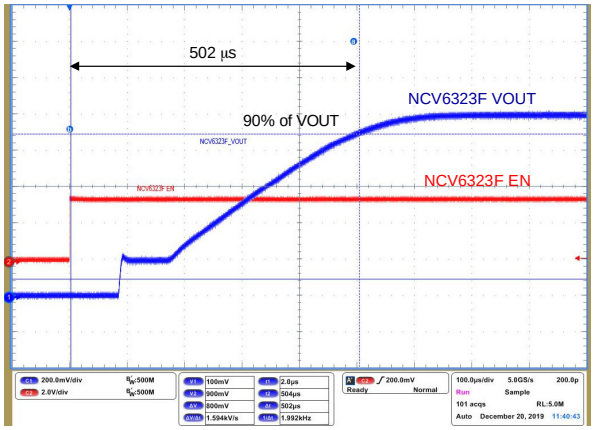


Figure 62. Startup Time T_{START} ($NCV6323FELMTW10, C_{OUT}$ = 10 µF)

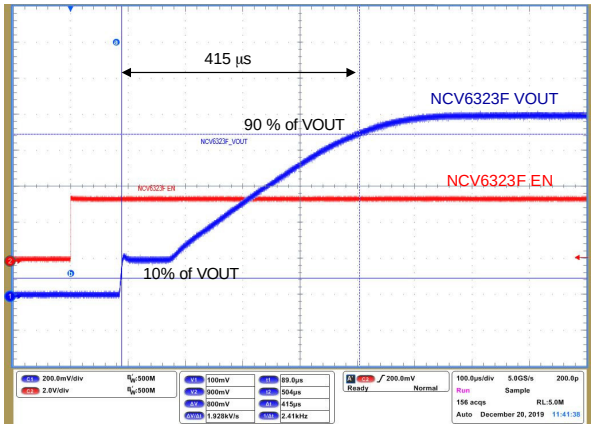


Figure 63. Soft Start Time T_{SS} ($NCV6323FELMTW10, C_{OUT}$ = 10 µF)

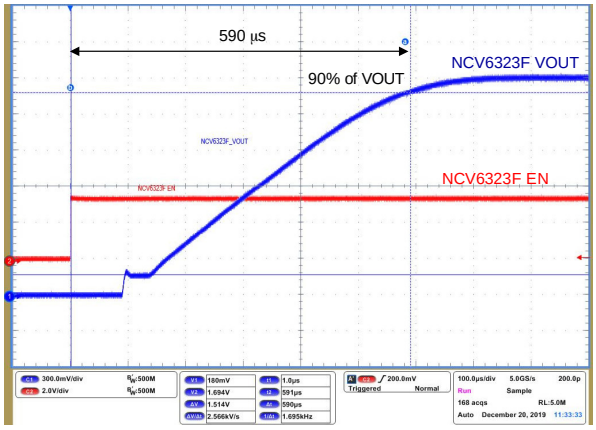


Figure 64. Startup Time T_{START} ($NCV6323FELMTW18, C_{OUT}$ = 10 µF)

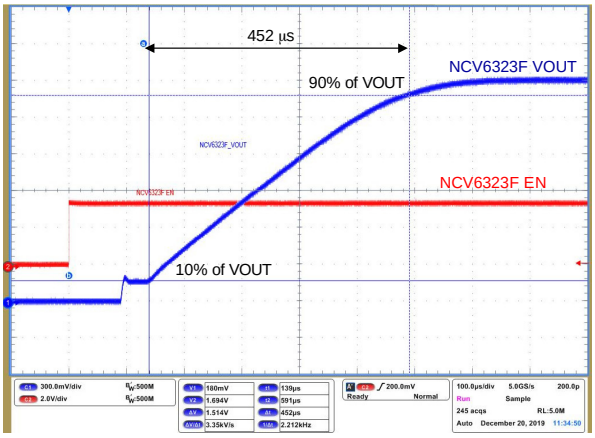


Figure 65. Soft Start Time T_{SS} ($NCV6323FELMTW18, COUT$ = 10 µF)

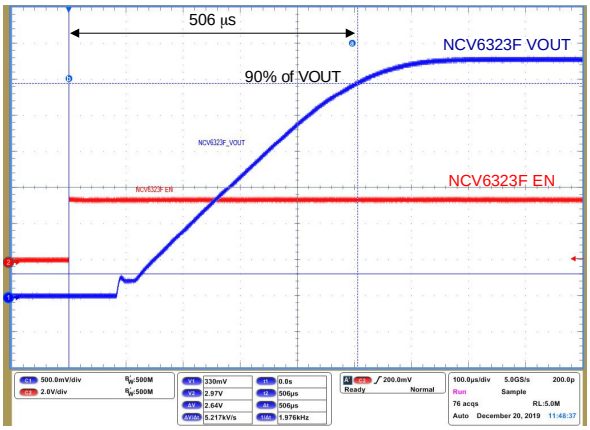


Figure 66. Startup Time T_{START} ($NCV6323FELMTW33, C_{OUT}$ = 10 µF)

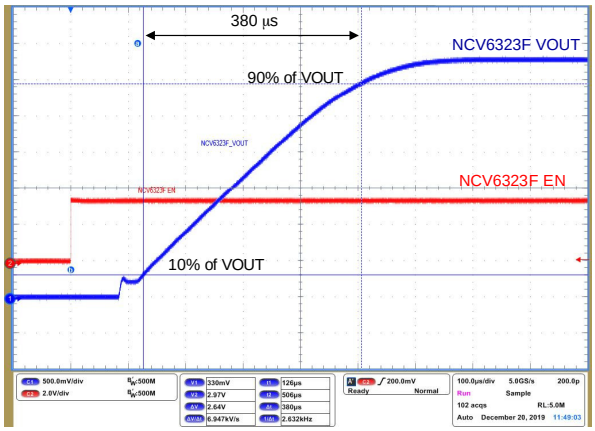


Figure 67. Soft Start Time T_{SS} ($NCV6323FELMTW33, COUT$ = 10 µF)

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TYPICAL OPERATING CHARACTERISTICS (continued)

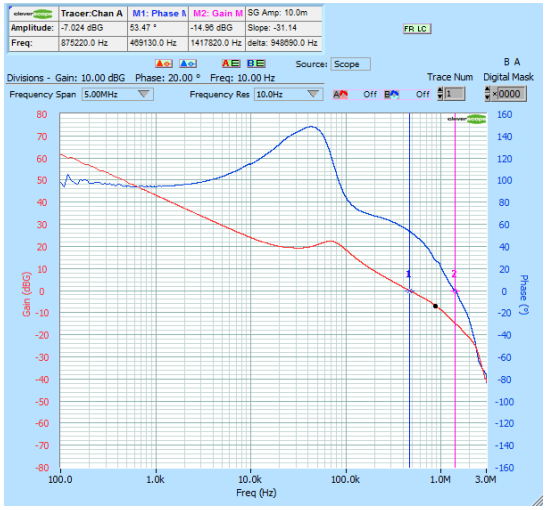


Figure 68. Bode Plot NCV6323FxLMTW18TBG L = 1.0 μH – COUT = 10 μF

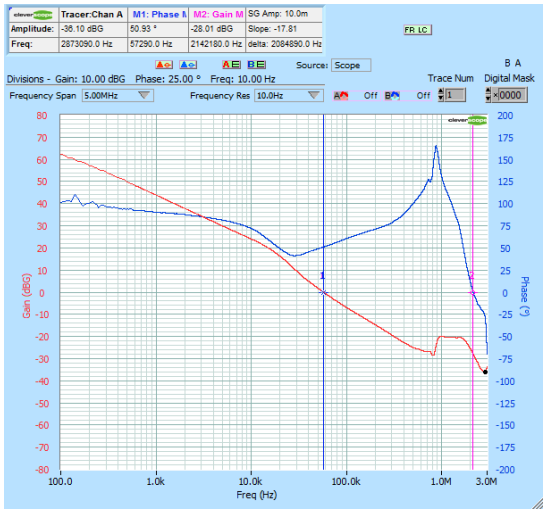


Figure 69. Bode Plot NCV6323FxLMTW18TBG L = 1.0 μH – COUT = 100 μF

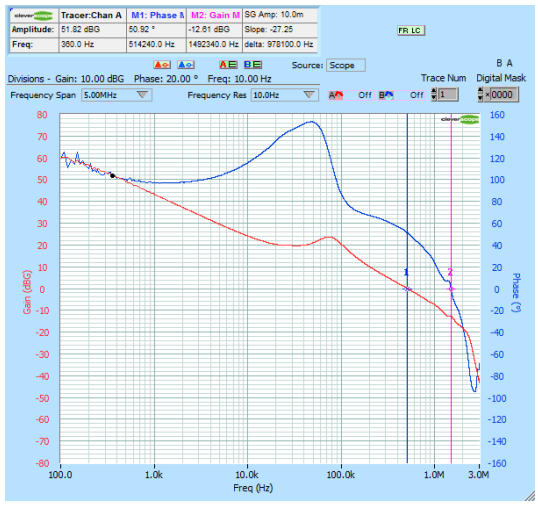


Figure 70. Bode Plot NCV6323FxLMTW33TBG L = 1.0 μH – COUT = 10 μF

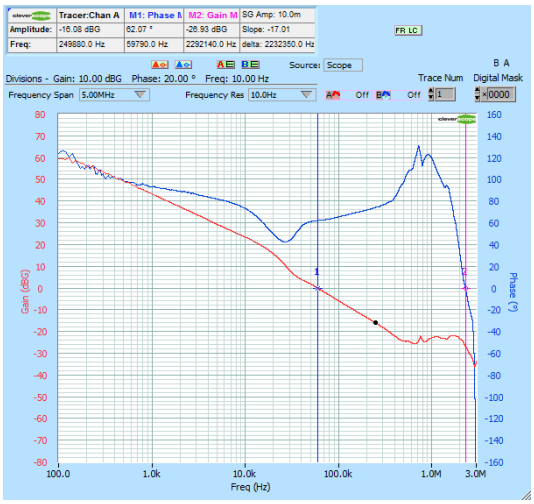


Figure 71. Bode Plot NCV6323FxLMTW33TBG L = 1.0 μH – COUT = 100 μF

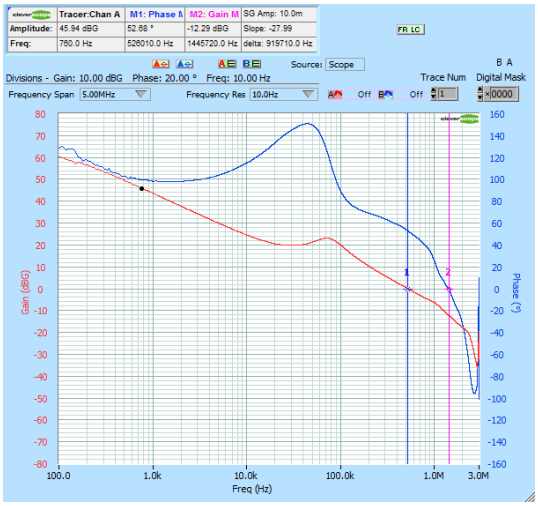


Figure 72. Bode Plot NCV6323FxLMTW12TBG L = 1.0 μH – COUT = 10 μF

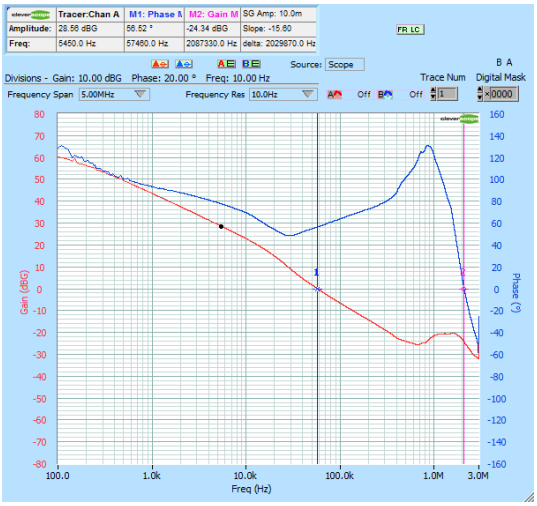


Figure 73. Bode Plot NCV6323FxLMTW12TBG L = 1.0 μH – COUT = 100 μF

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TYPICAL OPERATING CHARACTERISTICS (continued)

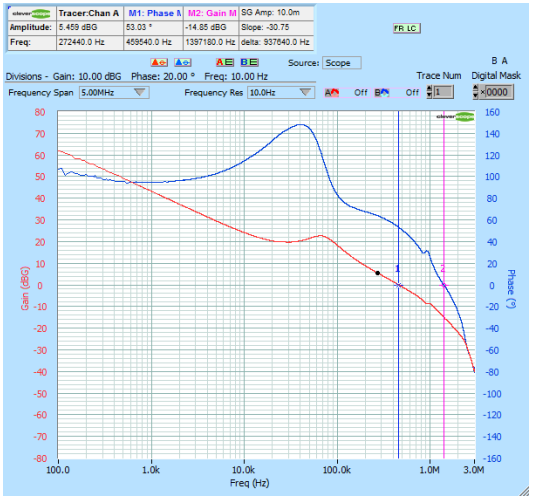


Figure 74. Bode Plot NCV6323FxLMTW10TBG L = 1.0 μH – COUT = 10 μF

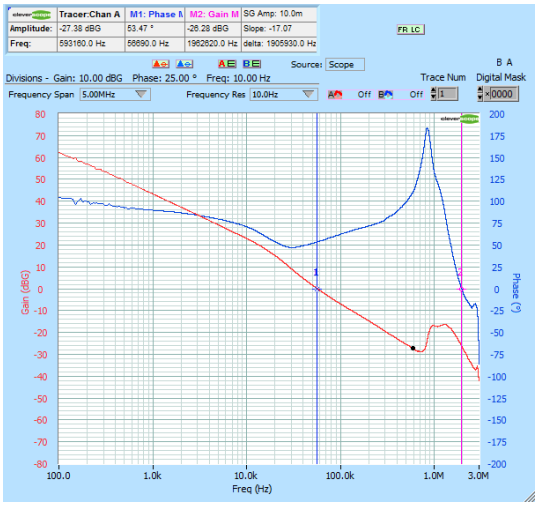


Figure 75. Bode Plot NCV6323FxLMTW10TBG L = 1.0 μH – COUT = 100 μF



Figure 76. Bode Plot NCV6323FxLMTW11TBG L = 1.0 μH – COUT = 10 μF



Figure 77. Bode Plot NCV6323FxLMTW11TBG L = 1.0 μH – COUT = 100 μF

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DETAILLED OPERATING DESCRIPTION

General

The NCV6323F is a voltage mode standalone synchronous PWM DC−DC converter optimized to supply the different sub systems of automotive applications from a pre−regulator supply rail in the 2.8 V to 5.5 V range. It can deliver up to 1.6 A to an internally factory set voltage (please refer to the ORDERING INFORMATION table). The 3 MHz switching frequency allows using small output filter components. A Power Good (PG) indicator is available. The synchronous rectification offers high system efficiency and integrated feedback network allows very simple and straightforward implementation to power supply designers with only a few components to select.

The NCV6323F is housed in a low profile 2.0 x 2.0 mm uDFN−8 package.

DC−DC Converter Operation

The converter integrates both high side and low side (synchronous) switches. Neither external transistors nor diodes are required for NCV6323F operation. The feedback and compensation networks are also fully integrated. It operates in PWM.

PWM Operation

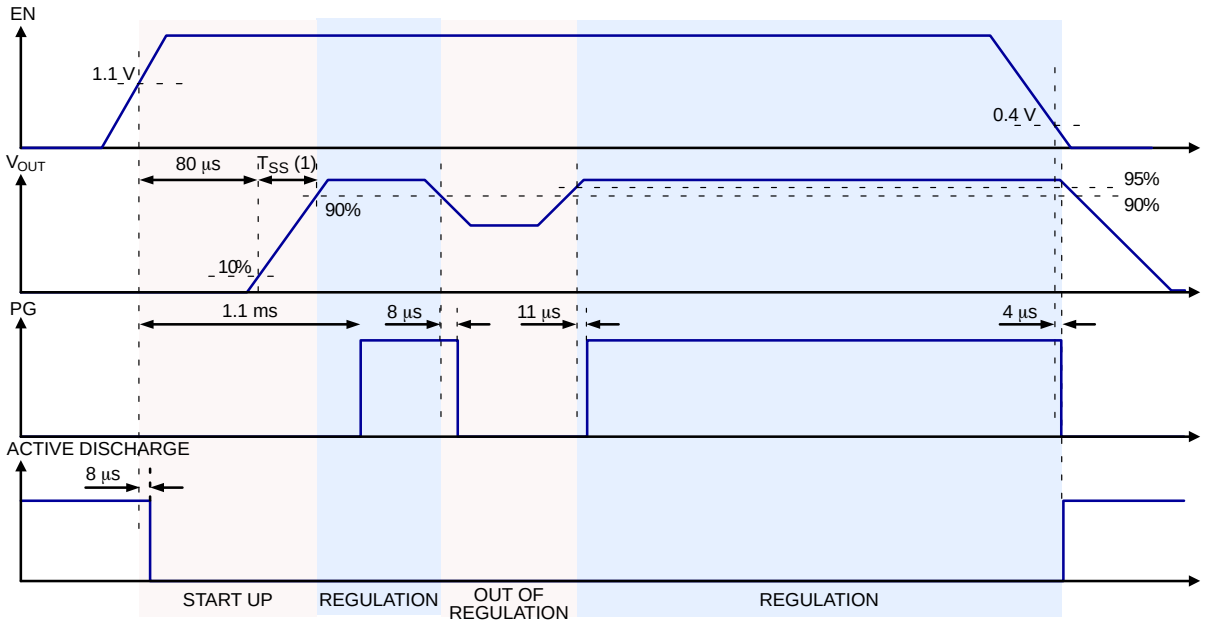
The device operates in PWM mode with 3 MHz typical fixed switching frequency. In this operating scheme, the output voltage is regulated by on−time Pulse Width Modulation (PWM) of an integrated high side P−MOSFET. A low side N−MOSFET, also integrated in the IC, operates as synchronous rectifier and its turn−on signal is complimentary to that of the P−MOSFET (with built in dead time control to avoid cross conduction)

Under Voltage Lockout

The input voltage VIN must reach or exceed 2.8 V (maximum) before the NCV6323F enables the converter output to begin the startup sequence. The UVLO threshold hysteresis is typically 150 mV.

Enable

The NCV6323F has an enable logic input pin EN. A high level (above 1.1 V) on this pin enables the device to active mode. A low level (below 0.4 V) on this pin disables the device and makes the device in shutdown mode. There is an internal filter with 5 µs time constant. The EN pin is pulled down by an internal 100 nA sink current source.



(1) T_{SS} timing depends on the IC version.
Please refer to the full part number of the considered version and to the electrical tables

Figure 78. Power Good and Active Discharge Timing Diagrams

Power Good Output (PG)

The device monitors the output voltage and provides a power good signal at the PG pin. This pin is an open−drain output. This signal indicates that the desired voltage is regulated properly and is valid as soon as the Enable (EN) pin enables the device. When EN is high, the power good pin is tied to low level when the output voltage is considered as out of regulation (less than 90% of the desired value). During the startup sequence, this signal indicates that the output voltage is not yet established, while during normal operation, a High to Low transition of PG indicates that the output voltage sags under 90% of its target and is out of regulation. A low level at the power good signal indicates a power failure. An internal 5% hysteresis is implemented on the power good comparator.

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When EN is low (NCV6323F disabled), the discharge path (refer to the “Discharge Path” section) drives the output voltage to ground. In that condition, the PG is maintained to low by a weak pull down.

Soft−Start (SS)

A soft start limits inrush current when the converter is enabled. After a minimum 80 μs typical delay time following the enable signal, the output voltage ramp is controlled during the T_{SS} time. The T_{SS} time is factory programmed. Please refer to the ordering information to select the T_{SS} that fit better with the application requirements or that is available. If not available, please contact your sales representative office.

T_{SS} = 440 μs (NCV6323F−xxE).

Active Output Discharge

An output discharge operation is active in when EN is low. A discharge resistor (450 Ω typical) is enabled in 4 μs after the High to Low transition of the EN signal to discharge the output capacitor through SW pin.

Cycle−by−Cycle Current Limitation

The NCV6323F protects the device from over current with a fixed−value cycle−by−cycle current limitation. The typical peak current limit ILMT is 2.6 A (10, 11, 12, 18 versions) and 2.45 A (33 version). If the inductor current exceeds the current limit threshold, the P−MOSFET will be turned off cycle−by−cycle. The maximum output current can be calculated by

$$I_{MAX} = I_{LIMIT} - \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times V_{IN} \times f_{SW} \times L} \quad \text{(eq. 1)}$$

Where V_{IN} is input supply voltage, V_{OUT} is output voltage, L is inductance of the filter inductor, and f_{SW} is 3 MHz normal switching frequency.

In output short circuit condition, if the short impedance becomes low enough to maintain the NCV6323F V_{OUT} lower than 300 mA (max), because of the internal delays in the detection system, the Peak Current Limit can become non operative.

Negative Current Protection

The NCV6323F includes a cycle by cycle 0.8 A typical negative current protection in the N−MOSFET Low Side Switch (LSS). This current limitation protects the internal LSS when the output cap has to be discharged during regulation to allow fast recovery to the target output voltage. This can happen mainly when the capacitive load is pretty high and the IC recovers after a fast negative load transient (load release).

In output short circuit condition, if the short impedance becomes low enough to maintain the NCV6323F V_{OUT} lower than 300 mA (max), because of the internal delays in the detection system, the Peak Current Limit can become non operative.

Thermal Shutdown (TSD)

The power dissipation of the output stage can lead the die temperature to exceed the maximum rating of the silicon. To avoid irreversible damage and hazard in its normal operation, the NCV6323F features a Thermal Shutdown to protect the device from overheating when the die temperature exceeds 150°C.

When activated, the TSD will immediately stop the power stage switching activity, turns it off and the output voltage is switched off. The PG indicator will transition to Low level, indicating a power fail.

During TSD activation, the die will cool down to a more acceptable temperature level and, when the temperature gets down below 125°C again , the switching activity will be released and the PG pin will transition to high again as soon as the output voltage has recovered.

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APPLICATION INFORMATION

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \quad \text{(eq. 2)}$$

The internal compensation network design of the NCV6323F is optimized for a typical output filter comprised of a 1.0 μH inductor and a 10 μF ceramic output capacitor, which has a double pole frequency at about 50 kHz. Other possible output filter combinations may have a double pole around 50 kHz to have optimum operation with the typical feedback network. Normal selection range of the inductor is from 0.47 μH to 4.7 μH, and normal selection range of the output capacitor is from 4.7 μF to 22 μF.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{L_PP} of approximately 20% to 50% of the maximum output current I_{OUT_MAX} for a trade−off between transient response and output ripple. The inductance corresponding to the given current ripple is

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{L_PP}} \quad \text{(eq. 3)}$$

The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is

$$I_{L_MAX} = I_{OUT_MAX} + \frac{I_{L_PP}}{2} \quad \text{(eq. 4)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Table xx shows some recommended inductors for high power applications and Table xx shows some recommended inductors for low power applications.

Table 1. LIST OF RECOMMENDED INDUCTORS FOR HIGH POWER APPLICATIONS

Manufacturer	Part #	Case Size (mm)	L (μH)	Rated Current (mA) (Inductance Drop)
MURATA	DFE252012PD−1R0M#	2.5 x 2.0 x 1.2	1.0	3800
MURATA	LQH2HPZ1R0MGR#	2.5 x 2.0 x 0.9	1.0	2100
MURATA	LQH2HPZ1R0NJR#	2.5 x 2.0 x 1.1	1.0	2600
TDK	TFM252012ALMA1R0MTAA	2.5 x 2.0 x 1.2	1.0	4200
TDK	TFM201610ALMA1R0MTAA	2.0 x 1.6 x 1.0	1.0	3700

Table 2. LIST OF RECOMMENDED INDUCTORS FOR LOW POWER APPLICATIONS

Manufacturer	Part #	Case Size (mm)	L (μH)	Rated Current (mA) (Inductance Drop)
MURATA	LQH3NPZ1R0MGR#	3.0 x 3.0 x 0.9	1.0	1700
TDK	MLD2016S1R0MTD25	2.0 x 1.6 x 0.9	1.0	1100
TDK	TFM201210ALMA1R0MTAA	2.0 x 1.25 x 1	1.0	2000

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For a given peak−to−peak ripple current IL_PP in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three ripple components as below

$$V_{OUT_PP} \approx V_{OUT_PP(C)} + V_{OUT_PP(ESR)} + V_{OUT_PP(ESL)} \quad \text{(eq. 5)}$$

Where $V_{OUT_PP(C)}$ is a ripple component by an equivalent total capacitance of the output capacitors, $V_{OUT_PP(ESR)}$ is a ripple component by an equivalent ESR of the output capacitors, and $V_{OUT_PP(ESL)}$ is a ripple component by an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUT_PP(C)} = \frac{I_{L_PP}}{8 \times C \times f_{SW}} \quad \text{(eq. 6)}$$

$$V_{OUT_PP(ESR)} = I_{L_PP} \times ESR \quad \text{(eq. 7)}$$

$$V_{OUT_PP(ESL)} = \frac{ESL}{ESL + L} \times V_{IN} \quad \text{(eq. 8)}$$

And the peak−to−peak ripple current is

$$I_{L_PP} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \quad \text{(eq. 9)}$$

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In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT_PP(C)}$. So that the minimum output capacitance C_{OUT_MIN} can be calculated regarding to a given output ripple requirement V_{OUT_PP} in PWM operation mode.

$$C_{OUT_MIN} = \frac{I_{L_PP}}{8 \times V_{OUT_PP} \times f_{SW}} \quad \text{(eq. 10)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance C_{IN_MIN} regarding to the input ripple voltage V_{IN_PP} is

$$C_{IN_MIN} = \frac{I_{OUT_MAX} \times (D - D^2)}{V_{IN_PP} \times f_{SW}} \quad \text{(eq. 11)}$$

Where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 12)}$$

In addition, the input capacitor needs to be able to absorb the input current, which has an RMS value of

$$I_{IN_RMS} = I_{OUT_MAX} \times \sqrt{D - D^2} \quad \text{(eq. 13)}$$

The input capacitor also needs to be sufficient to protect the device from over voltage spike, and normally at least a 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC on PCB.

Table 3. LIST OF RECOMMENDED INPUT AND OUTPUT CAPACITORS

Manufacturer	Part #	Case Size (mm)	Technology	C (μF)	Rated Voltage (V)
TDK	CGA4J3X7R1A475K125AB	0805	X7R	4.7	10
TDK	CGA3E3X7S1A225K080AB	0603	X7S	2.2	10
MURATA	GCM21BC71A475KA73	0805	X7S	4.7	10
MURATA	GCM188D70J106M	0603	X7T	10	6.3
MURATA	GCM21BR70J106KE22#	0805	X7R	10	6.3
TDK	CGA4J1X7R0J106K125	0805	X7R	10	6.3

Stability of the Regulation Loop

The NCV6323F is a voltage mode DC to DC converter with a double pole at the f_{LC} frequency and a zero at the f_0 frequency:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \quad \text{(eq. 14)}$$

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C} \quad \text{(eq. 15)}$$

With L = the output inductor and C the total amount of capacitance connected to the NCV6323F output. This capacitance value should not only take into account the LC filter capacitor, but also all other capacitors connected between the rail NCV6323F supplies and the GND.

The loop is compensated by a type III network.

As, besides the external LC filter, all the other parameters that govern the loop response and stability are integrated in the NCV6323F, it is important to evaluate and consider, during the design stage, the real value of the output capacitor C and select the right NCV6323F option.

In order to accommodate a large range of applications, 2 options of the compensation loop are available (please refer to the ORDERING INFORMATION table):

- NCV6323Fx*L* that address the application with output capacitor ranging from 10 to ~100 μF
- NCV6323Fx*H* that address the application with output capacitor ranging from 50 to ~250 μF

If the output capacitor is comprised within the overlap range (50 ~ 100 μF), it is suggested to select the L option if C ≤ 80 μF and the H option if C > 80 μF.

Maximum Current and Thermal Considerations

To avoid irreversible damage and overheating, the Thermal Shut Down (TSD) of the NCV6323F will stop the power stage switching activity as soon as the die temperature rises up to 150°C TSD threshold. Dissipation in the power stage mainly depends on the losses in the HSS (High Side Switch) and LSS (Low Side Switch) and is then directly function of the loading current.

The NCV6323F specification is guaranteed for a maximum Junction Temperature (T_{J_MAX}) of 125°C. When the junction temperature ranges from 125°C to the TSD threshold, the IC will still operate and will not be damaged, but the specifications are not guaranteed and the parameters value may deviate significantly. It is then important to try to keep the $T_J \le 125°C$.

The THERMAL INFORMATION table provides the thermal parameters ($R_{\Theta Jx}$) defined by the JEDEC JESD51−3 as well as some thermal characterization parameters (Ψ_{Jx}). The thermal characterization parameters are the result of measurements on the standard NCV6323F demo board, while the thermal parameters are the result of simulations in the JESD51 defined environment.

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Based on those parameters and the efficiency, a Safe Operating Area, that keeps the junction temperature lower than 125°C, can be defined.

On the standard demo board, the maximum power (P_{D_MAX}) the package can dissipate with 105°C ambient temperature (T_A), can be calculated as:

$$P_{D_MAX} = \frac{T_{J_MAX} - T_{A_MAX}}{R_{\Theta JA}} \quad \text{(eq. 16)}$$

With: T_{J_MAX} = maximum junction temperature (125°C), T_{A_MAX} = maximum ambient temperature (105°C) and $R_{\Theta JA}$ = Junction to Ambient thermal resistance measured on our evaluation board (~40°C/W), P_{D_MAX} = 500 mW.

Thus, for T_A = 105°C:

Table 4. MAXIMUM OUTPUT CURRENT AT T_A = 105°C

V_{IN} (V)	V_{OUT} (V)	Max I_{OUT} (A)
5.0	1.0	1.2
	1.1	1.2
	1.2	1.2
	1.8	1.2
	3.3	1.2
3.3	1.0	1.1
	1.1	1.1
	1.2	1.2
	1.8	1.2

The below figure is a simulation result showing the die temperature gradient when the NCV6323F dissipates 500 mW. As expected, the output stage is the hottest part of the die and gets to about 125°C.

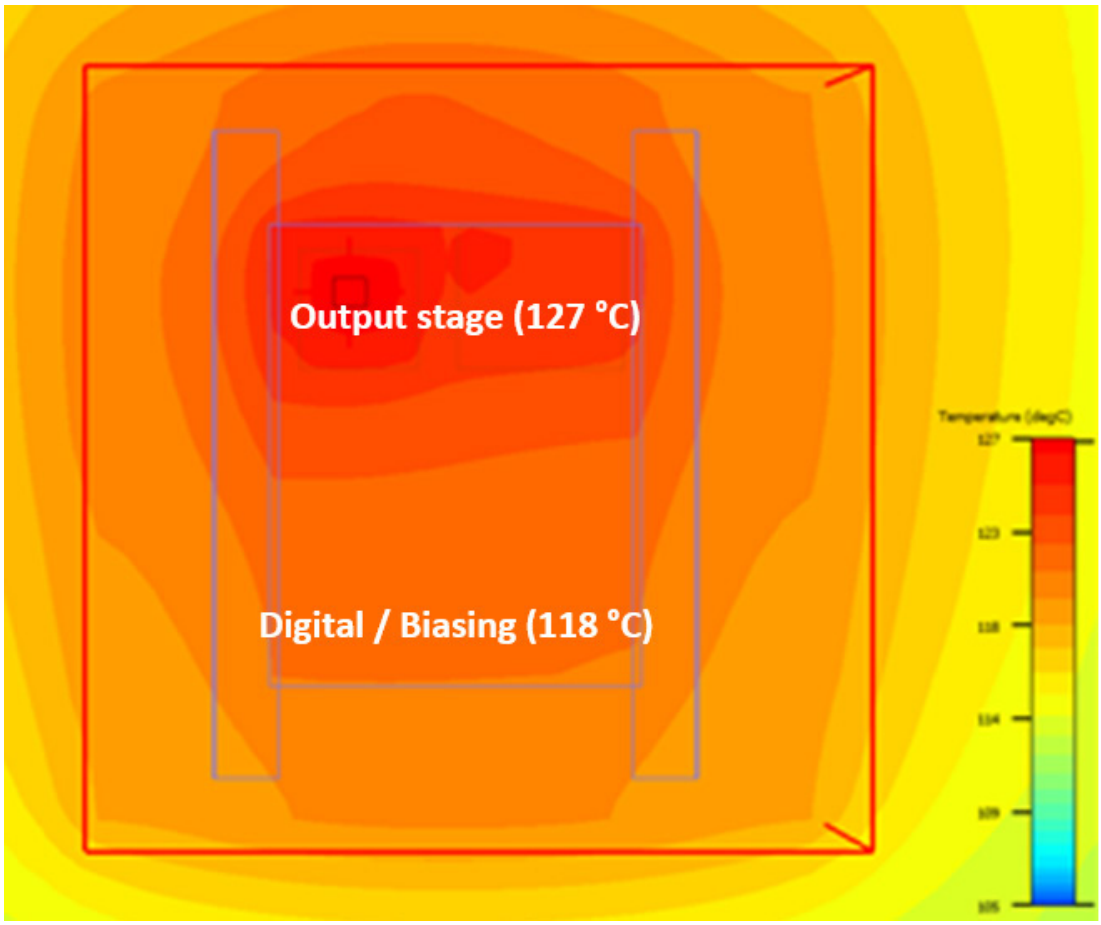


Figure 79. Die Temperature Simulation (500 mW Dissipated Power)

FeedBack (FB) Pin Leakage Current

The FB pin is internally connected to the resistor ladder that divides the V_{OUT} voltage and feeds the error amplifier. This ladder has a typical impedance of 260 kΩ, thus, the FB pin input leakage current value is:

$$I_{FB} = (V_{OUT} - 0.6) / 260.10^3 \quad \text{(eq. 17)}$$

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LAYOUT CONSIDERATIONS

Switching Noise Consideration

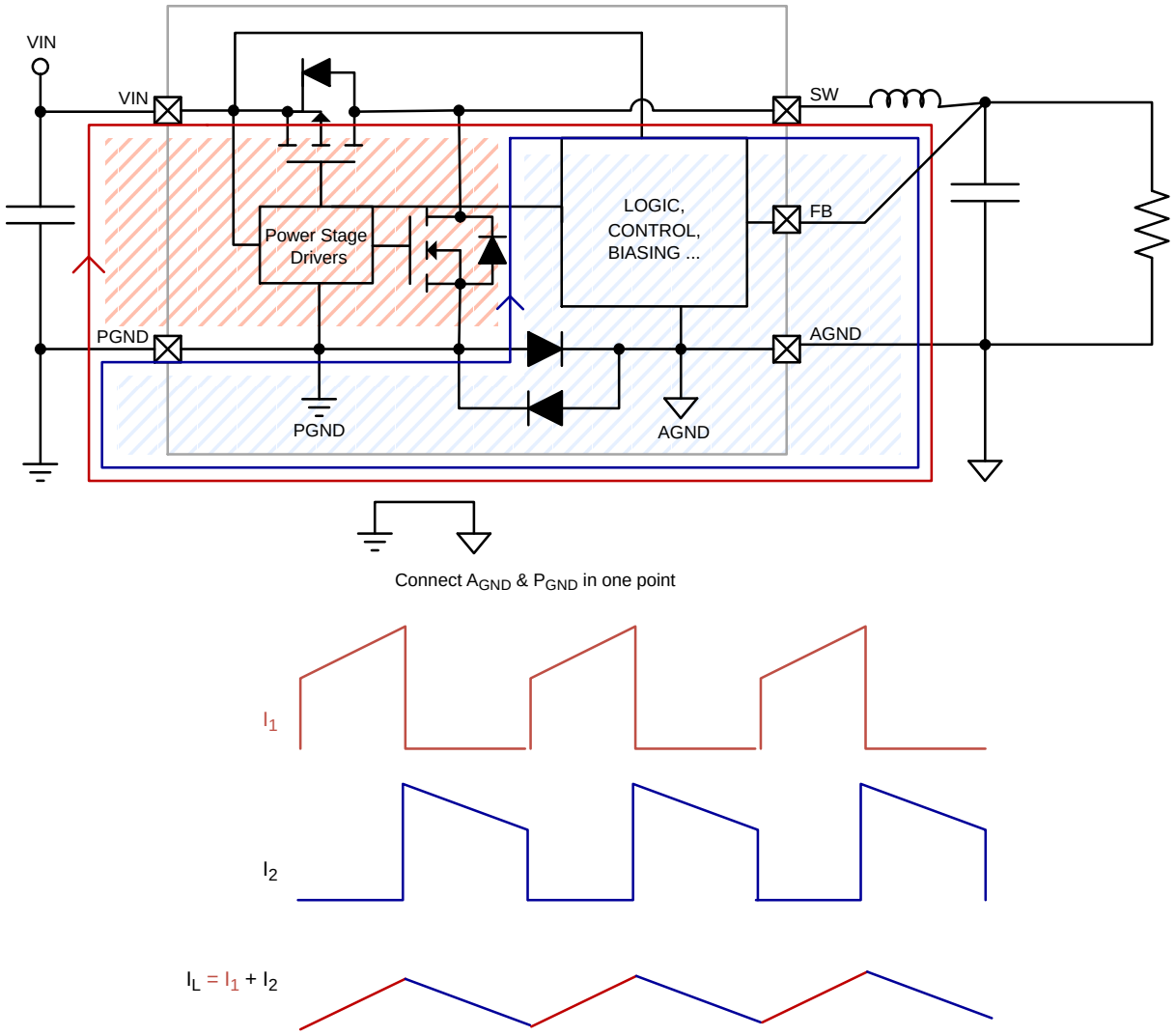


Figure 80. AC Current Flowing Loops

- The DC/DC buck converter has two main loops where high AC currents flow.
- When the High−Side Switch (HSS) is on, the current flows from VCC via HSS and L to the output capacitor and the load. The current flows back via ground to the input. The AC portion of the current will flow via the input and output capacitors. This current is shown in red color (I1).
- When HSS switches off, the inductor current will keep flowing in the same direction, and the Low−Side Switch (LSS) is switched on. The current flows via LSS, L, load and output capacitor and back via ground to LSS. This loop is shown in blue (I2).
- Both I1 and I2 are discontinuous currents, meaning that they have sharp rising and falling edges at the beginning and end of the active time. These sharp edges have fast rise and fall times (high dI/dt). Therefore they have a lot of high frequency content.
- I1 and I2 share a common path from switch node to inductor to output capacitor to ground back to the source of LSS. The sum of I1 and I2 is a relatively smooth continuous saw−tooth waveform, which has less high frequency content due to the absence of high dI/dt edges.
- From noise point of view, the current loop with the high dI/dt current is the red shaded area. This loop will generate the most high frequencies and should be considered the most critical loop for noise in buck converters. The dI/dt of the current in the blue shaded area is not as high as it is in the other area and generally generates a lot less noise.

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Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Since the red shaded area is the noisiest loop, it is critical to identify it and to place the input cap in such a way that this loop is minimized. It is also important to make sure that the path between the 2 terminals of the input cap and the PVIN & PGND pins is as short as possible and free of any vias to either the VIN or the GND PCB plane. It can also be a good practice to make a local PGND and VIN planes and to keep those planes as solid as possible below and in the input switching loop. Any trace or vias in this area reduces the plane effectiveness and increase the plane impedance. Vias from these planes to the other main planes of the PCB should be placed outside of the critical loop.
- Also, it is important to place the output capacitor ground in an area that does not overlap the input capacitor switching loop : this could generate extra high frequency noise in the output voltage
- Connecting the PGND plane to the main PCB GND plane (to whitch the AGND pin should be connected too) in one point (doing a kind of “star routing”) is also important to isolate the AGND and keep them quiet.
- Use wide and short traces for power paths (such as P_{VIN}, V_{OUT}, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW node should be a large copper pour, but compact because it is also a noise source.
- It would be good to have separated local ground planes for PGND and AGND and connect the two planes at one point. Directly connect AGND pin to the exposed pad and then connect to AGND ground plane through vias. Try best to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a “quiet” path for output voltage sense, and make it surrounded by a ground plane.

Component Placement

- C_{IN} Input capacitor placed as close as possible to the IC.
- PVIN directly connected to C_{IN} input capacitor, and then connected to the VIN plane. Local mini planes used on the top layer and the layer just below the top layer with laser vias.
- AVIN connected to the VIN plane just after the capacitor.
- AGND directly connected to the GND plane.
- PGND directly connected to C_{IN} input capacitor, and then connected to the GND plane: Local mini planes used on the top layer and the layer just below the top layer with laser vias.
- SW connected to the L_{OUT} inductor with local mini planes on the top layer.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pad must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and/or underneath the exposed pad to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed

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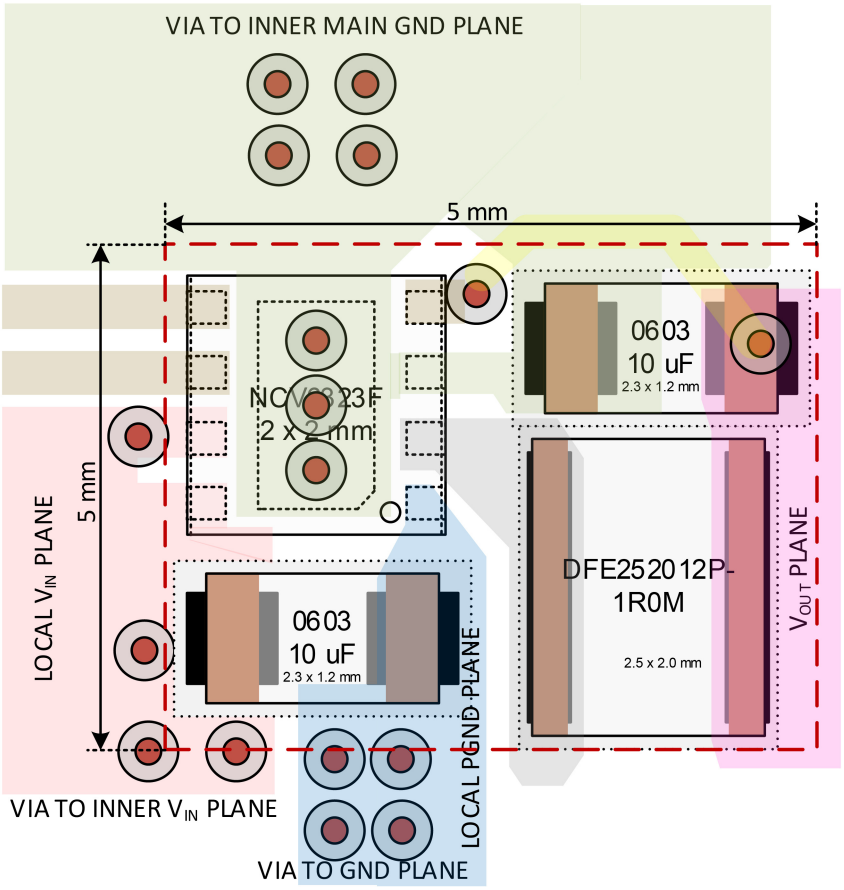


Figure 81. Recommended Minimal Size PCB Layout (Without Optional C_{AVIN})

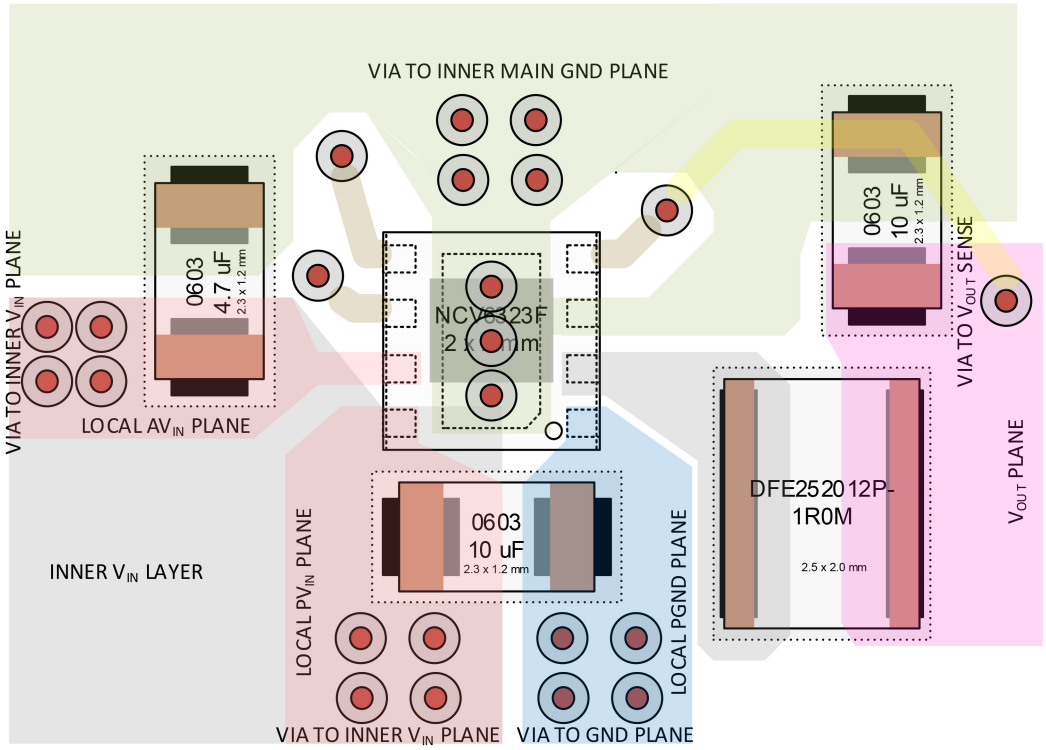


Figure 82. Recommended Large Size PCB Layout (With Optional C_{AVIN})

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ORDERING INFORMATION

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV6323F*EL*MTW*12*TBG	AA	WDFN8 with Wettable Flanks (Pb−Free)	3000 / Tape & Reel
NCV6323F*EL*MTW*18*TBG	AC	WDFN8 with Wettable Flanks (Pb−Free)	3000 / Tape & Reel
NCV6323F*EL*MTW*10*TBG	AD	WDFN8 with Wettable Flanks (Pb−Free)	3000 / Tape & Reel
NCV6323F*EL*MTW*33*TBG	AM	WDFN8 with Wettable Flanks (Pb−Free)	3000 / Tape & Reel
NCV6323F*EL*MTW*11*TBG	AL	WDFN8 with Wettable Flanks (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV6323F y z MTW xx(x) TBG

T_{SS} = Time for V_{OUT} to rise from 10 % to 90 % of Target (*) (**)	Compensation optimized for output capacitor range	Fixed Output Voltage Options (*)

y	T_{SS}
	0 (*)
	20 μs (*)
	40 μs (*)
	60 μs (*)
	80 μs (*)
	100 μs (*)
	120 μs (*)
	160 μs (*)
	180 μs (*)
	200 μs (*)
	220 μs (*)
	240 μs (*)
	360 μs (*)
	400 μs (*)
E	440 μs

Z	C_{OUT} Range
L	10 μF ≤ C_{OUT} < 100 μF
H	50 μF ≤ C_{OUT} < 250 μF (*)

xx (x)	V_{OUT}
10	1.0 V
12	1.2 V
13	1.3 V (*)
15	1.5 V (*)
18	1.8 V
25	2.5 V (*)
28	2.8 V (*)
33	3.3 V
09	0.9 V (*)
11	1.1 V
135	1.35 V (*)
185	1.85 V (*)
27	2.7 V (*)
285	2.85 V (*)
29	2.9 V (*)
30	3.0 V (*)

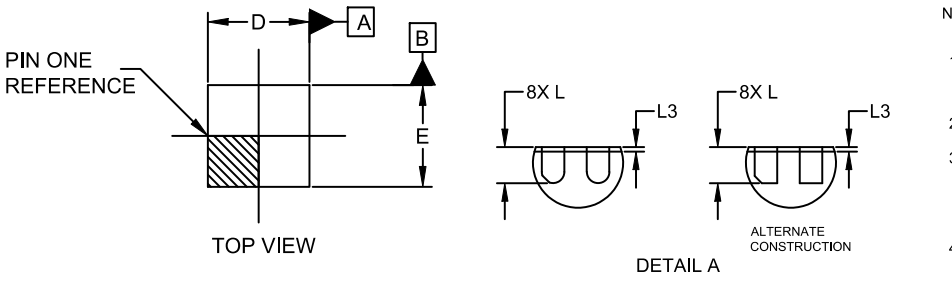
(*) Available upon request (Please contact your ON Semiconductor sales office)
(**) For more detailed information, refer to the Enable section of the DETAILLED OPERATING DESCRIPTION

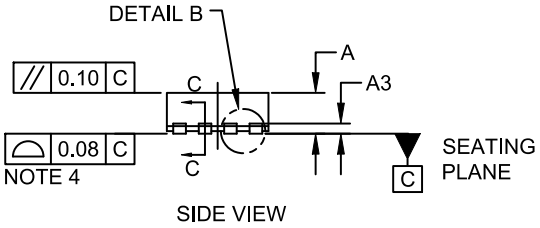
Figure 83.

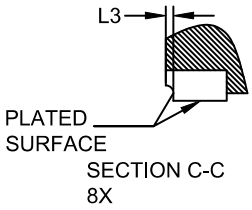
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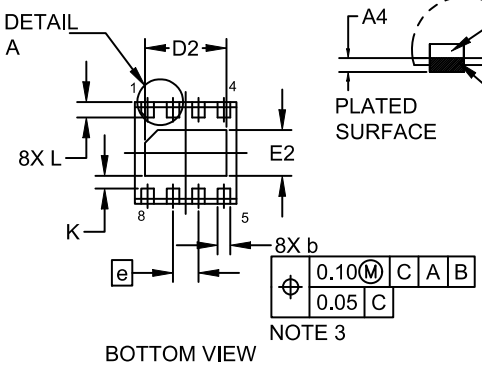
PACKAGE DIMENSIONS

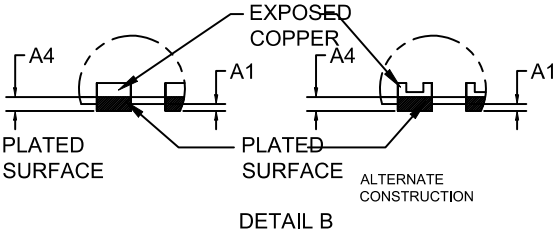
WDFNW8 2x2, 0.5P
CASE 511CL
ISSUE B







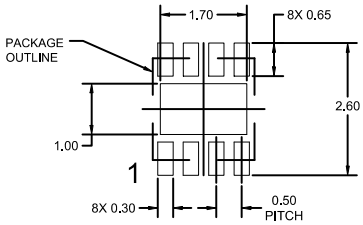




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINALS AND ARE MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e		0.50 BSC	
K		0.25 REF	
L	0.20	0.30	0.40
L3	---	---	0.10



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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