Compact, Low Power, 16-Bit, 2 MSPS/500 kSPS Easy Drive SAR ADC

FEATURES

- Small footprint, big performance
  - INL: ±0.5 LSB maximum
  - SNR: 86.1 dB with V_{REF} = 3.3 V
  - 1.35 nJ per conversion
  - 1.35 mW/0.68 mW at 1 MSPS/500 kSPS in sample mode
  - 370 µW/112 µW at 1 MSPS/300 kSPS in autonomous modes
  - 4.1 µW standby power
- Versatile signal conditioning integration
  - Easy Drive features enable small, low-power AFE designs
  - Compatible with differential and single-ended signal chains
  - Wide common-mode input range
- Minimizes digital host activity and power dissipation
  - Autonomous sampling with window comparator and interrupt generation
  - Averaging filter with continuous and burst sampling options
  - Power cycling synchronization for companion devices
- 4-wire SPI compatible with 1.8 V to 3.3 V logic
- 2.00 mm × 2.6 mm LFCSP and 1.67 mm × 1.97 mm WLCSP
- Wide operating temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered data acquisition
- Vital signs monitoring
- Biological and chemical analysis
- Geologic and seismic sensing
- Motion and robotics

GENERAL DESCRIPTION

The AD4052/AD4058 are versatile, 16-bit, successive approximation register (SAR) analog-to-digital converters (ADCs) that enable low-power, high-density data acquisition solutions without sacrificing precision. These ADCs offer a unique balance of performance and power efficiency, plus innovative features for seamlessly switching between high-resolution and low-power modes tailored to the immediate needs of the system. The AD4052/AD4058 are ideal for battery-powered, compact data acquisition and edge sensing applications.

The Easy Drive features enable highly efficient analog front end (AFE) designs. The small sampling capacitors (3.4 pF) maximize input impedance, thus reducing the dependence on high-bandwidth, power-hungry amplifiers typically required by SAR ADCs. The wide input common-mode range grants inherent support for both differential and single-ended signals.

The AD4052/AD4058 support microcontrollers with power-down modes and interrupt-driven firmware. The autonomous modes enable out-of-range event detection while the digital host sleeps. The averaging modes deliver on-demand, high-resolution measurements while offloading computations from the host processor. The self timed device enable signal (DEV_EN) synchronizes AFE device power cycling to the ADC sampling instant, optimizing system power consumption while minimizing power-up settling error artifacts. The AD4052/AD4058 also support power cycling the voltage reference and using the supply as the ADC reference voltage (V_{REF}) for additional power savings.

The device configuration and ADC data readback are supported via a robust, 4-wire serial peripheral interface (SPI) with cyclic redundancy check (CRC) supported for all data transfers. The AD4052/AD4058 are available in compact LFCSP and WLCSP packages and operate across a wide temperature range, making them ideal for a diverse set of applications.

FUNCTIONAL BLOCK DIAGRAM

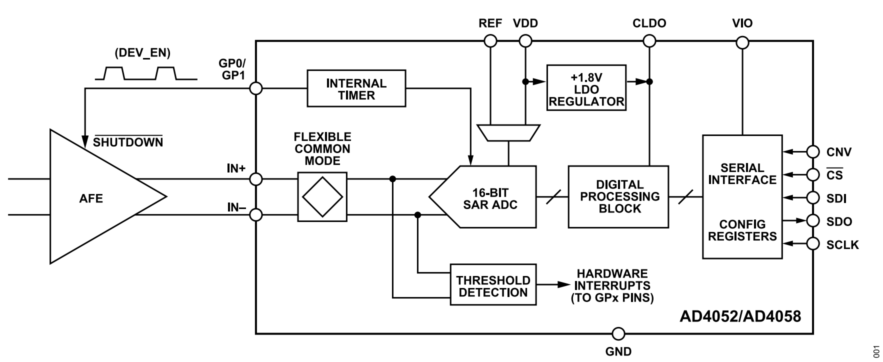

Figure 1. Functional Block Diagram

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REVISION HISTORY

2/2026—Rev. B to Rev. C

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SPECIFICATIONS

VDD = 2.3 V to 3.6 V, V_{REF} = 2.3 V to 3.6 V, VIO = 1.71 V to 3.6 V, reference capacitance (C_{REF}) = 2.2 µF, and operating at the maximum specified sample rate (f_S), unless otherwise specified. All other features in default configuration, minimum and maximum values at T_A = −40°C to +125°C, and typical values at T_A = +25°C, unless otherwise specified.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION					
ADC Resolution		16			Bits
Averaging Filter Resolution	Averaging mode, burst averaging mode	20			Bits
Comparator Mode Resolution	Autonomous modes	12			Bits
SAMPLING DYNAMICS					
Sampling Rate (f_S)[1]	AD4052			2	MSPS
	AD4058			500	kSPS
Aperture Delay			0.3		ns
ANALOG INPUT					
Input Voltage (V_{IN}) Range[2]	$V_{IN} = V_{IN+} − V_{IN−}$				
	Differential mode	$−V_{REF}$		$+V_{REF}$	V
	Single-ended mode	0		$+V_{REF}$	V
Absolute Input Voltage[2]	V_{IN+}, $V_{IN−}$	−0.1		VDD + 0.1	V
Common-Mode Input Voltage (V_{CM}) Range[3]	$V_{CM} = (V_{IN+} + V_{IN−})/2$	−0.1		VDD + 0.1	V
Analog Input Leakage Current	IN+, IN−		6		nA
Sampling Capacitance (C_{IN})			3.4		pF
Analog Input Capacitance[4]	IN+, IN−				
Track Phase			5.4		pF
Hold Phase			2.0		pF
DC ACCURACY	V_{REF} = 3.3 V				
No Missing Codes		16			Bits
Transition Noise	Sample mode (no averaging)				
	Differential mode		1.1		LSB rms
	Single-ended mode		2.2		LSB rms
Low Frequency Noise	Bandwidth = 0.1 Hz to 10 Hz		9.3		µVpp
Integral Nonlinearity (INL)		−0.5	±0.15	+0.5	LSB
Differential Nonlinearity (DNL)[5]		−0.5	±0.1	+0.5	LSB
Zero Error		-350	±30	+350	µV
Zero-Error Drift			±0.03		ppm/°C
Gain Error		−0.03	±0.0008	+0.03	%FS
Gain Error Drift			±0.15		ppm/°C
Total Unadjusted Error (TUE)[6]		−200	±8	+200	ppm
Autonomous Mode TUE[7]			±7		mV
REFERENCE					
V_{REF} Input Range		2.3		VDD	V
REF Standby Current	V_{REF} = 3.3 V		8		nA
REF Average Input Current[8]	V_{REF} = 3.3 V, f_S = 2 MSPS (AD4052)		60	65	µA
	V_{REF} = 3.3 V, f_S = 500 kSPS (AD4058)		15	18	µA
AC PERFORMANCE	V_{REF} = 3.3 V				
Total RMS Noise	Sample mode (no averaging)		112		µVrms

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SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Averaging mode and burst averaging mode, averaging ratio (N_{AVG}) = 4		56		µVrms
	Averaging mode and burst averaging mode, averaging ratio N_{AVG} = 4096		2.2		µVrms
Dynamic Range					
Differential Mode	Sample mode (no averaging)		86.1		
	Averaging mode, burst averaging mode, N_{AVG} = 4		92.1		
	Averaging mode, burst averaging mode, N_{AVG} = 4096		120.7		
Single-Ended Mode	Sample mode (no averaging)		80.1		
	Averaging mode, burst averaging mode, N_{AVG} = 4		86.1		
	Averaging mode, burst averaging mode, N_{AVG} = 4096		114.7		
Signal-to-Noise Ratio (SNR)	V_{IN} = −0.5 dBFS, input frequency (f_{IN}) = 1 kHz				
Differential Mode	Sample mode (no averaging)	83.6	86.1		dB
	Averaging mode, N_{AVG} = 4		92.1		dB
	Averaging mode, N_{AVG} = 256		110		dB
Single-Ended Mode	Sample mode (no averaging)		80.1		dB
	Averaging mode, N_{AVG} = 4		86.1		
	Averaging mode, N_{AVG} = 256		104		
Total Harmonic Distortion (THD)	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz, sample mode		-118	-109	dB
Signal-to-Noise and Distortion (SINAD)	V_{IN} = −0.5 dBFS, f_{IN} = 1 kHz, sample mode				
Differential Mode		83.6	86.1		dB
Single-Ended Mode			80.1		dB
−3 dB Input Bandwidth			200		MHz
DIGITAL INPUTS					
Input Low Voltage (V_{IL})		−0.1 × VIO		+0.3 × VIO	V
Input High Voltage (V_{IH})		0.7 × VIO		1.1 × VIO	V
Input Low Current (I_{IL})		−1		+1	µA
Input High Current (I_{IH})		−1		+1	µA
Digital Input Capacitance			3		pF
DIGITAL OUTPUTS					
Output Low Voltage (V_{OL})	Digital output current = +500 µA			0.3	V
Output High Voltage (V_{OH})	Digital output current = −500 µA	VIO − 0.3			V
Digital Output Short-Circuit Current	VIO = 3.3 V				
Sourcing	Logic high shorted to 0 V		48		mA
Sinking	Logic low shorted to 3.3 V		38		mA
POWER REQUIREMENTS					
VDD		2.3		3.6	V
VIO		1.71		3.6	V
POWER SUPPLY CURRENT	VDD = 3.3 V				
Sleep Mode Current	f_S = 0 SPS				
VDD			10		nA
VIO	VIO = 1.8 V		20		nA
	VIO = 3.3 V		120		nA
Standby Current	f_S = 0 SPS				

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SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VDD			990		nA
VIO	VIO = 1.8 V		50		nA
	VIO = 3.3 V		260		nA
VDD Active Supply Current [9]					
Sample Mode and Averaging Mode	f_S = 10 kSPS		5.3		µA
	f_S = 500 kSPS (AD4058)		0.2	0.27	mA
	f_S = 1 MSPS (AD4052)		0.4		mA
	f_S = 1.5 MSPS (AD4052)		0.6	0.75	mA
	f_S = 2 MSPS (AD4052)		0.8	1	mA
Autonomous Modes	f_S = 10 kSPS		4.8		µA
	f_S = 300 kSPS (AD4058)		34	67	µA
	f_S = 1 MSPS (AD4052)		112		µA
	f_S = 2 MSPS (AD4052)		224	300	µA
POWER DISSIPATION	VDD = VIO = 3.3 V				
Sleep Mode Power Dissipation	f_S = 0 SPS		430		nW
Standby Power Dissipation	f_S = 0 SPS		4.1		µW
VDD Energy per Conversion			1.35		nJ
VDD Active Power Dissipation [9]					
Sample Mode and Averaging Mode	f_S = 10 kSPS		17.5		µW
	f_S = 500 kSPS (AD4058)		0.68	0.89	mW
	f_S = 1 MSPS (AD4052)		1.35		mW
	f_S = 1.5 MSPS (AD4052)		2	2.5	mW
	f_S = 2 MSPS (AD4052)		2.7	3.3	mW
Autonomous Modes	f_S = 10 kSPS		16		µW
	f_S = 300 kSPS (AD4058)		112	220	µW
	f_S = 1 MSPS (AD4052)		370		µW
	f_S = 2 MSPS (AD4052)		740	990	µW

1 Sampling rate specifies the maximum sample rate capabilities of the AD4052/AD4058 ADCs. Output data rate is the number of ADC samples that can be transmitted over the serial interface per second and is a function of the serial interface timing specifications. In sample mode and averaging mode, the serial interface bottlenecks the AD4052 output data rate to <2 MSPS. In burst averaging mode and autonomous modes, the output data rate requirements are reduced, and the AD4052 ADC core can operate at the full 2 MSPS. See the Calculating Serial Interface Output Data Rate section for guidelines for estimating AD4052/AD4058 SPI output data rate for each operating mode.

2 V_{IN+} and V_{IN-} represent the voltages on the IN+ and IN− pins, respectively. The AD4052/AD4058 sample and convert the difference between V_{IN+} and V_{IN-}.

3 See the Wide Input Common-Mode Range section for a detailed description of the AD4052/AD4058 common-mode input voltage range.

4 In the track phase, the total input capacitance is the sum of C_{IN} and the pin capacitance. In the hold phase, C_{IN} is disconnected from the inputs, and the input capacitance is only the pin capacitance. See Figure 38.

5 The minimum and maximum DNL specifications are guaranteed by design.

6 TUE is defined as the largest deviation from the ideal DC transfer function over the full input range for any individual device. TUE includes the combined effects of zero-error, gain error, and INL error for each device.

7 Autonomous mode TUE applies to the comparator operation. See the Comparator Operation and the Autonomous Modes sections.

8 The averaging REF input current scales linearly with f_S (see Figure 21).

9 VDD supply current and power dissipation scale linearly with sample rate (see the VDD Power Dissipation section, Figure 24, and Figure 27).

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TIMING SPECIFICATIONS

VDD = V_{REF} = 2.3 V to 3.6 V, VIO = 1.71 V to 3.6 V, digital output load capacitance (C_{LOAD}) = 20 pF, and all other features in default configuration. Minimum and maximum limits at T_A = −40°C to +125°C and typical values at T_A = +25°C, unless otherwise indicated.

Table 2. ADC Timing Specifications

Parameter[1]	Symbol	Min	Typ	Max	Unit
Sampling Rate[2]	f_S				
AD4052				2	MSPS
AD4058				500	kSPS
Sample Period (Time Between Conversions)[2]	t_{CYC}				
AD4052		500			ns
AD4058		2000			ns
Conversion Time	t_{CONV}		270	320	ns
Acquisition Time[3, 4]	t_{ACQ}				
f_S = 2 MSPS		290	327		ns
f_S = 500 kSPS		1790	1827		ns
Quiet Time (Last SCLK Edge to CNV Rising Edge)	t_{QUIET}	15			ns
CNV High Time	t_{CNVH}	10			ns
CNV Low Time	t_{CNVL}	10			ns
Internal Timer Frequency[5]	f_{OSC}	−15%	f_{OSC}	+15%	ns

[1] The t_{CONV} specification is production tested. All other timing specifications in this table are guaranteed by characterization and design.

[2] Sampling rate specifies the maximum sample rate capabilities of the AD4052/AD4058 ADCs. Output data rate is the number of ADC samples that can be transmitted over the serial interface per second and is a function of the serial interface timing specifications. In sample mode and averaging mode, the serial interface bottlenecks the AD4052 output data rate to <2 MSPS. In burst averaging mode and autonomous modes, the output data rate requirements are reduced, and the AD4052 ADC core can operate at the full 2 MSPS. See the Calculating Serial Interface Output Data Rate section for guidelines for estimating AD4052/AD4058 SPI output data rate for each operating mode.

[3] The t_{ACQ} specification is the time available for the input sampling capacitors to acquire the input voltage for a given sample rate. The t_{ACQ} specification is equivalent to the time the ADC spends in the track phase. The t_{ACQ} specification is inversely proportional to sample rate. Therefore, the t_{ACQ} specification increases as the sample rate decreases. The minimum t_{ACQ} specification for any given sample period rate is given by the following equation: $t_{ACQ} = t_{CYC} - 210$ ns.

[4] See the Device Enable Signal section for a description of acquisition time while using the DEV_EN signal to power cycle the analog front end.

[5] The internal timer sets the sampling frequency in burst averaging mode and autonomous modes. The AD4052/AD4058 is guaranteed to operate at the maximum f_{OSC} specification. See Table 44 for the nominal sampling frequency options.

Table 3. SPI Timing—Configuration Mode, VIO ≥ 3.0 V

Parameter[1]	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Falling Edge to SDO Valid	t_{EN}			10	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			10	ns
SCLK Period	t_{SCLK}	40			ns
SCLK Low Time	t_{SCLKL}	15			ns
SCLK High Time	t_{SCLKH}	15			ns
SDI Valid Setup Time Prior to SCLK Rising Edge (SDI Setup Time)	t_{SSDI}	4			ns
SDI Valid Hold Time After SCLK Rising Edge (SDI Hold Time)	t_{HSDI}	2			ns
SCLK Falling Edge to Data Remains Valid (SDO Hold Time)	t_{HSDO}	2			ns
SCLK Falling Edge to Data Valid (SDO Valid Delay)	t_{DSDO}			11	ns
Operating Mode Update Delay	t_{MODE}	40			ns
Reset Delay	t_{RESET}		5		ms

[1] The t_{SCLK}, t_{SCLKL}, and t_{SCLKH} specifications are production tested. All other timing specifications in this table are guaranteed by characterization and design.

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SPECIFICATIONS

Table 4. SPI Timing—Configuration Mode, VIO ≥ 1.71 V

Parameter[1]	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ High Time	t_{CSH}	15			ns
$\overline{CS}$ Falling Edge to SDO Valid	t_{EN}			20	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			20	ns
SCLK Period	t_{SCLK}	62.5			ns
SCLK Low Time	t_{SCLKL}	25			ns
SCLK High Time	t_{SCLKH}	25			ns
SDI Valid Setup Time Prior to SCLK Rising Edge (SDI Setup Time)	t_{SSDI}	10			ns
SDI Valid Hold Time After SCLK Rising Edge (SDI Hold Time)	t_{HSDI}	4			ns
SCLK Falling Edge to Data Remains Valid (SDO Hold Time)	t_{HSDO}	2			ns
SCLK Falling Edge to Data Valid (SDO Valid Delay)	t_{DSDO}			22	ns
Operating Mode Update Delay	t_{MODE}	62.5			ns
Reset Delay	t_{RESET}		5		ms

1 The t_{SCLK}, t_{SCLKL}, and t_{SCLKH} specifications are production tested. All other timing specifications in this table are guaranteed by characterization and design.

Table 5. SPI Timing—ADC Modes, VIO ≥ 3.0 V

Parameter[1]	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Falling Edge to SDO Valid	t_{EN}			8	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			8	ns
SCLK Period	t_{SCLK}	12			ns
SCLK Low Time	t_{SCLKL}	5.4			ns
SCLK High Time	t_{SCLKH}	5.4			ns
SDI Valid Setup Time Prior to SCLK Rising Edge (SDI Setup Time)	t_{SSDI}	4			ns
SDI Valid Hold Time After SCLK Rising Edge (SDI Hold Time)	t_{HSDI}	2			ns
SCLK Falling Edge to Data Remains Valid (SDO Hold Time)	t_{HSDO}	1.5			ns
SCLK Falling Edge to Data Valid (SDO Valid Delay)	t_{DSDO}			8	ns
Exit Command to Register Access Delay	t_{CONFIG}			8	ns
Reset Delay	t_{RESET}		5		ms

1 The t_{SCLK}, t_{SCLKL}, and t_{SCLKH} specifications are production tested. All other timing specifications in this table are guaranteed by characterization and design.

Table 6. SPI Timing—ADC Modes, VIO ≥ 1.71 V

Parameter[1]	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Falling Edge to SDO Valid	t_{EN}			15	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			15	ns
SCLK Period	t_{SCLK}	17			ns
SCLK Low Time	t_{SCLKL}	7.5			ns
SCLK High Time	t_{SCLKH}	7.5			ns
SDI Valid Setup Time Prior to SCLK Rising Edge (SDI Setup Time)	t_{SSDI}	5			ns
SDI Valid Hold Time After SCLK Rising Edge (SDI Hold Time)	t_{HSDI}	4			ns
SCLK Falling Edge to Data Remains Valid (SDO Hold Time)	t_{HSDO}	1.5			ns
SCLK Falling Edge to Data Valid (SDO Valid Delay)	t_{DSDO}			15	ns
Exit Command to Register Access Delay	t_{CONFIG}			15	ns
Reset Delay	t_{RESET}		5		ms

1 The t_{SCLK} specification is production tested. All other timing specifications in this table are guaranteed by characterization and design.

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SPECIFICATIONS

Timing Diagrams

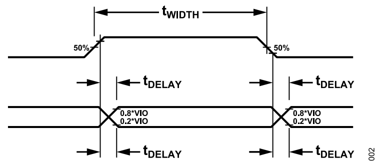

Figure 2. Voltage Levels for Timing Specifications

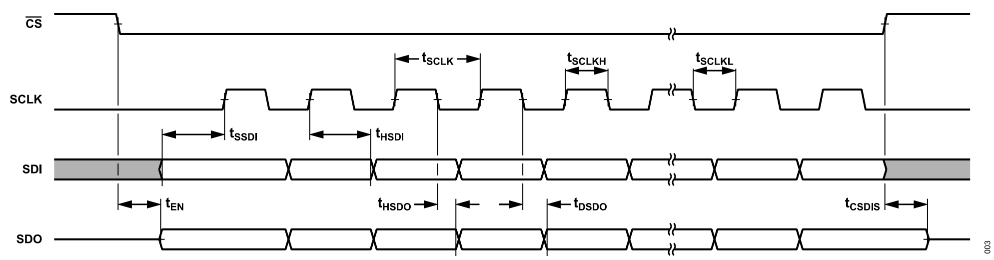

Figure 3. SPI Timing Specifications Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
IN+, IN−, REF to GND	−0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +3.96 V
CLDO to GND	−0.3 V to +2.1 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Temperature	
Storage	−55°C to +150°C
Operating T_J Range	−40°C to +125°C
Maximum Reflow (Package Body)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Unit
CP-14-7	73.9	52.3	°C/W
CB-16-26	49.6	0.6	°C/W

[1] Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB.

[2] θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

[3] θ_{JC} is the junction-to-case thermal resistance.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

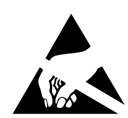
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4052/AD4058

Table 9. AD4052/AD4058, 14-Lead LFCSP and 16-Ball WLCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	4	3A
FICDM	1.25	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

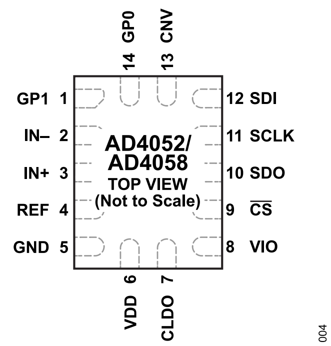

Figure 4. AD4052/AD4058 LFCSP Pin Configuration

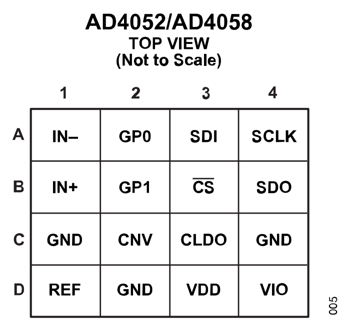

Figure 5. AD4052/AD4058 WLCSP Pin Configuration

Table 10. AD4052/AD4058 LFCSP and WLCSP Pin Function Descriptions

LFCSP Pin No.	WLCSP Pin No.	Mnemonic	Type	Description
1	B2	GP1	DO	General Purpose Output 1. The GP1 pin is a digital output that can be configured as multiple device interrupt signals. See the Interrupts and Control Signals section.
2	A1	IN−	AI	Negative Analog Input. See the Analog Inputs section.
3	B1	IN+	AI	Positive Analog Input. See the Analog Inputs section.
4	D1	REF	AI	Reference Input. Decouple the REF pin with a 2.2 μF capacitor to GND. See the Voltage Reference section.
5	C1, C4, D2	GND	P	Power Supply Ground.
6	D3	VDD	P	Analog Power Supply. Decouple the VDD pin with a 1 μF capacitor to GND. The VDD pin is also the input to the +1.8 V internal LDO regulator that supplies the CLDO pin supply voltage. See the Power Supplies section.
7	C3	CLDO	P	ADC Core Power Supply. The CLDO pin is powered by the +1.8 V internal LDO regulator. Decouple the CLDO pin with a 1 μF capacitor to GND. See the Power Supplies section.
8	D4	VIO	P	Logic Voltage Supply. The VIO pin sets the logic voltage levels for digital inputs and digital outputs. Decouple the VIO pin with a 1 μF capacitor to GND. See the Power Supplies section.
9	B3	$\overline{\text{CS}}$	DI	Chip Select Input (Active Low). See the Serial Interface section.
10	B4	SDO	DO	Serial Data Output. See the Serial Interface section.
11	A4	SCLK	DI	Serial Data Clock Input. See the Serial Interface section.
12	A3	SDI	DI	Serial Data Input. See the Serial Interface section.
13	C2	CNV	DI	Convert Input. In sample mode, averaging mode, and burst averaging mode, a rising edge on the CNV pin initiates a conversion. The CNV pin can optionally be connected to $\overline{\text{CS}}$. See the Serial Interface section.
14	A2	GP0	DO	General Purpose Output 0. The GP0 pin is a digital output that can be configured as multiple device control or interrupt signals. See the Interrupts and Control Signals section.

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TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 3.3 V, V_{REF} = 3.3 V, VIO = 3.3 V, C_{REF} = 2.2 µF, maximum f_S, T_A = 25°C, and all features in default configuration, unless otherwise specified.

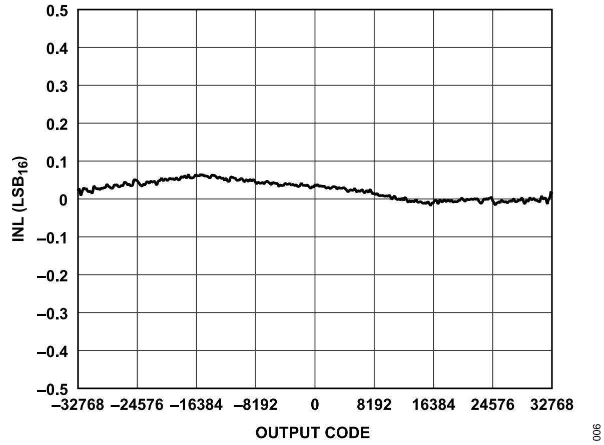

Figure 6. INL vs. Output Code

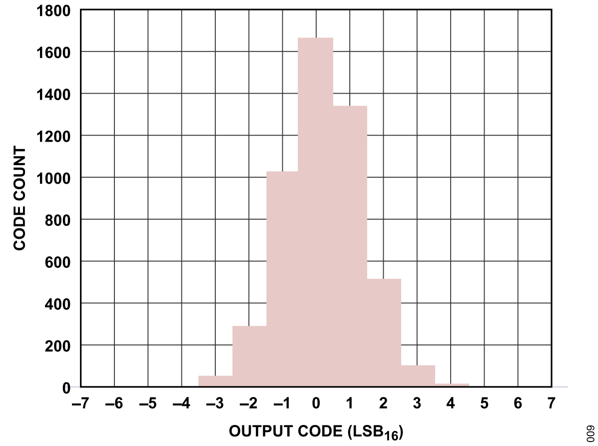

Figure 9. Histogram, Sample Mode (No Averaging)

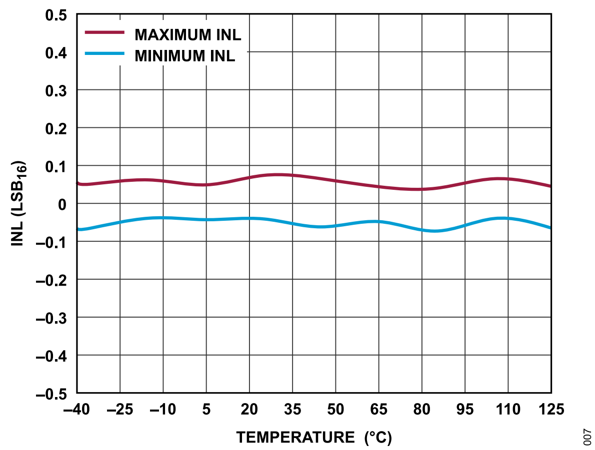

Figure 7. INL vs. Temperature

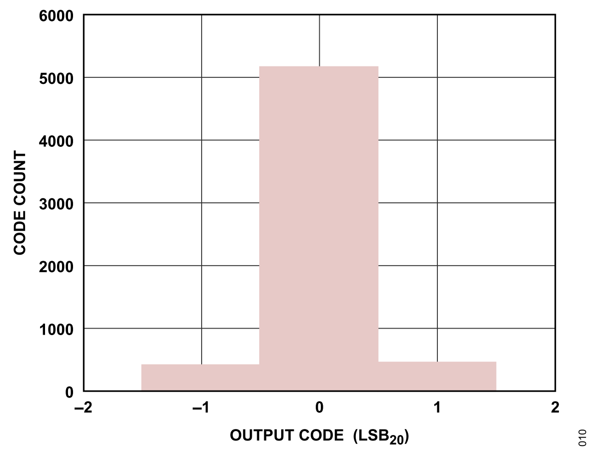

Figure 10. Histogram, Averaging Mode, N_{AVG} = 4096

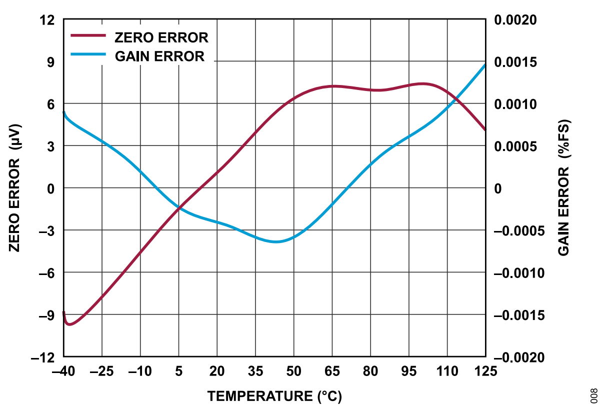

Figure 8. Zero Error and Gain Error vs. Temperature

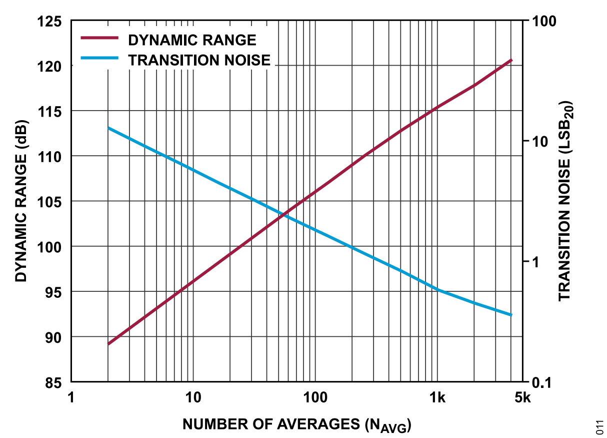

Figure 11. Dynamic Range and Transition Noise vs. N_{AVG}

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TYPICAL PERFORMANCE CHARACTERISTICS

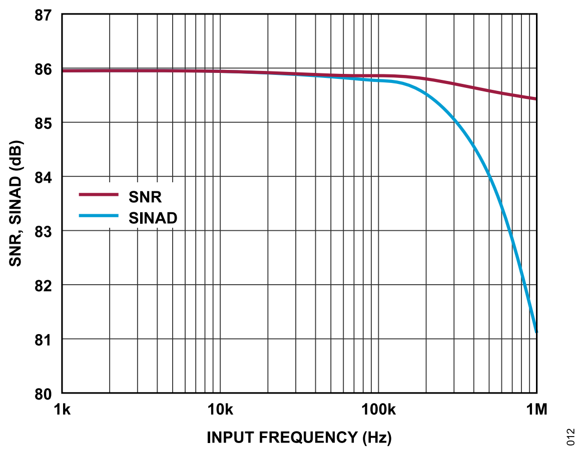

Figure 12. SNR, SINAD vs. Input Frequency

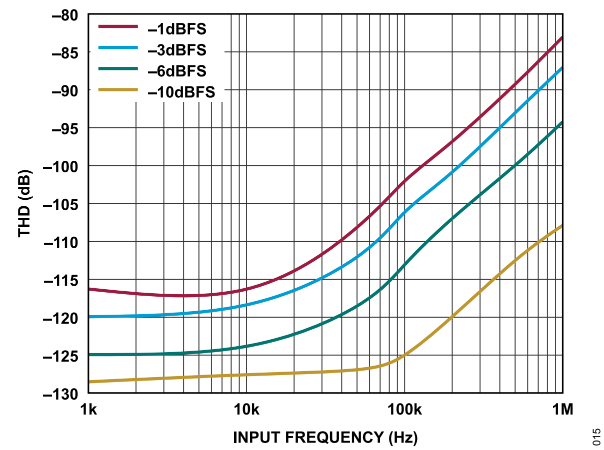

Figure 15. THD vs. Input Frequency and Amplitude

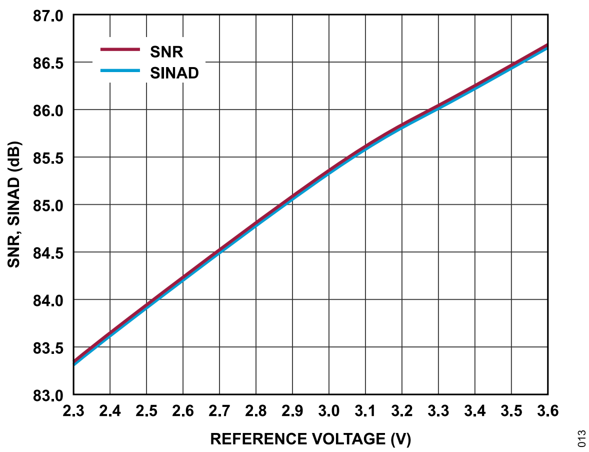

Figure 13. SNR, SINAD vs. Reference Voltage

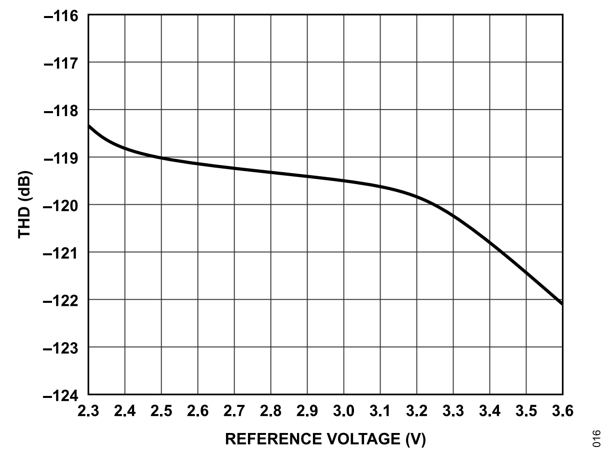

Figure 16. THD vs. Reference Voltage

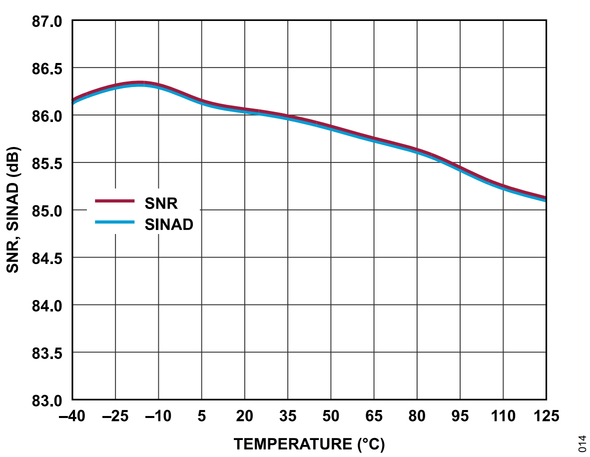

Figure 14. SNR, SINAD vs. Temperature

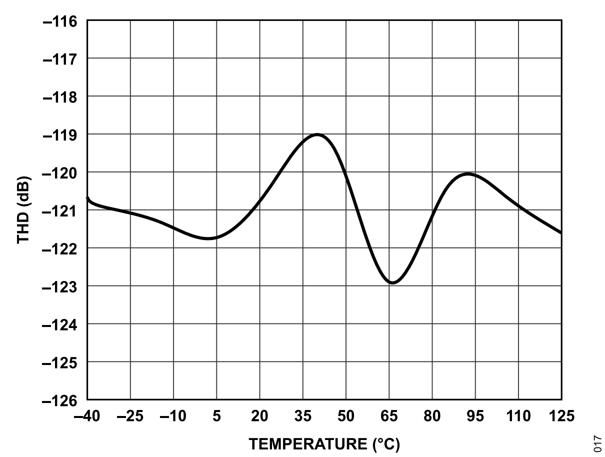

Figure 17. THD vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

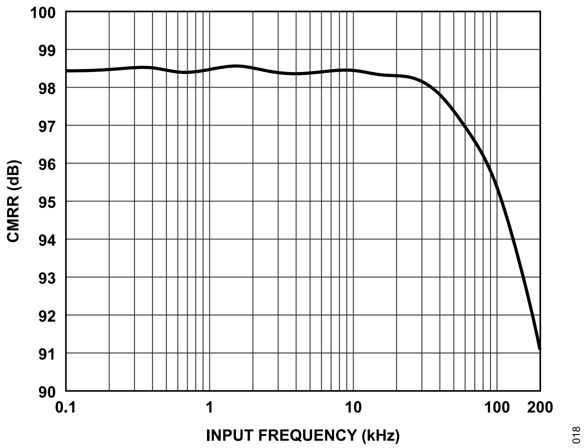

Figure 18. Common-Mode Rejection Ratio (CMRR) vs. Input Frequency

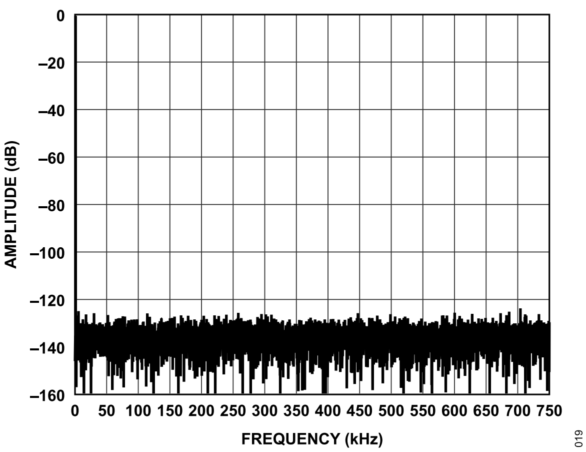

Figure 19. FFT, f_S = 1.5 MSPS, f_{IN} = 1 kHz

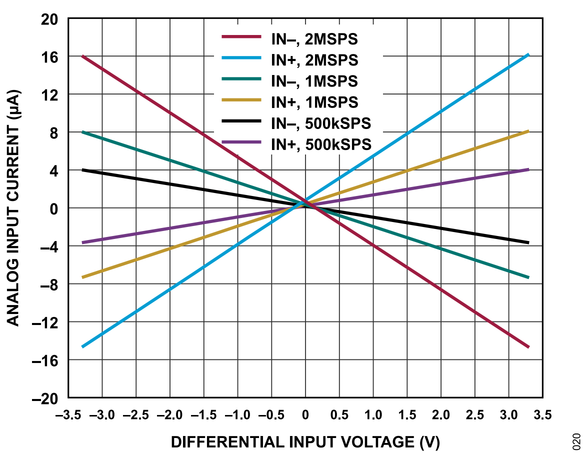

Figure 20. Analog Input Current vs. Differential Input Voltage

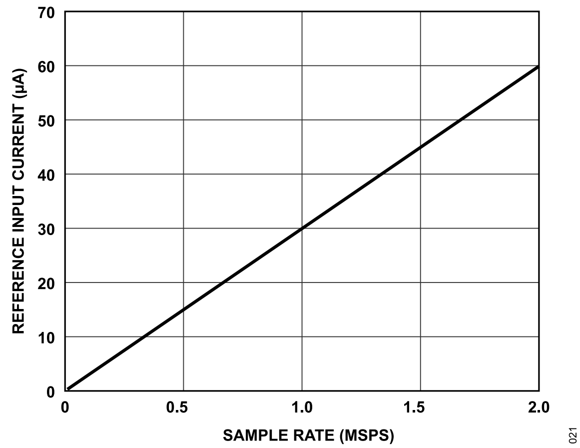

Figure 21. Reference Input Current vs. Sample Rate

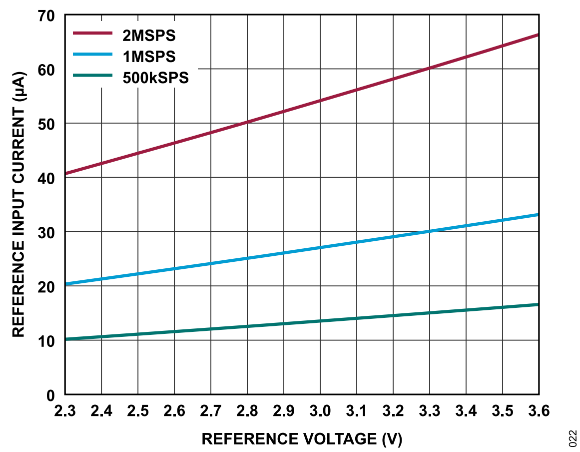

Figure 22. Reference Input Current vs. Reference Voltage

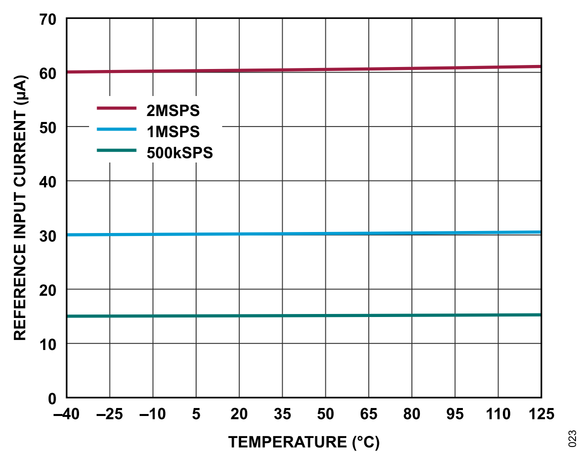

Figure 23. Reference Input Current vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

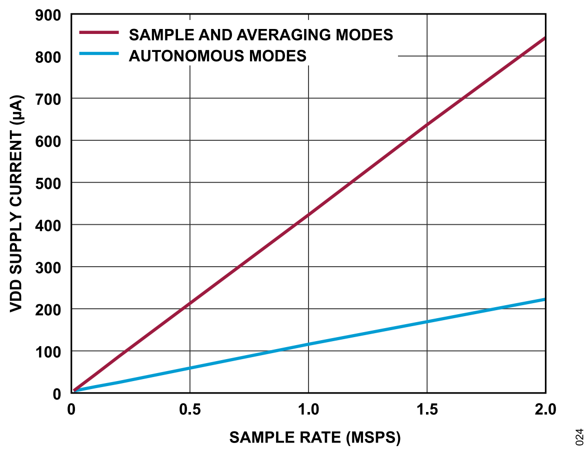

Figure 24. VDD Supply Current vs. Sample Rate

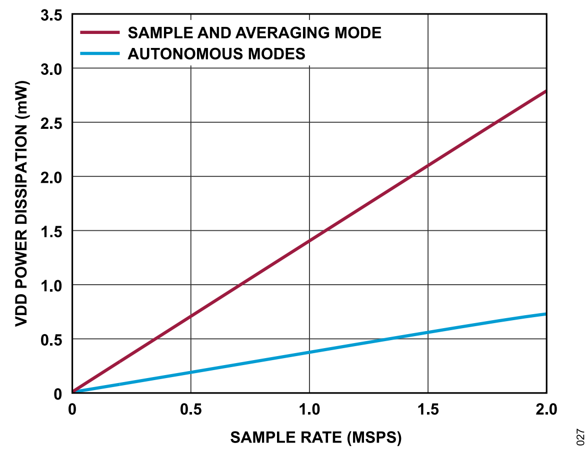

Figure 27. VDD Power Dissipation vs. Sample Rate

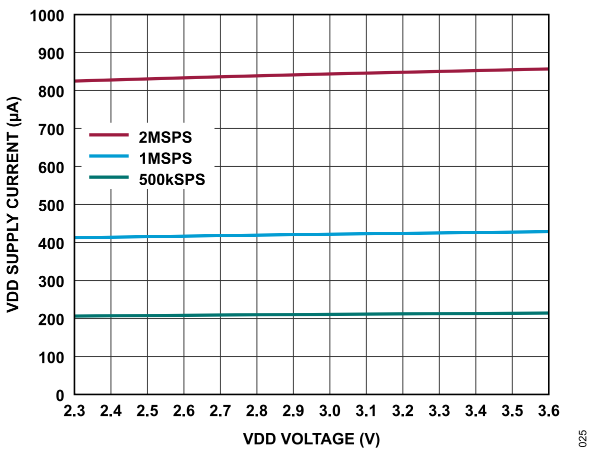

Figure 25. VDD Supply Current vs. VDD Voltage

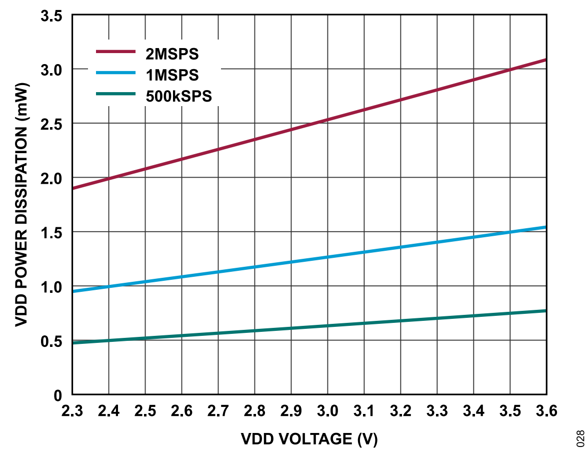

Figure 28. VDD Power Dissipation vs. VDD Voltage

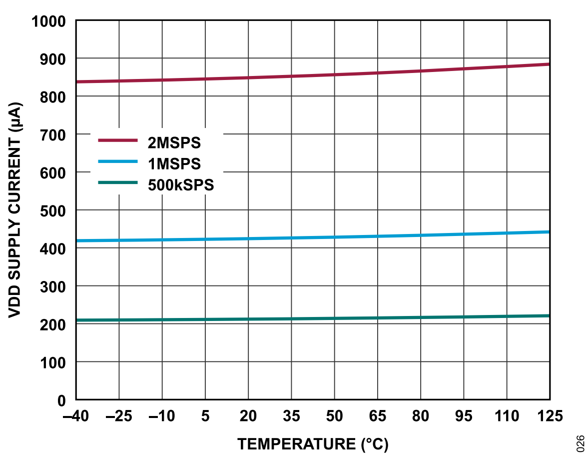

Figure 26. VDD Supply Current vs. Temperature

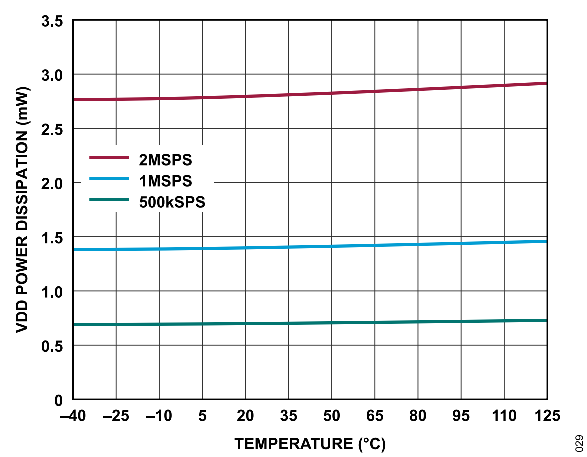

Figure 29. VDD Power Dissipation vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

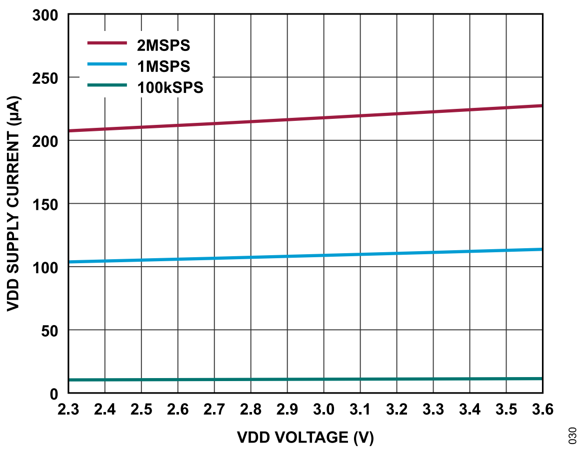

Figure 30. VDD Supply Current vs. VDD Voltage (Autonomous Modes)

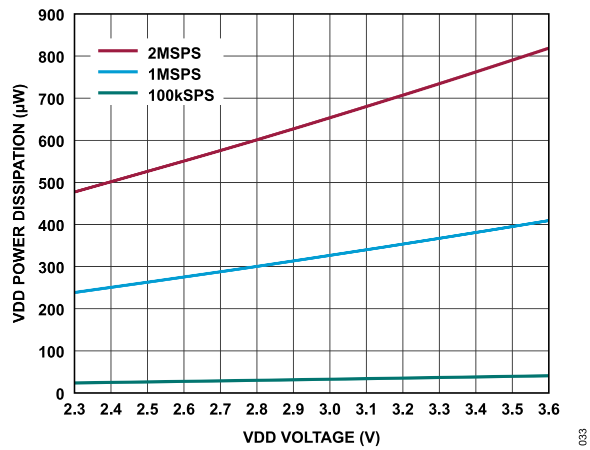

Figure 33. VDD Power Dissipation vs. VDD Voltage (Autonomous Modes)

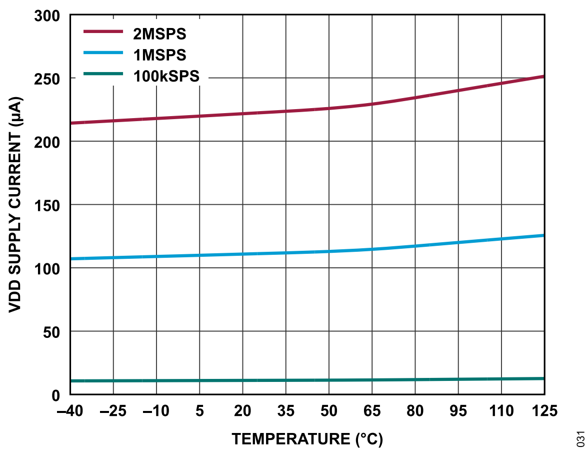

Figure 31. VDD Supply Current vs. Temperature (Autonomous Modes)

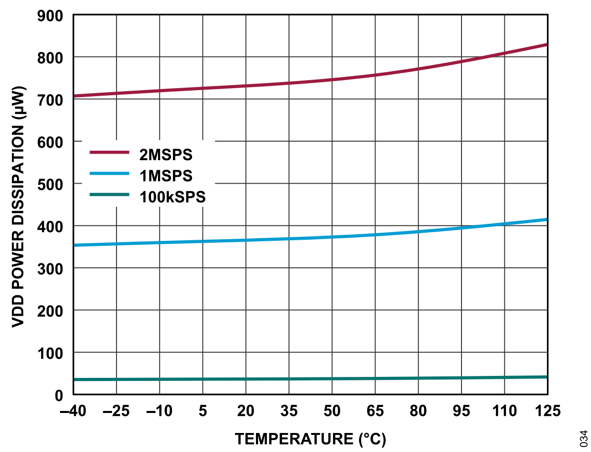

Figure 34. VDD Power Dissipation vs. Temperature (Autonomous Modes)

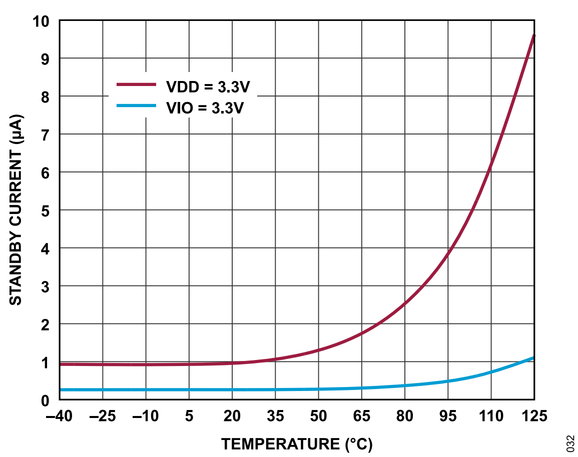

Figure 32. Standby Current vs. Temperature

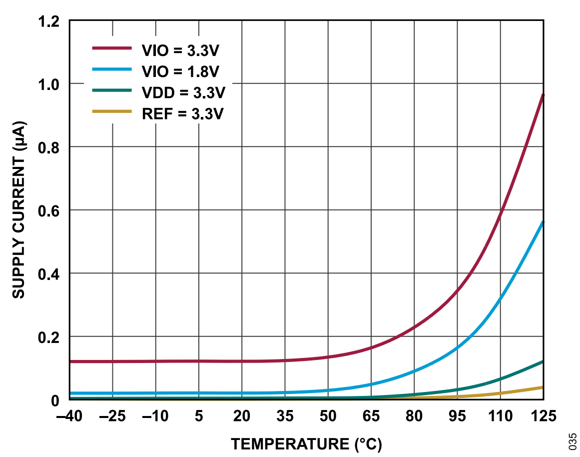

Figure 35. Supply Current (Sleep Mode) vs. Temperature

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TERMINOLOGY

Integral Nonlinearity (INL) Error

INL is the deviation of each individual code from a line drawn from the negative full scale through the positive full scale. The point used as the negative full scale occurs ½ LSB before the first code transition. The positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from each code center to the true straight line.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error (ZE)

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Gain Error (GE)

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above the nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Total Unadjusted Error (TUE)

TUE is the worst-case measured deviation from the ideal ADC transfer function over the full input range, specified in ppm of full-scale. TUE includes the combined effects of zero error, gain error, and INL error for any given device.

Dynamic Range (DR)

Dynamic range is the RMS voltage of a full-scale sine wave to the total RMS voltage of the noise measured. The value for dynamic range is expressed in decibels. Dynamic range is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the RMS amplitude of a full-scale input signal and the peak spurious signal.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS voltage of a full-scale sine wave to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonic components to the RMS value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the RMS voltage of a full-scale sine wave to the RMS sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value of SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD as follows:

ENOB = (SINAD dB − 1.76)/6.02.

ENOB is expressed in bits.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a −1 dBFS sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR(dB) = 10 \times \log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:

P_{ADC_IN} is the common-mode power at the frequency, f, applied to the inputs.

P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

Aperture Delay

Aperture delay is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

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THEORY OF OPERATION

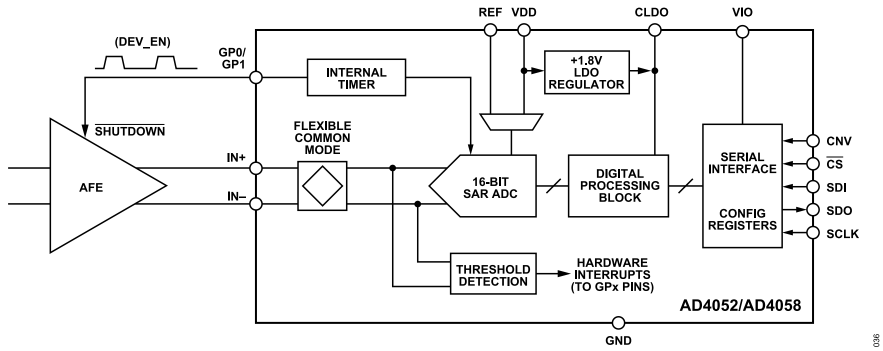

Figure 36. AD4052/AD4058 Functional Block Diagram

OVERVIEW

The AD4052/AD4058 are compact, ultra-low power, 16-bit, Easy Drive SAR ADCs. The AD4052/AD4058 feature set eases the design of low-power precision measurement systems by reducing the AFE design constraints and minimizing the digital host overhead. The low input capacitance and wide common-mode input range broaden the selection of compatible AFE components, allowing for simpler and lower power signal chain solutions. The block averaging filter provides noise reduction while offloading computations from the host processor. The internal timer block enables autonomous monitoring modes, burst sampling, and device power cycling controls synchronized to the ADC sampling instant. The CHOP signal can be used as the control signal for an auto-zero amplifier that employs chopping in applications that require very low 1/f noise and offset error. Various hardware interrupts allow the digital host to sleep between user-defined events.

The AD4052/AD4058 offer a unique balance of performance and power efficiency, with 86.1 dB of SNR and guaranteed INL of ±0.5 LSBs at only 1.35 nJ per conversion. The AD4052 only consumes 2.7 mW at 2 MSPS and the AD4058 only consumes 0.68 mW at 500 kSPS when operated on a single 3.3 V supply. The power dissipation scales linearly with sample rate for both the AD4052 and the AD4058 (see Figure 27). The devices consume 4.1 μW standby power while not performing conversions. A sleep mode is available to further reduce standby power to 430 nW during long periods of idle operation.

The AD4052/AD4058 feature 4-wire SPI with CRC for device configuration and ADC data readback, and the SPI is compatible with 1.8 V to 3.3 V logic levels.

The AD4052/AD4058 have several operating modes, each optimized for either high precision measurement or power-efficient signal monitoring. The Theory of Operation section describes the AD4052/AD4058 functional blocks, and the Modes of Operation section describes the utilization of the functional blocks in each operating mode. The Serial Interface section describes the SPI protocols for accessing configuration registers and ADC data. The Register Summary section documents the configuration registers.

CONVERTER OPERATION

The AD4052/AD4058 operate in two phases, the acquisition phase and the conversion phase. In the acquisition phase, the internal track-and-hold circuitry is connected to each input pin (IN+ and IN−) and acquires the voltage on each pin independently. The AD4052/AD4058 remain in the acquisition phase until the convert start trigger occurs to initiate a conversion. At the start of the conversion phase, the track-and-hold circuitry samples the acquired analog input signal, and the SAR ADC core generates a corresponding 16-bit digital code. The conversion phase ends when the 16-bit conversion result is ready, which is given by the t_{CONV} specification in Table 2. The AD4052/AD4058 acquisition and conversion phases overlap to maximize acquisition time (t_{ACQ}).

In sample mode and averaging mode, the conversion phase is started by a rising edge on the CNV pin. The AD4052/AD4058 offer several modes where the convert start is triggered by an internal oscillator instead, including the autonomous modes. Refer to the Modes of Operation section for specific ADC timing information for each of the relevant operating modes.

Transfer Function

Figure 37 shows the ideal transfer function of the AD4052/AD4058 SAR ADC cores. The AD4052/AD4058 encode the sampled voltage difference between IN+ and IN− as a fraction of the full-scale range (FSR) into a 16-bit digital code. The unit of 1 LSB refers to the smallest discrete voltage step that can be resolved by the ADC and is a function of the V_{REF} voltage. In averaging and burst averaging modes, the block averaging filter averages multiple 16-bit samples into one 20-bit code. Table 11 and Table 12 summarize the mapping of input voltages to digital output codes.

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THEORY OF OPERATION

The AD4052/AD4058 serial interface outputs the ADC data into multiples of bytes to maximize compatibility with microcontroller direct memory access (DMA) controllers. The ADC Mode Output Data Format section describes the serial interface data packet format for each of the AD4052/AD4058 operating modes.

As described in the Wide Input Common-Mode Range section, the AD4052/AD4058 support arbitrary input common-mode voltages, therefore the devices inherently support both differential and single-ended type signals. The AD4052/AD4058 support both twos complement (signed) and straight binary (unsigned) formats to map either differential signals or single-ended signals to the full 16-bit ADC transfer function. The DATA_FORMAT bit in the ADC_MODES register selects between the differential mode and single-ended mode transfer functions as seen in Table 11 and Table 12.

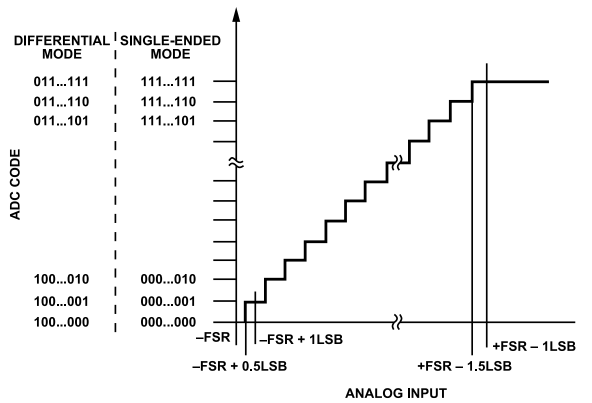

Figure 37. ADC Ideal Transfer Function

Table 11. ADC Input Voltage to Output Code Mapping (Sample Mode)

	Differential Mode		Single-Ended Mode	
Description	V_{IN}	**Digital Output Code**	V_{IN}	**Digital Output Code**
FSR − 1 LSB	(32767/32768) × V_{REF}	0x7FFF	(65535/65536) × V_{REF}	0xFFFF
...	...	...	...	...
Midscale + 1 LSB	(1/32768) × V_{REF}	0x0001	(32769/65536) × V_{REF}	0x8001
Midscale	0 V	0x0000	(½) × V_{REF}	0x8000
Midscale − 1 LSB	−(1/32768) × V_{REF}	0xFFFF	(32767/65536) × V_{REF}	0x7FFF
...	...	...	...	...
−FSR + 1 LSB	(−32767/32768) × V_{REF}	0x8001	(1/65536) × V_{REF}	0x0001
−FSR	$-V_{REF}$	0x8000	0 V	0x0000

Table 12. ADC Input Voltage to Output Code Mapping (Averaging and Burst Averaging Modes)

	Differential Mode		Single-Ended Mode	
Description	V_{IN}	**Digital Output Code**	V_{IN}	**Digital Output Code**
FSR − 1 LSB	(524287/524288) × V_{REF}	0x7FFFF	(1048575/1048576) × V_{REF}	0xFFFFF
...	...		...	...
Midscale + 1 LSB	(1/524288) × V_{REF}	0x00001	(524289/1048576) (8193/16384) × V_{REF}	0x80001
Midscale	0 V	0x00000	(½) × V_{REF}	0x80000
Midscale − 1 LSB	(−1/524288) (−1/8192) × V_{REF}	0xFFFFF	(524287/1048576) × V_{REF}	0x7FFFF
...	...	...	...	...
−FSR + 1 LSB	(−524287/524288) × V_{REF}	0x80001	(1/1048576) × V_{REF}	0x00001
−FSR	$-V_{REF}$	0x80000	0 V	0x00000

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THEORY OF OPERATION

ANALOG INPUTS

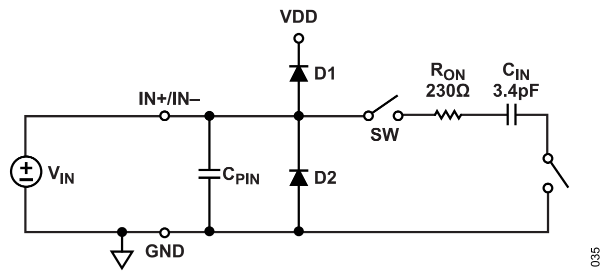

Figure 38. Equivalent Analog Input Circuit

Figure 38 shows an equivalent circuit for each of the AD4052/AD4058 analog inputs (IN+ and IN−). The analog inputs are modeled as a switched capacitive load. During the acquisition phase, the sampling switch (SW) connects each input pin to the 3.4 pF sampling capacitor (C_{IN}) in series with the 230 Ω switch on resistance (R_{ON}). During the conversion phase, SW disconnects to sample the voltages on the IN+ and IN− pins onto the sampling capacitors. D1 and D2 represent the ESD diodes from the IN+ and IN− pins to the VDD supply and GND, respectively. C_{PIN} represents the pin capacitance of each input pin to GND and is typically 2 pF.

See the AD4052/AD4058 Equivalent Analog Input Model section for more information on the effective loading characteristics of the AD4052/AD4058 analog inputs.

Easy Drive Features

The AD4052/AD4058 Easy Drive analog inputs are designed to enable compact, low-power precision signal chains by minimizing dependence on specialized high-speed, low-noise, high-power ADC driver amplifiers. The small sampling capacitors minimize the transient current glitches typical of SAR ADCs, and the long acquisition phase maximizes the settling time—even at high sample rates. The RC kickback filter uses smaller capacitors and larger resistors, alleviating amplifier stability concerns and enabling the use of tiny passive components (for example, 0201 NP0/C0G capacitors). These Easy Drive features ensure the AD4052/AD4058 interface with front-end circuits with high output impedance without incurring settling errors, expanding compatibility with low-power amplifiers and sensors (see the Analog Front-End Design section).

The AD4052/AD4058 are available in the LTspice component library and support cosimulation with a wide variety of companion amplifiers. The LTspice model emulates the input-referred noise spectral density and input transient loading for system noise and settling accuracy simulations.

VOLTAGE REFERENCE

The V_{REF} voltage sets the ADC FSR (see the Transfer Function section). The AD4052/AD4058 V_{REF} range is 2.3 V to VDD, where the maximum VDD supply voltage is 3.6 V (see Table 1).

The V_{REF} voltage is polled during the SAR bit trials to determine the ADC output code. During the bit trials, the SAR core exhibits transient charge draw. To ensure the V_{REF} voltage remains stable during the SAR bit trials, place a 2.2 µF decoupling capacitor as close to the REF pin as possible. Lower decoupling capacitance values (for example, 1 µF) may be used with slight performance degradations. See the Reference Circuit Design section for more recommendations for pairing voltage references with the AD4052/AD4058.

Reference Selection Modes

The AD4052/AD4058 V_{REF} voltage can be sourced from either the REF input pin or the VDD supply pin. By default, the REF pin acts as the V_{REF} source, and this setting is the intended mode to achieve the performance specifications given in Table 1. The VDD supply option is provided to support low-power measurements where accuracy is not critical or to allow the system to power cycle the voltage reference for long periods of time to save system power. The V_{REF} source option is controlled with the REF_SEL bit in the ADC_CONFIG register (see Table 39).

The AD4052/AD4058 include an automated gain scaling function, where the ADC core samples the REF voltage as a fraction of the VDD supply voltage and stores the appropriate gain scaling value into the MON_VAL register, such that using VDD as the V_{REF} source has the same ADC transfer function as REF. This allows the system to power down the voltage reference circuitry for extended periods of time with similar levels of performance. See the Achieving High Accuracy with Reference Shutdown section for a detailed description of the automated gain scaling feature.

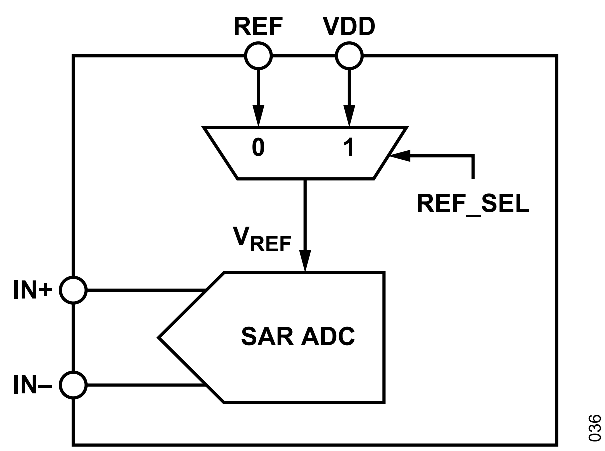

Figure 39. Reference Source Selection

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THEORY OF OPERATION

DIGITAL PROCESSING FEATURES

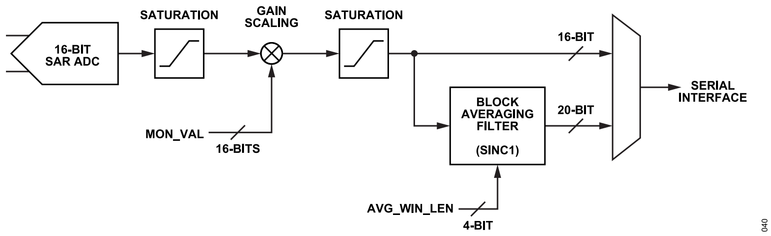

Figure 40. AD4052/AD4058 Digital Processing Functionality

The AD4052/AD4058 include several data processing features that can be applied to ADC data to offload computations from the digital host processor. Figure 40 shows a block diagram of the available data processing functions. Functionality and configuration of each block is described in detail in following sections. Note that these digital processing functions are not used in the autonomous modes.

Gain Scaling

The gain scaling function applies a 16-bit unsigned digital gain factor to the 16-bit ADC results. Gain scaling can be applied to calibrate out system gain error. The gain scaling factor is set by the MON_VAL bit field in the MON_VAL scaling register with the following equation:

$$Code_{OUT} = Code_{IN} \times \left({}^{MON\_VAL}\!/_{0x8000}\right) \quad (1)$$

where 0x0000 ≤ MON_VAL ≤ 0xFFFF, giving an effective gain range of 0 to 1.99997.

Gain scaling can also be used to scale the ADC transfer function when using the VDD supply as the V_{REF} source (see the Reference Selection Modes section). The AD4052/AD4058 can be configured to measure the ratio of the VDD supply and the REF input voltage and automatically adjust the MON_VAL register value to set the transfer functions to be the same. The external voltage reference circuitry can then be powered down to reduce system power dissipation. See the Achieving High Accuracy with Reference Shutdown section for more information.

Note that applying gain to the samples can cause numerical saturation when $Code_{OUT}$ in Equation 1 exceeds the 16-bit full scale (see the Full-Scale Saturation section). Ensure the MON_VAL bit field is set accordingly to prevent the gain scaling block output from saturating.

Gain scaling is disabled by default and enabled by setting the SCALE_EN bit field in the ADC_CONFIG register to 1 (see Table 39).

Full-Scale Saturation

The conversion results saturate digitally (prior to any data processing) when the sampled analog input voltage exceeds the input range limits specified in Table 1. The AD4052/AD4058 include saturation blocks at the output of the ADC core and the output of the gain scaling block that detect when the digital output codes or the ADC core and gain scaling block reach the maximum or minimum values, respectively.

The OVER_RNG_ERR and UNDER_RNG_ERR flags in the DEVICE_STATUS register are set when either of the saturation blocks detect a maximally or minimally saturated code. In differential mode, the 16-bit results saturate maximally at 0x7FFF and minimally at 0x8000. In single-ended mode the 16-bit results saturate maximally at 0xFFFF and minimally at 0x0000. (See the Transfer Function section for a description of differential and single-ended modes.)

The OVER_RNG_ERR and UNDER_RNG_ERR flags can be periodically polled when using the block averaging filter to verify none of the filter input data has saturated. The OVER_RNG_ERR and UNDER_RANGE_ERR flags are write-1-to-clear bits, and therefore, hold their states until the digital host is able to poll them.

Block Averaging Filter

The AD4052/AD4058 include a block averaging filter with programmable averaging ratios (N_{AVG}) from 2 to 4096. The block averaging filter is automatically enabled when the device is in averaging mode or burst averaging mode. The block averaging filter exhibits a SINC1 frequency response. Figure 41 shows the frequency response of the averaging filter for N_{AVG} of 2, 4, 8, 16, and 32.

When enabled, the block averaging filter accumulates a block of 16-bit ADC results before generating a 20-bit averaged result. N_{AVG} refers to the number of ADC samples per averaged result. The block averaging filter is reset (cleared) after processing each block of N_{AVG} samples. The N_{AVG} configuration is set by the AVG_WIN_LEN bit field in the AVG_CONFIG register (see Table 40) using the following equation:

$$N_{AVG} = 2^{AVG\_WIN\_LEN\, +\, 1} \quad (2)$$

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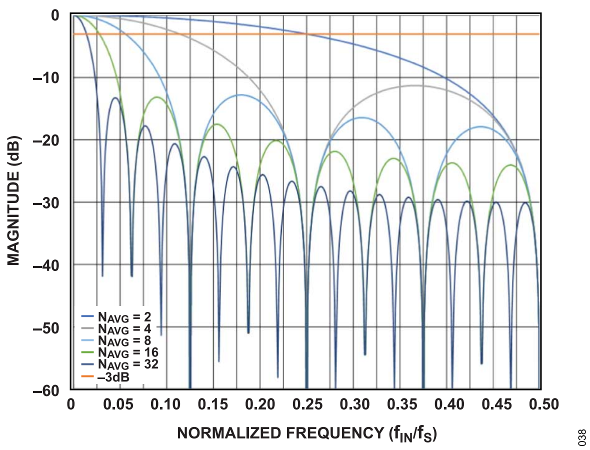

Figure 41. Frequency Response Examples for the Block Averaging Filter

INTERNAL TIMER

The AD4052/AD4058 include an internal timer to generate the ADC sampling clock in burst averaging mode and autonomous modes. The sampling frequency in these modes is set by the FS_BURST_AUTO bit field in the TIMER_CONFIG register and ranges from 2 MSPS to 111 SPS. See Table 44 in the Register Details section for the full set of nominal sampling clock frequencies (f_{OSC}) offered on the AD4052/AD4058. The actual sampling frequency in these modes is guaranteed to be within ±15% of f_{OSC} (see Table 2). Note that the 2 MSPS and 1 MSPS settings are invalid for the AD4058. On the AD4058, the FS_BURST_AUTO register must be updated accordingly before entering the burst averaging mode or the autonomous modes.

The internal timer also controls the DEV_EN signal delay (see the Device Enable Signal section). The t_{PWR_ON} delay is set by the TIMER_PWR_ON bit field, which is also in the TIMER_CONFIG register. The t_{PWR_ON} settings range from 0.5 μs to 9000 μs. See Table 44 in the Register Details section for the full set of nominal t_{PWR_ON} delay options.

POWER SUPPLIES

The AD4052/AD4058 have the following three power domains, the ranges for which are given in Table 1:

- VDD is the analog supply rail.
- CLDO is the +1.8 V ADC core supply rail, generated by an internal +1.8 V LDO regulator.
- VIO is the digital interface logic supply rail.

The VDD and VIO supplies must be supplied externally. The CLDO supply is generated internally by an internal +1.8 V LDO regulator sourced by the VDD rail. The VDD supply current is a function of the ADC sampling rate, because it supplies the internal LDO regulator that then supplies the SAR ADC core (see the VDD Power Dissipation section). In sleep mode, the internal LDO regulator is powered down to reduce the VDD standby current to 10 nA (see Table 1 and the Sleep Mode section).

The AD4052/AD4058 have no power supply sequencing requirements. The minimum allowable rise time for the VDD and VIO supplies is 100 μs. It is recommended to perform a device reset after the VDD and VIO supplies are stable (see the Power-On Reset section).

It is recommended to decouple the VDD, CLDO, and VIO pins to GND each with a 1 μF capacitor. When selecting VDD as the V_{REF} source (as described in the Reference Selection Modes section), or when driving the VDD and REF pins with a common external source, it is recommended to decouple VDD and REF with a shared 2.2 μF capacitor.

COMPARATOR OPERATION

The AD4052/AD4058 ADC cores offer a lower power, 12-bit window comparator mode for autonomous threshold detection and monitoring. Figure 42 shows a simplified schematic of the window comparator used in the autonomous modes.

The AD4052/AD4058 have two autonomous sampling modes, as described in the Autonomous Modes section. When either of the autonomous modes are enabled, the ADC enters comparator mode, and the internal timer acts as the sampling clock (see the Internal Timer section). The comparator steps through a sequence of comparisons against four user-programmable threshold regions on each sample and generates alert flags and hardware interrupts when the signal enters those regions.

Figure 43 illustrates the out-of-bounds regions set by the maximum and minimum threshold values. The maximum and minimum thresholds are user-programmable via the MAX_LIMIT and MIN_LIMIT bit fields. The MAX_LIMIT and MIN_LIMIT fields are each 12 bits wide for 12-bit comparator resolution. There are also independent hysteresis settings for maximum and minimum limits, set by the MAX_HYST and MIN_HYST fields, respectively, that define a second set of limits for autoclearing the alert signals. See the Autonomous Modes section for more information.

The data format of the MAX_LIMIT and MIN_LIMIT fields corresponds to the selected input range mode (as described in the Transfer Function section). The MAX_LIMIT and MIN_LIMIT fields are in twos complement in differential mode (DATA_FORMAT = 1'b1) and straight binary in single-ended mode (DATA_FORMAT = 1'b0). The MAX_HYST and MIN_HYST fields are always straight binary regardless of input mode setting.

The comparator includes two alert signals and two sticky alert bits in the register map. The MAX_INTR and MIN_INTR signals are the alert signals for maximum and minimum threshold events, respectively. The MAX_INTR and MIN_INTR signals may be routed to either or both of the GP0 and GP1 pins (see the Interrupts and Control Signals section). The MAX_FLAG and MIN_FLAG bits are sticky, write 1 to clear the bits in the DEVICE_STATUS register. The DEVICE_STATUS register also includes a threshold overrun bit (THRESH_OVERRUN) that is set whenever the comparator tries to

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set either the MAX_FLAG or MIN_FLAG bits before they have been cleared.

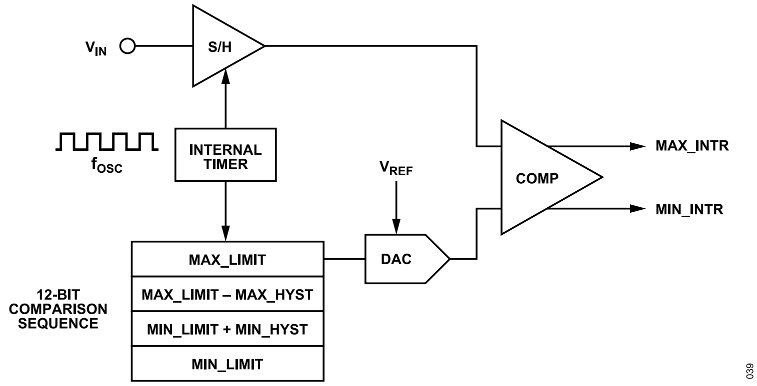

Figure 42. Simplified Schematic of Autonomous Mode Window Comparator

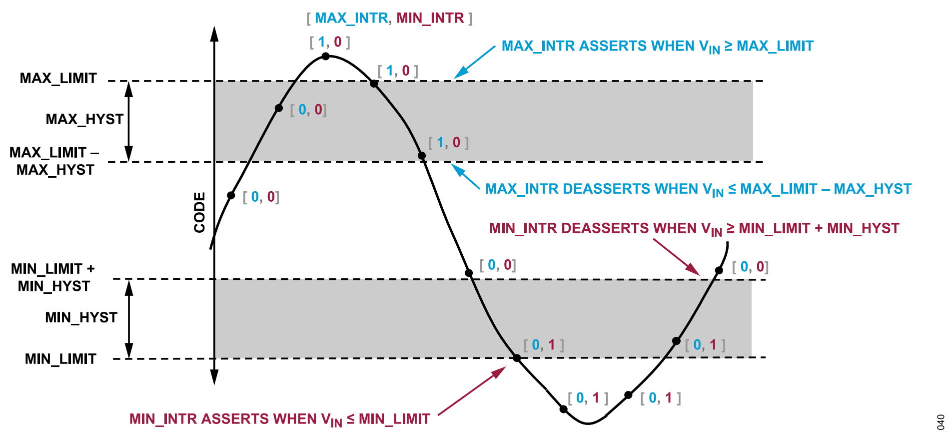

Figure 43. Threshold Event Regions

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INTERRUPTS AND CONTROL SIGNALS

The AD4052/AD4058 generate several digital signals for synchronizing the analog front-end and digital back-end processes to the ADC sampling. These signals can be assigned to the two general purpose pins (GP0 and GP1) via the GP0_MODE and GP1_MODE fields in the GP_CONFIG register, respectively. The following sections describe the functionality and timing details for each of the AD4052/AD4058 digital signals. Table 13 and Table 41 list the GPx signal assignments that correspond to each GPx_MODE bit field setting.

Table 13. GP0 and GP1 Signal Assignment Control

GPx_MODE Setting	GP0 Signal Assignment	GP1 Signal Assignment
3'h0	Disabled/high-Z (default)	Disabled/high-Z
3'h1	GP0_INTR	GP1_INTR
3'h2	$\overline{\text{RDY}}$	$\overline{\text{RDY}}$
3'h3	DEV_EN	DEV_EN
3'h4	CHOP	CHOP
3'h5	Logic low	Logic low
3'h6	Logic high	Logic high
3'h7	Invalid	DEV_RDY (default)

Static Logic Outputs

The AD4052/AD4058 GP0 and GP1 digital outputs can be set to a static logic low or logic high level. This function allows the digital host to control logic settings for external devices through the AD4052/AD4058 SPI and reduces the required number of GPIO resources. The logic output voltage specifications and corresponding load current conditions are given by V_{OL} and V_{OH} in Table 1.

Data Ready Signal

The data ready signal ($\overline{\text{RDY}}$) is an active-low interrupt signal that indicates when new ADC data are ready to read via the SPI. In sample mode, $\overline{\text{RDY}}$ goes high at the start of the conversion phase and returns low at the end of the conversion phase to indicate a new 16-bit result is available (see Figure 50). In averaging and burst averaging modes, $\overline{\text{RDY}}$ goes low after N_{AVG} conversions to indicate a new 20-bit averaged result is available (see Figure 52 and Figure 54).

Threshold Alert Signals

The comparator threshold alert signals MAX_INTR and MIN_INTR can be routed to the GP0 or GP1 pins via the GP0_INTR and GP1_INTR signals (see the Autonomous Modes section). Either of the GPx_INTR signals can be assigned to the MAX_INTR signal, the MIN_INTR signal, or the logical OR of both, giving the flexibility to either drive independent hardware interrupts for maximum and minimum crossings or to combine together for a single interrupt. By default, MAX_INTR is assigned to GP1_INTR and MIN_INTR is assigned to GP0_INTR.

The mapping of the alert signals to the GPx pins is controlled via the GP0_INTR_EN and GP1_INTR_EN bit fields in the INTR_CONFIG register (see Table 14 and Table 42).

Table 14. GPx_INTR Settings

GPx_INTR_EN Setting	GPx_INTR Signal Assignment
2'h0	Neither interrupt
2'h1	MIN_INTR
2'h2	MAX_INTR
2'h3	(MAX_INTR) OR (MIN_INTR)

Device Ready Signal

The device ready signal (DEV_RDY) is an active-high signal that indicates when the AD4052/AD4058 complete power-up or reset routines and are ready to accept serial interface communications. The DEV_RDY signal is routed to the GP1 pin after power-up or reset, so the digital host can monitor it to know when the AD4052/AD4058 are active. See the Device Reset section for timing diagrams of the DEV_RDY signal.

Device Enable Signal

The AD4052/AD4058 include a signal chain power-cycling control signal called DEV_EN. The DEV_EN signal synchronizes the enable and power-down states of signal chain devices (such as amplifiers, sensors, and voltage references) with the ADC sampling instant, optimizing system power consumption while minimizing sampling error from power-on delays. Figure 44 shows a typical application circuit utilizing the DEV_EN signal to power down an amplifier between samples.

When the DEV_EN signal is enabled, the internal timer acts as a one-shot timer triggered by the CNV rising edge. The timer delay (t_{PWR_ON}) controls how long the amplifier is powered on before the ADC sampling instant and is programmable to tailor to the connected device's specific power-on settling time specifications. Table 44 in the Register Details section shows the nominal t_{PWR_ON} settings available via the TIMER_PWR_ON bit field.

The DEV_EN signal is enabled by assigning it to either the GP0 or GP1 digital outputs (see Table 13). The DEV_EN signal can be configured as active high or active low via the DEV_EN_POL bit field in the GP_CONFIG register (see Table 41). DEV_EN is active high by default.

Figure 55, Figure 56, and Figure 57 in the Modes of Operation section show timing diagrams of the DEV_EN signal and the ADC sampling instant relative to CNV rising edge. In sample mode and averaging mode, DEV_EN deasserts after each conversion. In burst averaging mode, DEV_EN remains asserted until the last conversion in the burst of samples. DEV_EN is not supported in the autonomous modes.

Note that the device enable signal (DEV_EN) and the CHOP signal cannot be enabled at the same time.

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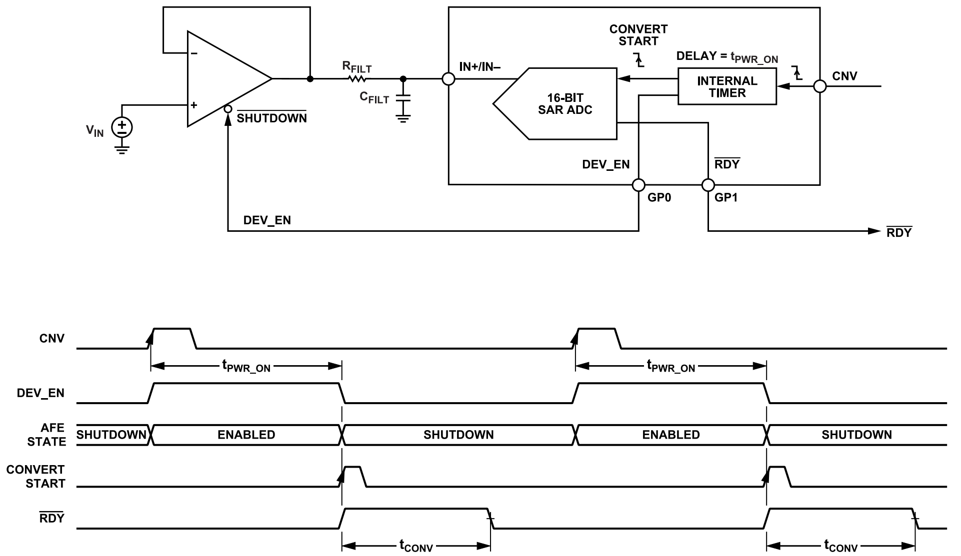

Figure 44. Typical Application Circuit with DEV_EN Signal

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Chop Control Signal

The AD4052/AD4058 include a control signal called CHOP that can be used as the control signal for an auto-zero amplifier that employs chopping in applications that require very low 1/f noise and offset error. The CHOP signal ensures the synchronization of the auto-zero amplifier's chopping and the ADC's sampling, removing the need for complex digital synchronization in the firmware.

The CHOP signal low-to-high and high-to-low transitions occur every K ADC conversions, where K is a power of 2 and is set by the CHOP_WIN_LEN bit field as defined in Table 43 and the following equation:

$$K = 2^{CHOP\_WIN\_LENGTH} \quad (3)$$

$$f_{CHOP} = \frac{\left(\frac{f_S}{2}\right)}{2^{CHOP\_WIN\_LENGTH}} = \frac{\left(\frac{f_S}{2}\right)}{K} \quad (4)$$

For example, when CHOP_WIN_LENGTH = 0, and K = 1, the CHOP signal frequency is half of the ADC sampling frequency (f_S). In this case, the CHOP signal transitions from low to high at the end of one ADC conversion, and then from high to low at the end of the next ADC conversion completing one CHOP cycle. Because each CHOP cycle lasts for two ADC conversion periods, the auto-zero amplifier's chopping frequency is a half of the ADC sampling rate.

The CHOP signal low-to-high and high-to-low transitions occur following the end of a conversion as shown in Figure 45. When the CHOP signal low-to-high and high-to-low transitions occur, the auto-zero amplifier's output sees glitching that needs to settle before the next ADC convert start. Synchronization of the ADC sampling and the auto-zero amplifier's chopping by the internal CHOP signal minimizes the error from these glitches by maximizing the allowed settling time for these glitches before the next ADC convert start.

The CHOP signal can be enabled by configuring either the GP0 or GP1 pin as the CHOP output (see Table 41).

The CHOP signal and the device enable signal (DEV_EN) cannot be enabled at the same time.

Figure 58, Figure 59, and Figure 60 in the Modes of Operation section show timing diagrams of the CHOP signal transitions relative to the CNV rising edge in sample mode, averaging mode, and burst averaging mode, respectively. The CHOP signal is not supported in the autonomous modes.

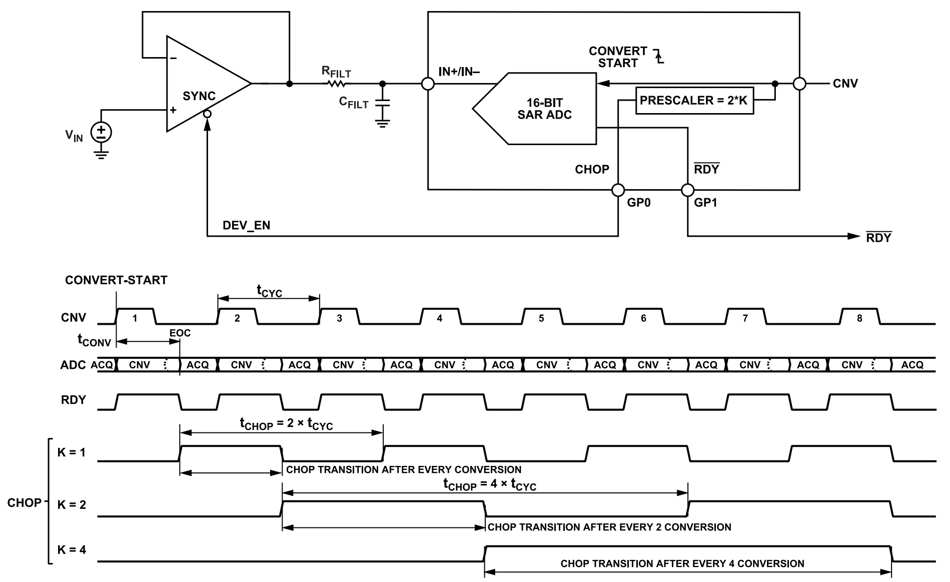

Figure 45. Typical Application Circuit with CHOP Signal

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THEORY OF OPERATION

Invert On CHOP

The AD4052/AD4058 also include a bit field called INVERT_ON_CHOP that can be enabled to use the CHOP signal as an ADC sample inversion controller.

Table 15 shows the logic table for sample inversion control based on the status of the INVERT_ON_CHOP setting and the CHOP signal state. When INVERT_ON_CHOP is enabled, the ADC inverts its transfer function in step with the CHOP signal. This allows the AD4052/AD4058 to function as the auto-zero demodulation stage if the chopper amplifier does not include it.

When the CHOP signal is enabled, the state of the INVERT_ON_CHOP field determines whether or not the ADC samples are inverted. However, when the CHOP signal is disabled, INVERT_ON_CHOP is considered "don't care" because the CHOP signal is always assumed to be low.

The INVERT_ON_CHOP function can be enabled or disabled by configuring the bit associated with it as low or high, as described in Table 41.

Table 15. INVERT_ON_CHOP logic table

INVERT_ON_CHOP	CHOP	Invert Sample
False	Low	False
True	Low	False
False	High	False
True	High	True

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MODES OF OPERATION

Table 16 shows an overview of the AD4052/AD4058 functional modes. The ADC and serial interface functionality for each mode is given in the subsequent sections.

Configuration mode is the default AD4052/AD4058 operating mode following power-up and device resets. The remaining operating modes are selected via the configuration registers as shown in Table 16. The SPI protocol for register writes and reads is described in the Configuration Mode section.

Figure 48 shows the AD4052/AD4058 operating mode selection as a state machine diagram. The ENTER_ADC_MODE bit field controls whether the AD4052/AD4058 is in configuration mode or in one of the five ADC modes as shown in Table 16. Configure the ADC_MODE and AUTO_MODE fields before setting ENTER_ADC_MODE to 1'b1 to select the desired operating mode.

Setting the ENTER_ADC_MODE to 1'b1 via a register write triggers the AD4052/AD4058 to transition from configuration mode to the selected ADC mode (see Figure 46).

The exit command triggers the AD4052/AD4058 to transition from the active ADC mode back to configuration mode. When the AD4052/AD4058 receives the exit command, it internally resets the ENTER_ADC_MODE bit to 1'b0. The exit command consists of the code 5'b10101 clocked in on the SDI pin on the first 5 SCLK rising edges following the $\overline{CS}$ falling edge. Figure 47 shows a timing diagram for the exit command. The t_{CONFIG} specification indicates the minimum delay between the exit command $\overline{CS}$ rising edge and when the AD4052/AD4058 can receive new register read and write SPI transactions (see Table 5 and Table 6).

Table 16. AD4052/AD4058 Functional Modes

Mode	ENTER_ADC_MODE	ADC_MODE	AUTO_MODE	POWER_MODE
Configuration Mode (Default)	1'b0	Don't Care	Don't care	2'b00
Sample Mode	1'b1	2'b00	Don't care	2'b00
Burst Averaging Mode	1'b1	2'b01	Don't care	2'b00
Averaging Mode	1'b1	2'b10	Don't care	2'b00
Monitor Mode	1'b1	2'b11	1'b0	2'b00
Trigger Mode	1'b1	2'b11	1'b1	2'b00
Sleep Mode	Don't care	Don't care	Don't care	2'b11

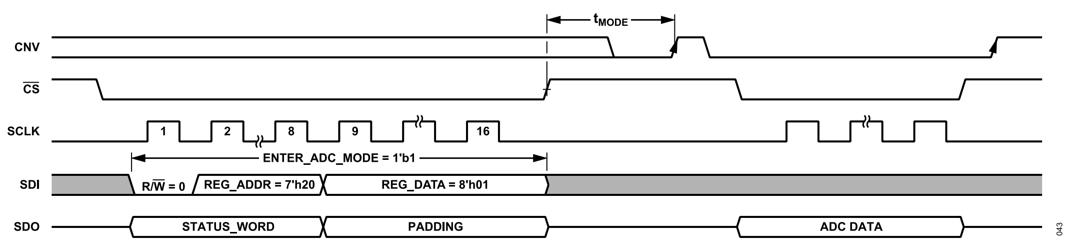

Figure 46. ENTER_ADC_MODE Timing Diagram

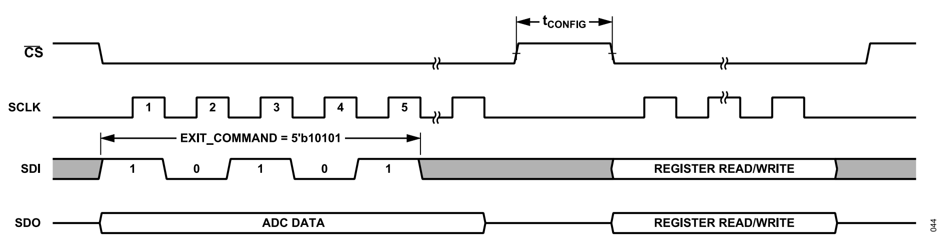

Figure 47. Exit Command Timing Diagram

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MODES OF OPERATION

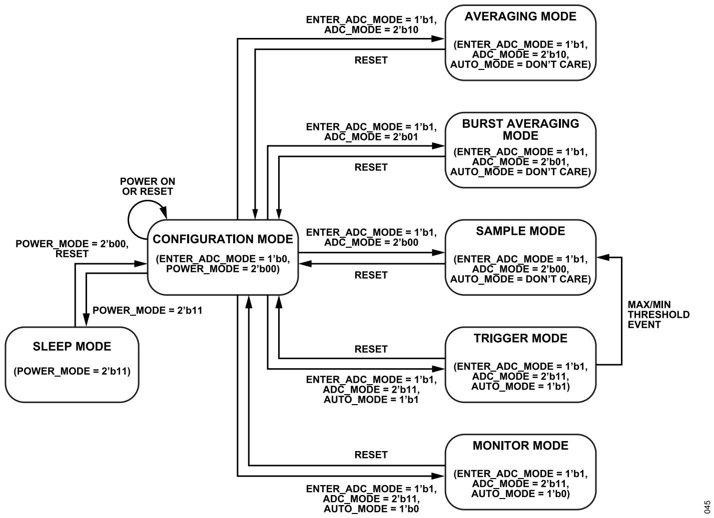

Figure 48. AD4052/AD4058 State Machine Diagram

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MODES OF OPERATION

SAMPLE MODE

In sample mode, a rising edge of the CNV signal triggers a single conversion. At the end of the conversion, the AD4052/AD4058 generate a 16-bit result that the digital host reads via the SPI. Table 16 lists the configuration register settings to select sample mode. Figure 49 shows a typical connection diagram for the AD4052/AD4058 digital interface, which includes a recommended 200 Ω series resistor close to the CNV pin.

Figure 50 shows an interface timing diagram for sample mode. The t_{CONV} specification quantifies the time delay between the CNV rising edge and the end of conversion. The digital host must wait for the maximum t_{CONV} delay before asserting $\overline{CS}$ and reading the result over the SPI. The $\overline{RDY}$ signal acts as an optional hardware interrupt to synchronize SPI reads to the ADC sampling phases (see the Data Ready Signal section). To ensure optimal performance, the digital host must also observe the t_{QUIET} specification that defines the minimum delay between the final SCLK falling edge and the next CNV rising edge.

By default, the output data are 16-bits long and are clocked out on the SDO on each SCLK falling edge. Sample mode also offers an optional sign-extension byte and CRC byte that can be appended to the 16-bit ADC data. See the ADC Mode Output Data Format section for details on the sample mode SDO data formatting options.

In sample mode, the maximum sampling rate (f_S) is limited by the output data rate of the SPI (f_{ODR}), which is a function of the output data length and serial clock frequency (f_{SCLK}). See the Calculating Serial Interface Output Data Rate section for details on estimating the maximum achievable f_S for the given operating conditions.

When the DEV_EN signal is enabled, the start of the conversion is delayed by the programmable t_{PWR_ON} delay relative to the CNV rising edge. See the Device Enable Signal section and Figure 55 for specific timing details when using the DEV_EN signal.

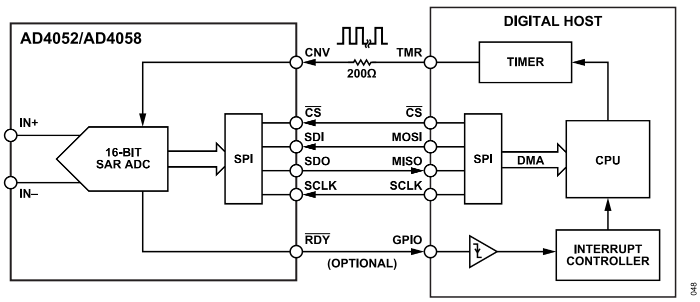

Figure 49. Sample Mode Example Connection Diagram

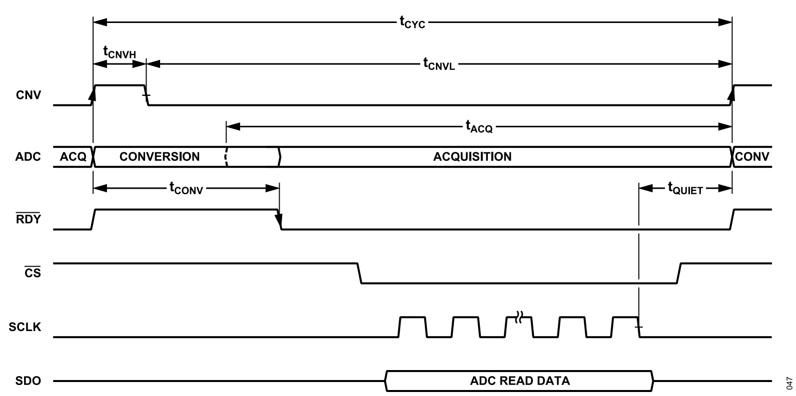

Figure 50. Sample Mode Timing Diagram

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MODES OF OPERATION

AVERAGING MODE

In averaging mode, each rising edge of the CNV signal triggers a conversion to start, and the averaging filter accumulates multiple consecutive conversion results to generate a 20-bit averaged result. Table 16 lists the configuration register settings to select averaging mode. Figure 51 shows a typical connection diagram for the AD4052/AD4058 digital interface that includes a recommended 200 Ω series resistor close to the CNV pin.

Figure 52 shows an interface timing diagram for averaging mode. All timing specifications in Figure 52 are given in the Timing Specifications section. The ADC sampling period (t_{CYC}) is set by the period of the CNV signal, and the output data rate (f_{ODR}) of the averaging filter is f_S divided by the averaging ratio (N_{AVG}). Larger averaging ratios yield greater noise reduction and resolution improvements, but slower f_{ODR}. The averaging filter supports averaging ratios from 2 to 4096 and is set by the AVG_WIN_LEN bit field, as described in the Block Averaging Filter section.

The digital host must wait for the averaged result to be ready before asserting $\overline{CS}$ to start an SPI frame. The $\overline{RDY}$ signal acts as an optional hardware interrupt to synchronize the SPI reads to the ADC sampling phases (see the Data Ready Signal section). To ensure optimal performance, the digital host must also observe the t_{QUIET} specification that defines the minimum delay between the final SCLK falling edge and the next CNV rising edge.

By default, the averaging mode output data are 24-bits long, including the 20-bit averaged ADC data with 4-bits of sign extension. Averaging mode also offers an optional sign-extension byte and CRC byte that can be appended to the 24-bit data. See the ADC Mode Output Data Format section for details on the averaging mode SDO data formatting options.

In averaging mode, the maximum sampling rate (f_S) is limited by the output data rate of the SPI (f_{ODR}), which is a function of the output data length and serial clock frequency (f_{SCLK}). See the Calculating Serial Interface Output Data Rate section for details on estimating the maximum achievable f_S for the given operating conditions.

When the DEV_EN signal is enabled, the start of the conversion is delayed by the programmable t_{PWR_ON} delay, relative to the CNV rising edge. See the Device Enable Signal section and Figure 55 for specific timing details when using the DEV_EN signal.

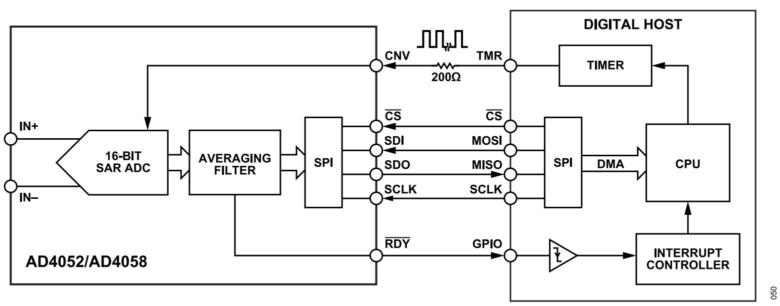

Figure 51. Averaging Mode Example Connection Diagram

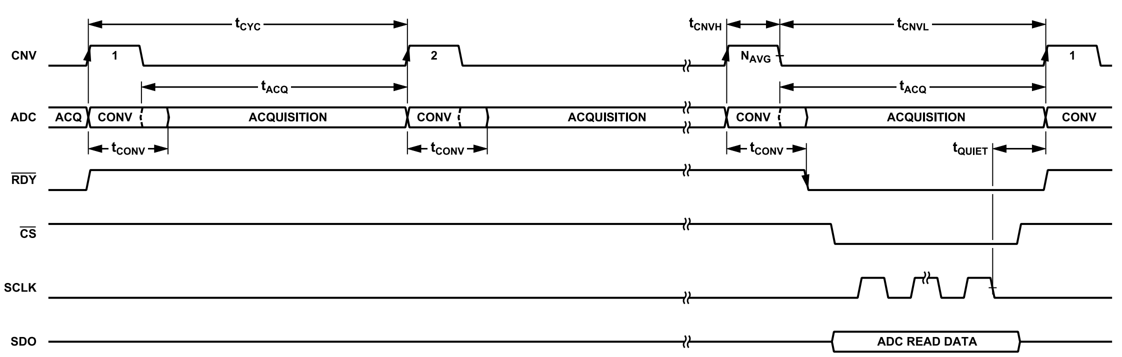

Figure 52. Averaging Mode Timing Diagram

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MODES OF OPERATION

BURST AVERAGING MODE

In burst averaging mode, a rising edge of the CNV signal triggers the internal timer to perform a burst of conversions for the averaging filter to accumulate and generate a 20-bit averaged result. Table 16 lists the configuration register settings to select burst averaging mode. Figure 53 shows a typical connection diagram for the AD4052/AD4058 digital interface that includes a recommended 200 Ω series resistor close to the CNV pin.

Figure 54 shows an interface timing diagram for burst averaging mode. All timing specifications in Figure 54 are given in the Timing Specifications section. The ADC sampling period (t_{CYC}) is set by the internal timer frequency (f_{OSC}) and the number of samples per burst is set by the averaging ratio (N_{AVG}). Table 44 lists the options for f_{OSC}. The averaging filter supports averaging ratios from 2 to 4096 and is set by the AVG_WIN_LEN bit field, as described in the Block Averaging Filter section.

The digital host must wait for the averaged result to be ready before asserting $\overline{CS}$ to start an SPI frame. The $\overline{RDY}$ signal acts as an optional hardware interrupt to synchronize the SPI reads to the ADC sampling phases (see the Data Ready Signal section). The total latency between the CNV rising edge and data ready is given by the following equation:

$$\frac{(N_{AVG} - 1)}{f_{OSC}} + t_{CONV} \quad (5)$$

To ensure optimal performance, the digital host must also observe the t_{QUIET} specification that defines the minimum delay between the final SCLK falling edge and the next CNV rising edge.

By default, the burst averaging mode output are 24-bits long, including the 20-bit averaged ADC data with 4-bits of sign extension. Burst averaging mode also offers an optional sign extension byte and CRC byte that can be appended to the 24-bit data. See the ADC Mode Output Data Format section for details on the burst averaging mode SDO data formatting options.

When the DEV_EN signal is enabled, the start of the burst of conversions is delayed by the programmable t_{PWR_ON} delay, relative to the CNV rising edge. The DEV_EN signal remains asserted until the end of the burst of samples. See the Device Enable Signal section and Figure 57 for specific timing details when using the DEV_EN signal.

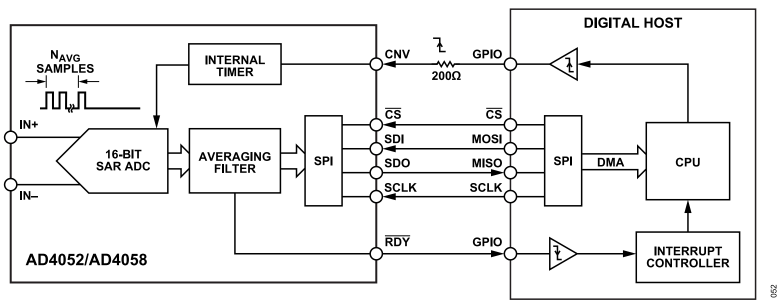

Figure 53. Burst Averaging Mode Example Connection Diagram

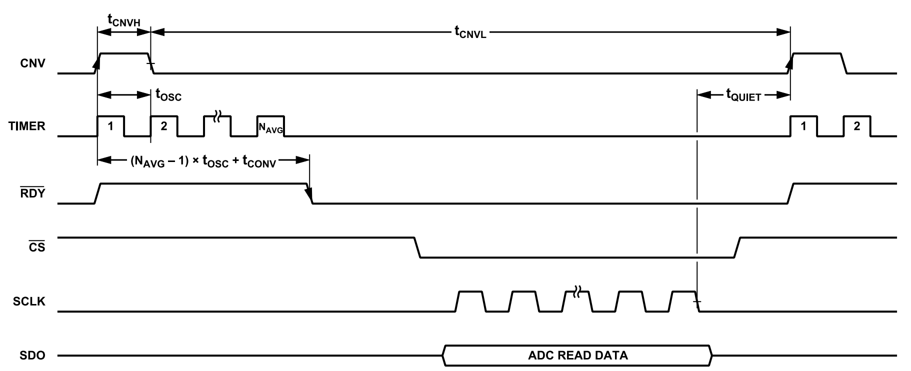

Figure 54. Burst Averaging Mode Timing Diagram

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MODES OF OPERATION

DEV_EN TIMING DIAGRAMS

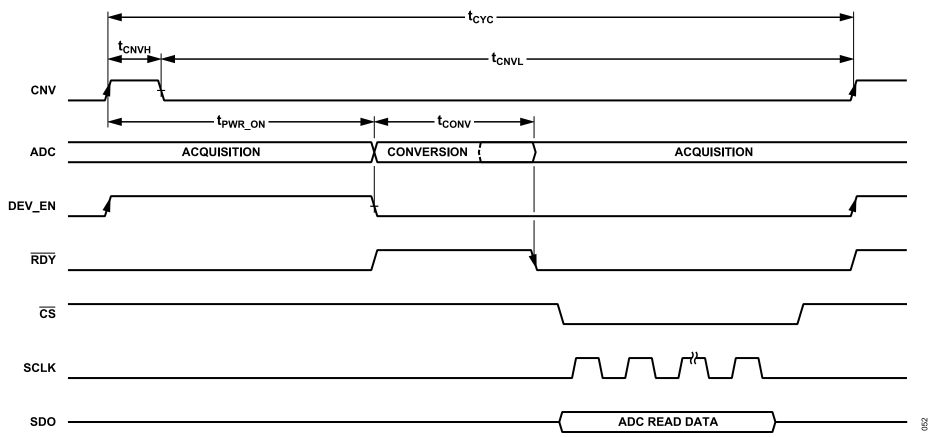

Figure 55. Sample Mode Timing with DEV_EN Enabled

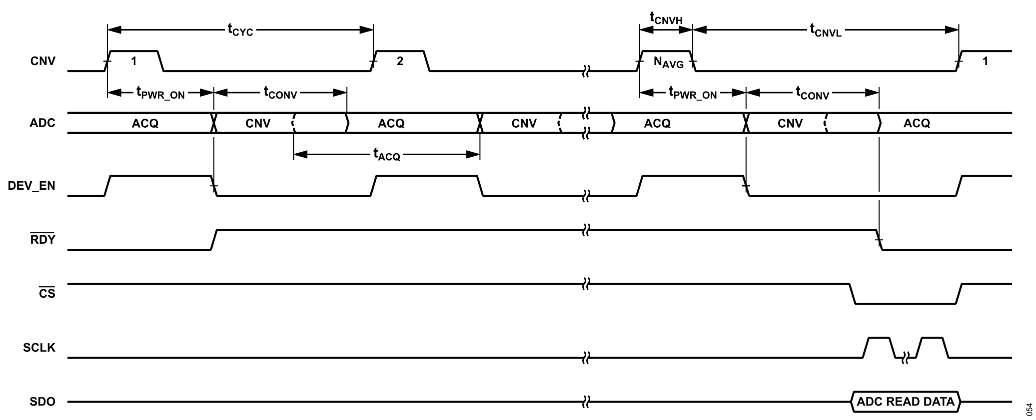

Figure 56. Averaging Mode Timing with DEV_EN Enabled

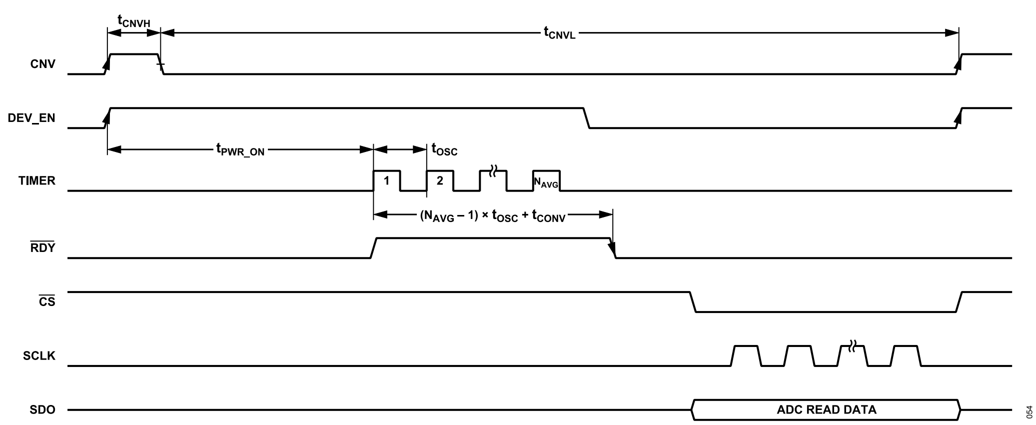

Figure 57. Burst Averaging Mode Timing with DEV_EN Enabled

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MODES OF OPERATION

CHOP TIMING DIAGRAMS

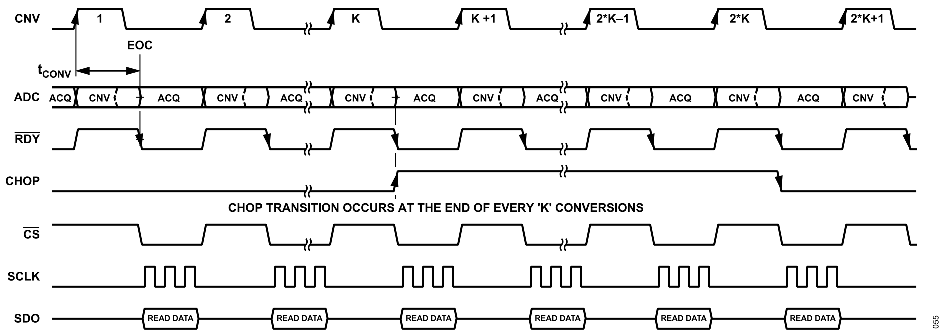

Figure 58. Sample Mode Timing with CHOP Enabled

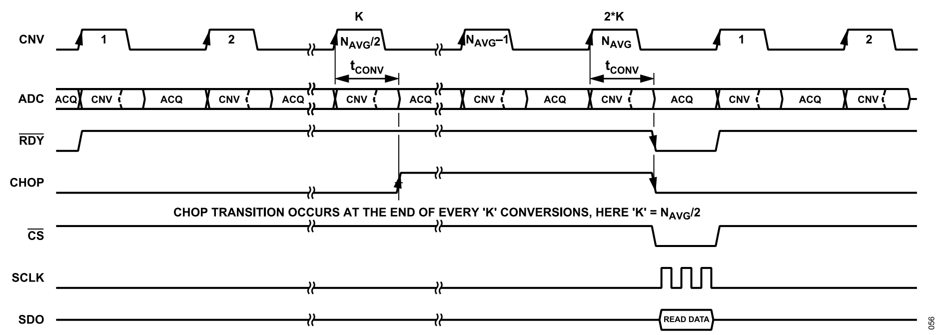

Figure 59. Averaging Mode Timing with CHOP Enabled

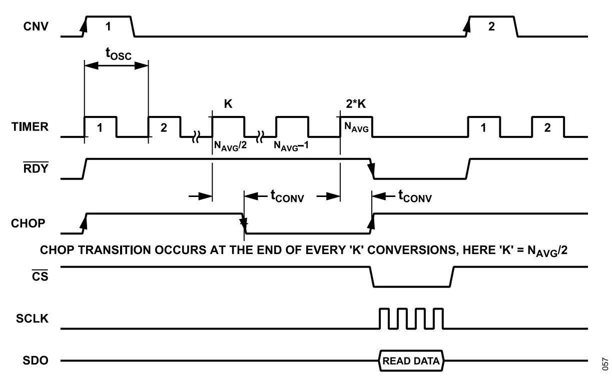

Figure 60. Burst Averaging Mode Timing with CHOP Enabled

AUTONOMOUS MODES

The autonomous modes allow the AD4052/AD4058 to autonomously monitor the input signal to detect out-of-range events. The autonomous modes feature lower power dissipation than nonautonomous modes, because the ADC core enters a low-power comparator mode, as described in the Comparator Operation section (see Table 1 for power dissipation specifications for each mode).

The AD4052/AD4058 offer two autonomous modes, monitor mode and trigger mode. Both autonomous modes are described in the subsequent sections. When either autonomous mode is selected, the ADC core functions as a window comparator, and the ADC sampling clock is driven by the internal timer, as described in the Comparator Operation section. The sampling clock frequency is set by the FS_BURST_AUTO bit field in the TIMER_CONFIG register (see Table 44).

The comparator performs the following four sample-and-comparison operations in a repeated sequence, each taking one sample period to execute, for a total sequence time of four sample periods:

1. $V_{IN} \geq$ MAX_LIMIT
2. $V_{IN} \leq$ MAX_LIMIT − MAX_HYST
3. $V_{IN} \geq$ MIN_LIMIT + MIN_HYST

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MODES OF OPERATION

4. V_{IN} ≤ MIN_LIMIT

The comparator includes two hardware alert signals for the maximum and minimum threshold events (MAX_INTR and MIN_INTR, respectively). These signals can be assigned to either or both of the GP0 and GP1 pins, as described in the Threshold Alert Signals section. Figure 63 shows a typical connection diagram for a microcontroller using these alert signals as hardware interrupts.

Monitor Mode

In monitor mode, the AD4052/AD4058 continuously operate in autonomous mode until the digital host sends the exit command to put it back into configuration mode (see Figure 48). Monitor mode makes use of the user-programmable hysteresis settings to self-clear the MAX_INTR and MIN_INTR signals when the input signal goes back in range (see Figure 43).

Figure 61 shows a flowchart for register configuration, the comparison sequence operations, and the behavior of the hardware interrupts and alert flags following threshold crossings in monitor mode. Table 16 lists the configuration register settings to select monitor mode.

When the maximum or minimum threshold crossings are detected, the MAX_INTR or MIN_INTR signal asserts, respectively. The internal timer continues to generate the sampling clock, and the MAX_INTR or MIN_INTR signal is deasserted when the sampled input signal is back in bounds as set by the MAX_HYST and MIN_HYST bit fields, respectively.

The MAX_FLAG or MIN_FLAG bit is also asserted when MAX_INTR or MIN_INTR asserts, respectively. The MAX_FLAG and MIN_FLAG are sticky and do not self-clear when the signal goes back in range. It is recommended to reset the MAX_FLAG and MIN_FLAG bits after sending the exit command and before returning to autonomous mode.

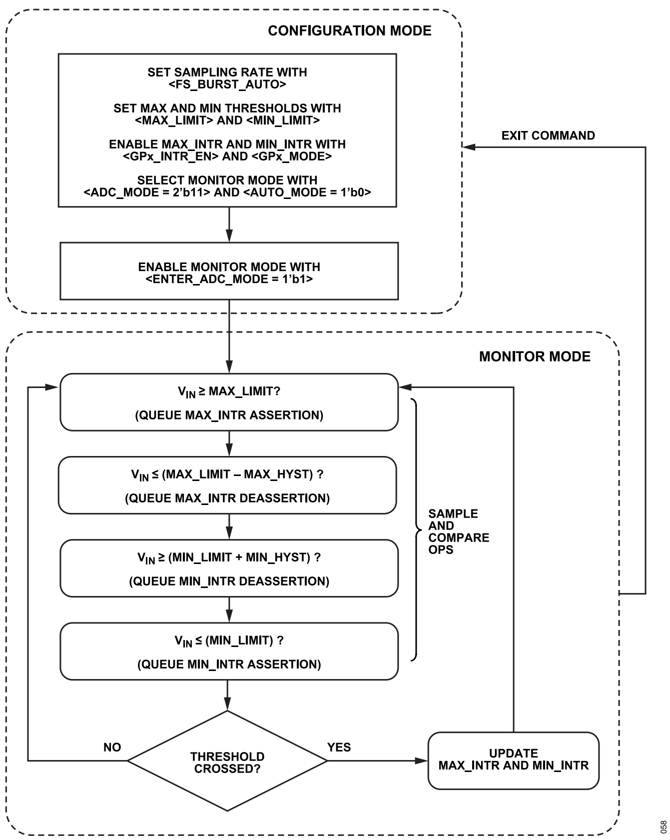

Figure 61. Monitor Mode Flowchart

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MODES OF OPERATION

Trigger Mode

In trigger mode, threshold crossings trigger the AD4052/AD4058 to automatically perform a 16-bit conversion of the input signal and transition into sample mode. The corresponding alert signals and status bits are asserted to send an interrupt to the digital host. The host can then read the 16-bit result from the SPI as described in the sample mode section or from the MAX_SAMPLE_REG or MIN_SAMPLE_REG registers in configuration mode.

Figure 62 shows a flowchart for register configuration, the comparison sequence operations, and the behavior of the hardware interrupts and alert flags following threshold crossings in trigger mode. Table 16 lists the configuration register settings to select trigger mode.

When a maximum or minimum crossing is detected, the MAX_INTR or MIN_INTR signal asserts, respectively. The internal timer is disabled to stop autonomous sampling, and the ADC core powers up to convert the input signal. Figure 64 shows a timing diagram for the threshold detection and ADC sampling in trigger mode. Following the threshold event, the firmware can either continue operating the AD4052/AD4058 in sample mode to perform more conversions, or the firmware can send the exit command to put the device into configuration mode and read the alert registers. The MAX_INTR and MIN_INTR signals hold their states until the host sends the exit command to transition to register mode.

Note that following the transition to sample mode, the ADC_MODE bit field in the register map is internally overwritten to 2'h0 and must be rewritten to 2'h3 to reenter autonomous mode.

The MAX_FLAG or MIN_FLAG bit is also asserted when MAX_INTR or MIN_INTR asserts, respectively. The MAX_FLAG and MIN_FLAG bits are sticky and do not clear until the host sets them to 1'b1 with a register write. It is recommended to reset the MAX_FLAG and MIN_FLAG bits after sending the exit command and before returning to autonomous mode.

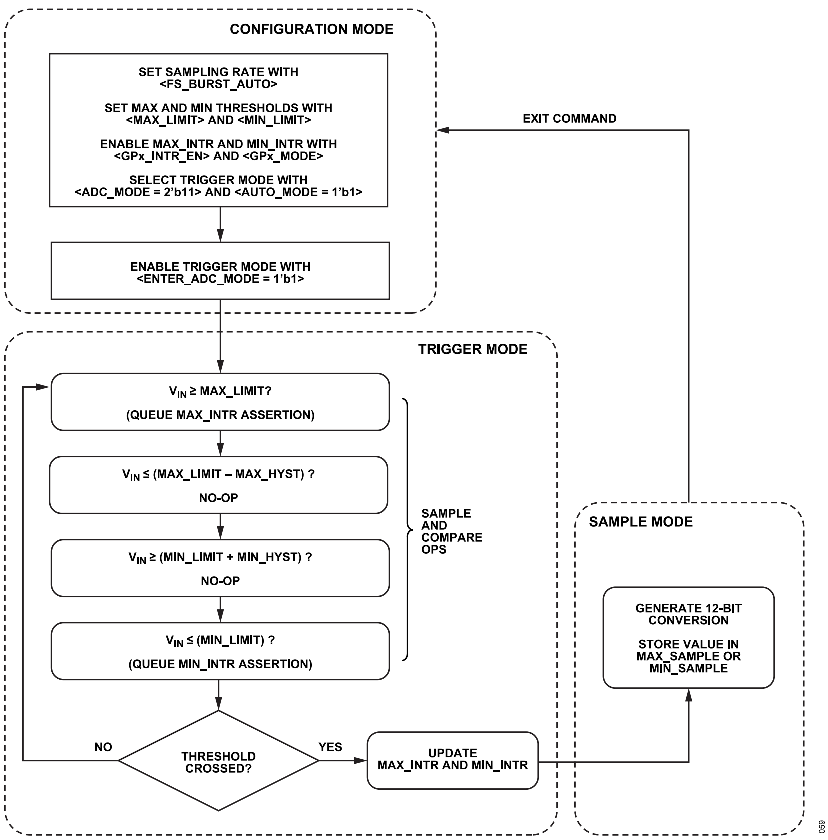

Figure 62. Trigger Mode Flowchart

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MODES OF OPERATION

Autonomous Mode Diagrams

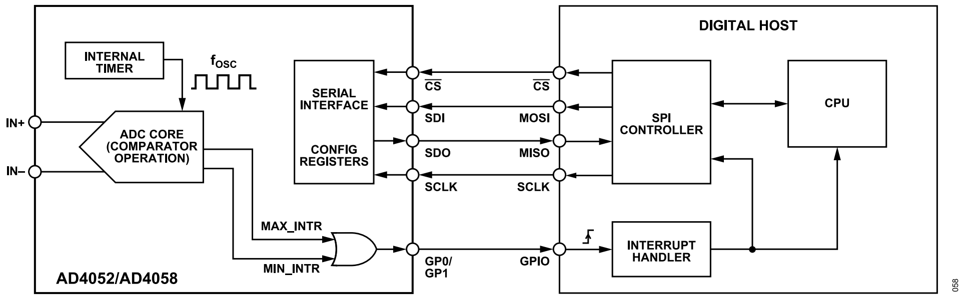

Figure 63. Autonomous Mode Example Connection Diagram

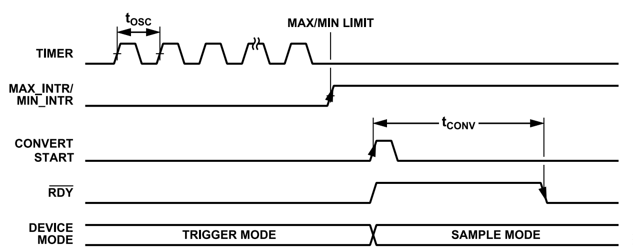

Figure 64. Trigger Mode Timing Diagram

SLEEP MODE

In sleep mode, the AD4052/AD4058 power down all functional blocks, except the digital interface, to achieve an ultra-low power consumption of 430 nW for extended periods of idle time (see Table 1). Set the POWER_MODE bit field in the DEVICE_CONFIG register to 2'h3 to put the AD4052/AD4058 into sleep mode.

The internal LDO regulator is powered down and stops supplying the +1.8 V CLDO supply while in sleep mode. This feature powers down the ADC core and most other functional blocks. The digital interface remains active, so the digital host can rewrite the POWER_MODE bit field to 2'h0 to exit sleep mode and power up the device. When the device exits sleep mode, it enters configuration mode. The configuration register states persist, so the digital host does not need to reprogram the device configuration after exiting sleep mode.

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SERIAL INTERFACE

The AD4052/AD4058 digital interface includes a 4-wire SPI for serial data transfer, a CNV input for triggering ADC conversions, and two general-purpose digital outputs, GP0 and GP1. The SPI is primarily used for reading and writing the AD4052/AD4058 configuration registers and for reading the ADC results. The Modes of Operation section describe the SPI functionality and protocols for each operating mode.

A 200 Ω series resistor is recommended between the AD4052/AD4058 CNV pin and the digital host (see Figure 72). When using pull-up or pull-down resistors on the digital traces, 100 kΩ is recommended to minimize excess power dissipation.

The AD4052/AD4058 SPI follows clock polarity (CPOL) = clock phase (CPHA) = 0 protocol, where the SCLK signal idles low, data is latched on SDI on SCLK rising edge, and data is updated on SDO on SCLK falling edge.

The AD4052/AD4058 include a CRC for register reads and writes and ADC data reads supporting robust data transfers. The ADC data are formatted to integer multiples of bytes to maximize compatibility with microcontroller internal memory transfer operations such as direct memory access (DMA) transfers from the SPI to the central processing unit (CPU). See the ADC Mode Output Data Format section for details on CRC and sign extension.

The interface logic level is set by the VIO supply voltage, as specified in Table 1. The AD4052/AD4058 support 1.8 V, 2.5 V, and 3.3 V logic systems. Note that the SPI timing specifications differ between each operating mode and for different VIO logic levels (see the Timing Specifications section).

CONFIGURATION MODE

Configuration mode is used to read and write to the user registers that configure the AD4052/AD4058 operating modes and features. Configuration mode is the default operating mode following power-up and device resets. In configuration mode, the digital host accesses the user registers via the SPI, and the AD4052/AD4058 CNV input is ignored to prevent the ADC core from performing unnecessary conversions. Register reads and writes are supported only in configuration mode.

Figure 65 shows the data format for register reads and writes in configuration mode. Register reads and writes consist of an instruction phase followed by a data phase. The following sections provide further details about each phase of register read and write transactions.

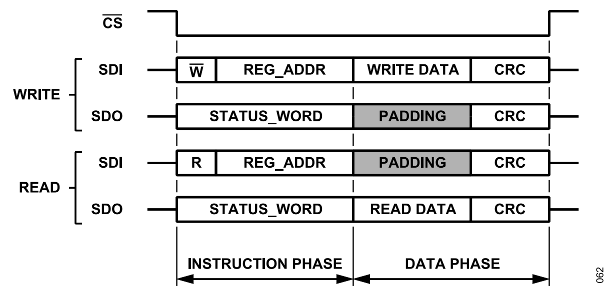

Figure 65. Configuration Mode SPI Format

Instruction Phase

The instruction phase begins following each $\overline{CS}$ falling edge. There is only one instruction phase per SPI frame, and the instruction phase is followed by one or more data phases. The instruction phase consists of the R/$\overline{W}$ bit, followed by the address of the register being accessed (REG_ADDR). Data are latched on the SDI input on the SCLK rising edges. The R/$\overline{W}$ bit specifies if the SPI transaction is a register read or a register write. Set R/$\overline{W}$ to 1 for register reads and 0 for register writes. The AD4052/AD4058 also output a status word (STATUS_WORD) on SDO during the instruction phase (see the Status Word section).

The addresses for all configuration registers are given in the Register Summary section. The default length of the instruction phase is 8 bits, with REG_ADDR length of 7 bits. The instruction phase can optionally be extended to 16 bits, with REG_ADDR length of 15 bits, in order to clock out the entire STATUS_WORD. Set the ADDR_LEN bit in the INTERFACE_CONFIG_B register to 0 to extend the instruction phase to 16 bits.

Status Word

The AD4052/AD4058 instruction phase includes a status word (STATUS_WORD) for transmitting basic device state information to the digital host. The STATUS_WORD is clocked out on the SDO pin during the instruction phase, as shown in Figure 65. Table 17 shows the contents of the STATUS_WORD. All STATUS_WORD bits correspond to select bit fields from the configuration registers (see the Register Details section).

The length of the STATUS_WORD is either 1 byte or 2 bytes long and is equal to the length of the register access command as set by the ADDR_LEN bit (see the Instruction Phase section). The least significant byte of the STATUS_WORD is always included, regardless of the ADDR_LEN setting. The most significant byte of the STATUS_WORD is only included when the ADDR_LEN bit is set to 0.

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SERIAL INTERFACE

Table 17. Status Word Contents

Status Word Index	Bit Field Name
15	NOT_RDY_ERR
14	0
13	0
12	SCLK_ERR
11	SPI_CRC_ERR
10	WR_INVALID
9	MB_ERR
8	ADDR_INVALID
7	DEVICE_READY
6	INTERFACE_ERR
5	FUSE_CRC_ERR
4	0
3	0
2	THRESH_OVERRUN
1	MAX_FLAG
0	MIN_FLAG

Data Phase

The data phase immediately follows the instruction phase. During the data phase, register data is either clocked out on the SDO pin (for register reads) or latched in on the SDI pin (for register writes). Each configuration mode SPI frame can have one or multiple data phases, as shown in Figure 66.

Each register address (REG_ADDR) corresponds to 1 byte of register memory, and each data phase must contain an integer multiple of 8 bits (8 SCLK periods) for the register read or write to be considered valid. Registers are not updated if the register write data phase is not an integer multiple of 8 bits.

The AD4052/AD4058 support bulk register reads and writes for efficient access to contiguous sections of the register map. Figure 66 shows the SPI protocol for bulk register reads and writes. To perform bulk read and write register transactions, hold the $\overline{CS}$ signal low and continue issuing SCLK pulses to execute multiple data phases in succession. When streaming registers, the instruction phase defines the REG_ADDR for the first data phase, and in each subsequent data phase the address decrements by 1.

When the interface CRC is enabled, a CRC byte is appended for each data phase byte (see the Register Access CRC section).

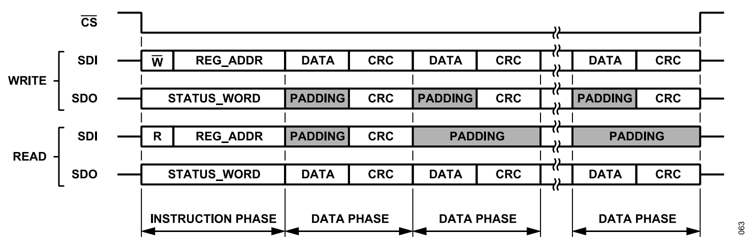

Figure 66. Streaming Registers in Configuration Mode

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SERIAL INTERFACE

Register Access CRC

The AD4052/AD4058 include optional error checking for register reads and writes based on CRC-8, using the following polynomial:

$$x^8 + x^2 + x + 1 \quad (6)$$

The CRC is enabled by setting the CRC_EN and CRC_EN_B bit fields to 0x1 and 0x2, respectively. When the CRC is enabled, an 8-bit checksum code is appended to each register data byte, as shown in Figure 66. The value of the checksum is calculated from the data read or written over the SPI, which allows the AD4052/AD4058 and the digital host to detect corrupted serial communications.

When the AD4052/AD4058 receive a checksum that is inconsistent with its corresponding SPI transaction, the transaction is considered invalid, and the SPI_CRC_ERR bit in the INTERFACE_STATUS register is set to 1. The SPI_CRC_ERR bit is a write-1-to-clear bit (R/W1C). When the CRC is enabled, it is recommended to check the SPI_CRC_ERR bit after each register read and write attempt.

When a register write has an invalid CRC, the contents of the register are not updated. For bulk register writes such as those shown in Figure 66, the AD4052/AD4058 also ignore data for registers following the invalid CRC. When a register read has an invalid CRC, the digital host must discard the received data and retry the register read.

The CRC-8 calculation is seeded by a nonzero value to detect if the data lines are stuck low. The seed for the first CRC following each $\overline{CS}$ falling edge is 0xA5. When performing bulk reads or writes, the seed for all subsequent CRCs is the least significant byte (LSByte) of the current register address. Table 18 summarizes the data and seed values for all possible register read and write transactions in configuration mode.

Table 18. CRC Data and Seed Values for Configuration Mode SPI Transactions

SPI Transaction Type	Pin	First CRC	Subsequent CRCs
Write	SDI	Seed = 0xA5, Data = [instruction phase data, register write data]	Seed = LSByte of register address, Data = register write data
	SDO	Seed = 0xA5, Data = [instruction phase data, register write data]	Seed = LSByte of register address, Data = register write data
Read	SDI	Seed = 0xA5, Data = [instruction phase data, padding]	Not applicable
	SDO	Seed = 0xA5, Data = [instruction phase data, register read data]	Seed = LSByte of register address, Data = register read data

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SERIAL INTERFACE

ADC MODE OUTPUT DATA FORMAT

This section describes the SPI output data format for the ADC modes described in the Modes of Operation section (sample mode, averaging mode, burst averaging mode, and trigger mode). The output word consists of the ADC results (ADC_DATA) and optional sign extension (SE_BYTE) and CRC bytes (CRC). The output word length is always an integer multiple of bytes to ensure compatibility with digital host serial interface and data packet transfers (such as DMA), which are often segmented into integer multiples of bytes.

Figure 67 shows all supported formats for sample and trigger modes, and Figure 68 shows all supported formats for averaging and burst averaging modes.

In sample and trigger modes, the ADC_DATA are 16 bits long (2 bytes). In averaging and burst averaging mode, the ADC_DATA are 20 bits long with 4 bits of sign extension (SE_BITS) for a total of 24 bits (3 bytes). The ADC_DATA are either twos complement or straight binary depending on the DATA_FORMAT bit setting (see the Transfer Function section).

Sign-Extension Byte

The optional SE_BYTE allows the AD4052/AD4058 output word length to match the digital host data transfer size, if needed. When enabled, a byte of MSB sign-extension is added to the ADC data. For example, the default ADC output word length in burst averaging mode is 3 bytes. However, the SE_BYTE can convert the output word to 4 bytes for direct compatibility with a 4-byte DMA transfer. The ADC_DATA are right-justified to maintain the integer values without bit-shifting in software.

The SE_BYTE is enabled by setting the SIGN_EXT_EN bit to 1. The SE_BYTE is disabled by default.

ADC CRC

When the CRC is enabled, an 8-bit checksum code is appended to the ADC result on the SDO pin. The CRC checksum is calculated using the same polynomial given in Equation 6 with the SDO data as the input and a seed value of 0xA5 for all reads. The CRC is enabled with the CRC_EN and CRC_EN_B bit fields, as described in the Register Access CRC section. The CRC is disabled by default.

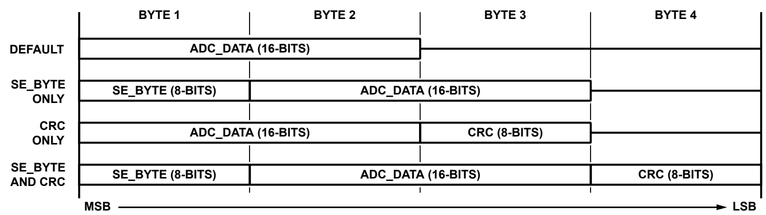

Figure 67. SPI Data Formats for Sample Mode and Trigger Mode

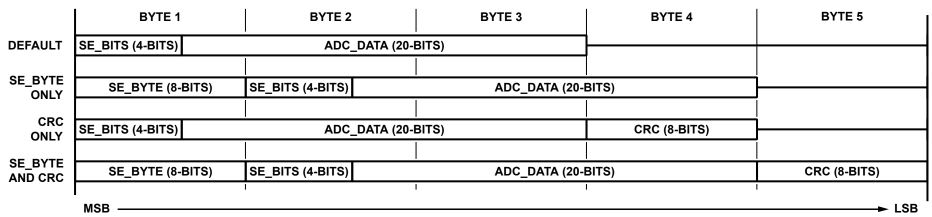

Figure 68. SPI Data Formats for Averaging Mode and Burst Averaging Mode

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SERIAL INTERFACE

DEVICE RESET

A device reset returns the device registers to the default settings and puts the AD4052/AD4058 into configuration mode. The following sections describe the AD4052/AD4058 device reset mechanisms.

The AD4052/AD4058 include a hardware interrupt signal (DEV_RDY) that indicates when the device reset is complete. The DEV_RDY signal is active high and is assigned to the GP1 pin by default, so the digital host can monitor the GP1 pin for a rising edge to inform the firmware that the AD4052/AD4058 SPI is ready. See the Device Ready Signal for more information.

The DEVICE_RESET bit in the DEVICE_STATUS register indicates when a device reset has occurred. The DEVICE_RESET bit is a write-1-to-clear bit and holds its state until the host writes it to the value 1'b1. The DEVICE_RESET bit can be referenced to confirm a reset executed as expected or if an unintended reset occurred (for example, if the power supplies failed during operation).

Reset Bits

A reset is initiated by setting both the SW_RESET and SW_RESETX bits in the INTERFACE_CONFIG_A register to 1'b1 in the same write instruction (see the Interface Configuration A Register section). Two reset bit fields are used to reduce the likelihood of an unintended reset from interference on the SPI signals. The reset bits are only available in configuration mode, because they are located in the INTERFACE_CONFIG_A configuration register.

Figure 69 shows the timing diagram for resetting the AD4052/AD4058 with the reset bits. The digital host must wait for the t_{RESET} delay to elapse before initiating SPI transactions (see Table 1).

Reset Pattern

The reset pattern shown in Figure 70 allows the digital host to reset the AD4052/AD4058 from any of its operating modes. The reset pattern is equivalent to an 18-byte SPI write with the code 48'hFFFF FFFF FFFE repeated three times.

Figure 70 shows the timing diagram for resetting the AD4052/AD4058 with the reset bits. The digital host must wait for the t_{RESET} delay to elapse before initiating SPI transactions (see Table 1).

Power-On Reset

The AD4052/AD4058 is designed to generate a power-on reset (POR) when the VDD and VIO rails are first applied or when the rails are power cycled. A POR on the VDD or VIO supplies resets the state of the user configuration registers. The configuration registers are not reset when the AD4052/AD4058 enter sleep mode and disable the internal LDO regulator (see the Sleep Mode section).

Figure 71 shows the timing diagram for the AD4052/AD4058 PORs. The digital host must wait for the t_{RESET} delay after the power supplies are stable. Then the digital host must perform a reset with the reset bits or the reset pattern. Finally, an additional t_{RESET} delay must elapse before performing other SPI transactions.

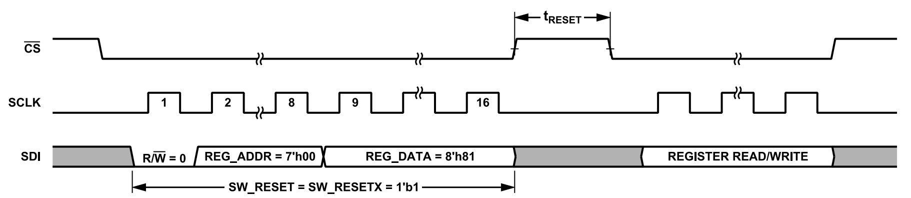

Figure 69. Reset Bit Timing Diagram

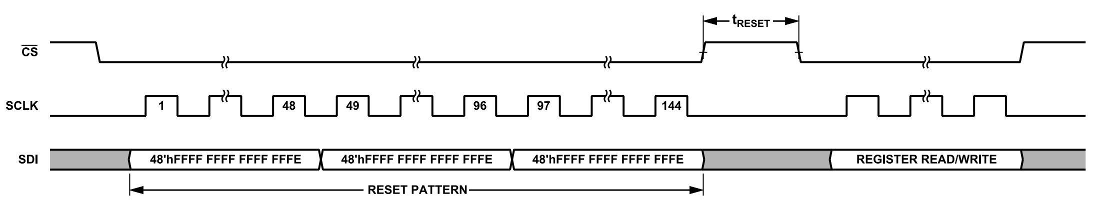

Figure 70. Reset Pattern Timing Diagram

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SERIAL INTERFACE

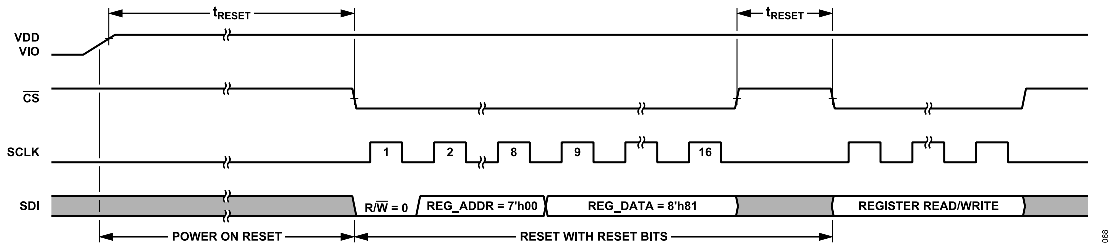

Figure 71. POR Timing Diagram

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APPLICATIONS INFORMATION

TYPICAL APPLICATIONS DIAGRAM

Figure 72 shows an example connection diagram with the AD4052/AD4058. Common companion circuitry for the AD4052/AD4058 includes power management, voltage reference circuitry, analog front-end and signal conditioning circuitry, and an SPI-compatible digital host (such as a microcontroller or a field programmable gate array (FPGA)).

The components shown in Figure 72 are general recommendations for best performance when operating the AD4052/AD4058 at 2 MSPS/500 kSPS and not intended for all use cases. The following sections provide more guidelines for component selection.

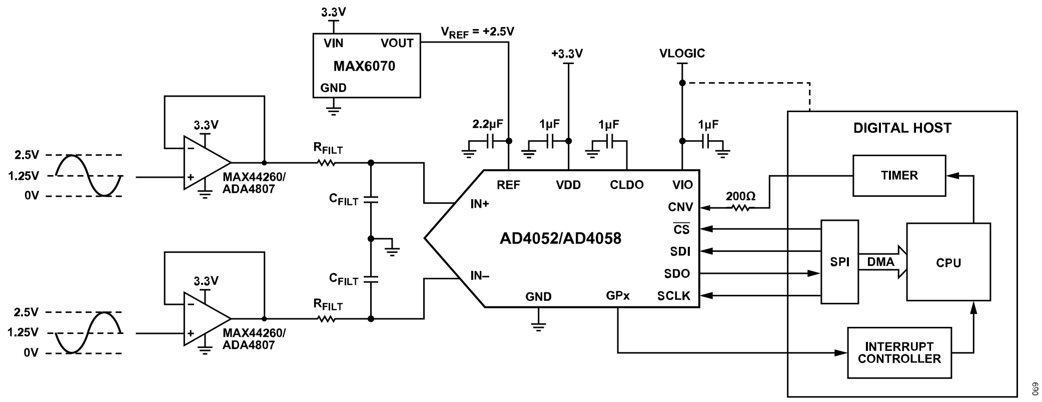

Figure 72. AD4052/AD4058 Typical Application Diagram

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APPLICATIONS INFORMATION

ANALOG FRONT-END DESIGN

Wide Input Common-Mode Range

The AD4052/AD4058 analog inputs feature a wide common-mode input voltage range that is only restricted by the absolute voltage range for each input (see Table 1). The IN+ and IN− signals can span anywhere between 0 V and V_{REF} without violating the common-mode input voltage specification (V_{CM}), ensuring compatibility with both differential and single-ended type signals. The V_{CM} voltage is given in the following equation and illustrated in Figure 73.

The AD4052/AD4058 convert the differential voltage between IN+ and IN−, and the common-mode signal is attenuated by the CMRR (see Table 1 and Figure 18).

$$V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \tag{7}$$

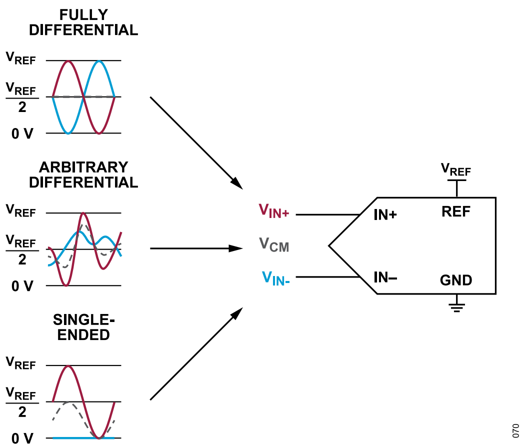

Figure 73. AD4052/AD4058 Wide Input Common-Mode Range

AD4052/AD4058 Equivalent Analog Input Model

As described in the Analog Inputs section, the AD4052/AD4058 analog inputs can be modeled as switched capacitive loads, with the IN+ and IN− inputs each connected to a 3.4 pF sampling capacitor through a set of sampling switches (SW1). As part of each conversion phase, the SW1 switch disconnects and reconnects the sampling capacitors (C_{IN}) from the IN+ and IN− pins, causing transient input current and voltage glitches at the output of the AFE circuit. The small C_{IN} of the AD4052/AD4058 ensures the magnitude of the transient current and voltage spikes is minimal compared to other SAR ADCs, but the AFE must still be designed to settle these glitches quickly enough (before the next conversion) to meet the accuracy and performance specifications in Table 1.

Figure 74 shows an equivalent load circuit model of the AD4052/AD4058 IN+ and IN− inputs. SW1 represents the sampling switches and SW2 represents the C_{IN} reset switch. The SW1 switch opens at the beginning of the conversion phase to sample the IN+ and IN− voltages on the C_{IN} capacitors. Before the start of the acquisition phase, the SW2 switch shorts the sampling capacitors together to reset them to a known, predictable state. Because the C_{IN} capacitance is the same for both IN+ and IN−, the reset voltages on each capacitor are equivalent and are given by the following equation:

$$\frac{V_{IN+} + V_{IN-}}{2} \tag{8}$$

where V_{IN+} and V_{IN-} are the sampled IN+ and IN− voltages, respectively. Note that this formula is the same as the common-mode input voltage formula given in Equation 7.

As mentioned in the Converter Operation section, the AD4052/AD4058 acquisition and conversion phases overlap. The acquisition phase starts 210 ns after the start of the conversion phase. At the start of the acquisition phase, the SW2 switch opens and the SW1 switch closes to reconnect C_{IN} to the AD4052/AD4058 inputs to acquire the signal. At the instant SW1 closes, the IN+ and IN− inputs sink or source some charge from the AFE circuit to recharge the C_{IN} capacitors to the intended signal voltage. The transient current spike causes transient voltage glitches on each pin, with magnitudes that are a function of the amount of charge pulled by the C_{IN} capacitors and the output impedance of the AFE circuit.

The SW2 switch is implemented to minimize linearity errors if the AFE cannot completely settle the input glitch before the next conversion phase. The SW2 switch ensures the charge transfer per sample is linearly related to the input signal voltage. The worst-case current and voltage glitch magnitude occur when the differential input voltage is equal to V_{REF}. For example, when V_{IN-} = 0 V, and $V_{IN+} = V_{REF}$ = 3.3 V, the charge transfer per sample is 5.6 pC into the IN− input and out of the IN+ input. The steady-state input current is, therefore, also linearly related to input voltage, as shown in Figure 20. Settling error with the AD4052/AD4058, therefore, appears as additional gain error rather than degradation in INL and THD.

An RC kickback filter is recommended on each of the IN+ and IN− pins to attenuate the voltage glitch on the output of the AFE circuit (see Figure 72). The Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter article provides guidance for selecting the RC components of the kickback filter to ensure proper settling. Table 19 provides general RC component recommendations for the AD4052/AD4058 for several sample rates (R_{FILT} and C_{FILT} are the resistor and capacitor values in the RC kickback filter, respectively). The values in Table 19 are provided for initial guidance, and the system designer must verify the companion amplifier is stable driving these RC loads.

The AD4052/AD4058 LTspice model emulates the equivalent analog input model shown in Figure 74 when configured for transient simulations.

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APPLICATIONS INFORMATION

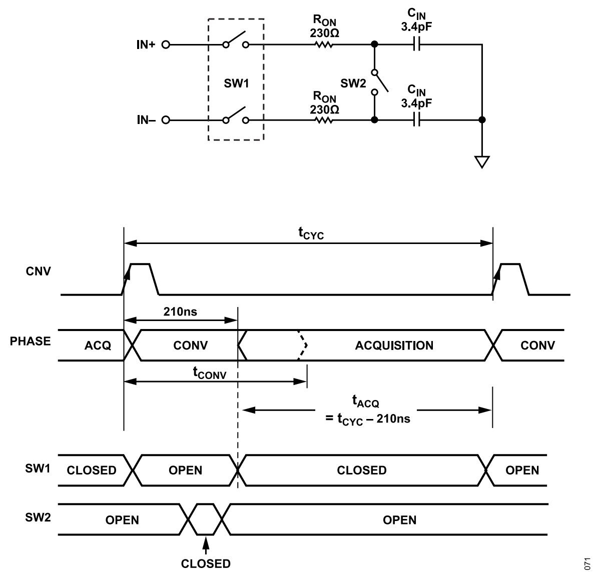

Figure 74. AD4052/AD4058 Equivalent Input Load Model

Table 19. AD4052/AD4058 RC Kickback Filter Recommendations

Sample Rate	t_{ACQ}	R_{FILT}	C_{FILT}	−3 dB Bandwidth
2 MSPS	290 ns	52.3 Ω	1 nF	3.04 MHz
		124 Ω	360 pF	3.57 MHz
1 MSPS	790 ns	143 Ω	1 nF	1.11 MHz
		332 Ω	360 pF	1.33 MHz
500 kSPS	1790 ns	301 Ω	1 nF	528.75 kHz
		634 Ω	360 pF	697.31 kHz
100 kSPS	9790 ns	1.78 kΩ	1 nF	89.4 kHz
		4.12 kΩ	360 pF	107.3 kHz

Noise and Distortion Considerations

The noise and distortion specifications of the AFE circuit must be considered, because they combine with the AD4052/AD4058 noise and distortion specifications to determine the overall system performance. The total system noise ($v_{N,TOTAL}$) is the root sum of squares (RSS) of the AFE RMS noise ($v_{N, AFE}$) and ADC RMS noise ($v_{N,ADC}$), referred to the inputs of the AD4052/AD4058 as shown the following equation:

$$v_{N,TOTAL} = \sqrt{v_{N,AFE}^{\,2} + v_{N,ADC}^{\,2}} \quad (9)$$

MT-049 and MT-050 describe how to estimate $v_{N,AFE}$ for operational amplifier circuits, as a function of the amplifier and passive component noise specifications and amplifier configuration. The *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter* article describes how to estimate system SNR vs. $v_{N,AFE}$ and $v_{N,ADC}$.

As noted in the AD4052/AD4058 Equivalent Analog Input Model section, the primary purpose of the RC kickback filter between the AFE and the ADC is to minimize settling error and not to filter AFE noise or perform anti-aliasing. The RC kickback filter bandwidth cannot be set arbitrarily low, and it is recommended to implement any additional noise or anti-alias filtering before or within the amplifier circuit instead of the RC kickback filter. NP0/C0G type dielectric capacitors are recommended for all capacitors used in the AFE circuit to minimize signal distortion artifacts caused by capacitor voltage and temperature derating.

REFERENCE CIRCUIT DESIGN

Equivalent REF Input Model

The AD4052/AD4058 require an external voltage reference to define the input range of the device. A low-noise, stable reference is critical for maximizing accuracy and performance.

The AD4052/AD4058 REF pin draws charge (Q_{CONV}) from the external reference circuit during each conversion phase to perform the SAR ADC bit trials. The REF input current (I_{REF}) can, therefore, be expressed as a transient current load that occurs once per conversion and as an equivalent average DC current load that is a function of the sample rate (see Table 1 and Figure 21). The

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voltage reference circuit must maintain a stable and accurate V_{REF} voltage, despite the charge transient from the AD4052/AD4058 REF pin, to prevent gain error or stuck bits in the conversion results.

A reference decoupling capacitor (C_{REF}) is strongly recommended to supply the instantaneous charge drawn by the REF pin while maintaining the V_{REF} voltage to within an LSB. For optimal performance, populate C_{REF} with a 2.2 µF capacitor with a case size of 0402 or larger to ensure suitable capacitor voltage coefficient. For space-constrained applications, a 1 µF capacitor in a case size of 0201 may be used with slight degradation to gain error and INL. Place the C_{REF} capacitor on the same PCB layer and as close to the REF pin as possible with a wide trace to minimize series impedance (see the Layout Recommendations section).

While the AD4052/AD4058 is idling (not performing conversions), the REF pin draws only a small standby current (8 nA). In applications where the AD4052/AD4058 intermittently switches between idling and performing bursts of conversions (for example, when using burst averaging mode), the I_{REF} quickly shifts from near-zero current to 60 µA/15 µA for f_S = 2 MSPS/ 500 kSPS. This step in load current triggers an output load transient response in the reference circuit that must be considered if V_{REF} varies by more than ½ LSB. The MAX6070 voltage reference is recommended for its exceptional transient response with low power dissipation. Figure 75 illustrates the transient loading effects on the reference circuit in response to a burst of conversions.

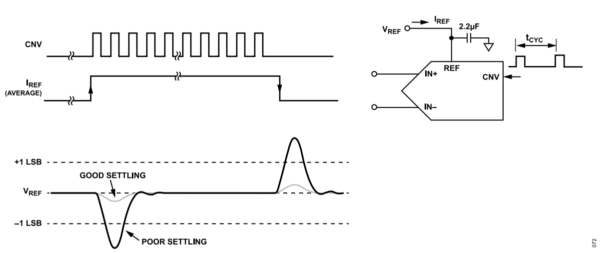

Figure 75. Burst Sampling and Voltage Reference Settling

Reference Noise Considerations

The voltage reference circuit noise is critical for achieving the system-level dynamic range and SNR target specifications. For large input signals near full scale, any noise from the reference circuit will couple into the conversion results and modulate around the fundamental frequency. Reference noise will also limit the SNR and resolution improvements gained from using high averaging ratios in averaging mode and burst averaging mode.

SYNCHRONIZED AMPLIFIER SHUTDOWN AND ADC SAMPLING

The DEV_EN signal is an amplifier power-down signal generated by the AD4052/AD4058 and synchronized to the ADC to maximize amplifier power-up settling time prior to the sampling instant. Figure 44 shows a typical connection diagram when using the AD4052/AD4058 DEV_EN signal with an operational amplifier. The DEV_EN signal is assigned to the GP0 output pin in this example.

As described in the Device Enable Signal section, the DEV_EN signal is asserted following the CNV signal rising edge to enable the connected amplifier. The sampling instant is delayed until the user-programmable t_{PWR_ON} delay elapses. After the t_{PWR_ON} delay elapses, the DEV_EN signal is deasserted to power down the amplifier. Consult the amplifier data sheet for its shutdown pin logic levels to ensure compatibility with the AD4052/AD4058 logic levels that are set by the VIO voltage and given in Table 1.

To ensure the amplifier output settles before the ADC sampling instant, set the t_{PWR_ON} delay to be longer than the amplifier turn-on time specification. Turn-on time indicates the time needed for the amplifier output to settle to a specified accuracy following assertion of its ENABLE/$\overline{\text{SHUTDOWN}}$ input. Note that turn-on time varies for different loads and amplifier configurations. The *Introduction to Dynamic Power Scaling* article provides guidance on configuring and evaluating operational amplifier power cycling relative to the SAR ADC sampling.

See Figure 55 and Figure 57 for timing diagrams using DEV_EN in the various AD4052/AD4058 operating modes.

ACHIEVING HIGH ACCURACY WITH REFERENCE SHUTDOWN

Low-noise, high-accuracy voltage references are generally recommended to pair with precision SAR ADCs to maximize system-level performance. The voltage reference circuit also needs to have low output impedance and fast transient response to deal with the SAR ADC REF input transient load, especially when performing bursts of samples (see the Reference Circuit Design section). Low-power voltage references generally cannot satisfy all of these requirements simultaneously, which often forces system designers to add a reference buffer amplifier, increasing overall system power dissipation.

The MAX6070 is an exceptionally low-power voltage reference that can drive the AD4052/AD4058 REF pin directly without an intermediate reference buffer amplifier. For extremely power-sensitive applications, however, the AD4052/AD4058 offer unique features that allow the voltage reference to be disabled without degrading precision.

The AD4052/AD4058 can select the VDD supply as the V_{REF} source, as described in the Reference Selection Modes section. To maintain accuracy while using VDD as the V_{REF}, the AD4052/AD4058 can directly measure the ratio between the VDD supply and the REF input voltages and calculate a corresponding digital correction factor to automatically scale the ADC samples accordingly. The digital correction uses the MON_VAL field described in the Gain Scaling section to scale the ADC transfer function between the REF and VDD domains.

The automatic MON_VAL scaling calculation consist of two phases. Figure 76 illustrates the AD4052/AD4058 configuration while meas-

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uring and calculating the MON_VAL digital correction factor. Figure 77 shows the configuration after MON_VAL is updated and the AD4052/AD4058 begin sampling the inputs with VDD as the V_{REF} source. Table 20 gives the relevant configuration settings for both phases.

In the MON_VAL calculation phase, the REF pin is driven by an accurate voltage reference, like the MAX6070, and the REF pin is selected as the V_{REF} source. The VDD voltage is internally scaled by ½ and sampled by the ADC. A CNV rising edge triggers a burst of samples in burst averaging mode. When the averaged result is generated, the AD4052/AD4058 automatically calculate a 16-bit digital correction factor and load it into the MON_VAL field. The $\overline{\text{RDY}}$ signal can optionally be assigned to the GP0 or GP1 pins to indicate when the calculation is complete.

In the MON_VAL application phase, the ADC is reconfigured to sample the input signal via the IN+ and IN− pins, with VDD selected as the V_{REF} source. The external voltage reference is powered down to reduce system power. When the ADC samples the inputs, the MON_VAL scaling factor is applied to the digital output codes to scale them to the transfer function set by the REF voltage instead of the VDD voltage.

Depending on the stability of the VDD supply circuit, the MON_VAL calculation may need to be repeated periodically to maintain system accuracy targets.

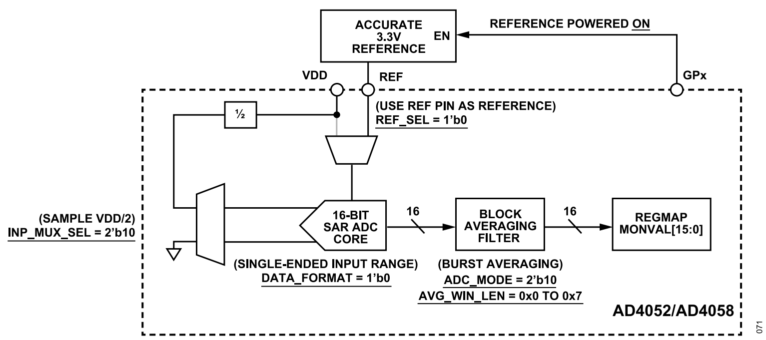

Figure 76. MON_VAL Calculation Configuration

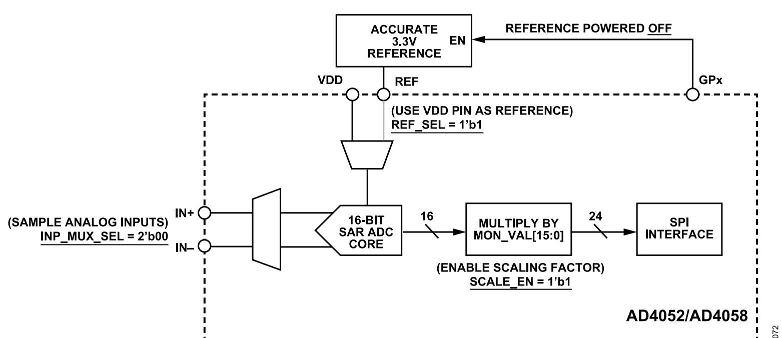

Figure 77. MON_VAL Application Configuration

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Table 20. Configuration Settings for MON_VAL Scaling

Bit Field Name	MON_VAL Calculation	MON_VAL Application
REF_SEL	1'b0: V_{REF} = REF	1'b1: V_{REF} = VDD
DATA_FORMAT	1'b0: Single-ended mode	Don't care
INP_MUX_SEL	2'b10: Sample VDD/2	2'b00: Sample IN+ and IN−
ADC_MODE	2'b10: Burst averaging mode	Don't care
AVG_WIN_LEN	Don't care[1]	Don't care
SCALE_EN	1'b0: Scaling disabled	1'b1: Scaling enabled
GP0_SEL	3'b010: $\overline{\text{RDY}}$ on GP0[2]	Don't care
GP1_SEL	3'b110: Logic high on GP1[3]	3'b011: Logic low on GP1[3]

[1] MON_VAL calculations do not require a specific value for N_{AVG}, but it is recommended to set N_{AVG} based on the VDD supply circuit noise and the system accuracy targets.

[2] Optional. The $\overline{\text{RDY}}$ signal can act as a hardware interrupt to notify the digital host when MON_VAL calculation is complete.

[3] Optional. The static logic levels can act as the voltage reference enable pin if its input logic levels are consistent with the AD4052/AD4058 output logic levels.

VDD POWER DISSIPATION

SAR ADCs such as the AD4052/AD4058 are ideal for precision measurement applications with tight power dissipation budgets. The ADC core is effectively duty-cycled and only consumes active power while performing a conversion, so the effective power dissipation is lower at slower sample rates. Figure 78 illustrates the instantaneous and average VDD input current (I_{DD}) vs. ADC sampling. Table 1 gives the average supply current and power dissipation for several operating modes and sample rates.

The AD4052/AD4058 ADC core is exceptionally power efficient and can operate in several lower power operating modes. As described in the Analog Front-End Design section, slower sampling rates also relax the load drive requirements for the AFE and reference circuitry, allowing the AD4052/AD4058 to interface with low-power amplifiers and voltage references for overall system power optimization.

While the AD4052/AD4058 is idle, VDD draws only 990 nA standby current (see Figure 32). In sample mode and averaging mode, the AD4052/AD4058 average VDD current is 0.4 mA at 1 MSPS, and 0.2 mA at 500 kSPS, equivalent to 400 pC per conversion. In the autonomous modes, the VDD current is reduced to 112 µA at 1 MSPS, and 56 µA at 500 kSPS, equivalent to 112 pC per comparison operation. Figure 24 and Figure 27 show the average I_{DD} and power dissipation vs. the ADC sample rate and operating mode. The supply current and power dissipation scale linearly with the sample rate.

In burst averaging mode, the AD4052/AD4058 performs a burst of conversions to generate an averaged result. The average power dissipation in burst averaging mode is, therefore, a function of the average number of conversions performed per second over many bursts of samples. This is a function of the burst sampling rate, N_{AVG}, and the period of the CNV signal. Figure 79 illustrates the VDD power dissipation over the burst sampling and idle phases in burst averaging mode.

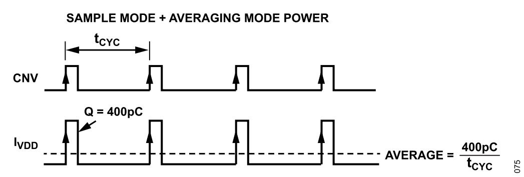

Figure 78. I_{DD} vs. Conversion Periods in Sample Mode and Averaging Mode

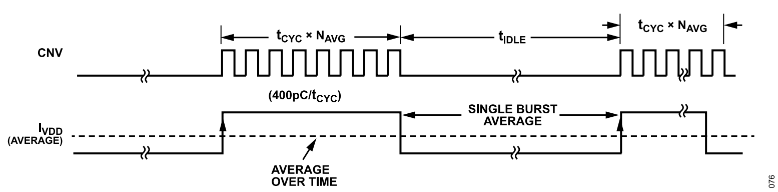

Figure 79. I_{DD} vs. Burst Conversions in Burst Averaging Mode

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CALCULATING SERIAL INTERFACE OUTPUT DATA RATE

The AD4052/AD4058 ADC core performance is specified for f_S up to 2 MSPS/500 kSPS, but the maximum achievable output data rate (f_{ODR_MAX}) is a function of the serial interface specifications and may limit the practical f_S. In sample mode and averaging mode, for example, the digital host must read the entire ADC result between the end of the previous conversion and the start of the next conversion, or else the result is lost. Therefore, the maximum f_S and the minimum sample period (t_{CYC}) for a given application using these modes is a function of the AD4052/AD4058 and digital host timing specifications.

In burst averaging mode and the autonomous modes, the ADC sampling rate is set by the internal timer (see the Internal Timer section). The serial interface does not limit the sampling rate in these modes because the digital host does not have to read out an entire sample within one conversion period.

Figure 80 illustrates the timing restrictions for reading out ADC data in sample mode and averaging mode. The minimum t_{CYC} for sample mode and averaging mode can be estimated with the following equations:

$$t_{CYC\_MIN} = t_{CONV} + t_{EN} + t_{QUIET} + t_{SCLK} \times (N_{BITS} - 1/2) \quad (10)$$

$$f_{ODR\_MAX} = \frac{1}{t_{CYC\_MIN}} \quad (11)$$

where:
t_{CYC_MIN} is the minimum achievable sample period.
f_{ODR_MAX} is the maximum achievable output data rate.
t_{CONV} is the maximum conversion time specification.
t_{EN} is the maximum delay between $\overline{CS}$ falling edge and valid data on SDO.
t_{QUIET} is the minimum quiet time specification.
t_{SCLK} is the serial clock period.
N_{BITS} is the length of the ADC data packet in bits.

The default values for N_{BITS} are 16 bits for sample mode and 20 bits for averaging mode (see the ADC Mode Output Data Format section for all options of N_{BITS} for each operating mode).

The AD4052/AD4058 uses SPI Mode 0 (CPOL = CPHA = 0), so the MSB is launched on the SDO pin following each $\overline{CS}$ falling edge, with a delay given by the t_{EN} specification. Equation 10 assumes the first SCLK rising edge occurs as quickly as possible while adhering to the t_{EN} specification, but the $\overline{CS}$ falling edge to SCLK rising edge delay may vary between digital hosts.

The fastest (minimum) t_{SCLK} periods in Table 5 and Table 6 are only achievable for digital hosts that can latch SDO data on the falling edge of SCLK, such as FPGAs, because the maximum t_{DSDO} delay is longer than half of the minimum t_{SCLK} specification. For standard microcontrollers interfacing with the AD4052/AD4058, data are latched on the SCLK rising edges, so the minimum practical t_{SCLK} is at least 2 × t_{DSDO}. Table 21 provides examples of f_{ODR_MAX} using Equation 10 and Equation 11 and assuming t_{SCLK} = 2 × t_{DSDO} instead of the minimum t_{SCLK} specifications in the Timing Specifications.

Note that the t_{DSDO} delay is specified for a C_{LOAD} of 20 pF. The estimates in Table 21 do not account for differences in C_{LOAD}, the setup and hold time specifications of the digital host SPI, or additional sources of delay within the digital host SPI transactions (for example, delays to transfer SPI data buffer contents to other peripherals or the latency of its interrupt handler). The practical serial clock rate varies between applications and must be independently verified.

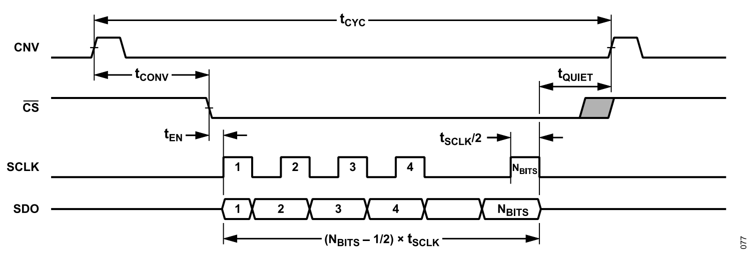

Figure 80. Sample Mode and Averaging Mode Serial Interface Readback Timing

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Table 21. Serial Interface Output Data Rate Examples

VIO Range	Example f_{SCLK}[1]	N_{BITS}	f_{ODR_MAX}
VIO ≥ 3 V	62.5 MHz	16	1.69 MSPS
		24	1.39 MSPS
		32	1.18 MSPS
		40	1.02 MSPS
3 V > VIO ≥1.7 V	33.3 MHz	16	1.22 MSPS
		24	947 kSPS
		32	772 kSPS
		40	650 kSPS

[1] The example f_{SCLK} in this table correspond to t_{SCLK} = 2 × t_{DSDO}, where t_{DSDO} is the maximum data valid delay given in Table 5 and Table 6.

LAYOUT RECOMMENDATIONS

The following PCB layout guidelines are recommended to maximize performance using the AD4052/AD4058:

- Include a solid ground plane in the PCB layer underneath the AD4052/AD4058. Ensure there are low-impedance connections between the AD4052/AD4058 GND pins and the ground plane layer.
- Ensure the analog input and REF traces are physically separated from the digital interface traces to minimize crosstalk from digital signal edges. Include a GND fill between the analog and digital traces. Avoid routing the digital interface traces underneath the AD4052/AD4058 or the analog signal traces without including a solid ground plane layer in between.
- Ensure the impedance between the voltage reference circuitry and the AD4052/AD4058 REF pin is as low as possible to prevent V_{REF} settling issues. Place a low effective series resistance (ESR) decoupling capacitor as close to the AD4052/AD4058 REF pin as possible (see the Reference Circuit Design section). Use wide traces between the voltage reference and the AD4052/AD4058 REF pin.
- Place the RC kickback filter capacitors as close to the IN+ and IN− pins as possible (see the Analog Front-End Design section).
- Place the supply decoupling capacitors as close to the VDD, CLDO, and VIO pins as possible (see the Power Supplies section).

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REGISTER SUMMARY

The AD4052/AD4058 has programmable user registers for configuring the device. These registers are accessible while the AD4052/AD4058 is in configuration mode. Table 22 shows an overview of the AD4052/AD4058 user register map, and the Register Details section details the location and functions of the bit fields in each register. The access column in the various register details tables specifies whether the bit fields are read-only (R), read/write (R/W), or write-1-to-clear (R/W1C) bits.

Table 22. AD4052/AD4058 Register Summary

Address	Name	Description	Reset	Access
0x00	INTERFACE_CONFIG_A	Interface Configuration A.	0x10	R/W
0x01	INTERFACE_CONFIG_B	Interface Configuration B.	0x08	R/W
0x02	DEVICE_CONFIG	Device Configuration.	0xF0	R/W
0x03	DEVICE_TYPE	Device Type.	0x07	R
0x04	PRODUCT_ID_L (AD4052)	Product Identification (LSByte).	0x72	R
0x04	PRODUCT_ID_L (AD4058)	Product Identification (LSByte).	0x78	R
0x05	PRODUCT_ID_H	Product Identification (MSByte).	0x00	R
0x06	DEVICE_GRADE	Device Grade.	0x00	R
0x0A	SCRATCH_PAD	Scratch Pad.	0x00	R/W
0x0B	SPI_REVISION	SPI Revision.	0x84	R
0x0C	VENDOR_L	Vendor Identification (LSByte).	0x56	R
0x0D	VENDOR_H	Vendor Identification (MSByte).	0x04	R
0x0E	STREAM_MODE	Reserved.	0x00	R/W
0x0F	TRANSFER_CONFIG	Reserved.	0x00	R/W
0x10	INTERFACE_CONFIG_C	Interface Configuration C.	0x13	R/W
0x11	INTERFACE_STATUS	Interface Status.	0x00	R/W
0x12 to 0x1F	RESERVED	Reserved.	0x00	R
0x20	MODE_SET	Device Mode Select.	0x00	R/W
0x21	ADC_MODES	ADC Operating Mode Configuration.	0x80	R/W
0x22	ADC_CONFIG	ADC Setup Configuration.	0x00	R/W
0x23	AVG_CONFIG	Averaging Filter Configuration.	0x00	R/W
0x24	GP_CONFIG	General Purpose Pin Configuration.	0xF0	R/W
0x25	INTR_CONFIG	Interrupt Configuration.	0x21	R/W
0x26	CHOP_CONFIG	Chop Signal Configuration.	0x00	R/W
0x27	TIMER_CONFIG	Timer Configuration.	0x00	R/W
0x28	MAX_LIMIT_REG[7:0]	Maximum Threshold Configuration.	0x0000	R/W
0x29	MAX_LIMIT_REG[15:8]			
0x2A	MIN_LIMIT_REG[7:0]	Minimum Threshold Configuration.	0x0000	R/W
0x2B	MIN_LIMIT_REG[15:8]			
0x2C	MAX_HYST_REG	Maximum Threshold Hysteresis.	0x00	R/W
0x2D	MIN_HYST_REG	Minimum Threshold Hysteresis.	0x00	R/W
0x2E	MON_VAL_REG[7:0]	MON_VAL Scaling.	0x0000	R/W
0x2F	MON_VAL_REG[15:8]			
0x30 to 0x3F	RESERVED	Reserved.	0x00	R
0x40	FUSE_CRC	Fuse CRC.	0x00	R/W
0x41	DEVICE_STATUS	Device Status.	0x40	R/W
0x42	MAX_SAMPLE_REG[7:0]	Maximum Interrupt Sample.	0x0000	R
0x43	MAX_SAMPLE_REG[15:8]			
0x44	MIN_SAMPLE_REG[7:0]	Minimum Interrupt Sample.	0x0000	R
0x45	MIN_SAMPLE_REG[15:8]			

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REGISTER DETAILS

INTERFACE CONFIGURATION A REGISTER

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

Interface Configuration Settings

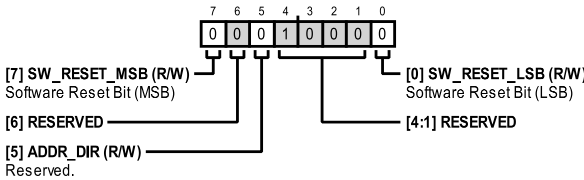

Table 23. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET_MSB	Software Reset Bit (MSB). Set both SW_RESET_MSB and SW_RESET_LSB to 1 in the same register write to initiate a software reset of the device.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_DIR	Reserved. This bit must be set to 0. The ADDR_DIR bit is not reset by software resets, and it must be reset by the software reset pattern or power-on reset.	0x0	R/W
[4:1]	RESERVED	Reserved.	0x8	R
0	SW_RESET_LSB	Software Reset Bit (LSB). Set both SW_RESET_MSB and SW_RESET_LSB to 1 in the same register write to initiate a software reset of the device.	0x0	R/W

INTERFACE CONFIGURATION B REGISTER

Address: 0x01, Reset: 0x08, Name: INTERFACE_CONFIG_B

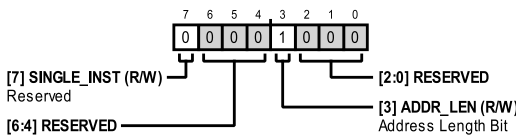

Table 24. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Reserved. This bit must be set to 0.	0x0	R/W
[6:4]	RESERVED	Reserved.	0x0	R
3	ADDR_LEN	Address Length Bit. Sets the length of the register address in the instruction phase to 7 or 15 bits. 0: 15-Bit Addressing. 1: 7-Bit Addressing.	0x1	R/W
[2:0]	RESERVED	Reserved.	0x0	R

DEVICE CONFIGURATION REGISTER

Address: 0x02, Reset: 0xF0, Name: DEVICE_CONFIG

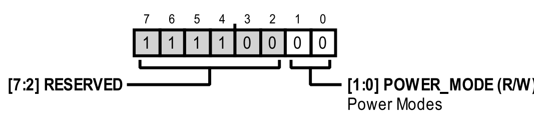

Table 25. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x3C	R
[1:0]	POWER_MODE	Power Modes.	0x0	R/W

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REGISTER DETAILS

Table 25. Bit Descriptions for DEVICE_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
		0x0: Active Mode. 0x1: Invalid. 0x2: Invalid. 0x3: Sleep Mode (Low Power).		

DEVICE TYPE REGISTER

Address: 0x03, Reset: 0x07, Name: DEVICE_TYPE

Indicates the type of device (precision ADC). The device type register is used in conjunction with the product identification registers to identify the AD4052/AD4058 from other Analog Devices, Inc., products.

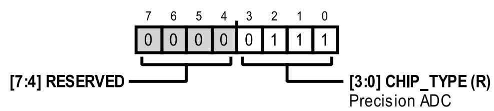

Table 26. Bit Descriptions for DEVICE_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

PRODUCT IDENTIFICATION (LSBYTE) REGISTER

Address: 0x04, Reset: 0x70, Name: PRODUCT_ID_L

Least significant byte of the unique product identification bit field. The product identification registers are used in conjunction with the device type register to identify the AD4052/AD4058 from other Analog Devices products.

Table 27. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0] (AD4052)	Product Identification Field. The unique PRODUCT_ID value for the AD4052 is 0x0072.	0x72	R
[7:0]	PRODUCT_ID[7:0] (AD4058)	Product Identification Field. The unique PRODUCT_ID value for the AD4058 is 0x0078.	0x78	R

PRODUCT IDENTIFICATION (MSBYTE) REGISTER

Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Most significant byte of the unique product identification bit field. The product identification registers are used in conjunction with the device type register to identify the AD4052/AD4058 from other Analog Devices products.

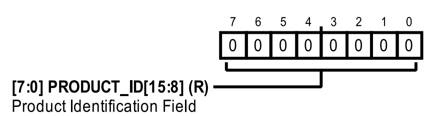

Table 28. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product Identification Field. The unique PRODUCT_ID value for the AD4052/AD4058 is .	0x0	R

DEVICE GRADE REGISTER

Address: 0x06, Reset: 0x00, Name: DEVICE_GRADE

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REGISTER DETAILS

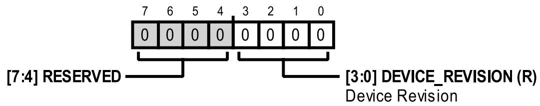

Table 29. Bit Descriptions for DEVICE_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision. Indicates the device hardware revision.	0x0	R

SCRATCH PAD REGISTER

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Interface read/write test register.

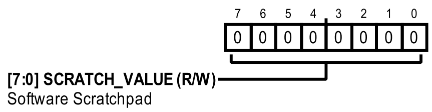

Table 30. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Use this register to test SPI communications with the device. Values written to this register have no impact on device behavior.	0x0	R/W

VENDOR IDENTIFICATION (LSBYTE) REGISTER

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

Indicates Analog Devices as the vendor for the device. The vendor identification register is used in conjunction with the product identification registers to identify the AD4052/AD4058 from other Analog Devices products.

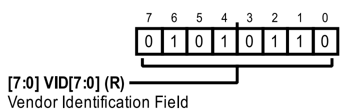

Table 31. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor Identification Field. The VID[15:0] field is the same value (0x0456) for all Analog Devices precision ADCs.	0x56	R

VENDOR IDENTIFICATION (MSBYTE) REGISTER

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

Indicates Analog Devices as the vendor for the device. The vendor identification register is used in conjunction with the product identification registers to identify the AD4052/AD4058 from other Analog Devices products.

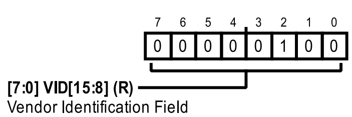

Table 32. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor Identification Field. The VID[15:0] field is the same value (0x0456) for all Analog Devices precision ADCs.	0x04	R

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REGISTER DETAILS

RESERVED REGISTERS

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

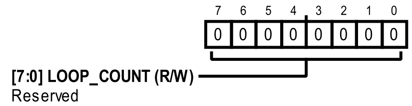

Table 33. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Reserved. This bit field must be set to 0x00.	0x0	R/W

Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

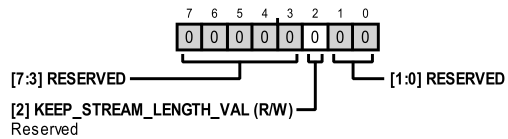

Table 34. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	Reserved. This bit must be set to 0.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

INTERFACE CONFIGURATION C REGISTER

Address: 0x10, Reset: 0x13, Name: INTERFACE_CONFIG_C

Additional interface configuration settings.

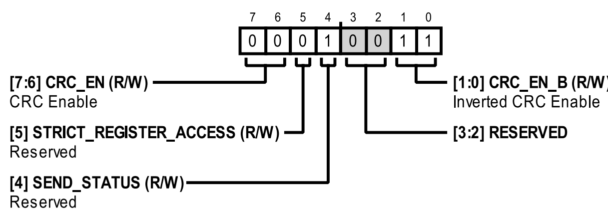

Table 35. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_EN	CRC Enable. Set CRC_EN to 0x1 and CRC_EN_B to 0x2 in the same register write to enable interface CRC. 0: CRC Disabled. 1: CRC Enabled. Enables CRC if CRC_EN_B = 0x2.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Reserved. This bit must be set to 0.	0x0	R/W
4	SEND_STATUS	Reserved. This bit must be set to 1.	0x1	R/W
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	CRC_EN_B	Inverted CRC Enable. To enable CRC, write as the inverted value of CRC_ENABLE.	0x3	R/W

INTERFACE STATUS REGISTER

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS

Status bits indicating errors in register reads and/or writes in configuration mode. The interface status bits are active high and are cleared by writing a 1 to their corresponding bit locations.

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REGISTER DETAILS

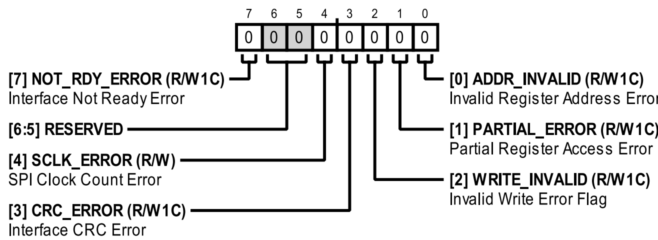


Table 36. Bit Descriptions for INTERFACE_STATUS

Bits	Bit Name	Description	Reset	Access
7	NOT_RDY_ERROR	Interface Not Ready Error. This error bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization. For example, before a device reset is complete.	0x0	R/W1C
[6:5]	RESERVED	Reserved.	0x0	R
4	SCLK_ERROR	SPI Clock Count Error. This error bit is set when an incorrect number of serial clock periods is received in a configuration mode SPI transaction. For example, if the data phase does not contain an integer multiple of 8 SCLK periods.	0x0	R/W
3	CRC_ERROR	Interface CRC Error. This error bit is set when the device receives an invalid CRC checksum value on SDI (in configuration mode). This error bit is only active when CRC is enabled.	0x0	R/W1C
2	WRITE_INVALID	Invalid Write Error Flag. This error bit is set to 1 when the digital host attempts a register write to a register that contains exclusively read-only bits.	0x0	R/W1C
1	PARTIAL_ERROR	Partial Register Access Error. This error bit is set to 1 when the digital host fails to read or write from both bytes of a 2-byte register (in configuration mode). For example, terminating a read from the MAX_LIMIT_REG register after reading only 1 of its 2 bytes.	0x0	R/W1C
0	ADDR_INVALID	Invalid Register Address Error. This error bit is set to 1 when the digital host attempts to read from or write to an undefined register address.	0x0	R/W1C

DEVICE MODE SELECT REGISTER

Address: 0x20, Reset: 0x00, Name: MODE_SET

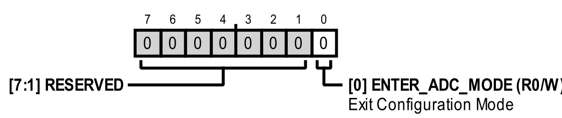
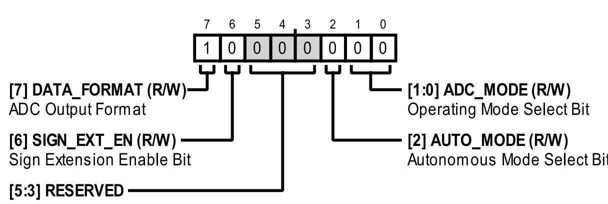


Table 37. Bit Descriptions for MODE_SET

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ENTER_ADC_MODE	Exit Configuration Mode. Write 1 to exit configuration mode at the next CSB rising edge. The device enters the operating mode selected by the ADC_MODE and AUTO_MODE bits. This bit is cleared automatically by the exit command.	0x0	R0/W

ADC OPERATING MODE CONFIGURATION REGISTER

Address: 0x21, Reset: 0x80, Name: ADC_MODES



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REGISTER DETAILS

Table 38. Bit Descriptions for ADC_MODES

Bits	Bit Name	Description	Reset	Access
7	DATA_FORMAT	ADC Output Format. 0: Straight Binary (Unsigned). 1: Twos Complement (Signed).	0x1	R/W
6	SIGN_EXT_EN	Sign Extension Enable Bit. Set this bit to enable the sign extension byte on ADC read data.	0x0	R/W
[5:4]	RESERVED	Reserved. Must be set to 0x0.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	AUTO_MODE	Autonomous Mode Select Bit. 0: Monitor Mode. 1: Trigger Mode.	0x0	R/W
[1:0]	ADC_MODE	Operating Mode Select Bit. 0x0: Sample Mode. 0x1: Burst Averaging Mode. 0x2: Averaging Mode. 0x3: Autonomous Mode. Select between monitor and trigger modes via the AUTO_MODE bit.	0x0	R/W

ADC SETUP CONFIGURATION REGISTER

Address: 0x22, Reset: 0x00, Name: ADC_CONFIG

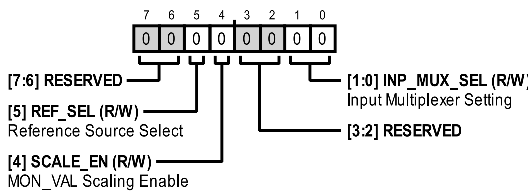
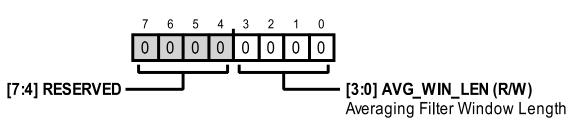


Table 39. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REF_SEL	Reference Source Select. Selects which pin is used as the ADC reference source. 0: REF. 1: VDD.	0x0	R/W
4	SCALE_EN	MON_VAL Scaling Enable. MON_VAL scaling is enabled when SCALE_EN is set to 1 while the input multiplexer is configured to monitor the analog inputs (see the INP_MUX_SEL bit).	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	INP_MUX_SEL	Input Multiplexer Setting. 0x0: Analog Inputs. ADC connected to analog inputs (IN+ and IN−). 0x1: Invalid. 0x2: VDD/2. ADC monitors the VDD supply voltage scaled by ½ . This setting is used to determine the ratio of REF to VDD and to set the MON_VAL scaling factor accordingly. 0x3: Invalid.	0x0	R/W

AVERAGING FILTER CONFIGURATION REGISTER

Address: 0x23, Reset: 0x00, Name: AVG_CONFIG



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REGISTER DETAILS

Table 40. Bit Descriptions for AVG_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	AVG_WIN_LEN	Averaging Filter Window Length. Sets the averaging ratio for averaging and burst averaging modes. The averaging ratio ranges from 2 to 4096 in powers of 2. 0x0: 2. 0x1: 4. 0x2: 8. 0x3: 16. 0x4: 32. 0x5: 64. 0x6: 128. 0x7: 256. 0x8: 512. 0x9: 1024. 0xA: 2048. 0xB: 4096.	0x0	R/W

GENERAL PURPOSE PIN CONFIGURATION REGISTER

Address: 0x24, Reset: 0xF0, Name: GP_CONFIG

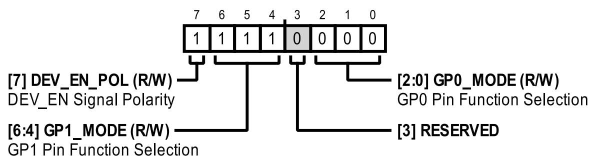

Table 41. Bit Descriptions for GP_CONFIG

Bits	Bit Name	Description	Reset	Access
7	DEV_EN_POL	DEV_EN Signal Polarity. Sets the polarity of the DEV_EN signal for compatibility with active high and active low amplifier enable pins. 0: DEV_EN Active Low. 1: DEV_EN Active High (Default).	0x1	R/W
[6:4]	GP1_MODE	GP1 Pin Function Selection. 0x0: Disabled/High-Z. 0x1: GP1_INTR Signal. 0x2: Data Ready Signal. 0x3: DEV_EN Signal. 0x4: CHOP Signal. 0x5: Static Logic Low (GND). 0x6: Static Logic High (VIO). 0x7: DEV_RDY Signal (Default).	0x7	R/W
3	INVERT_ON_CHOP	Invert on Chop Enable or Disable control. 0: Invert on Chop Disabled 1: Invert on Chop Enabled	0x0	R/W
[2:0]	GP0_MODE	GP0 Pin Function Selection. 0x0: Disabled/High-Z (Default). 0x1: GP0_INTR Signal. 0x2: Data Ready Signal. 0x3: DEV_EN Signal. 0x4: CHOP Signal.	0x0	R/W

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REGISTER DETAILS

Table 41. Bit Descriptions for GP_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
		0x5: Static Logic Low. 0x6: Static Logic High. 0x7: Invalid.		

NOTE - The CHOP signal and the DEV_EN signal cannot be enabled at the same time.

INTERRUPT CONFIGURATION REGISTER

Address: 0x25, Reset: 0x21, Name: INTR_CONFIG

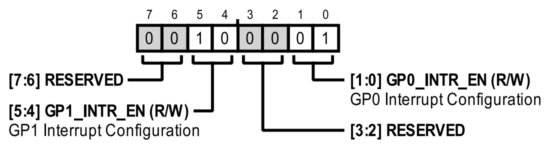
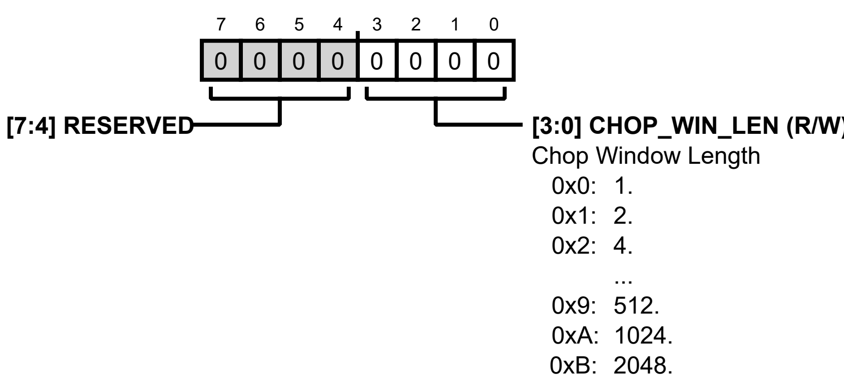


Table 42. Bit Descriptions for INTR_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	GP1_INTR_EN	GP1 Interrupt Configuration. Selects which of the threshold detection interrupt signals are passed through to the GP1_INTR output signal. 0x0: Neither Interrupt. 0x1: MIN_INTR. 0x2: MAX_INTR. 0x3: Either Interrupt. GP1 outputs the logical OR of MAX_INTR and MIN_INTR signals.	0x2	R/W
[3:2]	RESERVED	Reserved.	0x0	R
[1:0]	GP0_INTR_EN	GP0 Interrupt Configuration. Selects which of the threshold detection interrupt signals are passed through to the GP0_INTR output signal. 0x0: Neither Interrupt. 0x1: MIN_INTR. Default. 0x2: MAX_INTR. 0x3: Either Interrupt. GP0 outputs the logical OR of MAX_INTR and MIN_INTR signals.	0x1	R/W

CHOP SIGNAL CONFIGURATION REGISTER

Address: 0x26, Reset: 0x00, Name: CHOP_CONFIG



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REGISTER DETAILS

Table 43. Bit Descriptions for CHOP_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHOP_WIN_LEN	Chop Window Length. Sets the number of ADC samples taken before switching the CHOP signal state. Set CHOP_WIN_LEN to implement the desired ratio of the CHOP signal period and ADC sampling period. 0x0: 1. 0x1: 2. 0x2: 4. 0x3: 8. 0x4: 16. 0x5: 32. 0x6: 64. 0x7: 128. 0x8: 256. 0x9: 512. 0xA: 1024. 0xB: 2048.	0x0	R/W

TIMER CONFIGURATION REGISTER

Address: 0x27, Reset: 0x00, Name: TIMER_CONFIG

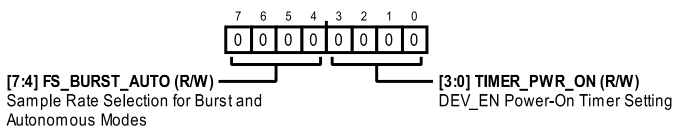

Table 44. Bit Descriptions for TIMER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:4]	FS_BURST_AUTO [1]	Sample Rate Selection for Burst and Autonomous Modes. 0x0: 2 MSPS. 0x1: 1 MSPS. 0x2: 300 kSPS. 0x3: 100 kSPS. 0x4: 33.3 kSPS. 0x5: 10 kSPS. 0x6: 3 kSPS. 0x7: 1 kSPS. 0x8: 500 SPS. 0x9: 333 SPS. 0xA: 250 SPS. 0xB: 200 SPS. 0xC: 166 SPS. 0xD: 140 SPS. 0xE: 125 SPS. 0xF: 111 SPS.	0x0	R/W
[3:0]	TIMER_PWR_ON	DEV_EN Power-On Timer Setting. Selects the delay between DEV_EN assertion and ADC sampling instant when DEV_EN is selected for either GP0 or GP1 pins. 0x0: 500 ns. 0x1: 1 µs. 0x2: 3.3 µs. 0x3: 10 µs.	0x0	R/W

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REGISTER DETAILS

Table 44. Bit Descriptions for TIMER_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
		0x4: 30 μs. 0x5: 100 μs. 0x6: 330 μs. 0x7: 1 ms. 0x8: 2 ms. 0x9: 3 ms. 0xA: 4 ms. 0xB: 5 ms. 0xC: 6 ms. 0xD: 7 ms. 0xE: 8 ms. 0xF: 9 ms.		

[1] NOTE that the 2 MSPS and 1 MSPS settings are invalid for the AD4058. On the AD4058, the FS_BURST_AUTO register must be updated accordingly before entering the burst averaging mode or the autonomous modes.

MAXIMUM THRESHOLD CONFIGURATION REGISTER

Address: 0x28 to 0x29, Reset: 0x0000, Name: MAX_LIMIT_REG

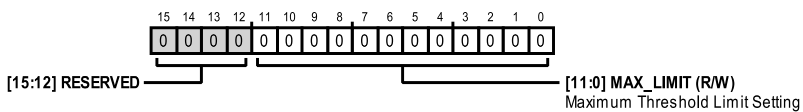


Table 45. Bit Descriptions for MAX_LIMIT_REG

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	MAX_LIMIT	Maximum Threshold Limit Setting. Sets the maximum threshold limit for autonomous modes. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R/W

MINIMUM THRESHOLD CONFIGURATION REGISTER

Address: 0x2A to 0x2B, Reset: 0x0000, Name: MIN_LIMIT_REG

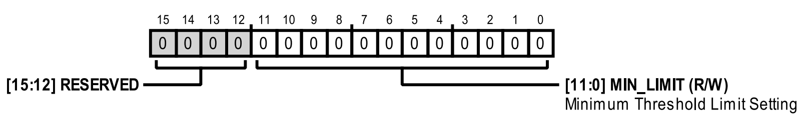
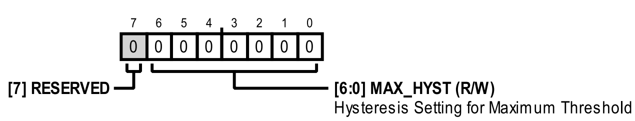


Table 46. Bit Descriptions for MIN_LIMIT_REG

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	MIN_LIMIT	Minimum Threshold Limit Setting. Sets the minimum threshold limit for autonomous modes. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R/W

MAXIMUM THRESHOLD HYSTERESIS REGISTER

Address: 0x2C, Reset: 0x00, Name: MAX_HYST_REG



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REGISTER DETAILS

Table 47. Bit Descriptions for MAX_HYST_REG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	MAX_HYST	Hysteresis Setting for Maximum Threshold. Sets the hysteresis setting for self-clearing the MAX_INTR signal in monitor mode. Uses straight binary format.	0x0	R/W

MINIMUM THRESHOLD HYSTERESIS REGISTER

Address: 0x2D, Reset: 0x00, Name: MIN_HYST_REG

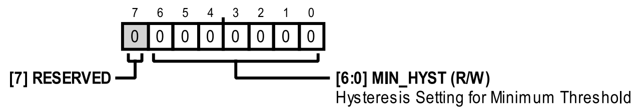

Table 48. Bit Descriptions for MIN_HYST_REG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	MIN_HYST	Hysteresis Setting for Minimum Threshold. Sets the hysteresis setting for self-clearing the MIN_INTR signal in monitor mode. Uses straight binary format.	0x0	R/W

MON_VAL SCALING REGISTER

Address: 0x2E to 0x2F, Reset: 0x0000, Name: MON_VAL_REG

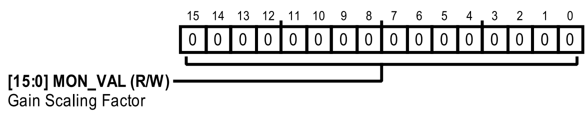

Table 49. Bit Descriptions for MON_VAL_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MON_VAL	Gain Scaling Factor. Sets the scaling factor for ADC results when using MON_VAL scaling. MON_VAL can be automatically generated or set manually. See the Gain Scaling and Achieving High Accuracy with Reference Shutdown sections.	0x0	R/W

FUSE CRC REGISTER

Address: 0x40, Reset: 0x00, Name: FUSE_CRC

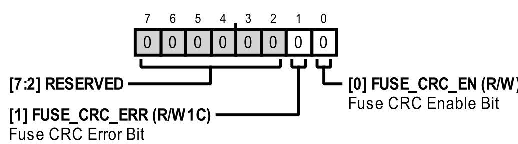

Table 50. Bit Descriptions for FUSE_CRC

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	FUSE_CRC_ERR	Fuse CRC Error Bit. Indicates an invalid fuse map CRC check. If this bit is set following the fuse map CRC check, reset the device.	0x0	R/W1C
0	FUSE_CRC_EN	Fuse CRC Enable Bit. Setting this bit to 1 triggers a CRC check on the internal device fuse map. This bit self-clears when the fuse map CRC check is complete.	0x0	R/W

DEVICE STATUS REGISTER

Address: 0x41, Reset: 0x40, Name: DEVICE_STATUS

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REGISTER DETAILS

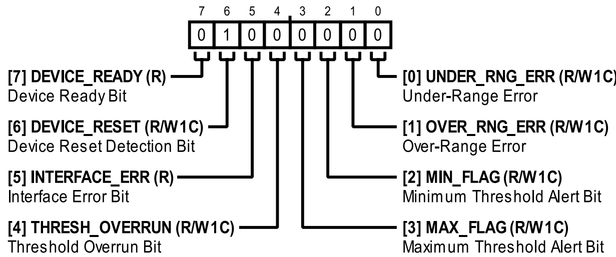

Table 51. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	DEVICE_READY	Device Ready Bit. This bit is automatically set to 1 when the device reset and startup sequence is complete and is ready for serial communications from the digital host.	0x0	R
6	DEVICE_RESET	Device Reset Detection Bit. Indicates a device reset occurred. This bit is cleared by setting it to 1.	0x1	R/W1C
5	INTERFACE_ERR	Interface Error Bit. Indicates if one or more interface communication errors occurs. This bit is the logical OR of all bits in INTERFACE_STATUS register.	0x0	R
4	THRESH_OVERRUN	Threshold Overrun Bit. This bit is set to 1 when a threshold overrun event is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C
3	MAX_FLAG	Maximum Threshold Alert Bit. This bit is set to 1 when a maximum threshold violation is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C
2	MIN_FLAG	Minimum Threshold Alert Bit. This bit is set to 1 when a minimum threshold violation is detected. This bit is sticky and is only cleared by writing it to a 1.	0x0	R/W1C
1	OVER_RNG_ERR	Overrange Error. Write 1 to clear.	0x0	R/W1C
0	UNDER_RNG_ERR	Underrange Error. Write 1 to clear.	0x0	R/W1C

MAXIMUM INTERRUPT SAMPLE REGISTER

Address: 0x42 − 0x43, Reset: 0x0000, Name: MAX_SAMPLE_REG

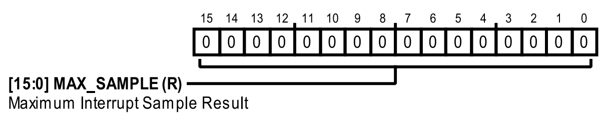

Table 52. Bit Descriptions for MAX_SAMPLE_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MAX_SAMPLE	Maximum Interrupt Sample Result. Contains ADC result generated by maximum threshold interrupt in trigger mode. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R

MINIMUM INTERRUPT SAMPLE REGISTER

Address: 0x44 − 0x45, Reset: 0x0000, Name: MIN_SAMPLE_REG

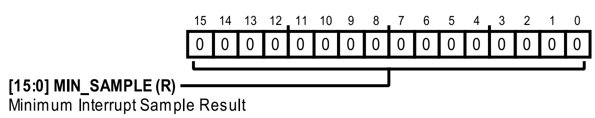

Table 53. Bit Descriptions for MIN_SAMPLE_REG

Bits	Bit Name	Description	Reset	Access
[15:0]	MIN_SAMPLE	Minimum Interrupt Sample Result. Contains ADC result generated by minimum threshold interrupt in trigger mode. Uses the same data format (twos complement or straight binary) as the ADC as set by the DATA_FORMAT bit.	0x0	R

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OUTLINE DIMENSIONS

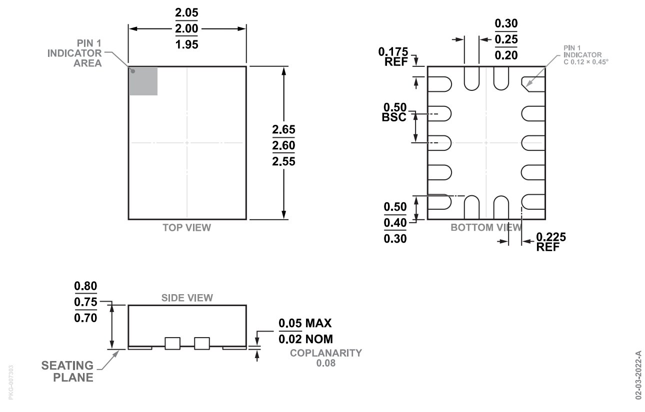

Figure 81. 14-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2.6 mm Body and 0.75 mm Packaging Height
(CP-14-7)
Dimensions shown in millimeters

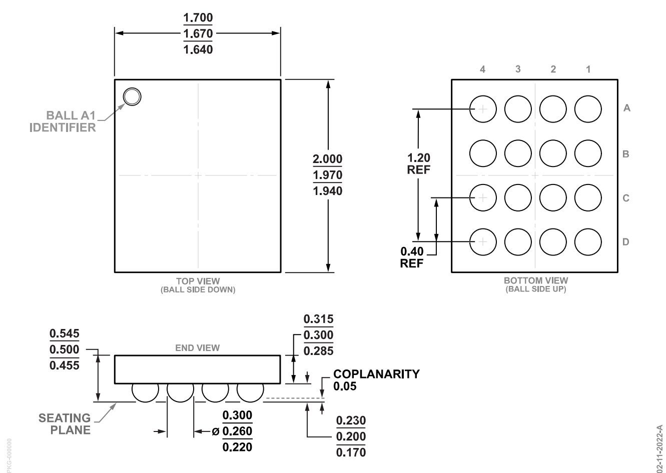

Figure 82. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4052BCPZ-RL7	−40°C to +125°C	14-Lead LFCSP (2.00 mm × 2.6 mm × 0.75 mm)	REEL, 3000	CP-14-7
AD4052BCBZ-RL7	−40°C to +125°C	16-Ball WLCSP (1.67 mm × 1.97 mm × 0.5 mm)	REEL, 3000	CB-16-26
AD4052BCPZ-R2	−40°C to +125°C	14-Lead LFCSP (2.00 mm × 2.6 mm × 0.75 mm)	REEL, 1250	CP-14-7
AD4058BCPZ-RL7	−40°C to +125°C	14-Lead LFCSP (2.00 mm × 2.6 mm × 0.75 mm)	REEL, 3000	CP-14-7
AD4058BCBZ-RL7	−40°C to +125°C	16-Ball WLCSP (1.67 mm × 1.97 mm × 0.5 mm)	REEL, 3000	CB-16-26
AD4058BCPZ-R2	−40°C to +125°C	14-Lead LFCSP (2.00 mm × 2.6 mm × 0.75 mm)	REEL, 250	CP-14-7

1 Z = RoHS Compliant Part.

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OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
EVAL-AD4052-ARDZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

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