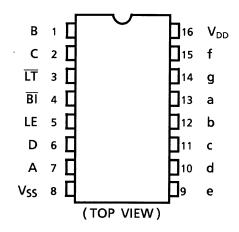
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

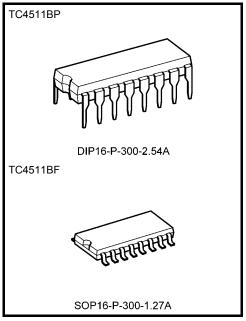
# TC4511BP, TC4511BF

### TC4511B BCD-to-Seven Segment Latch/Decoder/Driver

TC4511B is decoder which converts the input of BCD code into the 7 segment display element driving signal and the output has complementary connection of NPN bipolar transistor and N-channel MOS FET. Therefore, not only capability of directly driving cathode common type LED, this has capability of driving various display elements with simple interface circuits.  $\overline{LT}$  input and  $\overline{BI}$  input are to force all the outputs to be "H" (illuminated) and "L" (not illuminated) respectively regardless of BCD input. As the latch controlled by common LE input is inserted in each of four input lines, static display of dynamic information can be achieved. When an invalid BCD input, "10" or higher is applied, all the outputs become "L" (not illuminated).

### Pin Assignment

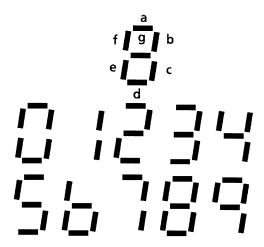




Weight

DIP16-P-300-2.54A : 1.00 g (typ.) SOP16-P-300-1.27A : 0.18 g (typ.)

### **Display**



Start of commercial production 1978-04

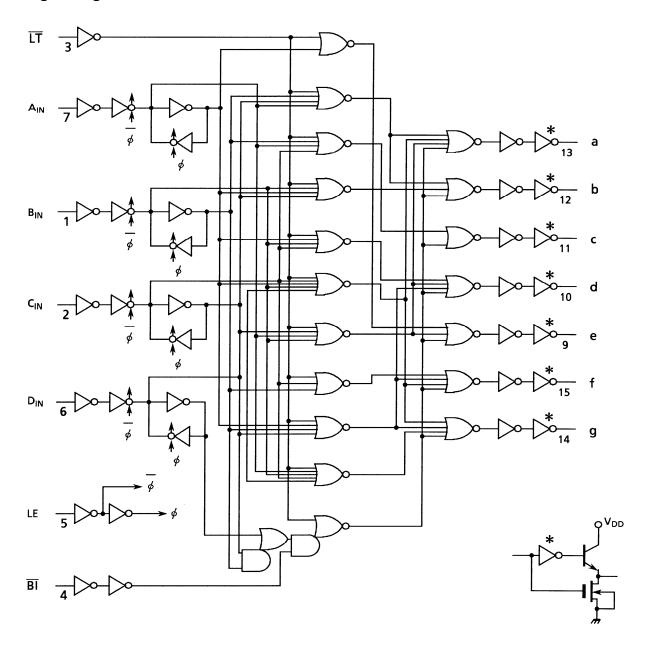
### **Truth Table**

Inputs					Outputs					Display				
LE	BI	ĪΤ	D	С	В	Α	а	b	С	d	е	f	g	Mode
*	*	L	*	*	*	*	Н	Н	Н	Н	Н	Н	Н	8
*	L	Н	*	*	*	*	L	L	L	L	L	L	L	Blank
L	Н	Η	L	L	L	L	Н	Н	Н	Н	Н	Н	L	0
L	Н	Η	L	L	L	Н	L	Н	Н	L	Ш	L	L	1
L	Н	Η	L	L	Н	L	Н	Н	L	Н	Н	L	Н	2
L	Н	Н	L	L	Н	Н	Н	Н	Н	Н	L	L	Н	3
L	Н	Η	L	Η	L	L	L	Н	Н	L	Ш	Н	Н	4
L	Н	Н	L	Н	L	Н	Н	L	Н	Н	L	Н	Н	5
L	Н	Η	L	Η	Н	L	L	L	Н	Н	Н	Н	Н	6
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	L	L	L	7
L	Н	Η	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	8
L	Н	Η	Н	L	L	Н	Н	Н	Н	L	Ш	Н	Н	9
L	Н	Н	Н	L	Н	L	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	L	Н	Н	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	Н	*	*	L	L	L	L	L	L	L	Blank
Н	Н	Н	*	*	*	*	ΔΔ							

<sup>\*:</sup> Don't care

 $\Delta\!\Delta\!$  . Depends upon the BCD code previously applied when LE "L"

# **Logic Diagram**



### **Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
DC supply voltage	$V_{DD}$	$V_{SS}$ – 0.5 to $V_{SS}$ + 20	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5	V
DC input current	I <sub>IN</sub>	±10	mA
Output high current	Іон	-50	mA
Power dissipation	PD	300 (DIP)/180 (SOIC)	mW
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C
Storage temperature range	T <sub>stg</sub>	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Range ( $V_{SS} = 0 \text{ V}$ ) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	$V_{DD}$	_	3	_	18	V
Input voltage	$V_{IN}$		0	_	$V_{DD}$	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{DD}$  or  $V_{SS}$ .

# Static Electrical Characteristics ( $V_{SS} = 0 V$ )

Characteristics		Sym-	Test Condition	-40°		)°C		25°C		85°C		l lmi4
Charac	teristics	bol		V <sub>DD</sub> (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit
			1	5	4.1	_	4.1	4.41	_	4.2	_	
High-level voltage	output	$V_{OH}$	I <sub>OUT</sub>   < 1 μA	10	9.1	_	9.1	9.41	_	9.2	_	V
			$V_{IN} = V_{SS}, V_{DD}$	15	14.1	_	14.1	14.41	_	14.2	_	
			  I <sub>OUT</sub>   < 1 μA	5	_	0.05	_	0.00	0.05	_	0.05	
Low-level voltage	output	$V_{OL}$	$V_{IN} = V_{SS}, V_{DD}$	10	_	0.05	_	0.00	0.05	_	0.05	V
			VIN - VSS, VDD	15	_	0.05	_	0.00	0.05	_	0.05	
			I <sub>OH</sub> = 0 mA		4.10	_	4.10	4.41	_	4.20	_	
			I <sub>OH</sub> = 10 mA	5	3.90	_	3.90	4.25	_	3.90	_	
			I <sub>OH</sub> = 20 mA		3.55	_	3.55	4.19	_	3.30	_	
			$V_{IN} = V_{DD}, V_{SS}$									
			I <sub>OH</sub> = 0 mA		9.10	_	9.10	9.41	_	9.20	_	l
Output hig	ıh voltage	V <sub>OH</sub>	I <sub>OH</sub> = 10 mA	10	9.00	_	9.00	9.25	_	9.00	_	V
Output riig	iii voitage	VOH	I <sub>OH</sub> = 20 mA		8.70	_	8.70	9.20	_	8.40	_	v
			$V_{IN} = V_{DD}, V_{SS}$									
			I <sub>OH</sub> = 0 mA		14.10	_	14.10	14.41	_	14.20	_	
			I <sub>OH</sub> = 10 mA	15	14.00	_	14.00	14.26	_	14.00	_	
			I <sub>OH</sub> = 20 mA		13.75	_	13.75	14.21	_	13.50	_	
			$V_{IN} = V_{DD}, V_{SS}$									
			V <sub>OUT</sub> = 0.4 V	5	0.61	_	0.51	1.2	_	0.42	_	
Output lov	vvoltage	lo	V <sub>OUT</sub> = 0.5 V	10	1.5	_	1.3	3.2	_	1.1	_	mA
Output 10V	v voltage	l <sub>OL</sub>	V <sub>OUT</sub> = 1.5 V	15	4.0	_	3.4	12.0	—	2.8	_	111/5
			$V_{IN} = V_{DD}, V_{SS}$									
		.,	V <sub>OUT</sub> = 0.5 V, 4.5 V	5	3.5	_	3.5	2.75	_	3.5	_	
Input high	voltage		V <sub>OUT</sub> = 1.0 V, 9.0 V	10	7.0	_	7.0	5.50	_	7.0	_	V
input nign	voltage	V <sub>IH</sub>	V <sub>OUT</sub> = 1.5 V, 13.5 V	15	11.0	_	11.0	8.25	_	11.0	_	v
			$ I_{OUT}  < 1 \mu A$									
			V <sub>OUT</sub> = 0.5 V, 4.5 V	5		1.5	_	2.25	1.5	_	1.5	
Input low v	voltage	V <sub>IL</sub>	V <sub>OUT</sub> = 1.0 V, 9.0 V	10	_	3.0	_	4.5	3.0	_	3.0	V
input low v	voitage	۷IL	V <sub>OUT</sub> = 1.5 V, 13.5 V	15	_	4.0	_	6.75	4.0	_	4.0	v
	_		$ I_{OUT}  < 1 \mu A$									
Input	"H" level	ΞH	V <sub>IH</sub> = 18 V	18		0.1	_	10 <sup>-5</sup>	0.1		1.0	μА
current	"L" level	I <sub>ΙL</sub>	V <sub>IL</sub> = 0 V	18	_	-0.1	_	-10 <sup>-5</sup>	-0.1	_	-1.0	μΛ
			West Mary	5	_	5	_	0.005	5	_	150	
Quiescent current	Quiescent supply current		$V_{IN} = V_{SS}, V_{DD}$ (Note)	10	_	10	_	0.010	10		300	μА
Carrone			(11310)	15	_	20	—	0.015	20	—	600	

Note: All valid input combinations.

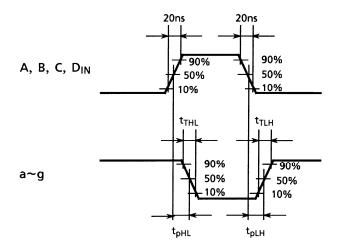
# Dynamic Electrical Characteristics (Ta = 25°C, $V_{SS}$ = 0 V, $C_L$ = 50 pF, $R_L$ = 10 k $\Omega$ )

		Test Condition		Min	Тур.	Max	Unit
Characteristics	Symbol		V <sub>DD</sub> (V)				
Output transition time			5	_	25	80	
Output transition time	tTLH	_	10	_	15	60	ns
(low to high)			15	_	15	50	
Output transition time			5	_	70	200	
(high to low)	t <sub>THL</sub>	_	10	_	35	100	ns
(High to low)			15	_	30	80	
Propagation delay time			5	_	200	1040	
(DATA-OUT)	t <sub>pLH</sub>	_	10	_	90	420	ns
(DATA-001)			15	_	65	300	
Propagation delay time			5	_	230	1040	
	t <sub>pHL</sub>	_	10	_	110	420	ns
DATA-OUT)			15	_	80	300	
Propagation delay time			5	_	75	640	
	t <sub>pLH</sub>	_	10	_	45	260	ns
(BI -OUT)  Propagation delay time (BI -OUT)			15	_	35	200	
Propagation delay time			5	_	90	640	
	t <sub>pHL</sub>	_	10	_	50	260	ns
(51 001)			15	_	45	200	
Propagation delay time			5	_	60	300	
(TT-OUT)	t <sub>pLH</sub>	_	10	_	40	150	ns
(1. 33.)			15	_	35	100	
Propagation delay time			5	_	75	300	
(TT-OUT)	t <sub>pHL</sub>	_	10	_	45	150	ns
(21 001)			15	_	35	100	
Propagation delay time			5	_	180	600	
(LE-OUT)	t <sub>pLH</sub>	_	10	_	90	300	ns
( )			15	_	65	250	
Propagation delay time			5	_	230	600	
(LE-OUT)	t <sub>pHL</sub>	_	10	_	110	300	ns
(== + + + + + + + + + + + + + + + + + +			15	_	85	250	
Min pulse time			5	_	40	300	
(LE)	t <sub>W</sub> ∟	_	10	_	20	150	ns
()			15	_	15	120	
Min set-up time			5	_	35	150	
(DATA-LE)	t <sub>SU</sub>	_	10	_	15	70	ns
,			15	_	10	40	
Min hold time			5	_	_	0	
(DATA-LE)	tH	_	10	_	_	0	ns
			15	_	_	0	
Input capacitance	C <sub>IN</sub>	_		—	5	7.5	pF

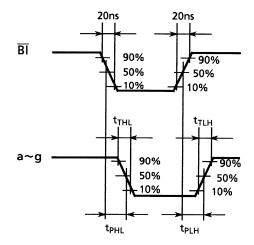
6 2014-03-01

### **Waveform for Measurement of Dynamic Characteristics**

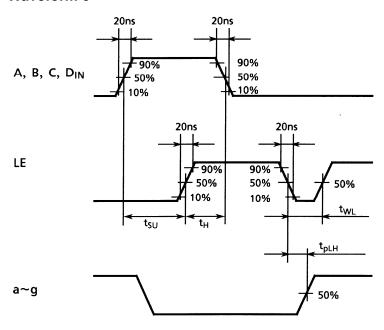
### Waveform 1



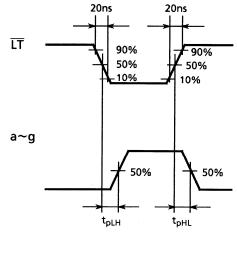
### Waveform 2



### Waveform 3



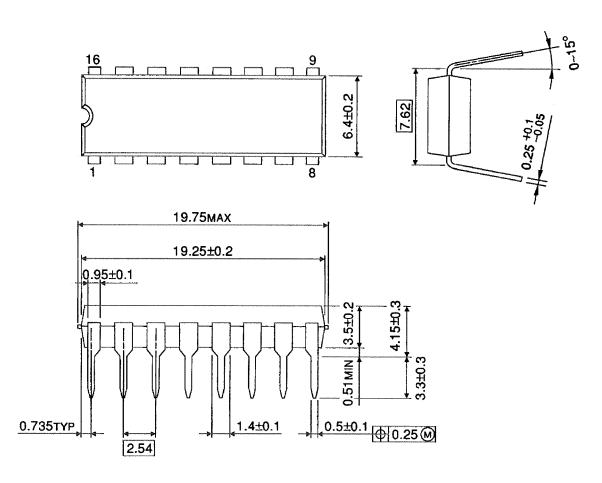
### Waveform 4





# **Package Dimensions**

DIP16-P-300-2.54A Unit: mm

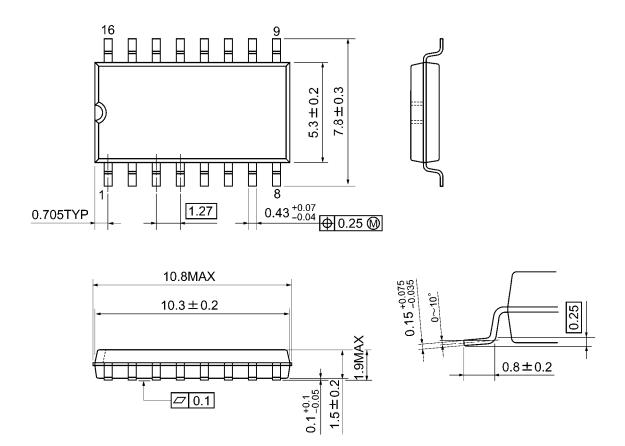


Weight: 1.00 g (typ.)



### **Package Dimensions**

SOP16-P-300-1.27A Unit: mm



9

Weight: 0.18 g (typ.)

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