Datasheet

Serial EEPROM Series Standard EEPROM

Microwire BUS EEPROM(3-Wire)

BU9888FV-W

●General Description

BU9888FV-W is a serial EEPROM of serial 3-line interface method.

●Features

- 256word×16bits architecture 4k bit serial EEPROM
- Operating voltage range(3.0V to 3.6V)
- Write Cycle time tE/W=2ms(Max)
- Address auto increment function at read action
- Write mistake prevention function
  - Write prohibition at power on
  - Write prohibition by command code
  - Write mistake prevention function at low voltage
- Program cycle auto delete and auto end function
- Program condition display READY / BUSY
- Low current consumption
  - At write action(3.6V): Icc1 = 3.5mA(Max.)
  - At read action(3.6V): Icc2 = 2.0mA(Max.)
  - At standby action (3.6V): ISB = 2.0μA(Max.)
- Data retention for 40 years
- Data rewrite up to 100,000 times
- Data at shipment all addresses FFFFh

●Package W(Typ.) x D(Typ.) x H(Max.)



SSOP-B8
3.00mm x 6.40mm x 1.35mm

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	300	mW	Degradation is done at 3.0mW/℃ for operation above 25℃
Storage Temperature	Tstg	-65 to +125	℃	
Operating Temperature	Topr	-20 to +85	℃	
Terminal Voltage	—	-0.3 to V_{CC}+0.3	V	The Max value of Terminal Voltage is not over 6.5V

●Memory cell characteristics(Ta=25℃, V_{CC} = 3.0V to 3.6V)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Erase/Write Cycle *1	100,000	—	—	Cycles
Data Retention *1	40	—	—	Years

*1 Not 100% TESTED

●Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	3.0 to 3.6	V
Input Voltage	VIN	0 to V_{CC}	

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●**Electrical Characteristics -DC Operating** (Unless otherwise specified Ta=-20℃ to +85℃, V_{CC} =3.0V to 3.6V)

Parameter	Symbol	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
"L" Input Voltage	VIL	-0.3	–	0.2×V_{CC}	V	
"H" Input Voltage	VIH	0.8×V_{CC}	–	V_{CC} +0.3	V	
"L" Output Voltage	VOL	0	–	0.4	V	IOL=2.1mA
"H" Output Voltage	VOH	2.4	–	V_{CC}	V	IOH=-0.4mA
Input Leakage Current	ILI	-1	–	1	μA	VIN=0 to V_{CC}
Output Leakage Current	ILO	-1	–	1	μA	VOUT=0 to V_{CC}, CS=0V
Operating Current	ICC1	–	–	3.5	mA	fSK=2MHz, tE/W=2ms(WRITE), TEST1=Vcc
	ICC2	–	–	2.0	mA	fSK=2MHz, (READ), TEST1=V_{CC}
Standby Current	ISB	–	–	2.0	μA	CS=0V, TEST1=V_{CC}, DO=OPEN

●**Electrical Characteristics -AC Operating** (Ta=-20℃ to +85℃, Vcc = 3.0V to 3.6V)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SK Clock Frequency	fSK	–	–	2	MHz
SK High Time	tSKH	230	–	–	ns
SK Low Time	tSKL	230	–	–	ns
CS Low Time	tCS	200	–	–	ns
CS Setup Time	tCSS	200	–	–	ns
DI Setup Time	tDIS	100	–	–	ns
CS Hold Time	tCSH	0	–	–	ns
DI Hold Time	tDIH	100	–	–	ns
Data "1" Output Delay Time	tPD1	–	–	200	ns
Data "0" Output Delay Time	tPD0	–	–	200	ns
CS to Status Valid	tSV	–	–	150	ns
CS to Output High-Z	tDF	–	–	150	ns
Write Cycle time	tE/W	–	–	2	ms

●**Sync Data Input / Output Timing**

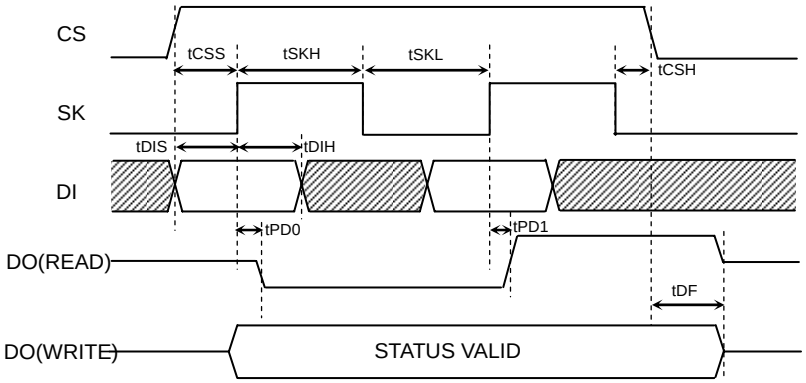


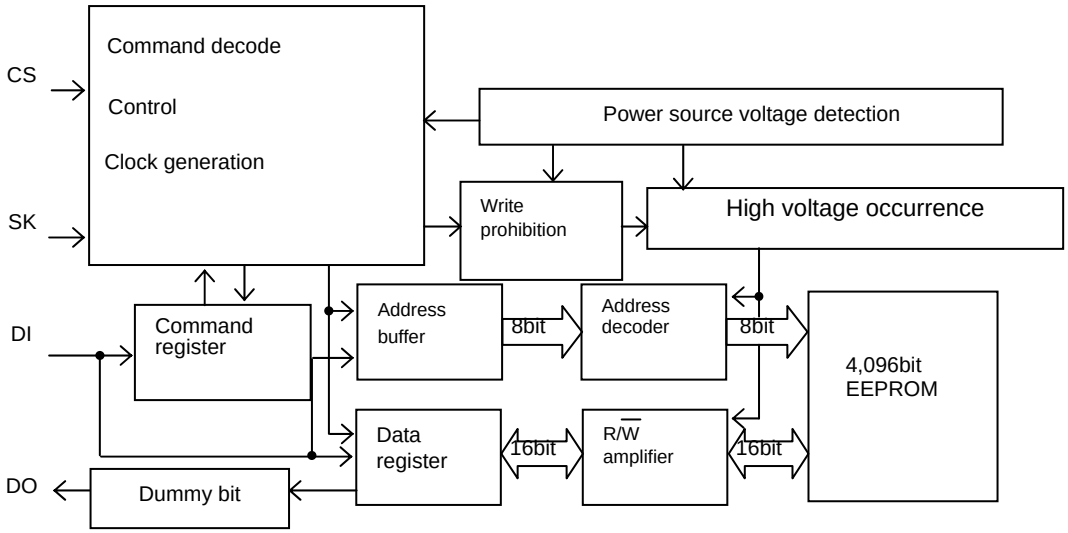
Figure 1. Sync data input / output timing

○Data is taken by DI in sync with the rise of SK.
○At read action, data is output from DO in sync with the rise of SK.
○The status signal at write (READY / $\overline{\text{BUSY}}$) is output after tCS from the fall of CS after write command input, at the area DO where CS is “H”, and valid until the next command start bit is input. And, while CS is “L”, DO becomes High-Z.
○After completion of each mode execution, set CS “L” once for internal circuit reset, and execute the following action mode.

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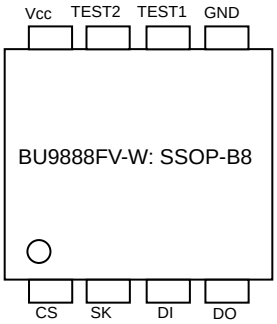
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●Block Diagram



●Pin Configuration

TOP VIEW



●Pin Descriptions

Pin name	I / O	Function
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Serial data input
DO	Output	Serial data output
TEST1	Input	Test pin. Please connect to power.
TEST2	-	Test pin. Please open at using.
Vcc	-	Power source
GND	-	All input / output reference voltage, 0V

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●**Typical Performance Curves**

(The following characteristic data are Typ. Values.)

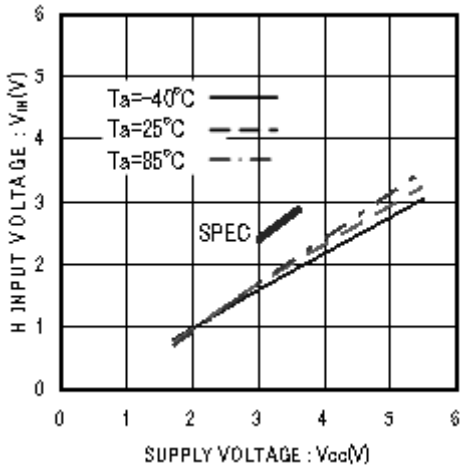


Figure 2. 'H' input voltage
VIH(CS,SK,DI)

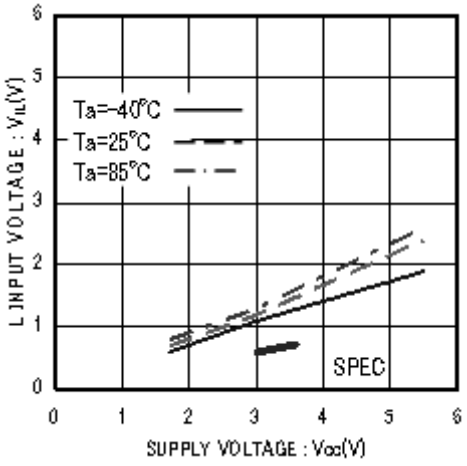


Figure 3. 'L' input voltage
VIL(CS,SK,DI)

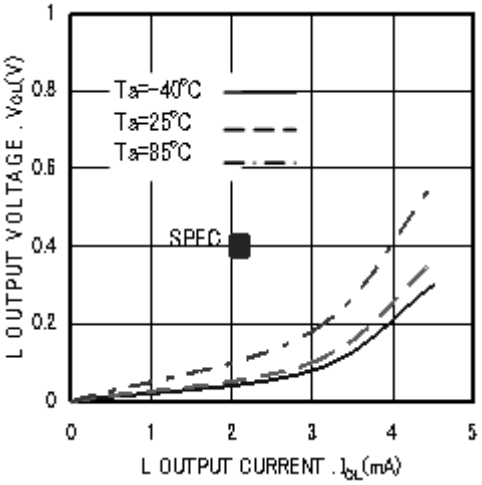


Figure 4. 'L' output voltage
VOL-IOL(Vcc=3.0V)

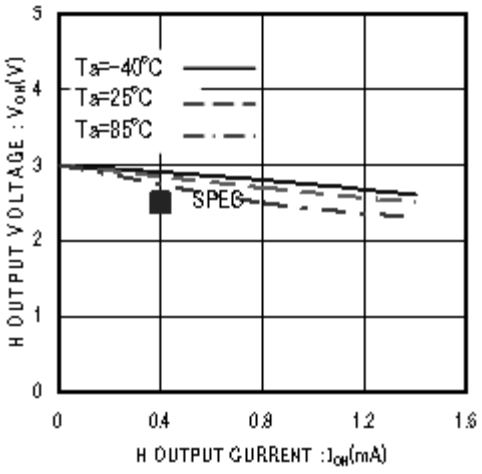


Figure 5. 'H' output voltage
VOH-IOH(Vcc=3.0V)

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●**Typical Performance Curves - Continued**

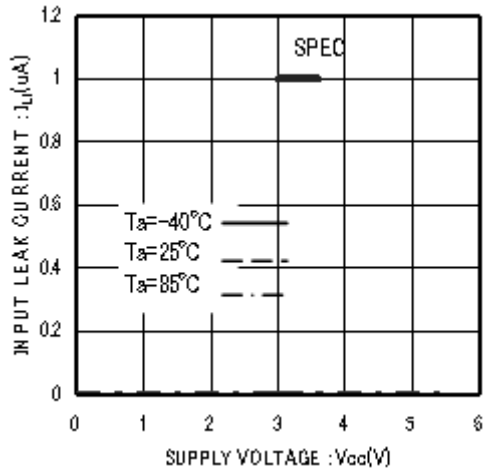


Figure 6. Input leak current
I_{LI}(CS,SK.DI)

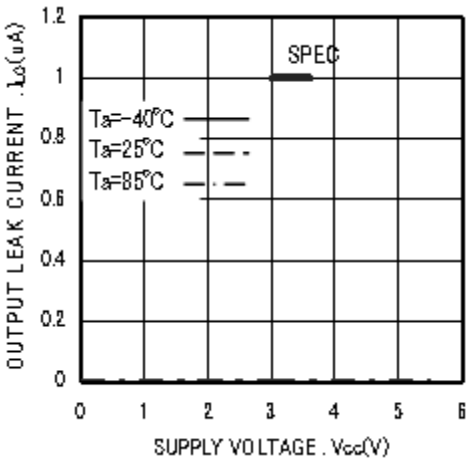


Figure 7. Output leak current
I_{LO}(DO)

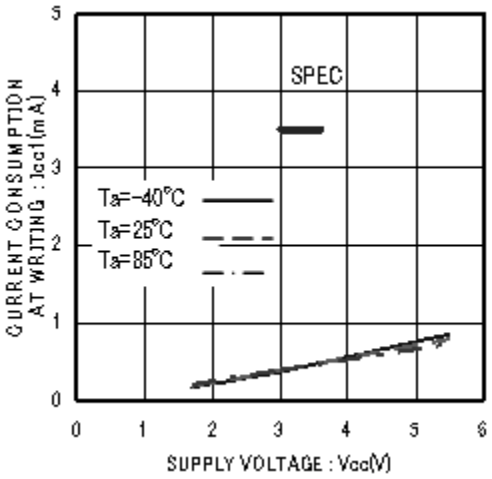


Figure 8. Current consumption at WRITE Action I_{cc1}(f_{SK}=2MHz)

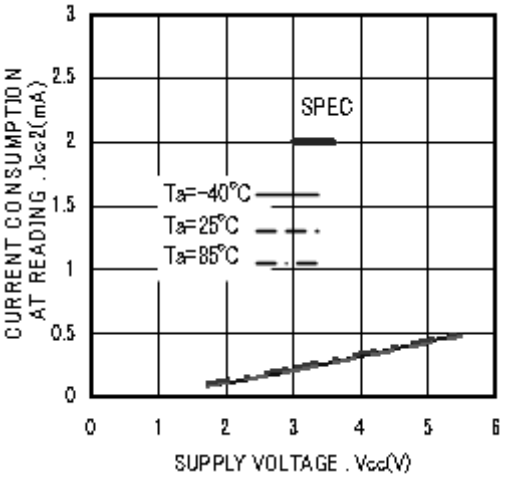


Figure 9. Consumption current at READ Action I_{cc2}(f_{SK}=2MHz)

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●**Typical Performance Curves - Continued**

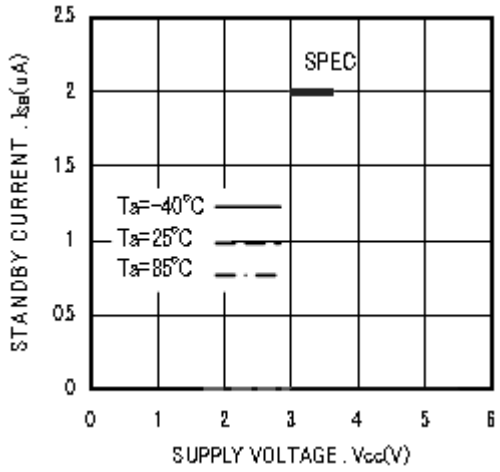


Figure 10. Consumption current at standby action I_{SB}

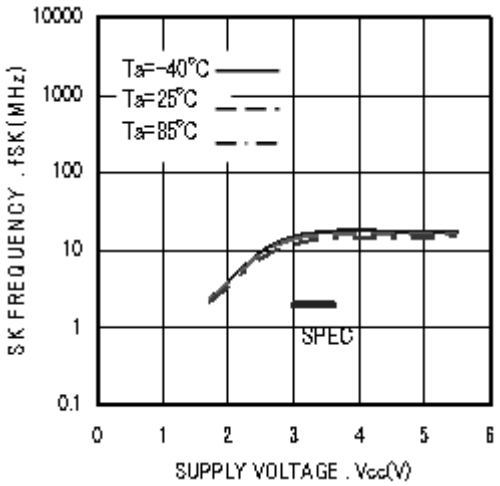


Figure 11. SK frequency f_{SK}

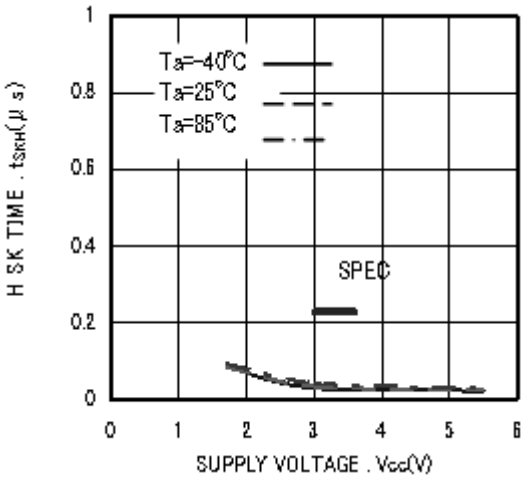


Figure 12. SK high time t_{SKH}

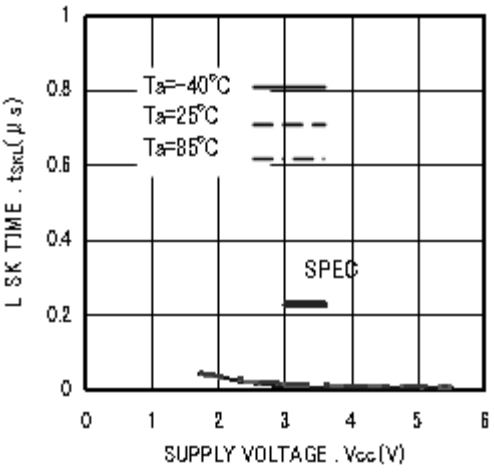


Figure 13. SK low time t_{SKL}

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●Typical Performance Curves - Continued

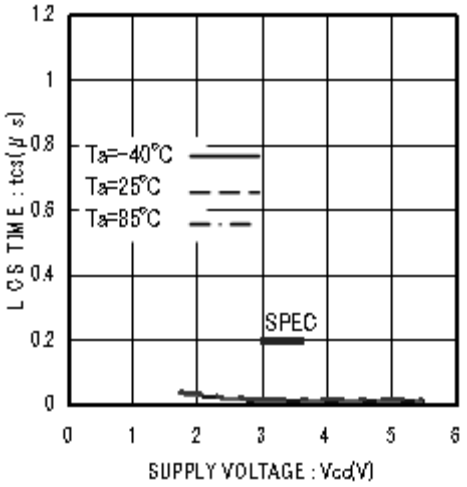


Figure 14. CS Low time tCS

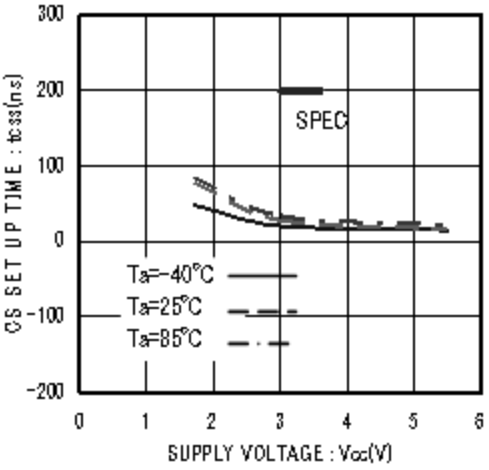


Figure 15. CS Setup time tCSS

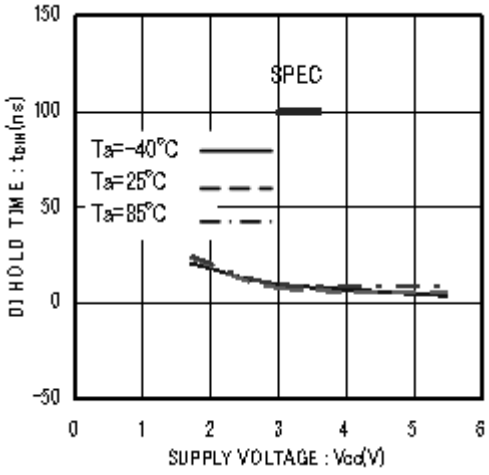


Figure 16. DI Hold time tDIH

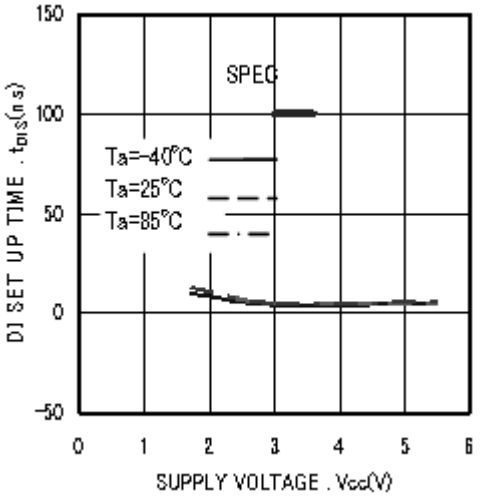


Figure 17. DI Setup time tDIS

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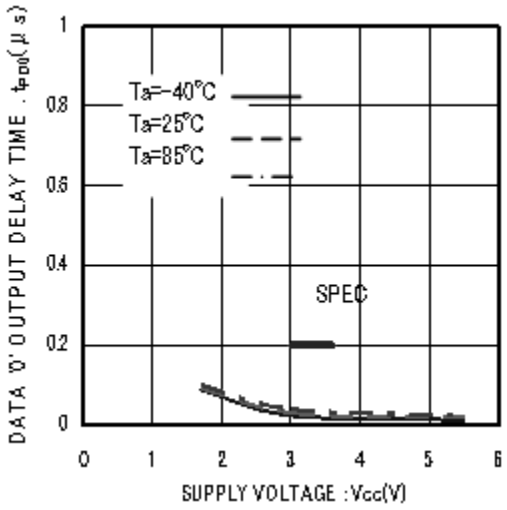


Figure 18. Data '0' output delay time t_{PD0}

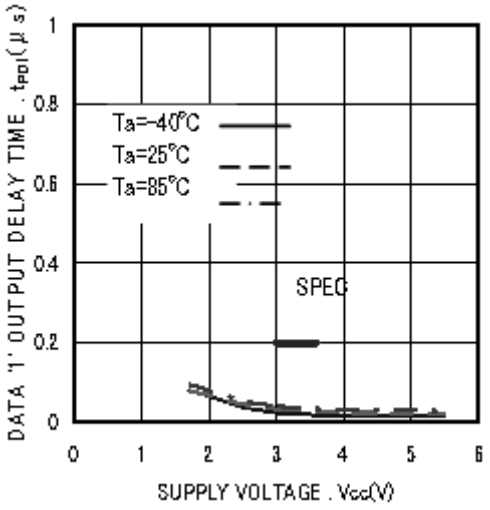


Figure 19. Data '1' output delay time t_{PD1}

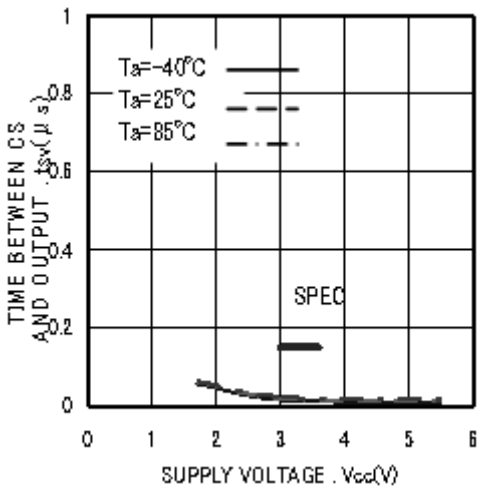


Figure 20. Time from CS to output establishment t_{SV}

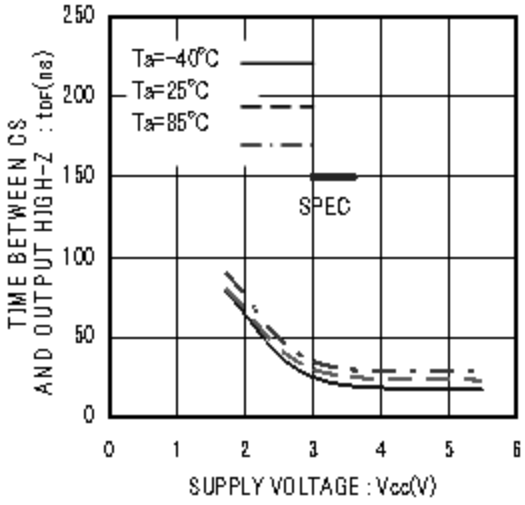


Figure 21. Time from CS to High-Z t_{DF}

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●Typical Performance Curves - Continued

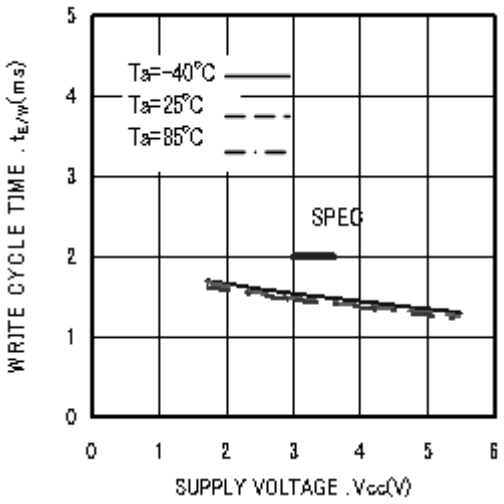


Figure 22. Write cycle time $t_{E/W}$

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●**Command mode**

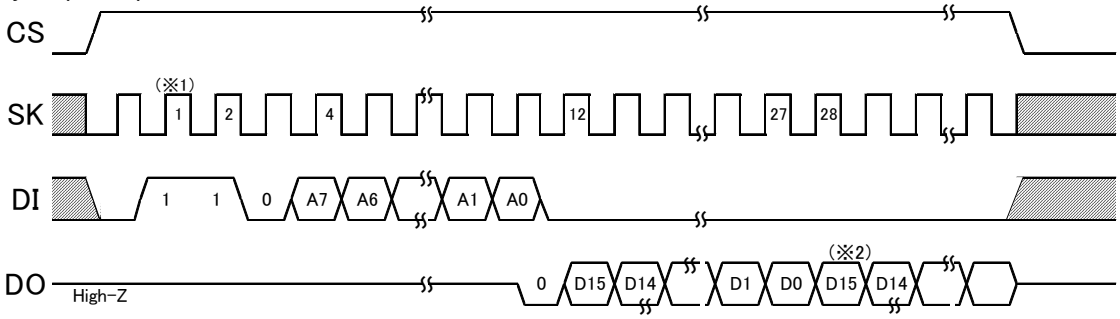
Command	Start bit	Ope code	Address	Data
Read (READ) (*1)	1	10	A7, A6, A5, A4, A3, A2,A1, A0	D15 to D0(READ DATA)
Write enable (WEN)	1	00	1 1 * * * * * *	
Write (WRITE) (*2)	1	01	A7, A6, A5, A4, A3, A2, A1, A0	D15 to D0(WRITE DATA)
Write disable (WDS)	1	00	0 0 * * * * * *	

・Input the address and the data in MSB first manners.
・As for ＊, input either VIH or VIL.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first “1” input after the rise of CS.
*1As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)
*2When the read and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.

●**Timing chart**

1. Read cycle (READ)



(※2) Next address data(Auto increment function)

Figure 23. Read cycle

(※1) Start bit
When data “1” is input for the first time after the rise of CS, this is recognized as a start bit. And when “1” is input after plural “0” are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

○When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, “0” (dummy bit) is output. And, the following data is output in sync with the rise of SK. This IC has an address auto increment function valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at “H”.

2. Write cycle (WRITE)

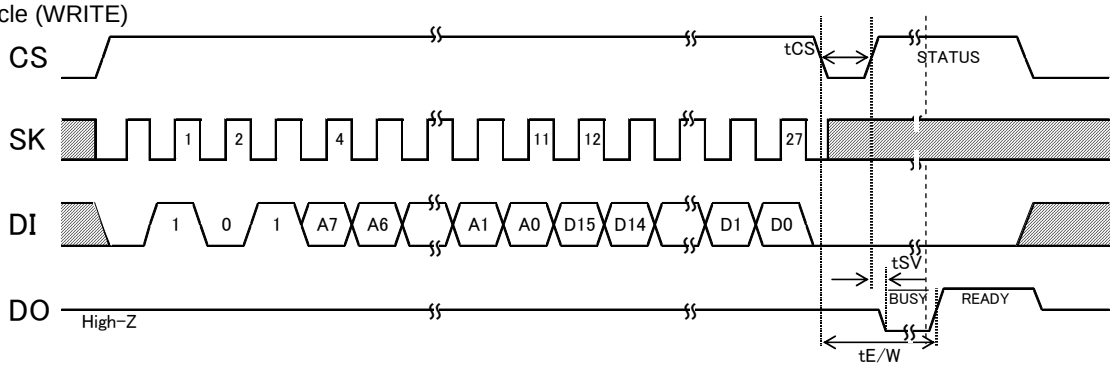


Figure 24. Write cycle

○In this command, input 16bit data (D15 to D0) are written to designated addresses (A7 to A0). The actual write starts by the fall of CS of D0 taken SK clock. When STATUS is not detected, (CS=”L” fixed) Max. 2ms in conformity with tE/W, and when STATUS is detected (CS=”H”), all commands are not accepted for areas where “L” ($\overline{\text{BUSY}}$) is output from D0, therefore, do not input any command.

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3. Write enable (WEN)

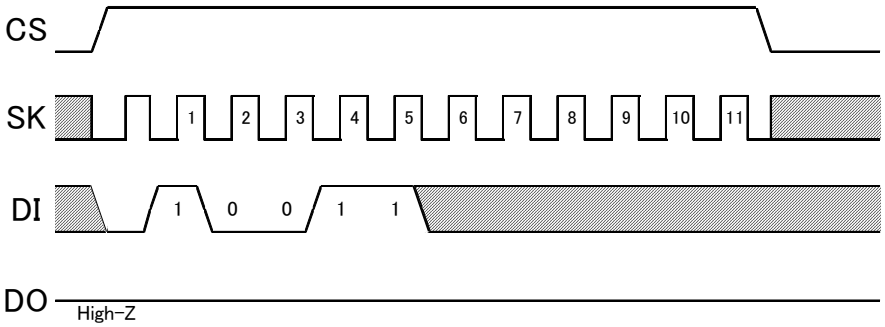


Figure 25. Write enable (WEN) cycle

○At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid unitl the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / diable command. Input to SK after 8 clocks of this command is available by either “H” or “L”, but be sure to input it.

4. Write disable (WDS) cycle

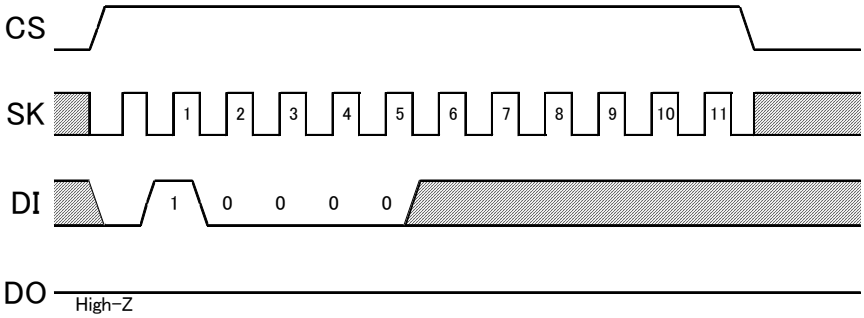


Figure 26. Write disable (WDS) cycle

○When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write. Input to SK after 8 clocks of this command is available by either “H” or “L”, but be sure to input it.

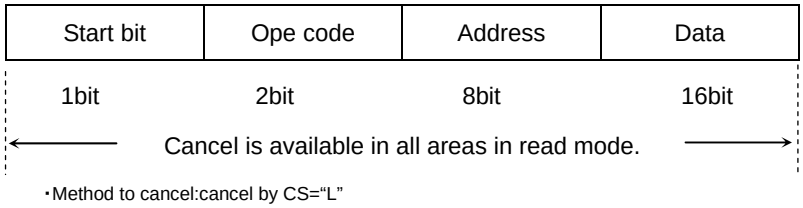
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●Application

1) Method to cancel each command

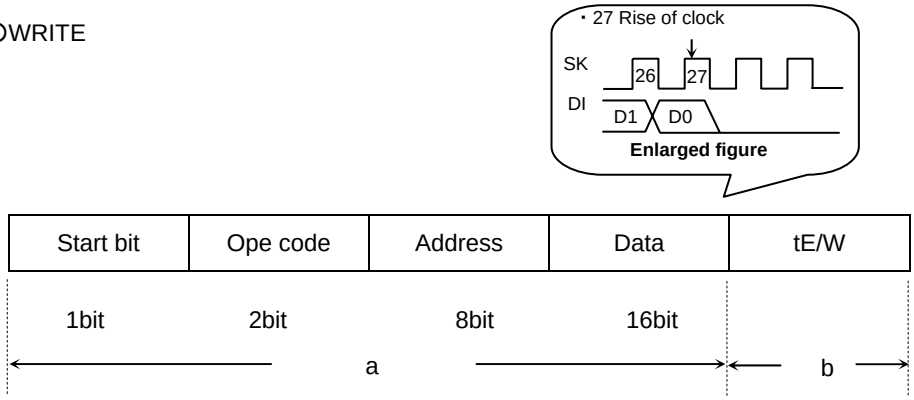
○READ



・Method to cancel:cancel by CS="L"

Figure 27. READ cancel available timing

○WRITE



a:From start bit to 27 clock rise
Cancel by CS="L"

b:27 clock rise and after
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

Figure 28. Write cancel available timing

2) At standby

○Standby current

When CS is "L", SK input is "L", DI input is "H", and even with middle electric potential, current does not increase.

○Timing

As shown in Figure 29, when SK at standby is "H", if CS is started, DI status may be read at the rise edge.
At standby and at power ON/OFF, when to start CS, set SK input or DI input to "L" status. (Refer to Figure 30)

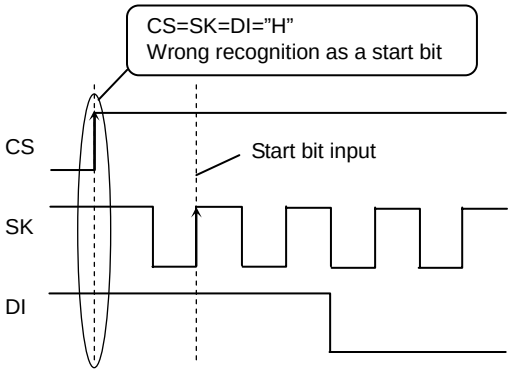


Figure 29. Wrong action timing

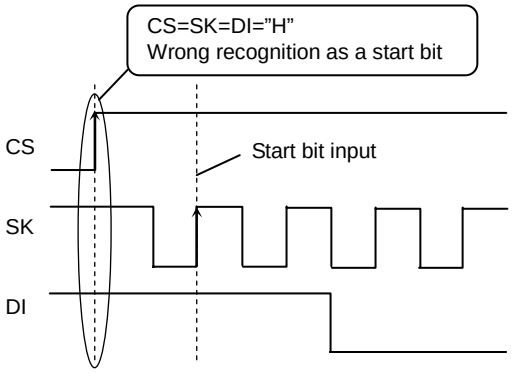


Figure 30. Normal action timing

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3) Equivalent circuit

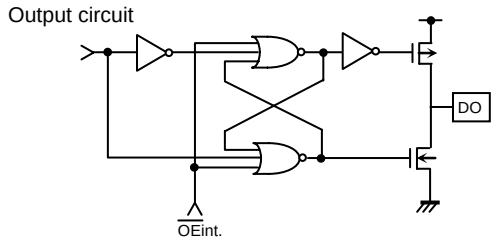


Figure 31. Output circuit (DO)

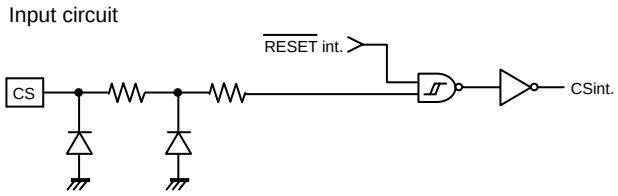


Figure 32. Input circuit (CS)

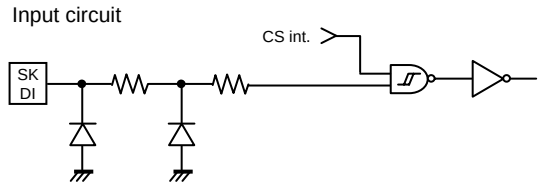


Figure 33. Input circuit (SK,DI)

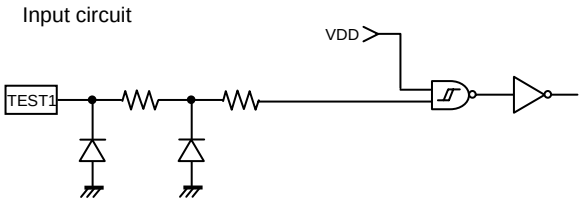


Figure 34. Input circuit (TEST1)

4) I/O peripheral circuit

4-1) Pull down CS.

By making CS="L" at power ON/OFF, mistake in operation and mistake write are prevented.

○Pull down resistance Rpd of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary.
Select an appropriate value to this resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

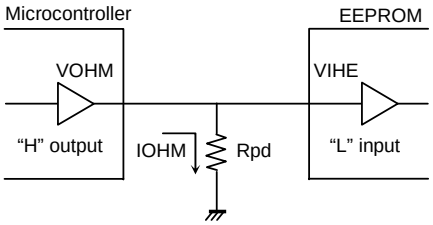


Figure 35. CS pull down resistance

$$Rpd \geqq \frac{VOHM}{IOHM} \quad \cdots ①$$

$$VOHM \geqq VIHE \quad \cdots ②$$

Example) When V_{CC} =5V, VIHE=2V, VOHM=2.4V, IOHM=2mA,
from the equation ①,

$$Rpd \geqq \frac{2.4}{2 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 1.2\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and VIHE (=2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

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4-2) DO is available in both pull up and pull down.

Do output become “High-Z” in other READY / $\overline{\text{BUSY}}$ output timing than after data output at read command and write command. When malfunction occurs at “High-Z” input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO. When there is no influence upon the microcontroller actions, DO may be OPEN.

If DO is OPEN, and at timing to output status READY, at timing of CS=“H”, SK=“H”, DI=“H”, EEPROM recognizes this as a start bit, resets READY output, and DO=”High-Z”, therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

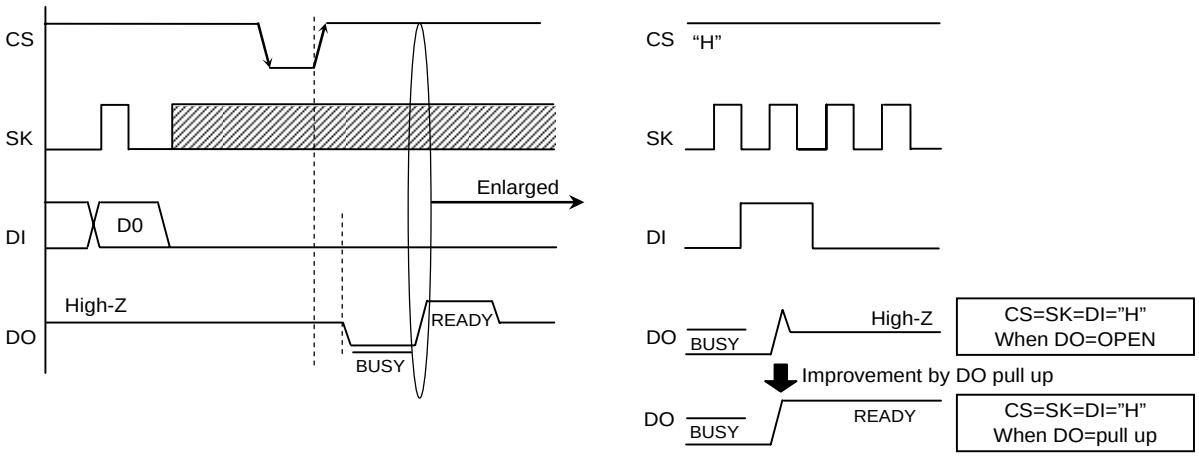


Figure 36. READY output timing at DO=OPEN

○Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller

VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.

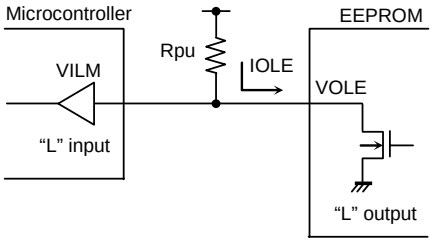


Figure 37. DO pull up resistance

$$Rpu \geqq \frac{Vcc\text{-}VOLE}{IOLE} \quad \cdots ③$$

$$VOLE \leqq VILM \quad \cdots ④$$

Example) When V_{CC} =5V, VOLE=0.4V, IOLE=2.1mA, VILM=0.8V, from the equation ③,

$$Rpu \geqq \frac{5\text{-}0.4}{2.1 \times 10^{-3}}$$

$$\therefore \quad Rpu \geqq 2.2\ [k\Omega]$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM(=0.8V), the equation ④ is also satisfied.

- VOLE : EEPROM VOL specifications
- IOLE : EEPROM IOL specifications
- VILM : Microcontroller VIL specifications

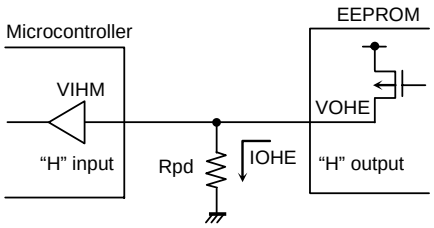


Figure 38. DO pull down resistance

$$Rpd \geqq \frac{VOHE}{IOHE} \quad \cdots ⑤$$

$$VOHE \geqq VIHM \quad \cdots ⑥$$

Example) When V_{CC} =5V, VOHE=Vcc－0.2V, IOHE=0.1mA, VIHM=Vcc×0.7V from the equation ⑤,

$$Rpd \geqq \frac{5-0.2}{0.1 \times 10^{-3}}$$

$$\therefore \quad Rpd \geqq 48\ [k\Omega]$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or below, and with VIHM (=3.5V), the equation ⑥ is also satisfied.

- VOHE : EEPROM VOH specifications
- IOHE : EEPROM IOH specifications
- VIHM : Microcontroller VIH specifications

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5) READY / $\overline{BUSY}$ status display (DO terminal)
(common to BR93L46-W / A46-WM,BR93L56-W / A56-WM, BR93L66-W / A66-WM, BR93L76-W / A76-WM, BR93L86-W / A86-WM)
This display outputs the internal status signal. When CS is started after tCS (Min.200ns) from CS fall after write command input, “H” or “L” is output.

$R/\overline{B}$ display=“L” ($\overline{BUSY}$) = write under execution
(DO status)

After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically.
And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

$R/\overline{B}$ display = “H” (READY) = command wait status
(DO status)

Even after tE/W (max.5ms) from write of the memory cell, the following command is accepted.
Therefore, CS=“H” in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore, DI=“L” in the area
CS=“H”. (Especially, in the case of shared input port, attention is required.)

* Do not input any command while status signal is output.
Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted.
Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

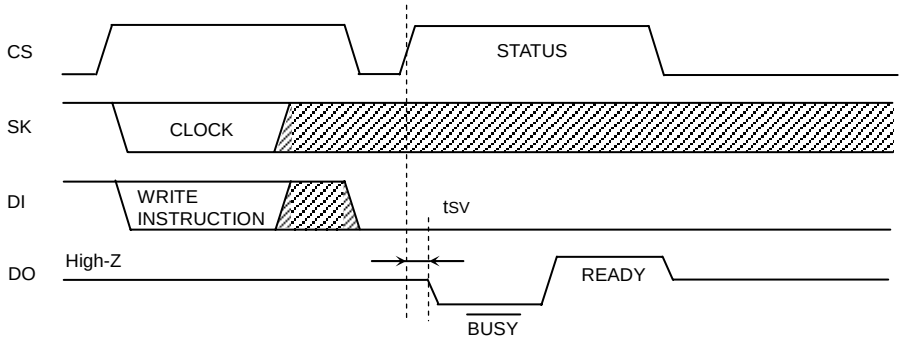


Figure 39. $R/\overline{B}$ status output timing chart

6) When to directly connect DI and DO
This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

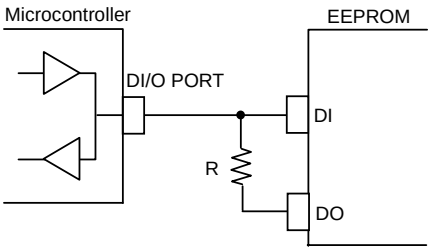


Figure 40. DI, DO control line common connection

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○Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

(1) 1 clock cycle to take in A0 address data at read command
Dummy bit “0” is output to DO terminal.
→When address data A0 = “1” input, through current route occurs.

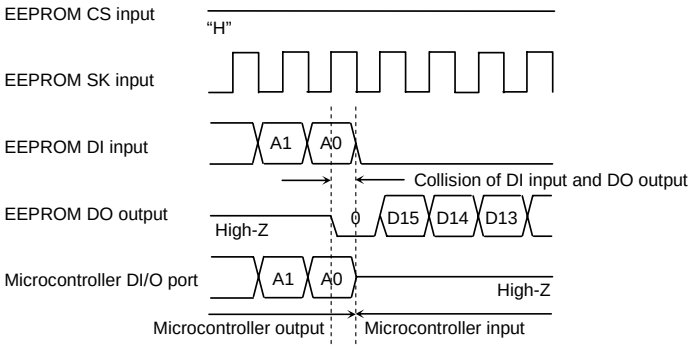


Figure 41. Collision timing at read data output at DI, DO direct connection

(2) Timing of CS = “H” after write command. DO terminal in READY / $\overline{\text{BUSY}}$ function output.
When the next start bit input is recognized, “HIGH-Z” gets in.
→Especially, at command input after write, when CS input is started with microcontroller DI/O output “L”, READY output “H” is output from DO terminal, and through current route occurs.

Feedback input at timing of these (1) and (2) does not cause disorder in basic operations, if resistance R is inserted.

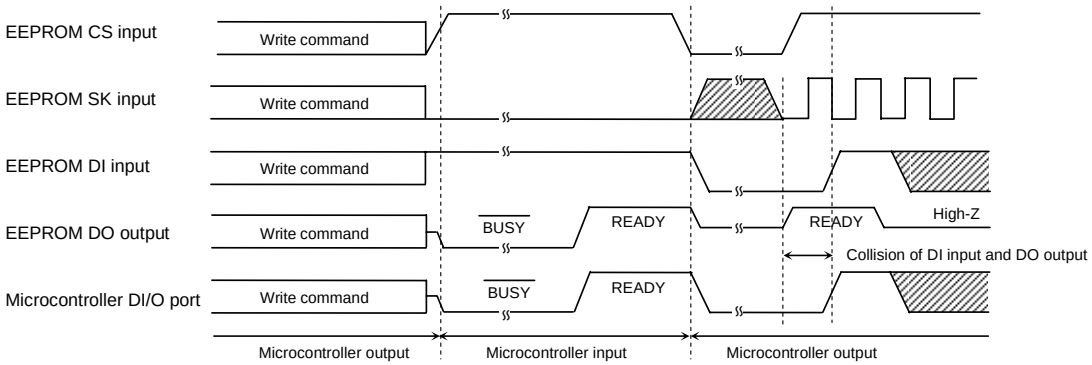


Figure 42. Collision timing at DI, DO direct connection

Note) As for the case (2), attention must be paid to the following.
When status READY is output, DO and DI are shared, DI=”H” and the microcontroller DI/O=”High-Z” or the microcontroller DI/O=”H”,if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at status READY output, set SK=“L”, or start CS within 4 clocks after “H” of READY signal is output.

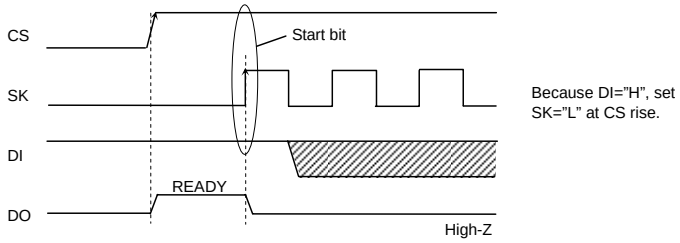


Figure 43. Start bit input timing at DI, DO direct connection

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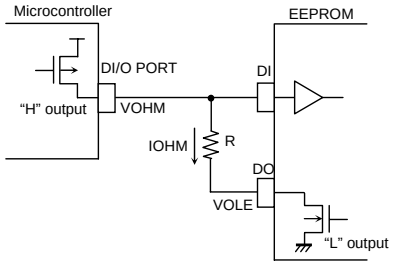
○Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

(1) Address data A0 = “1” input, dummy bit “0” output timing
(When microcontroller DI/O output is “H”, EEPROM DO outputs “L”, and “H” is input to DI)

・Make the through current to EEPROM 10mA or below.

・See to it that the level VIH of EEPROM should satisfy the following.



Conditions

$VOHM \leqq VIHE$

$VOHM \leqq IOHM \times R + VOLE$

At this moment, if VOLE=0V,

$VOHM \leqq IOHM \times R$

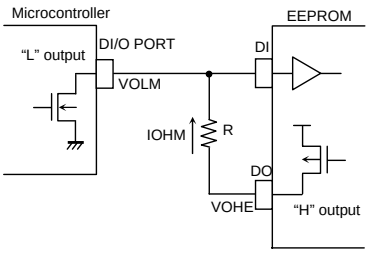
$\therefore \quad R \geqq \frac{VOHM}{IOHM} \quad \cdots ⑦$

・VIHE : EEPROM VIH specifications
・VOLE : EEPROM VOL specifications
・VOHM : Microcontroller VOH specifications
・IOHM : Microcontroller IOH specifications

Figure 44. Circuit at DI, DO direct connection (Microcontroller DI/O “H” output, EEPROM “L” output)

(2) DO status READY output timing
(When the microcontroller DI/O is “L”, EEPROM DO output “H”, and “L” is input to DI)

・Set the EEPROM input level VIL so as to satisfy the following.



Conditions

$VOLM \geqq VILE$

$VOLM \geqq VOHE - IOLM \times R$

As this moment, VOHE=Vcc

$VOLM \geqq Vcc - IOLM \times R$

$\therefore \quad R \geqq \frac{Vcc - VOLM}{IOLM} \quad \cdots ⑧$

・VILE : EEPROM VIL specifications
・VOHE : EEPROM VOH specifications
・VOLM : Microcontroller VOL specifications
・IOLM : Microcontroller IOL specifications

Figure 45. Circuit at DI, DO direct connection (Microcontroller DI/O “L” output, EEPROM “H” output)

Example) When Vcc=5V, VOHM=5V, IOHM=0.4mA, VOLM=5V, IOLM=0.4mA,

From the equation ⑦,

$R \geqq \frac{VOHM}{IOHM}$

$R \geqq \frac{5}{0.4 \times 10^{-3}}$

$\therefore \quad R \geqq 12.5\ [k\Omega] \quad \cdots ⑨$

From the equation⑧,

$R \geqq \frac{Vcc - VOLM}{IOLM}$

$R \geqq \frac{5 - 0.4}{2.1 \times 10^{-3}}$

$\therefore \quad R \geqq 2.2\ [k\Omega] \quad \cdots ⑩$

Therefore, from the equations ⑨ and ⑩,

$\therefore \quad R \geqq 12.5\ [k\Omega]$

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7) Notes on power ON/OFF

・At power ON/OFF, set CS “L”.

When CS is “H”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS “L”. (When CS is in “L” status, all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS “L”.

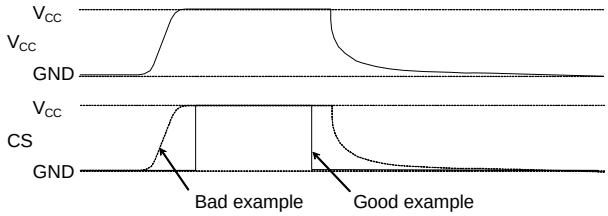


Figure 46. Timing at power ON/OFF

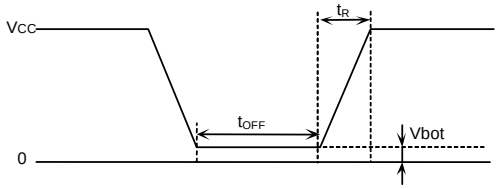
(Bad example) CS pin is pulled up to Vcc.
In this case, CS becomes “H” (active status), and EEPROM may have malfunction, mistake write owing to noise and the likes.
Even when CS input is High-Z, the status becomes like this case, which please note.

(Good example) It is “L” at power ON/OFF.
Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR citcuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is “H” at power ON/OFF, it may become write enable status owing to noises and the likes. For secure actions, observe the follwing conditions.

1. Set CS=”L”
2. Turn on power so as to satisfy the recommended conditions of t_R, t_{OFF}, Vbot for POR circuit action.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Figure 47. Rise waveform diagram

○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ.=1.2V) or below, it prevent data rewrite.

8) Noise countermeasures

○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC VCC and GND, At that moment, attach it as close to IC as possible.And, it is also recommended to attach a bypass capacitor between board VCC and GND.

○SK noise

When the rise time (t_R) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time (t_R) of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

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●**Notes for use**

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short-circuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short-circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficient.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

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●Ordering Information

B U 9 8 8 8 F V - W	E 2

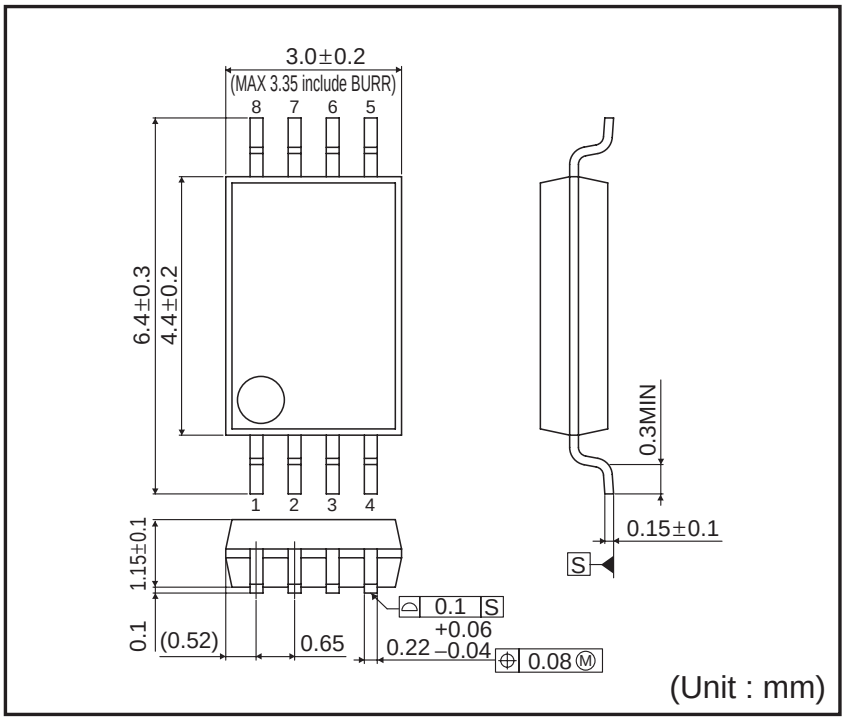
Part Number

Package
FV: SSOP-B8

Packaging and forming specification
E2: Embossed tape and reel

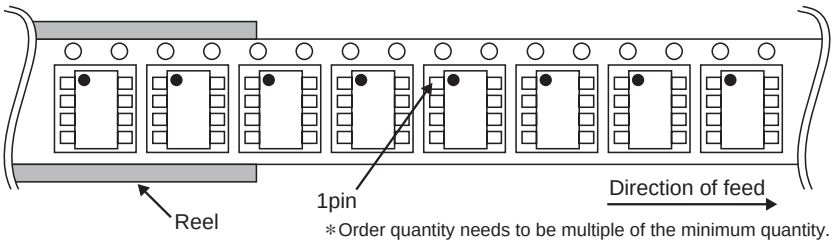
●Physical Dimension Tape and Reel Information

SSOP-B8 (BU9888FV-W)



<Tape and Reel information>

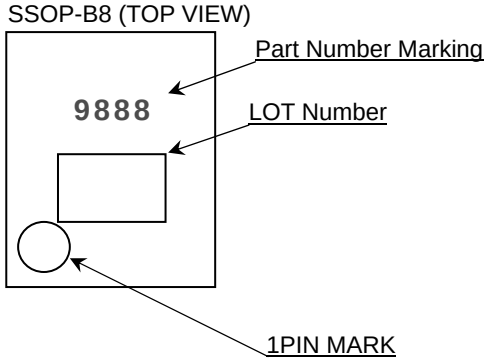
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

SSOP-B8 (TOP VIEW)



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●**Revision History**

Date	Revision	Changes
10.Sep.2012	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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Buy

Distribution Inventory

Part Number	bu9888fv-w
Package	SSOP-B8
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes

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