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## FDMC7582

### N-Channel PowerTrench® MOSFET 25 V, 49 A, 5.0 mΩ

#### Features

- Max  $r_{DS(on)}$  = 5.0 mΩ at  $V_{GS} = 10$  V,  $I_D = 16.7$  A
- Max  $r_{DS(on)}$  = 7.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 13.6$  A
- State-of-the-art switching performance
- Lower output capacitance, gate resistance, and gate charge boost efficiency
- Shielded gate technology reduces switch node ringing and increases immunity to EMI and cross conduction
- Clip bonding technology further reduces On resistance and source inductance
- RoHS Compliant

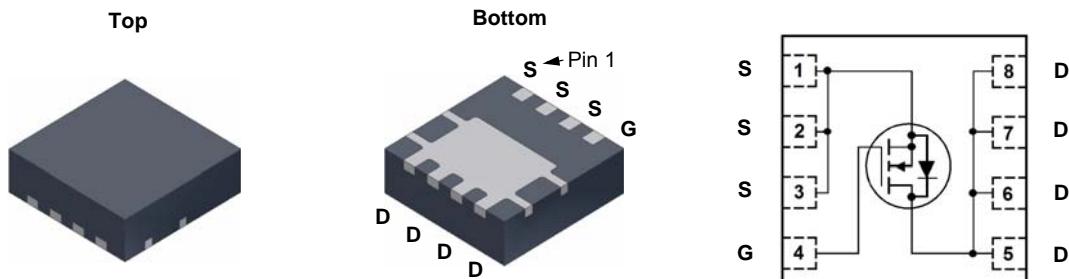


#### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance..

#### Application

- High side switching for high end computing
- High power density DC-DC synchronous buck
- Low loss load switch
- Communication & telecon Point of Load



Power 33

#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Package limited) $T_c=25$ C	49	A
	- Continuous (Silicon Limited) $T_c=25$ C	76	
	- Continuous $T_A = 25$ °C (Note 1a)	16.7	
	- Pulsed	60	
$E_{AS}$	Single Pulse Avalanche Energy	38	mJ
$P_D$	Power Dissipation $T_c = 25$ °C	52	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7582	FDMC7582	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	25			V
$\frac{\Delta V_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		19		$\text{mV/}^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			100	nA

## On Characteristics

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 16.7 \text{ A}$		4.0	5.0	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}$ , $I_D = 13.6 \text{ A}$		6.0	7.5	
		$V_{GS} = 10 \text{ V}$ , $I_D = 16.7 \text{ A}$ , $T_J = 125^\circ\text{C}$		5.4	7.0	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}$ , $I_D = 16.7 \text{ A}$		58		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 13 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		1348	1795	pF
$C_{oss}$	Output Capacitance			372	495	pF
$C_{rss}$	Reverse Transfer Capacitance			79	120	pF
$R_g$	Gate Resistance		0.1	0.9	2.9	$\Omega$

## Switching Characteristics

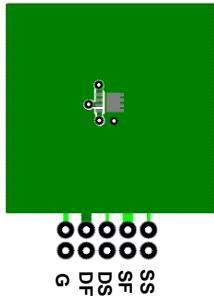
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13 \text{ V}$ , $I_D = 16.7 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_{\text{GEN}} = 6 \Omega$		8.8	18	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			20	36	ns
$t_f$	Fall Time			1.6	10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge at 10V	$V_{DD} = 13 \text{ V}$ , $I_D = 16.7 \text{ A}$		20	28	nC
$Q_{g(\text{TOT})}$	Total Gate Charge at 4.5V			9.5	13	nC
$Q_{gs}$	Total Gate Charge			3.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.5		nC

## Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = 16.7 \text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0 \text{ V}$ , $I_S = 2 \text{ A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 16.7 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$		22	39	ns
$Q_{rr}$	Reverse Recovery Charge			7	14	nC

### Notes:

1.  $R_{\text{thJA}}$  is determined with the device mounted on a  $1 \text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5 \text{ in.}$  board of FR-4 material.  $R_{\text{thJC}}$  is guaranteed by design while  $R_{\text{thCA}}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4.  $E_{AS}$  of 38 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 0.3 \text{ mH}$ ,  $I_{AS} = 16 \text{ A}$ ,  $V_{DD} = 23 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

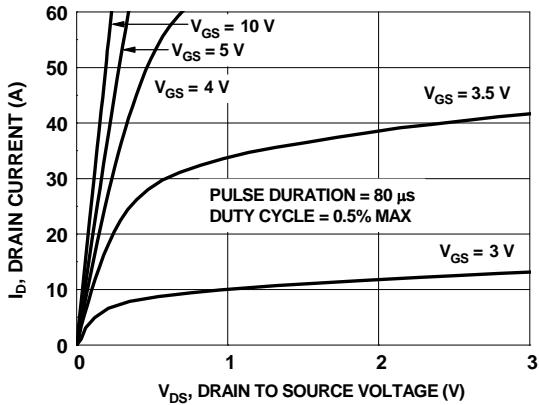


Figure 1. On Region Characteristics

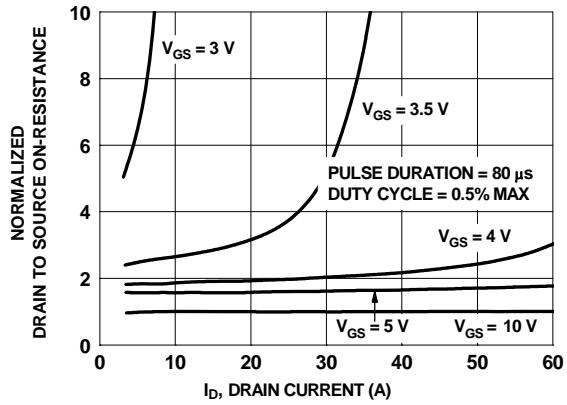


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

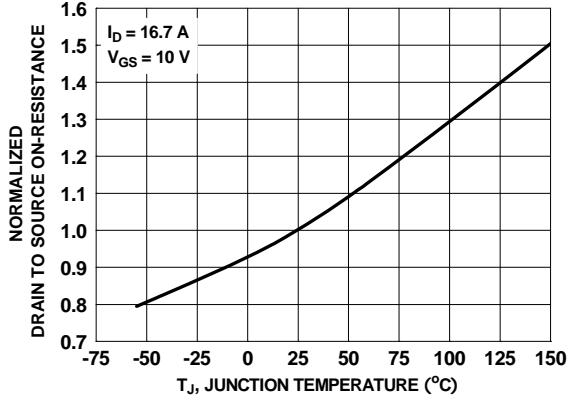


Figure 3. Normalized On Resistance vs Junction Temperature

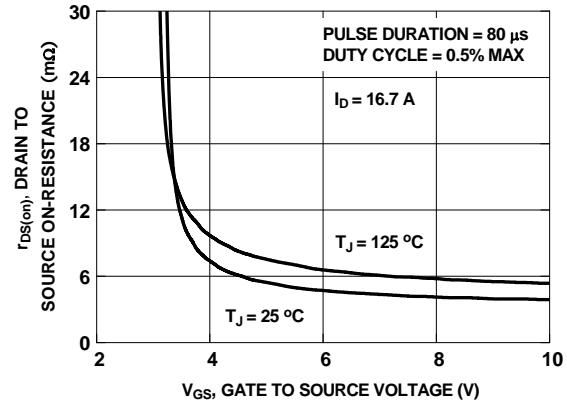


Figure 4. On-Resistance vs Gate to Source Voltage

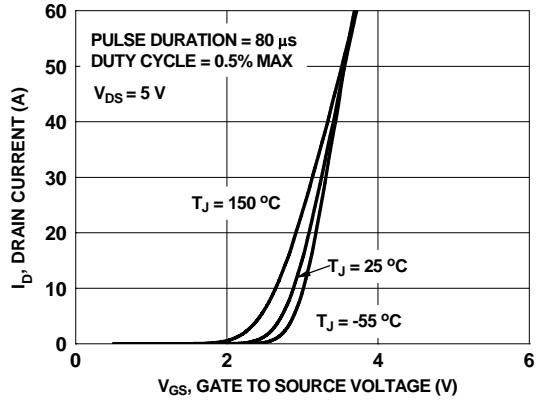


Figure 5. Transfer Characteristics

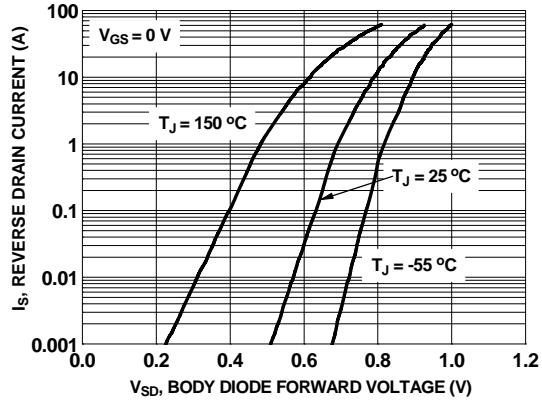


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

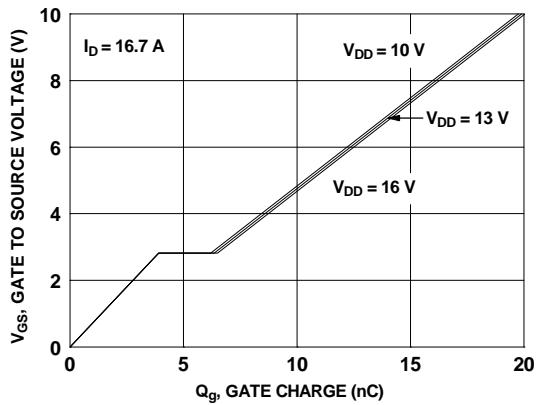


Figure 7. Gate Charge Characteristics

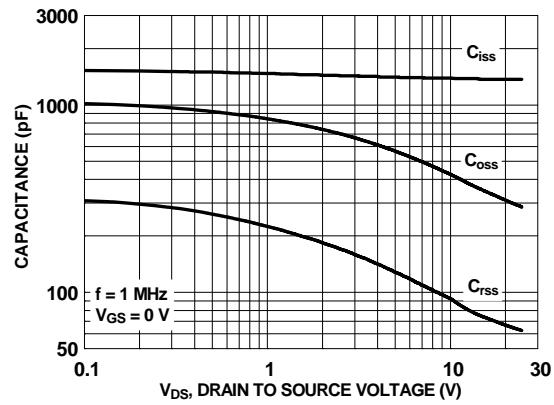


Figure 8. Capacitance vs Drain to Source Voltage

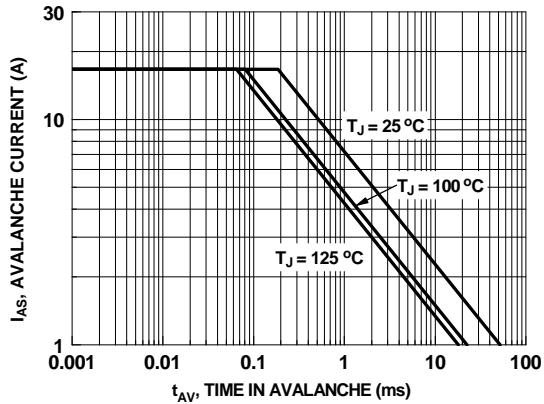


Figure 9. Unclamped Inductive Switching Capability

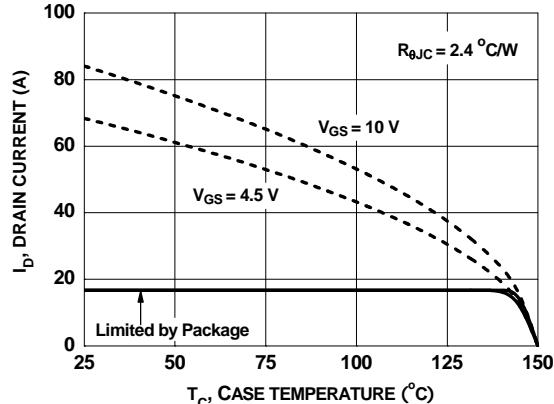


Figure 10. Maximum Continuous Drain Current vs Case Temperature

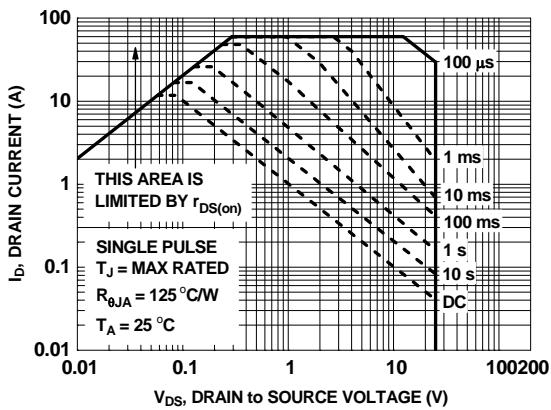


Figure 11. Forward Bias Safe Operating Area

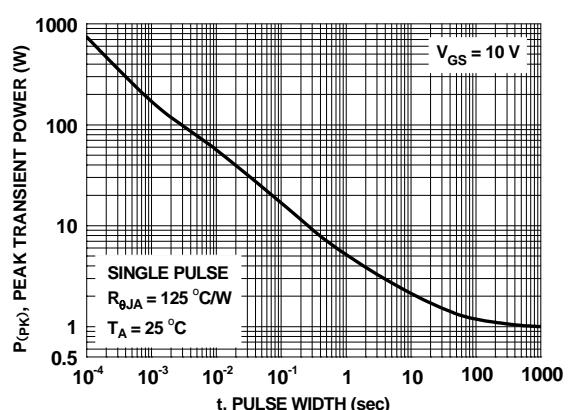
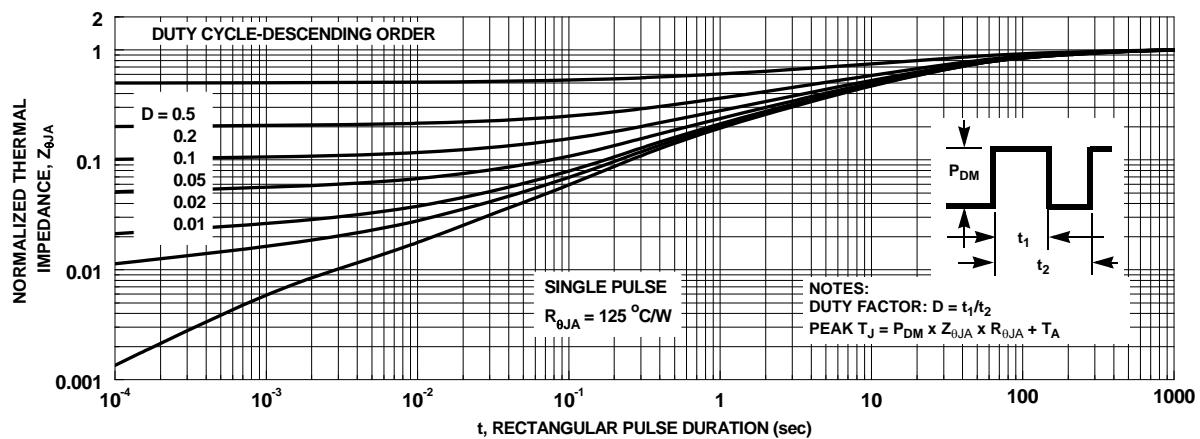
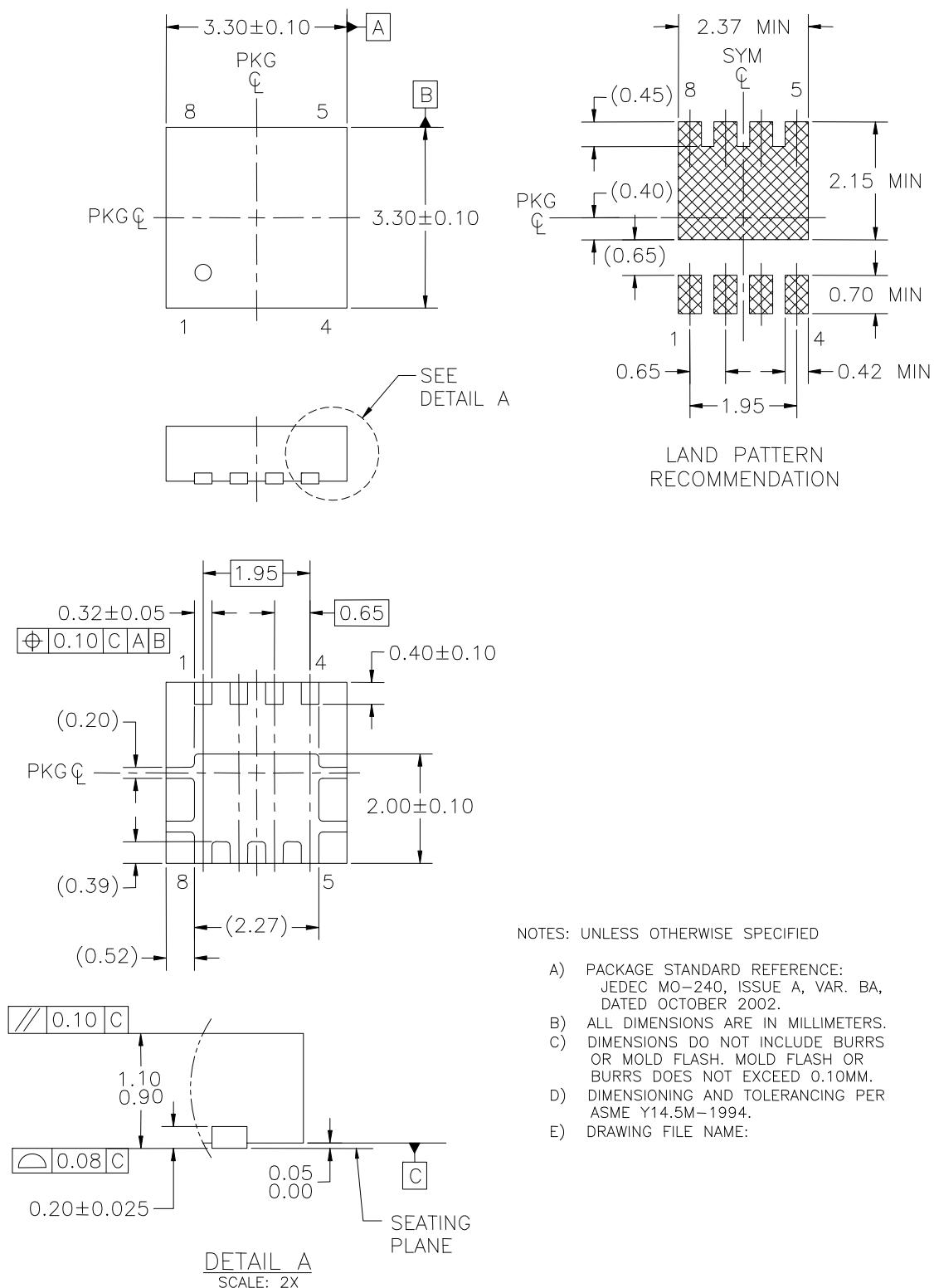


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

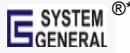


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