Data Sheet

CADEKA
Amplify the Human Experience

Comlinear® CLC1007, CLC2007, CLC4007

Single, Dual, and Quad, Low Cost, High Speed RRO Amplifier

Comlinear CLC1007, CLC2007, CLC4007 Rev - 1

FEATURES

- 260MHz bandwidth
- Fully specified at +3V, +5V and +/-5V supplies
- Output voltage range: 0.03V to 4.95V; V_S = +5; R_L = 2kΩ
- Input voltage range: -0.3V to +4.1V; V_S = +5
- 220V/μs slew rate
- 2.6mA supply current per amplifier
- ±100mA linear output current
- ±125mA short circuit current
- CLC2007 directly replaces AD8052, AD8042 and AD8092
- CLC1007 directly replaces AD8051, AD8041 and AD8091

APPLICATIONS

- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Telecom and optical terminals
- Video driver

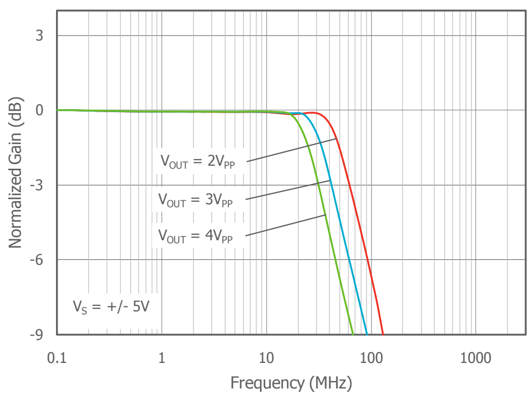
General Description

The COMLINEAR CLC1007 (single), CLC2007 (dual) and CLC4007(quad) are low cost, voltage feedback amplifiers. These amplifiers are designed to operate on +3V to +5V, or ±5V supplies. The input voltage range extends 300mV below the negative rail and 0.9V below the positive rail.

The CLC1007, CLC2007, and CLC4007 offer superior dynamic performance with a 260MHz small signal bandwidth and 220V/μs slew rate. The combination of low power, high output current drive, and rail-to-rail performance make these amplifiers well suited for battery-powered communication/computing systems and video applications

The combination of low cost and high performance make the CLC1007, CLC2007, and CLC4007 suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, and color copiers and video transmission.

Large Signal Frequency Response at +/-5V



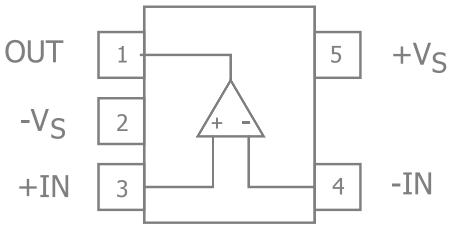
Ordering Information

Part Number	Package	MSL Rating	Pb-Free	RoHS Compliant	Operating Termperature	Packaging Method
CLC1007ISO8	SOIC-8	MSL-3	Yes	Yes	-40°C to +125°C	Reel
CLC1007ISTX	TSOT-5	MSL-1	Yes	Yes	-40°C to +125°C	Reel
CLC2007ISO8	SOIC-8	MSL-3	Yes	Yes	-40°C to +125°C	Rail
CLC2007ISO8X	SOIC-8	MSL-3	Yes	Yes	-40°C to +125°C	Reel
CLC2007IMP8X*	MSOP-8	MSL-1	Yes	Yes	-40°C to +125°C	Reel
CLC4007ISO14	SOIC-14	MSL-3	Yes	Yes	-40°C to +125°C	Rail
CLC4007ISO14X	SOIC-14	MSL-3	Yes	Yes	-40°C to +125°C	Reel
CLC4007ITP14*	TSSOP-14	TBD	Yes	Yes	-40°C to +125°C	Rail
CLC4007ITP14X*	TSSOP-14	TBD	Yes	Yes	-40°C to +125°C	Reel

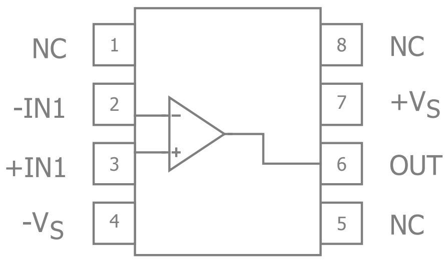
*Advance Information, contact CADEKA for availability.

CLC1007 Pin Configurations

TSOT-5



SOIC-8



CLC1007 Pin Assignments

TSOT-5

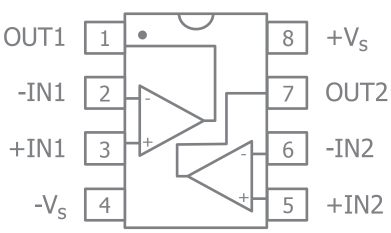
Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

SOIC-8

Pin No.	Pin Name	Description
1	NC	No Connect
2	-IN	Negative input
3	+IN	Positive input
4	$-V_S$	Negative supply
5	NC	No Connect
6	OUT	Negative input
7	$+V_S$	Positive supply
8	NC	No Connect

CLC2007 Pin Configuration

SOIC-8 / MSOP-8



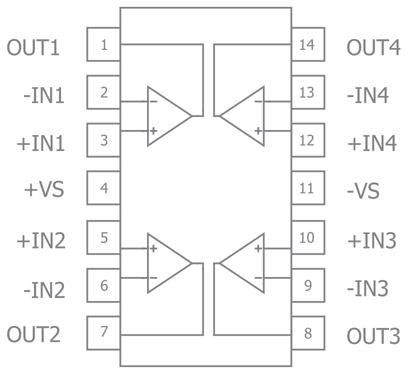
CLC2007 Pin Assignments

SOIC-8 / MSOP-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

CLC4007 Pin Configuration

SOIC/TSSOP



CLC4007 Pin Assignments

SOIC/TSSOP

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	+14	V
Input Voltage Range	$-V_S$-0.5V	$+V_S$+0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		170	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
8-Lead MSOP		139		°C/W
8-Lead SOIC		100		°C/W
14-Lead SOIC		88		°C/W
14-Lead TSSOP		96		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	CLC1007		CLC2007		CLC4007	
	TSOT-5	SOIC-8	MSOP-8	SOIC-8	TSSOP-14	SOIC-14
Human Body Model (HBM)	1kV	TBD	TBD	1kV	TBD	TBD
Charged Device Model (CDM)	2kV	TBD	TBD	2kV	TBD	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+125	°C
Supply Voltage Range	2.7		12.6	V

Electrical Characteristics at +3V

T_A = 25°C, R_f = 1.5kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		90		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.2V_{pp} , R_F = 0		245		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.2V_{pp}		85		MHz
$f_{0.1dB}$	0.1dB gain flatness	V_{OUT} = 0.2V_{pp}, R_L=150Ω		16		MHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}		55		MHz
DG	Differential Gain	DC-coupled Ouput		0.03		%
		AC-coupled Ouput		0.04		%
DP	Differential Phase	DC-coupled Ouput		0.03		°
		AC-coupled Ouput		0.06		°
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%)		5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		25		ns
OS	Overshoot	V_{OUT} = 0.2V step		8		%
SR	Slew Rate	G=-1, 2V step		175		V/µs
Distortion/Noise Response						
THD	Total Harmonic Distortion	1MHz, Vout=1Vpp		75		dBc
e_n	Input Voltage Noise	> 50kHz		16		nV/√Hz
X_{TALK}	Crosstalk	f=5MHz		58		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.5		mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			1.4		µA
dI_b	Average Drift			2		nA/°C
I_{os}	Input Offset Current			0.05		µA
PSRR	Power Supply Rejection Ratio	DC		102		dB
A_{OL}	Open-Loop Gain	R_L = 2kΩ[(2)]		92		dB
I_S	Supply Current	per channel		2.6		mA
Input Characteristics						
C_{IN}	Input Capacitance			0.5		pF
CMIR	Common Mode Input Range			-0.3 to 2.1		V
CMRR	Common Mode Rejection Ratio	DC , V_{cm}=0V to 1.5V		100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 150Ω		0.3 to 2.75		V
		R_L = 2kΩ		0.02 to 2.96		V
I_{OUT}	Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±125		mA
V_S	Power Supply Operationg Range			2.7 to 12		V

Notes:

1. 100% tested at 25°C
2. Guranteed by characterization, simulation or statistical anlysis

Electrical Characteristics at +5V

T_A = 25°C, R_f = 1.5kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		95		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.2V_{pp} , R_F = 0		250		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.2V_{pp}		85		MHz
$f_{0.1dB}$	0.1dB gain flatness	V_{OUT} = 0.2V_{pp}, R_L=150Ω		35		MHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}		65		MHz
DG	Differential Gain	DC-coupled Ouput		0.03		%
		AC-coupled Ouput		0.04		%
DP	Differential Phase	DC-coupled Ouput		0.03		°
		AC-coupled Ouput		0.06		°
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		25		ns
OS	Overshoot	V_{OUT} = 0.2V step		5		%
SR	Slew Rate	G=-1 , 4V step,		220		V/μs
Distortion/Noise Response						
THD	Total Harmonic Distortion	1MHz, V_{OUT}=2V_{PP}		-75		dB
e_n	Input Voltage Noise	> 50kHz		16		nV/√Hz
X_{TALK}	Crosstalk	f=5MHz		58		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-7	0.5	7	mV
dV_{IO}	Average Drift			5		μV/°C
I_b	Input Bias Current (1)		-2	1.4	2	μA
dI_b	Average Drift			2		nA/°C
I_{os}	Input Offset Current (1)		-0.75	0.05	0.75	μA
PSRR	Power Supply Rejection Ratio (1)	DC	80	102		dB
A_{OL}	Open-Loop Gain	R_L = 2kΩ(2)	80	92		dB
I_S	Supply Current (1)	per channel		2.6	4	mA
Input Characteristics						
C_{IN}	Input Capacitance			0.5		pF
CMIR	Common Mode Input Range			-0.3 to 4.1		V
CMRR	Common Mode Rejection Ratio (1)	DC , V_{cm}= 0V to 3.5V	75	100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 150Ω(1)	4.65	0.1 to 4.9	0.35	V
		R_L = 2kΩ		0.03 to 4.95		V
I_{OUT}	Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		±125		mA
V_S	Power Supply Operationg Range			2.7 to 12		V

Notes:

1. 100% tested at 25°C
2. Guranteed by characterization, simulation or statistical anlysis

Electrical Characteristics at ±5V

T_A = 25°C, R_f = 1.5kΩ, R_L = 2kΩ to GND, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		90		MHz
UGBW	Unity Gain Bandwidth	V_{OUT} = 0.2V_{pp} , R_F = 0		260		MHz
BW_{SS}	-3dB Bandwidth	V_{OUT} = 0.2V_{pp}		85		MHz
$f_{0.1dB}$	0.1dB gain flatness	V_{OUT} = 0.2V_{pp}, R_L=150Ω		22		MHz
BW_{LS}	Large Signal Bandwidth	V_{OUT} = 2V_{pp}		65		MHz
DG	Differential Gain	DC-coupled Ouput		0.03		%
		AC-coupled Ouput		0.04		%
DP	Differential Phase	DC-coupled Ouput		0.03		°
		AC-coupled Ouput		0.06		°
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step, R_L = 100Ω		25		ns
OS	Overshoot	V_{OUT} = 0.2V step		5		%
SR	Slew Rate	G=-1 , 5V step		225		V/µs
Distortion/Noise Response						
THD	Total Harmonic Distortion	1MHz, V_{OUT}=2V_{PP}		76		dBc
e_n	Input Voltage Noise	> 50kHz		16		nV/√Hz
X_{TALK}	Crosstalk	f=5MHz		58		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.5		mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			1.3		µA
dI_b	Average Drift			2		nA/°C
I_{os}	Input Offset Current			0.04		µA
PSRR	Power Supply Rejection Ratio	DC		102		dB
A_{OL}	Open-Loop Gain	R_L = 2kΩ (2)		92		dB
I_S	Supply Current	per channel		2.6		mA
Input Characteristics						
C_{IN}	Input Capacitance			0.5		pF
CMIR	Common Mode Input Range			-5.3 to 4.1		V
CMRR	Common Mode Rejection Ratio (1)	DC , V_{cm}= -5V to 3.5V		100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 150Ω		-4.8 to 4.8		V
		R_L = 2kΩ		-4.95 to 4.93		V
I_{OUT}	Output Current			+/ -100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		+/-125		mA
V_S	Power Supply Operationg Range			2.7 to 12		V

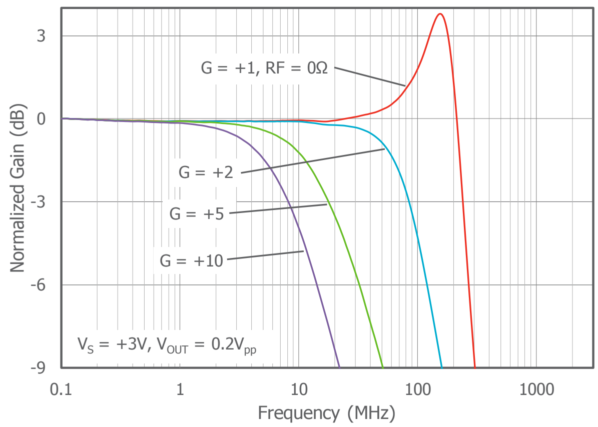
Notes:

1. 100% tested at 25°C
2. Guranteed by characterization, simulation or statistical anlysis

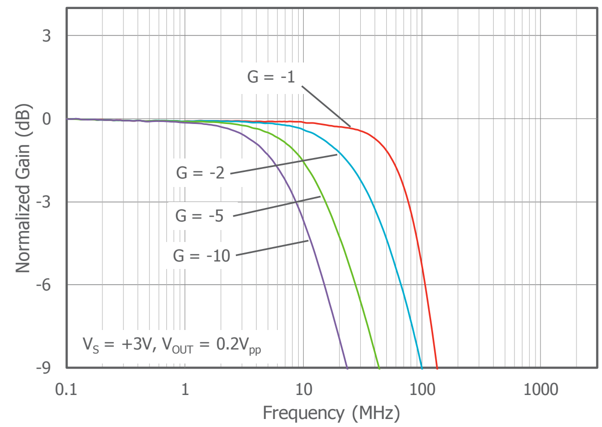
Typical Performance Characteristics

TA = 25°C, V_S = +3V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

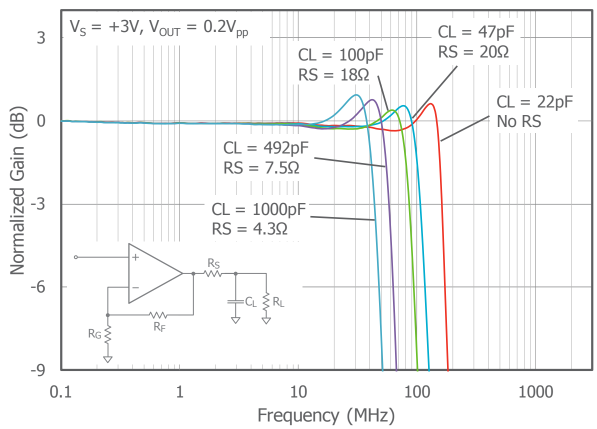
Non-Inverting Freq. Resp.



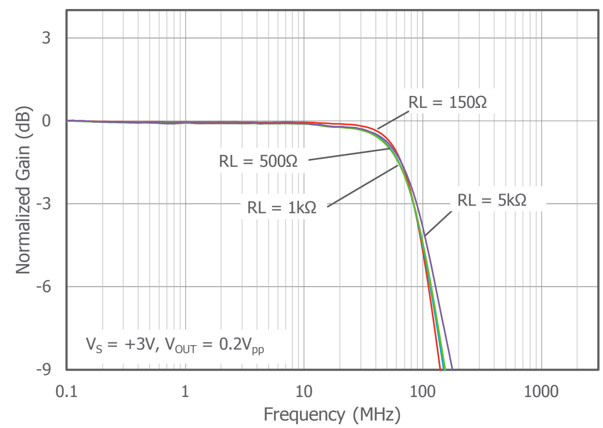
Inverting Freq. Resp.



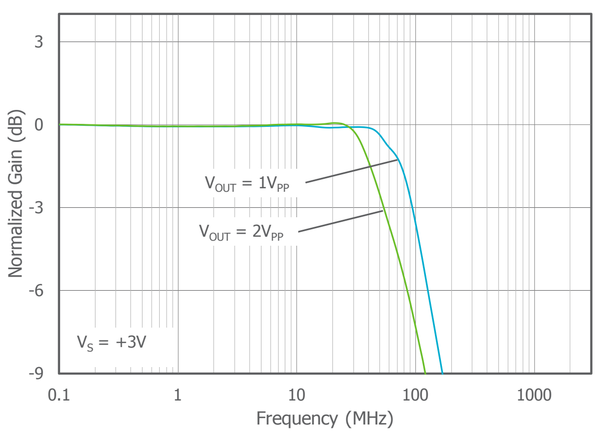
Freq. Resp. vs CL



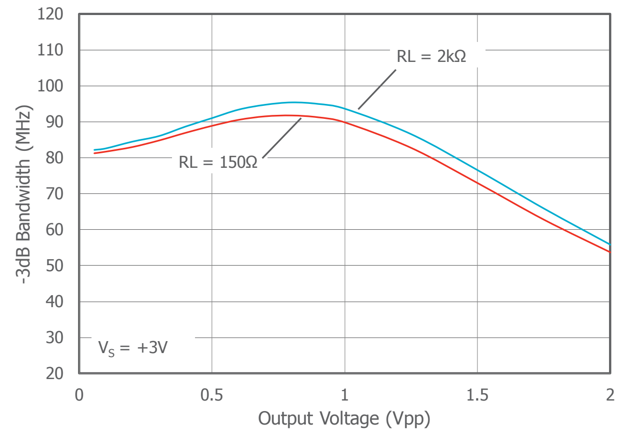
Freq. Resp. vs RL



Large Signal Freq. Resp.



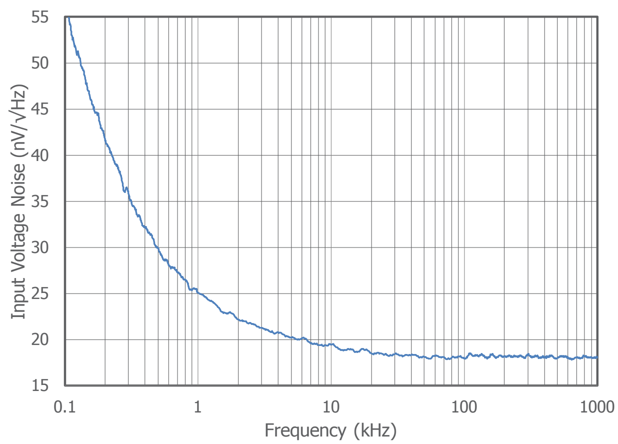
-3db BW vs Output Voltage



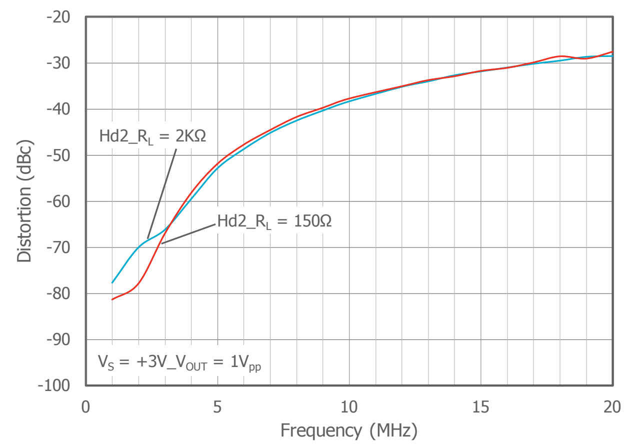
Typical Performance Characteristics

TA = 25°C, V_S = +3V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

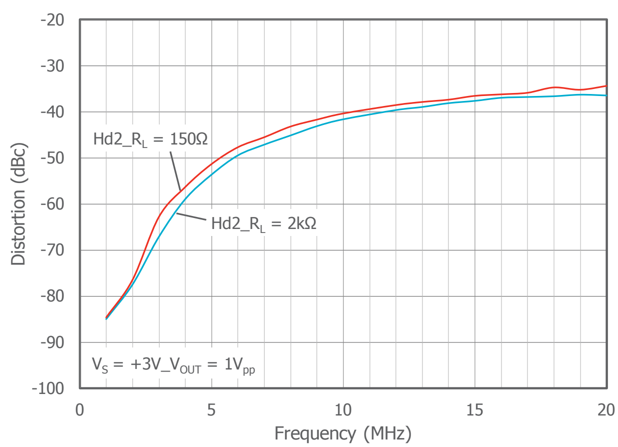
Input Voltage Noise vs Freq.



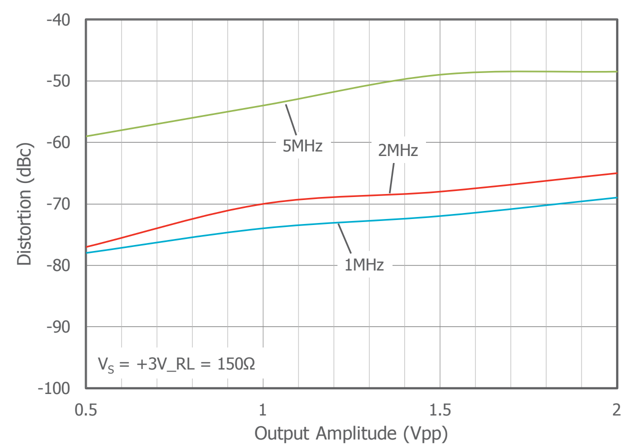
2nd Harmonic Distortion Vs RL over Freq.



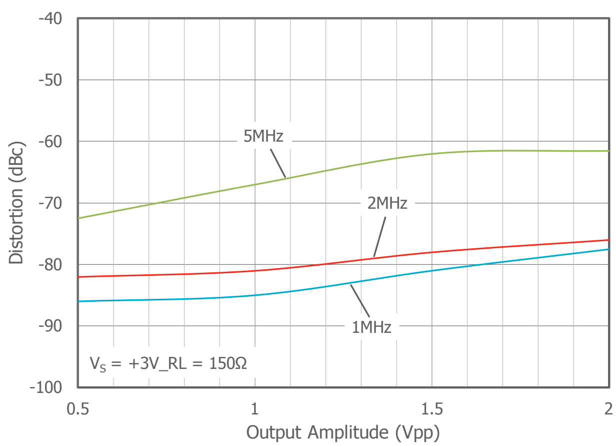
3rd Harmonic Distortion Vs RL over Freq.



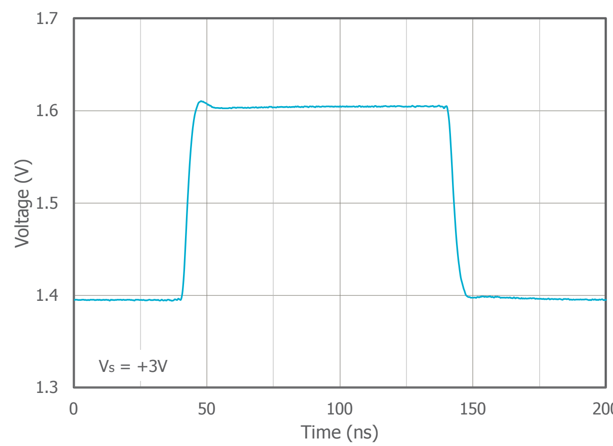
2nd Harmonic Distortion Vs Vo over Freq.



3rd Harmonic Distortion Vs Vo over Freq.



Non-Inverting Small Signal Pulse Response

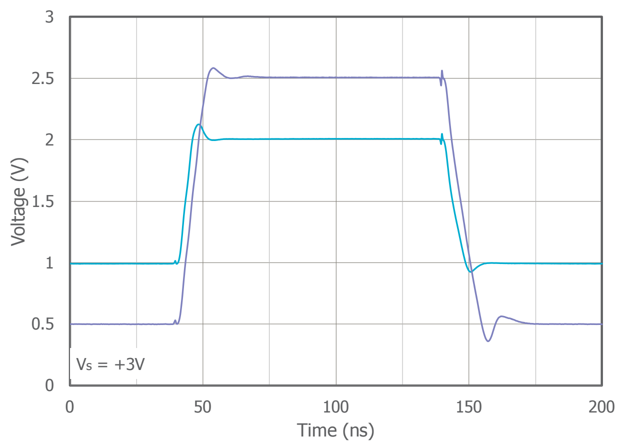


Comlinear CLC1007, CLC2007, CLC4007 Rev - 1

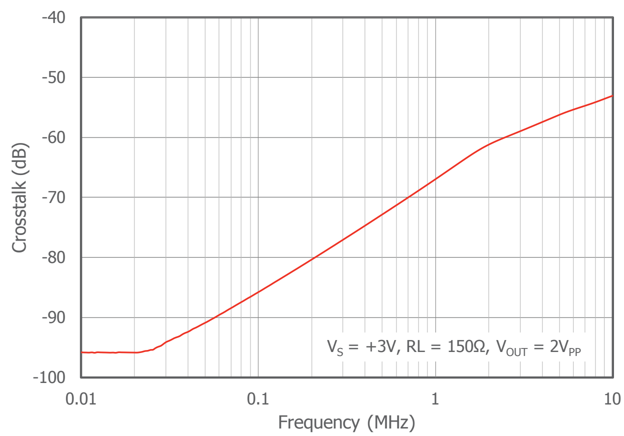
Typical Performance Characteristics

TA = 25°C, V_S = +3V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

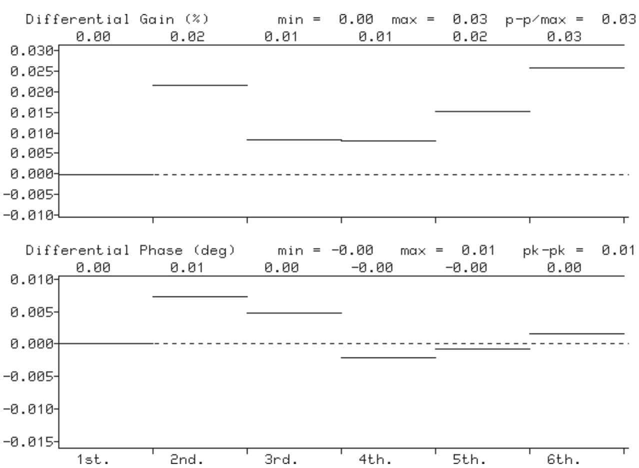
Non-Inverting Large Signal Pulse Response



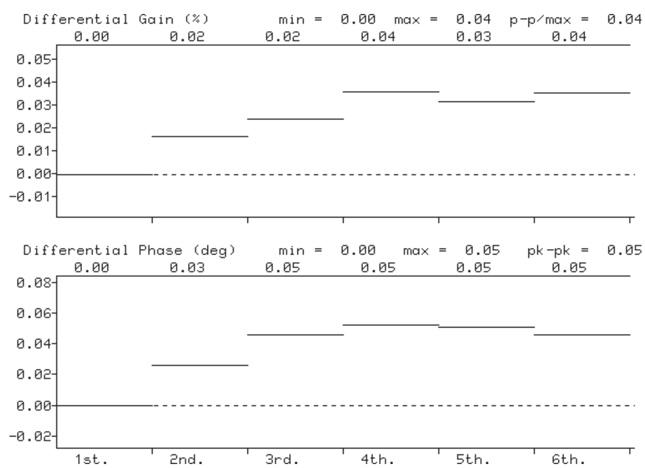
Crosstalk vs Frequency



Differential Gain & Phase_DC Coupled



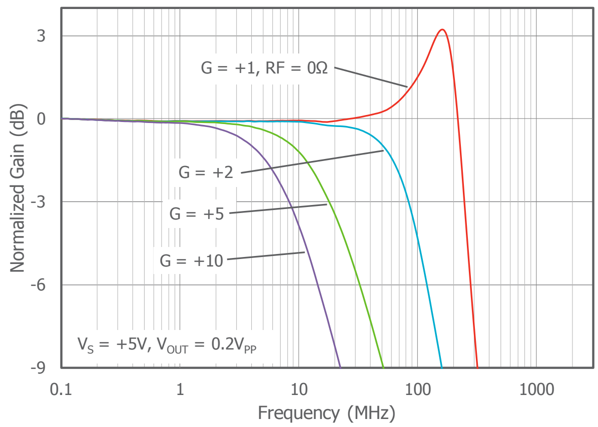
Differential Gain & Phase_AC Coupled



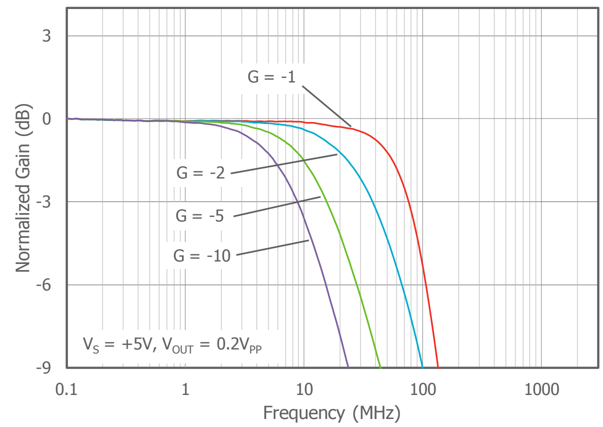
Typical Performance Characteristics

TA = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

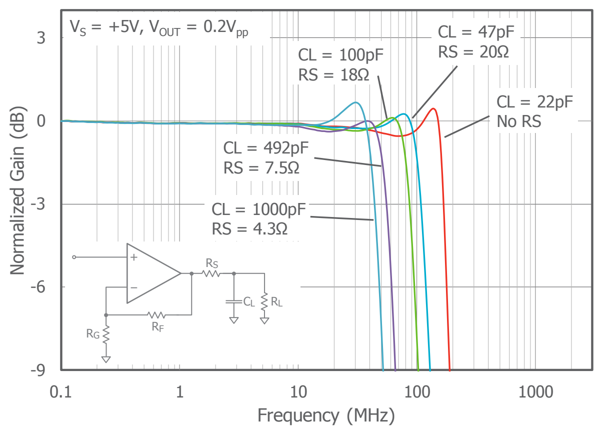
Non-Inverting Freq. Resp.



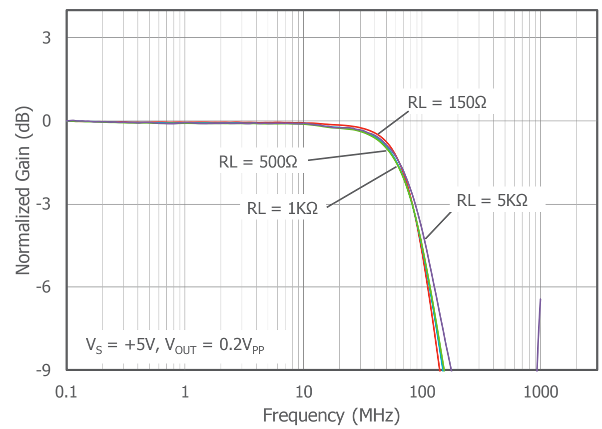
Inverting Freq. Resp.



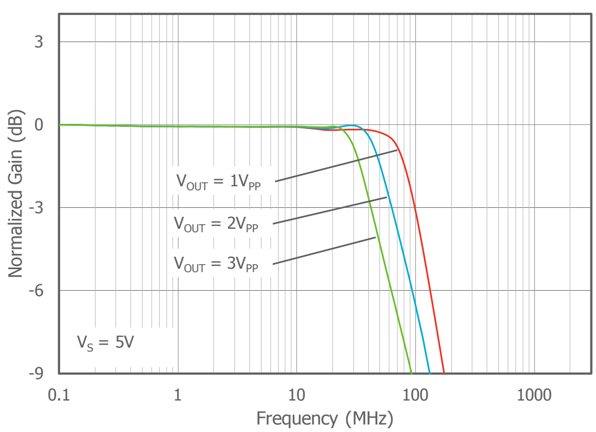
Freq. Resp. vs CL



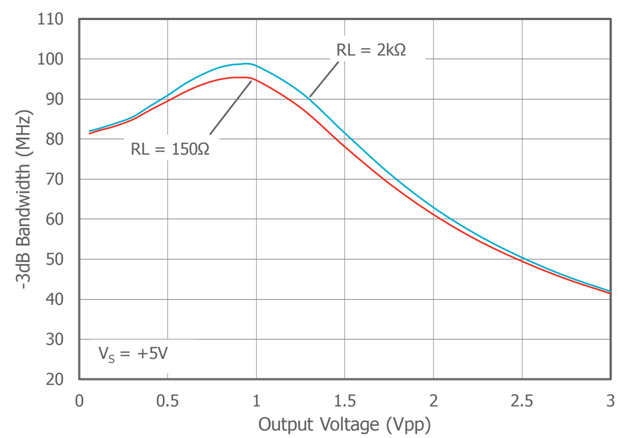
Freq. Resp. vs RL



Large Signal Freq. Resp.



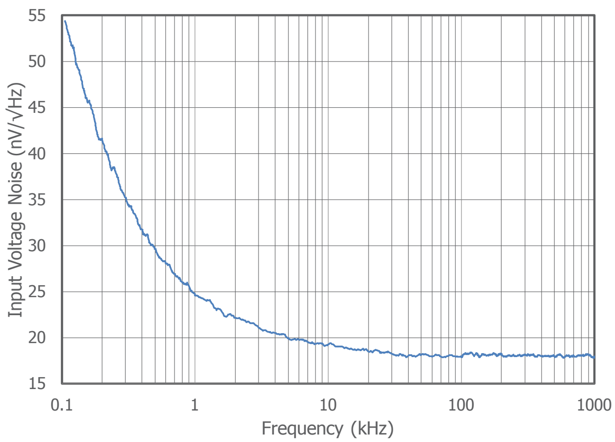
-3db BW vs Output Voltage



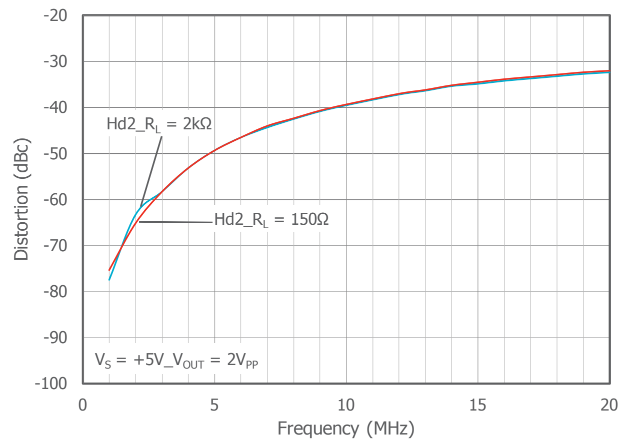
Typical Performance Characteristics

TA = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

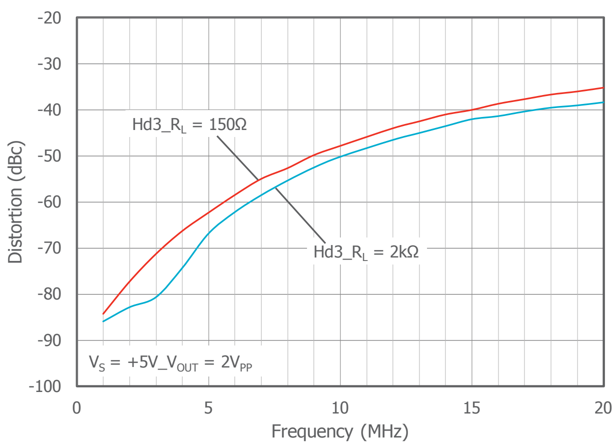
Input Voltage Noise vs Freq.



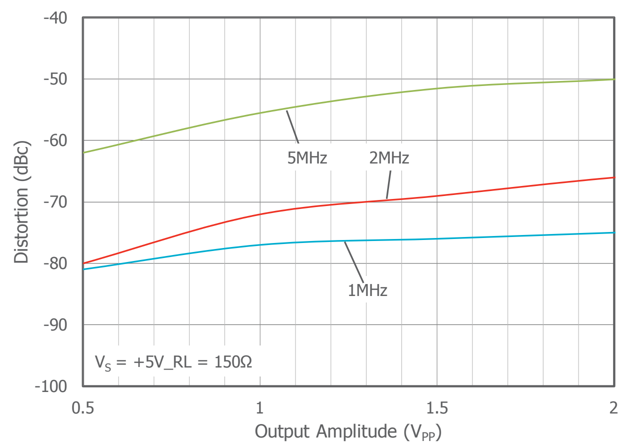
2nd Harmonic Distortion Vs RL over Freq.



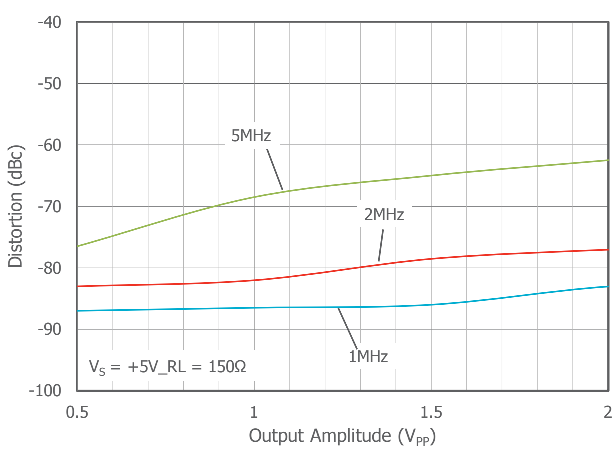
3rd Harmonic Distortion Vs RL over Freq.



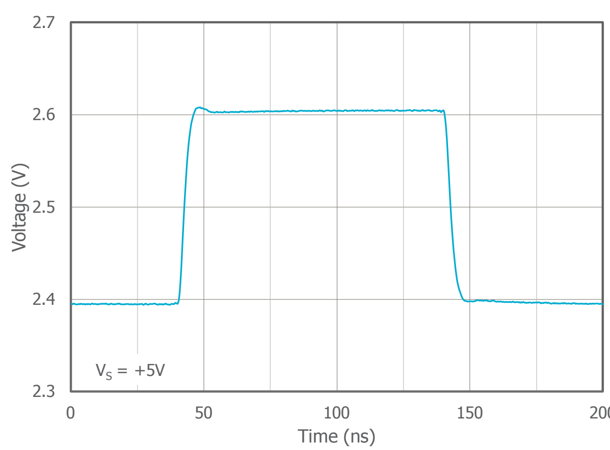
2nd Harmonic Distortion Vs Vo over Freq.



3rd Harmonic Distortion Vs Vo over Freq.



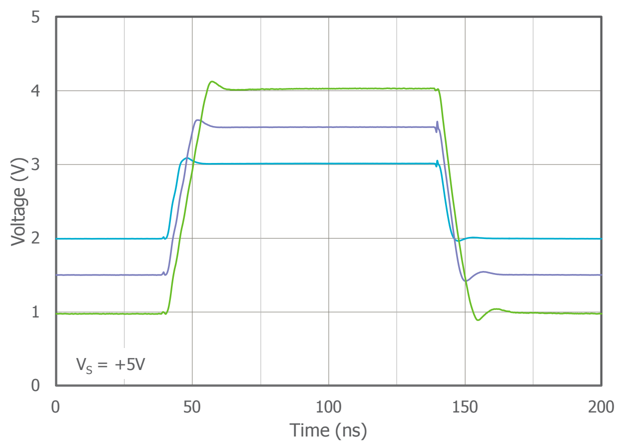
Non-Inverting Small Signal Pulse Response



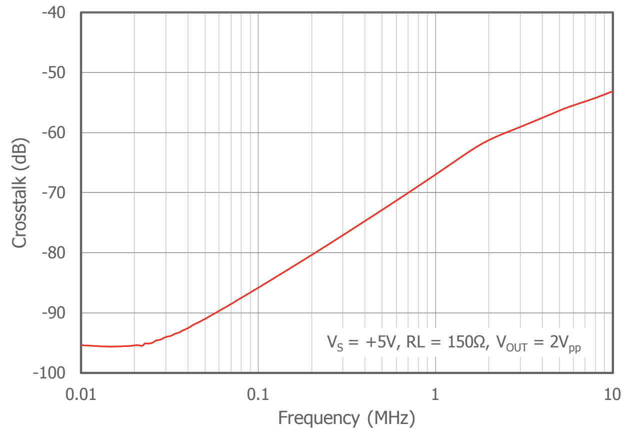
Typical Performance Characteristics

TA = 25°C, V_S = +5V, R_L = 2kΩ to V_S/2, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

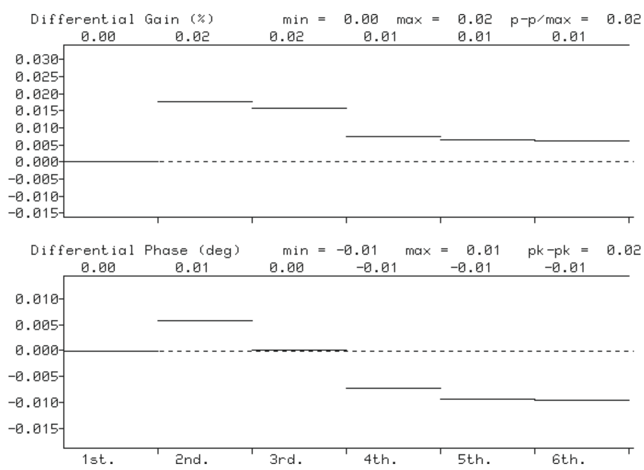
Non-Inverting Large Signal Pulse Response



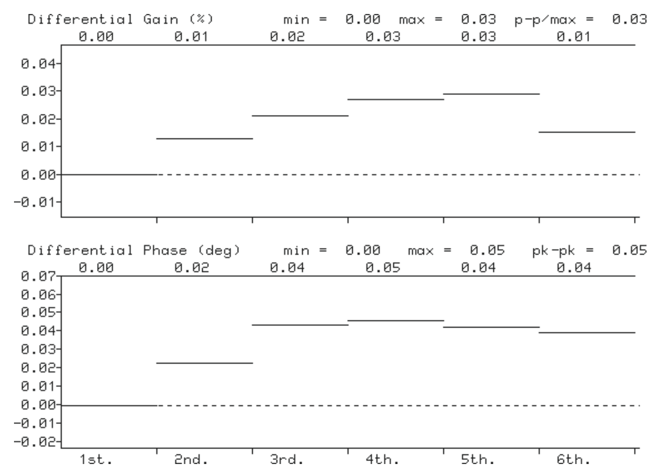
Crosstalk vs Frequency



Differential Gain & Phase_DC Coupled



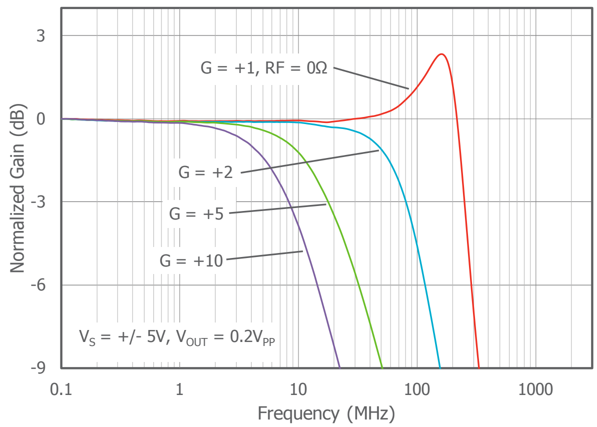
Differential Gain & Phase_AC Coupled



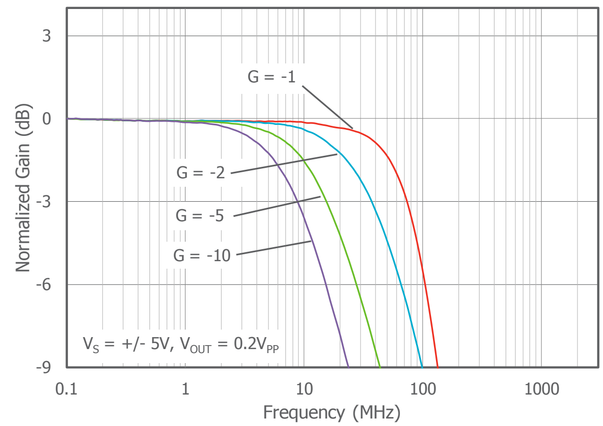
Typical Performance Characteristics

TA = 25°C, V_S = ±5V, R_L = 2kΩ to GND, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

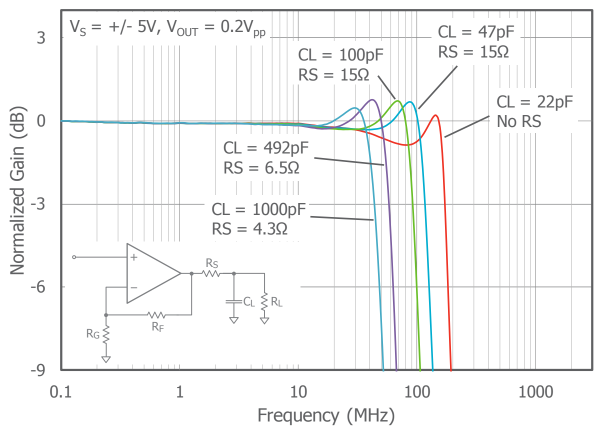
Non-Inverting Freq. Resp.



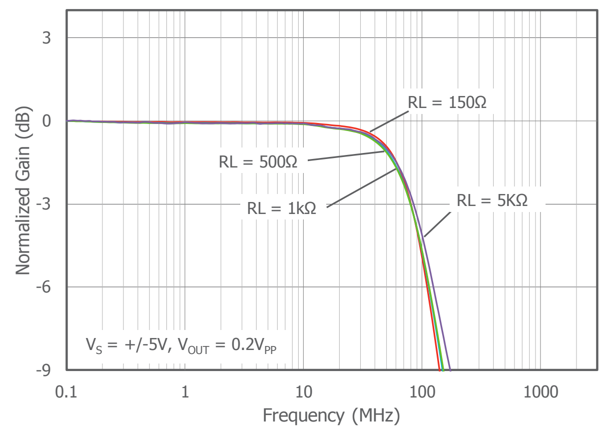
Inverting Freq. Resp.



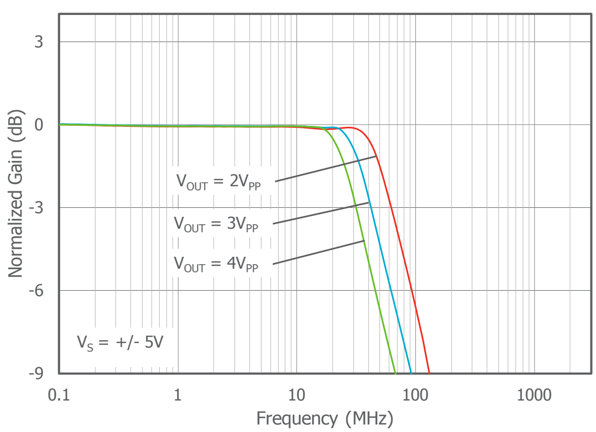
Freq. Resp. vs CL



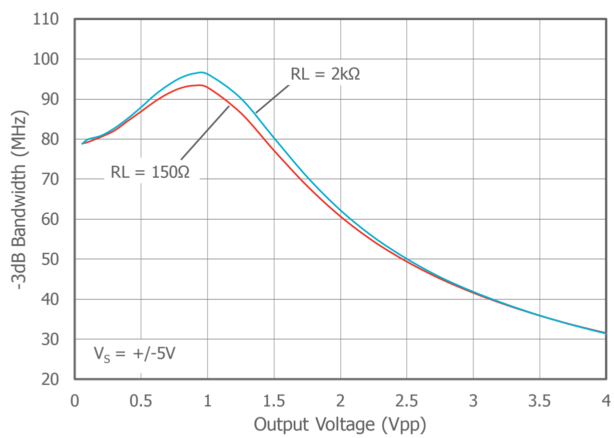
Freq. Resp. vs RL



Large Signal Freq. Resp.



-3db BW vs Output Voltage

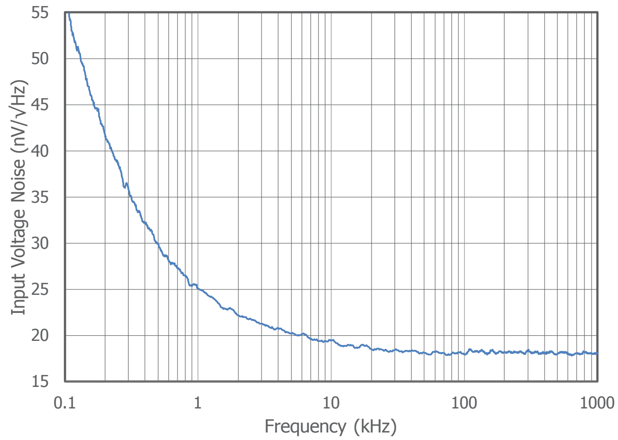


Comlinear CLC1007, CLC2007, CLC4007 Rev - 1

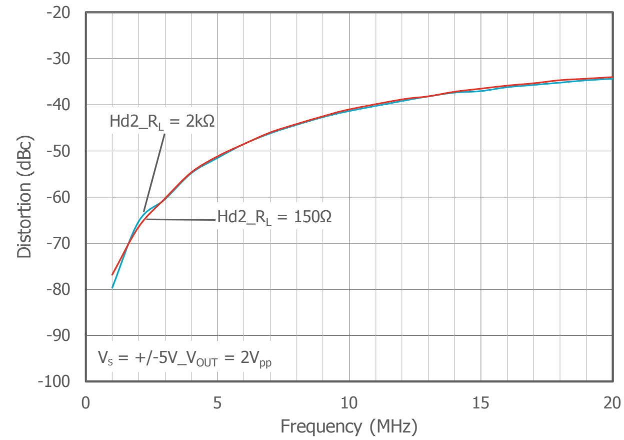
Typical Performance Characteristics

TA = 25°C, V_S = ±5V, R_L = 2kΩ to GND, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

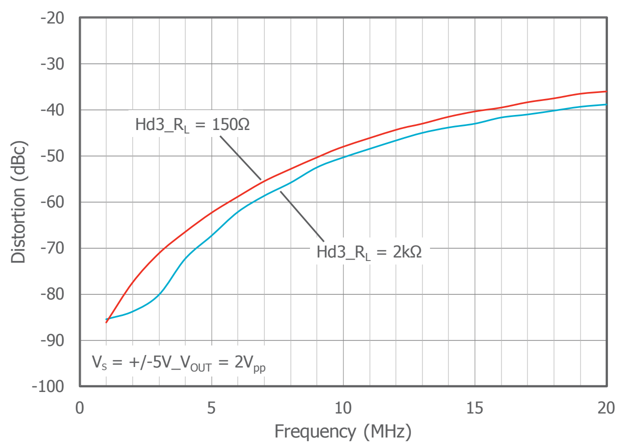
Input Voltage Noise vs Freq.



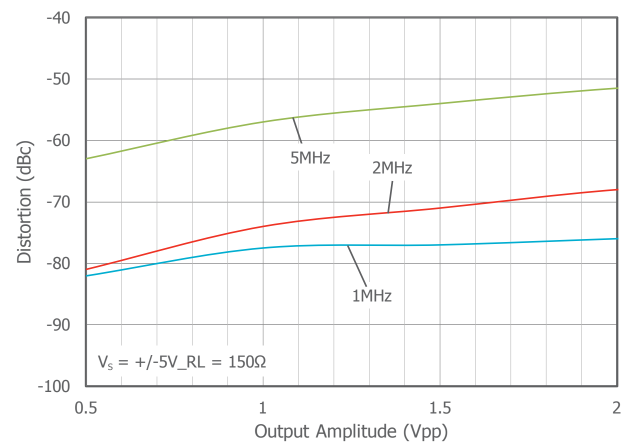
2nd Harmonic Distortion Vs RL over Freq.



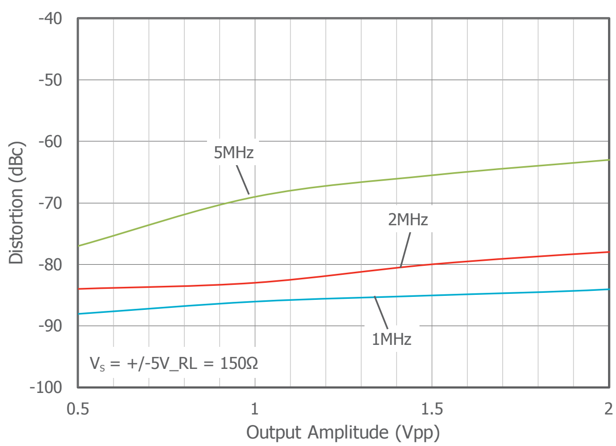
3rd Harmonic Distortion Vs RL over Freq.



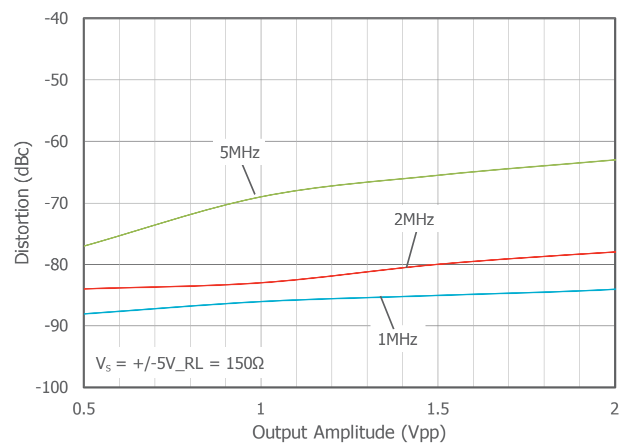
2nd Harmonic Distortion Vs Vo over Freq.



3rd Harmonic Distortion Vs Vo over Freq.



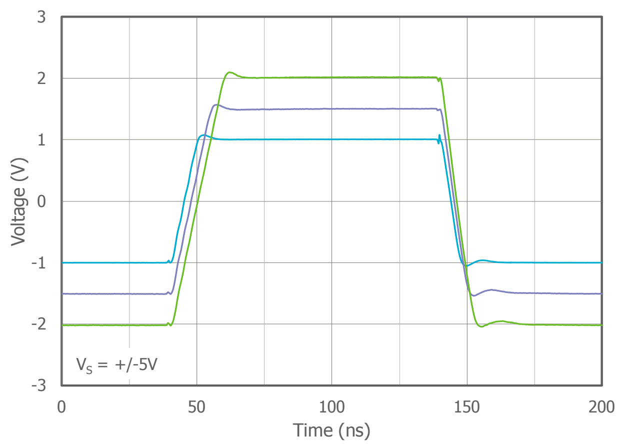
Non-Inverting Small Signal Pulse Response



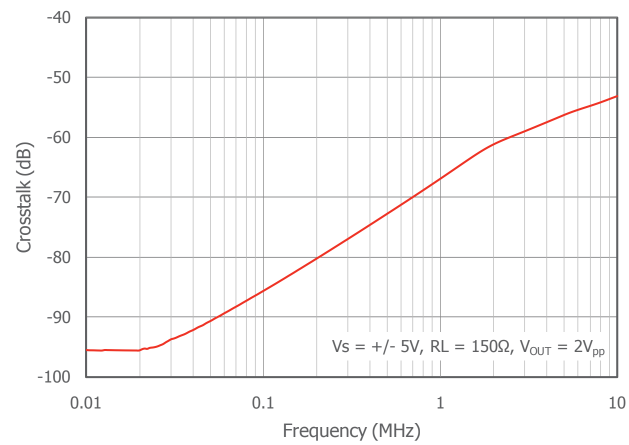
Typical Performance Characteristics

TA = 25°C, V_S = ±5V, R_L = 2kΩ to GND, A_V=+2, R_F=1.5kΩ ; unless otherwise noted.

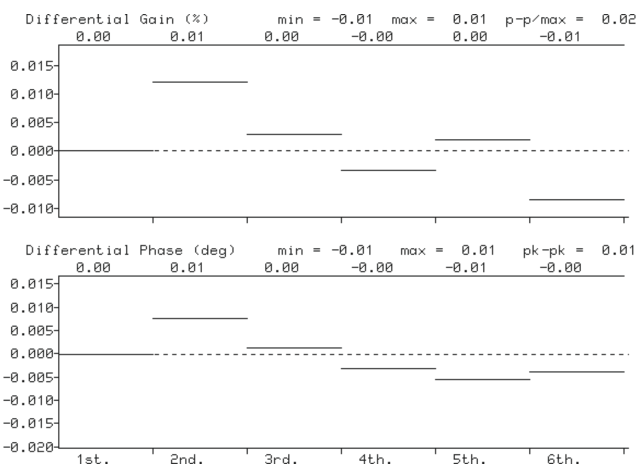
Non-Inverting Large Signal Pulse Response



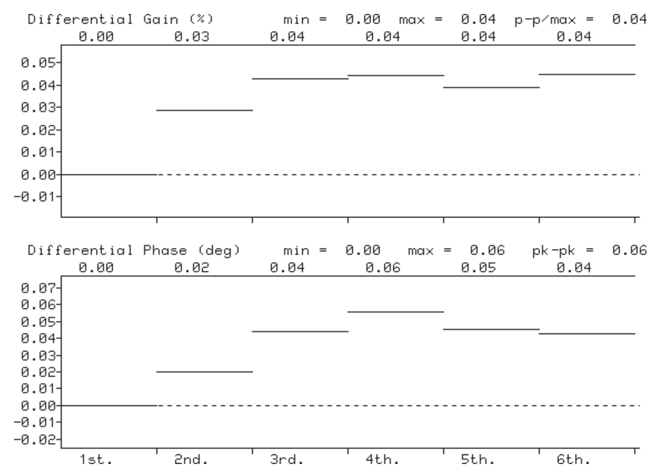
Crosstalk vs Frequency



Differential Gain & Phase_DC Coupled



Differential Gain & Phase_AC Coupled



Application Information

General Description

The CLC1007, CLC2007, and CLC4007 are single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process using a patent pending topography. They feature a rail-to-rail output stage and are unity gain stable.

The common mode input range extends to 300mV below ground and to 0.9V below V_S. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

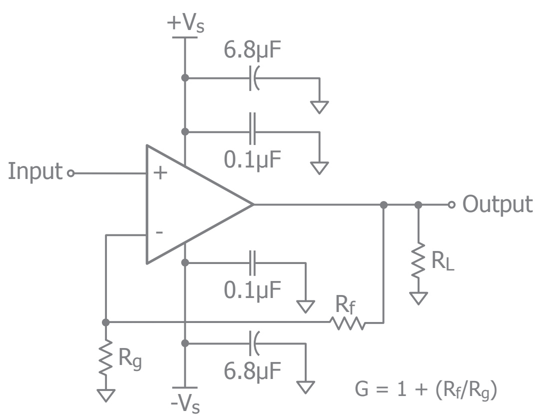


Figure 1. Typical Non-Inverting Gain Circuit

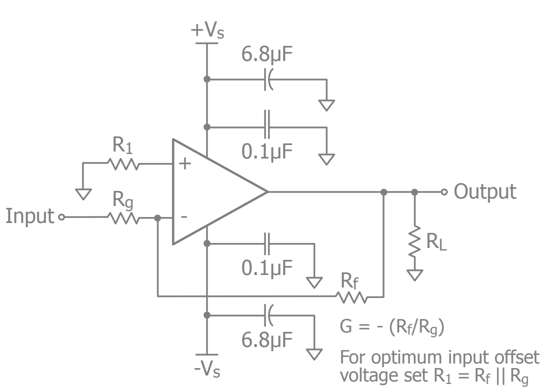


Figure 2. Typical Inverting Gain Circuit

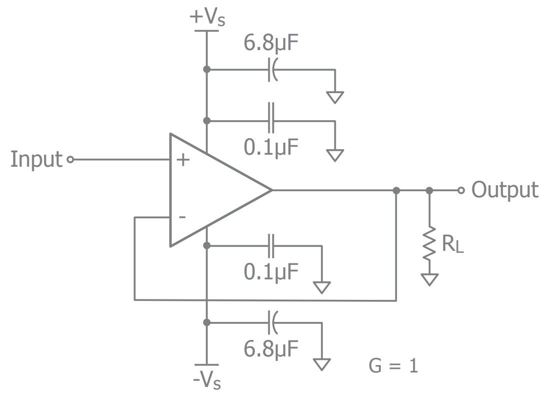


Figure 3. Unity Gain Circuit

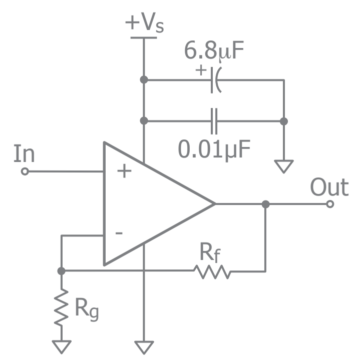


Figure 4. Single Supply Non-Inverting Gain Circuit

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC1007, CLC2007, and CLC4007 will typically recover in less than 20ns from an overdrive condition. Figure 5 shows the CLC2007 in an overdriven condition.

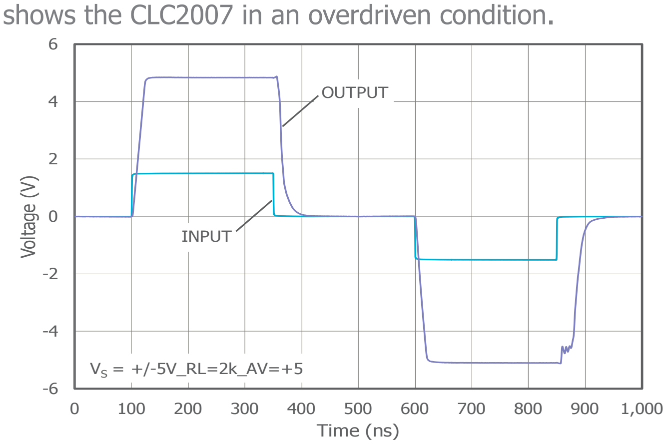


Figure 5: Overdrive Recovery

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 170°C. To calculate the junction temperature, the package thermal resistance value Theta$_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC1007 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

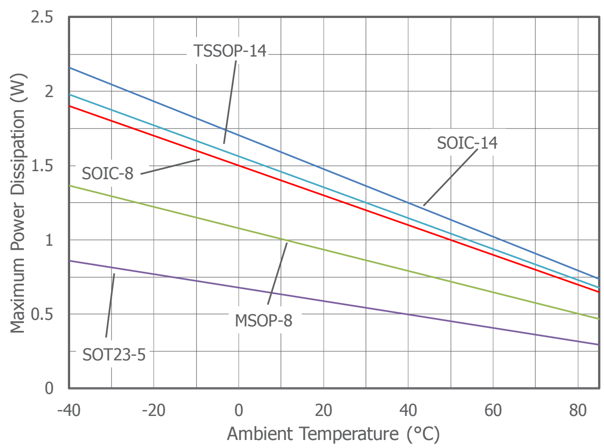


Figure 6. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 7.

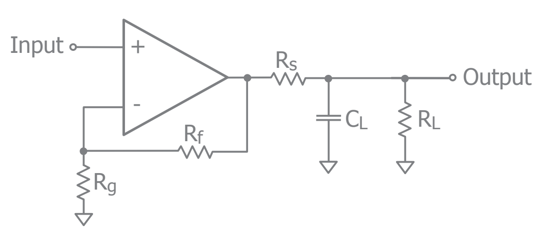


Figure 7. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response.

CL (Pf)	Rs (Ω)	-3db BW (MHz)
22pF	0	118
47pF	15	112
100pF	15	91
492pF	6.5	59

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1007 in TSOT-5
CEB003	CLC1007 in SOIC
CEB006	CLC2007 in SOIC
CEB010	CLC2007 in MSOP
CEB018	CLC4007 in SOIC

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 10-18. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

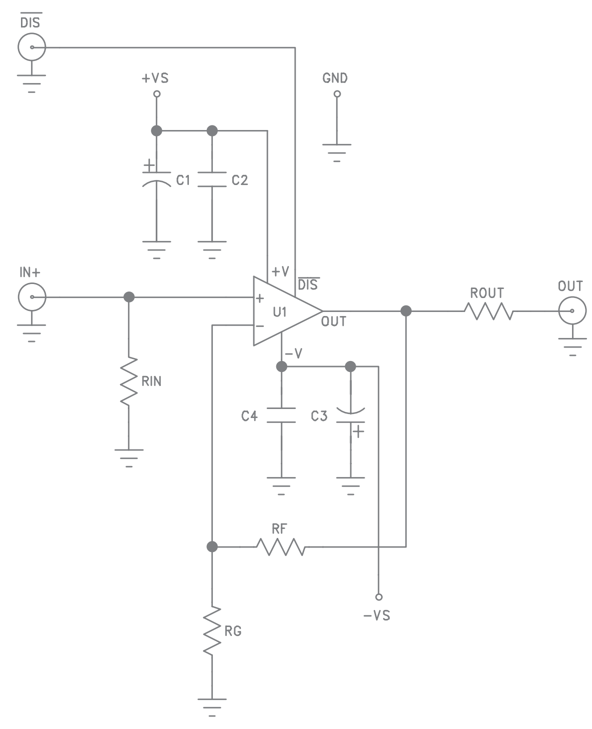


Figure 8. CEB002 & CEB003 Schematic

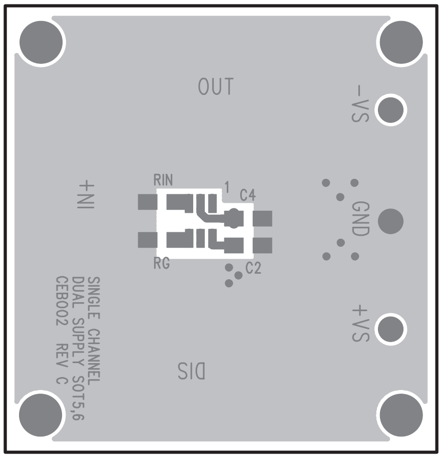


Figure 9. CEB002 Top View

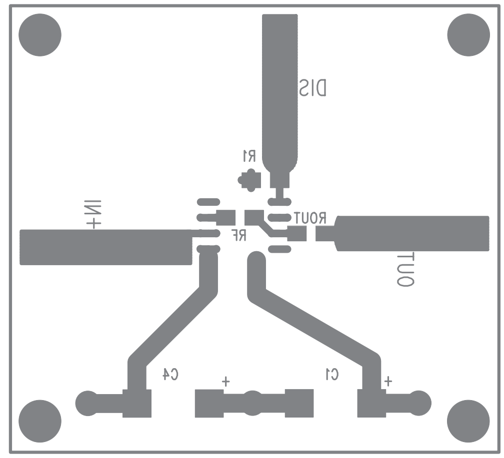


Figure 12. CEB003 Bottom View

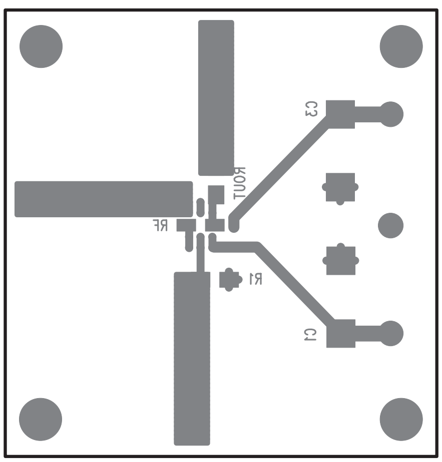


Figure 10. CEB002 Bottom View

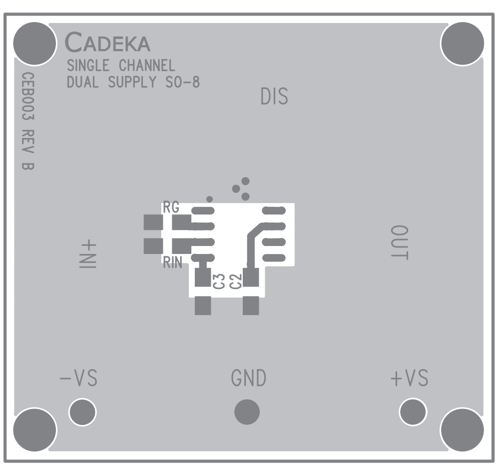


Figure 11. CEB003 Top View

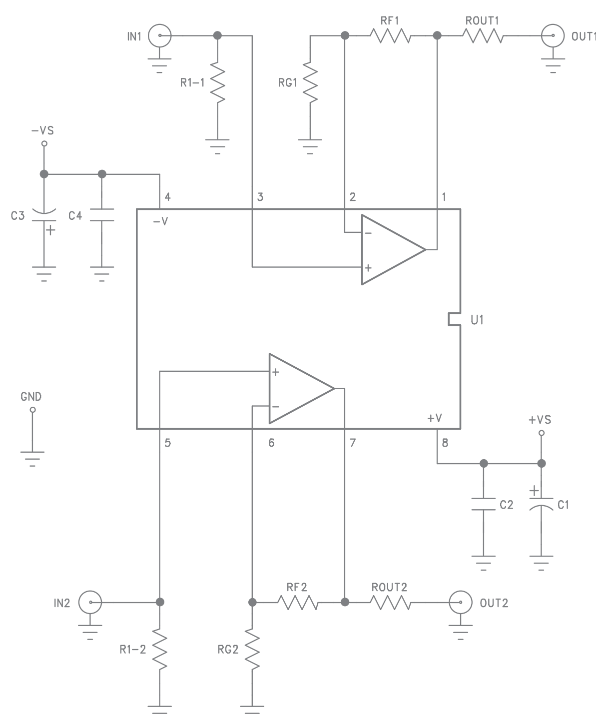


Figure 13. CEB006 & CEB010 Schematic

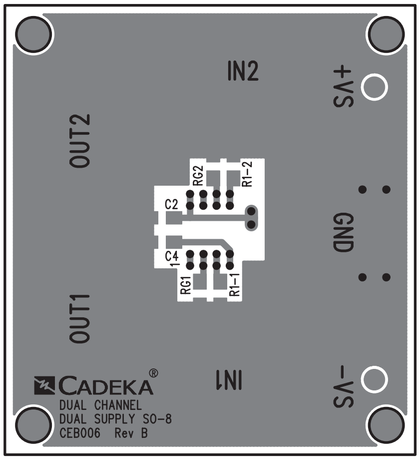


Figure 14. CEB006 Top View

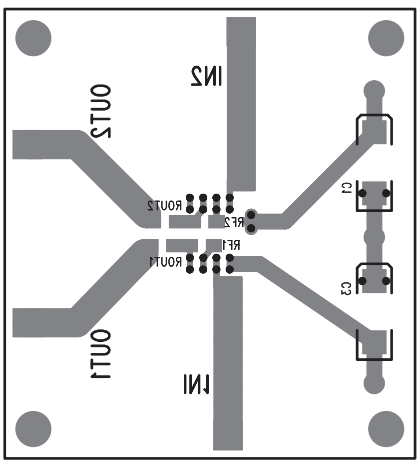


Figure 15. CEB006 Bottom View

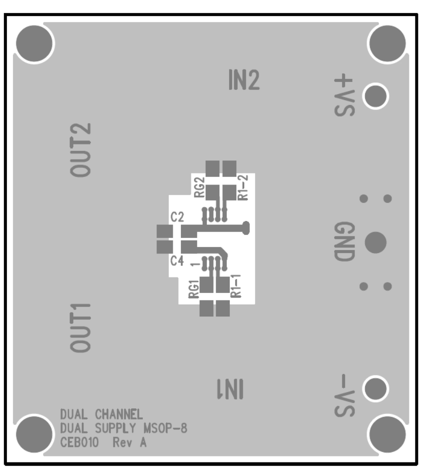


Figure 16. CEB010 Top View

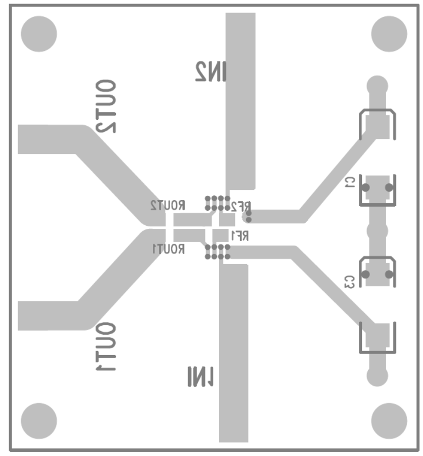


Figure 17. CEB010 Bottom View

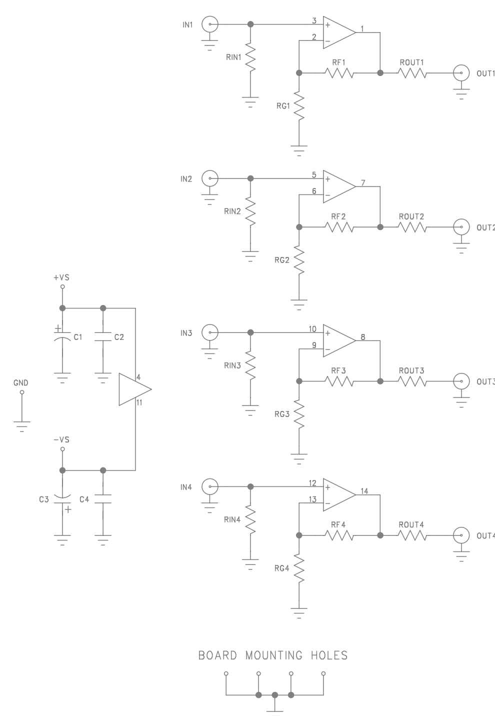


Figure 18. CEB018 Schematic

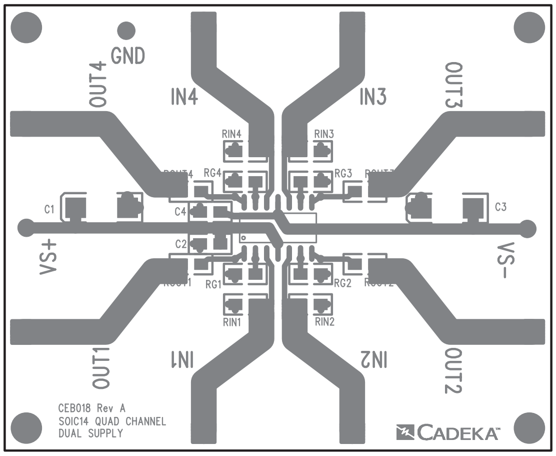


Figure 19. CEB018 Top View

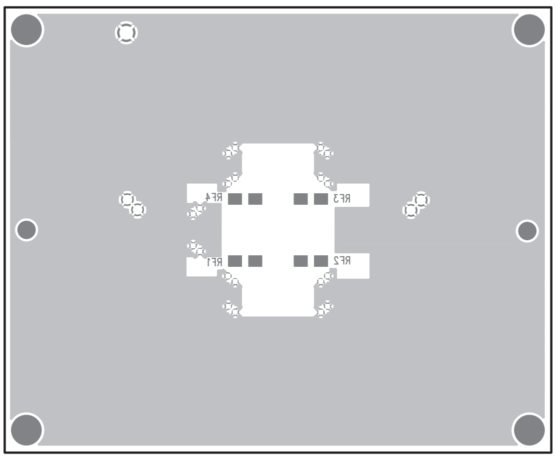
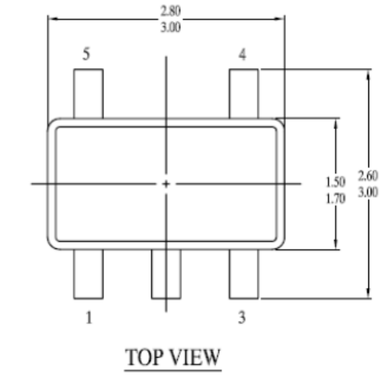


Figure 20. CEB018 Bottom View

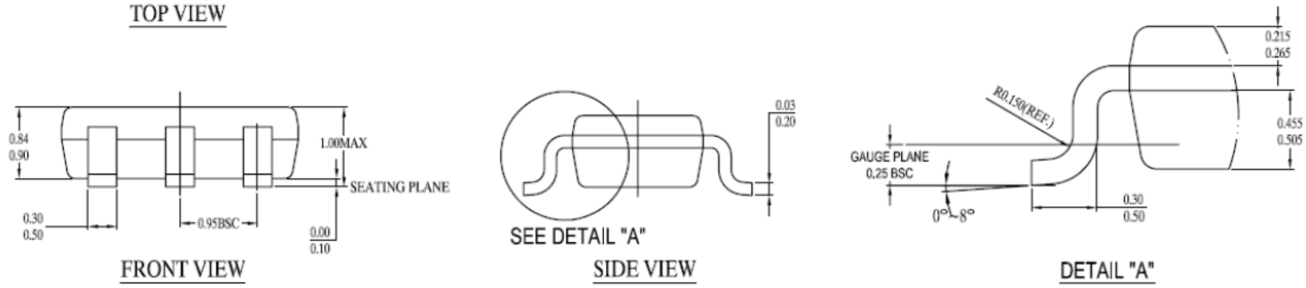
Mechanical Dimensions continued

TSOT-5 Package

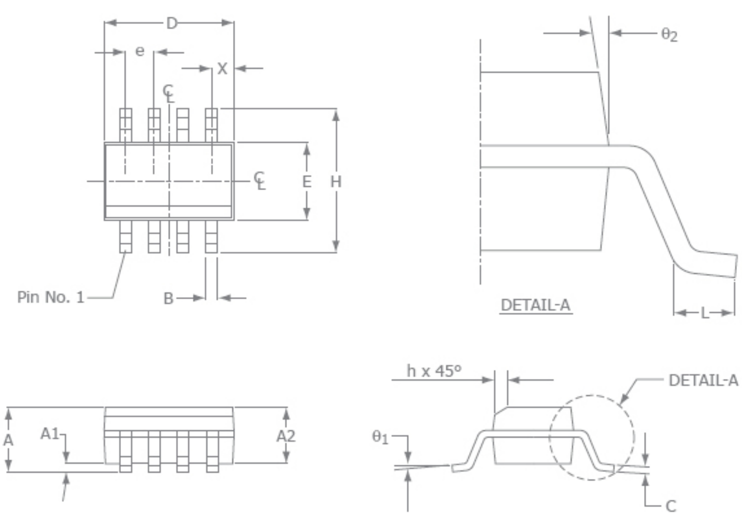


NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE INTERLEAD FALSH OR PROTRUSION
3. PACKAGE WIDTH DOES NOTINCLUDE INTERLEAD FALSH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFROMS TO JEDEC MO-193, VARIATION AA.
6. DRAWING IS NOT TO SCALE.



SOIC-8 Package



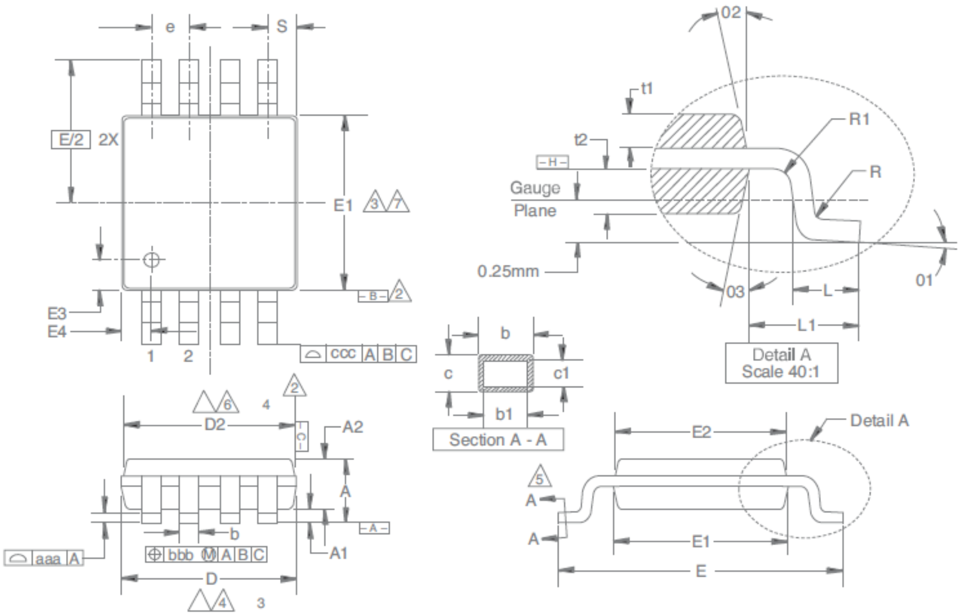
SOIC-8		
SYMBOL	**MIN**	**MAX**
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

Mechanical Dimensions continued

MSOP-8 Package



Symbol	Min	Max
A	1.10	–
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	+0.15/-0.06
R1	0.15	+0.15/-0.06
t1	0.31	±0.08
t2	0.41	±0.08
b	0.33	+0.07/-0.08
b1	0.30	±0.05
c	0.18	±0.05
c1	0.15	+0.03/-0.02
01	3.0°	±3.0°
02	12.0°	±3.0°
03	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	–
aaa	0.10	–
bbb	0.08	–
ccc	0.25	–
e	0.65 BSC	–
S	0.525 BSC	–

NOTE:

1 All dimensions are in millimeters (angle in degrees), unless otherwise specified.

2 Datums -B- and -C- to be determined at datum plane -H-.

3 Dimensions "D" and "E1" are to be determined at datum -H-.

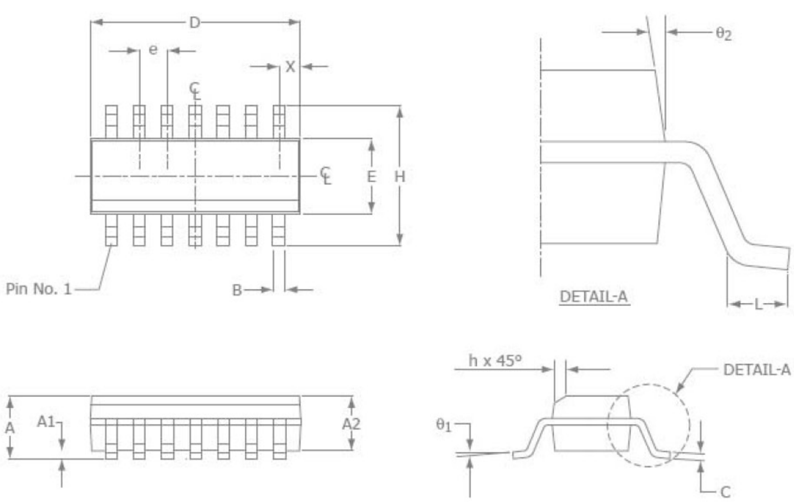
4 Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.

5 Cross sections A – A to be determined at 0.13 to 0.25mm from the leadtip.

6 Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.

7 Dimension "E1" and "E2" does not include interlead flash or protrusion.

SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	8.56	8.74
E	3.84	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.51 ref	
θ_2	7° BSC	

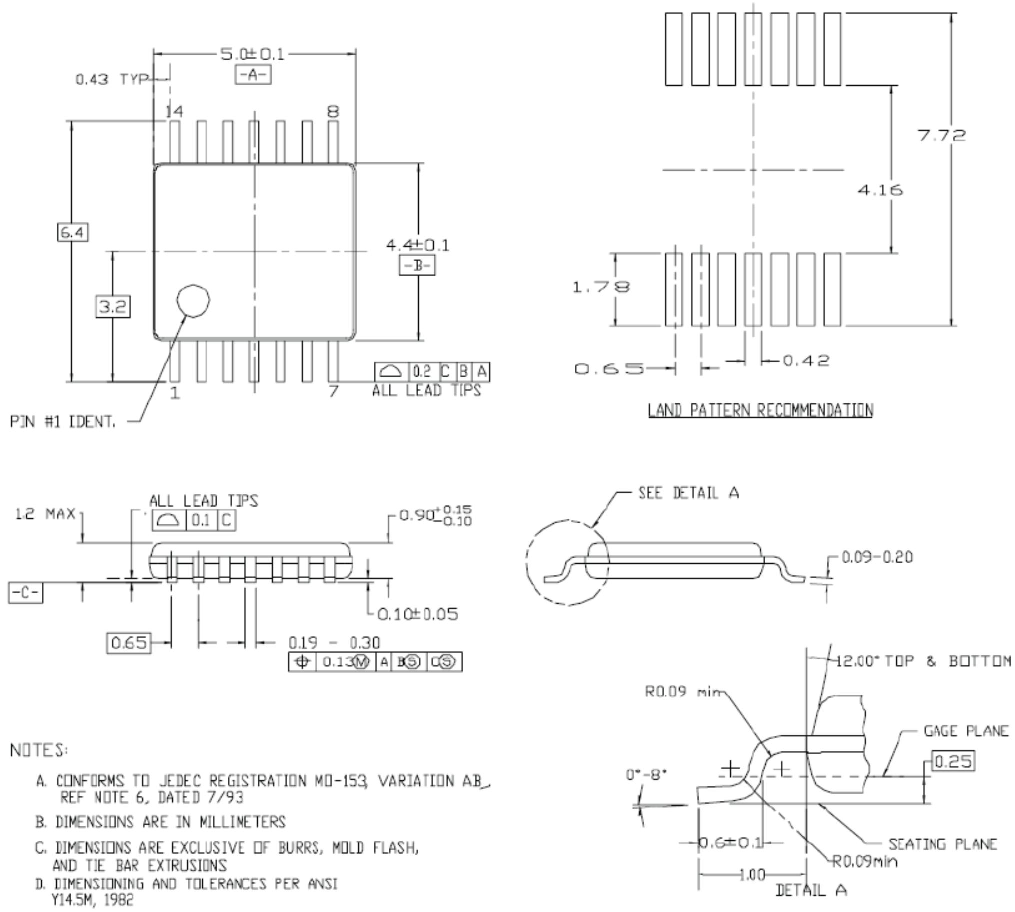
NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") ma
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

Comlinear CLC1007, CLC2007, CLC4007 Rev - 1

Mechanical Dimensions continued

TSSOP-14 Package



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