IRFN9140 (JANTX2N7236U)

PD-91553G

Power MOSFET
Surface Mount (SMD-1)
-100V, -18A, P-channel, HEXFET™ MOSFET Technology

Features

- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Surface mount
- Dynamic dv/dt rating
- Light Weight

Potential Applications

- DC-DC converter
- Motor drives

Product Summary

- **BV_{DSS}:** -100V
- **I_D:** -18A
- **$R_{DS(on),max}$:** 0.20Ω
- **$Q_{G,max}$:** 60nC
- **REF:** MIL-PRF-19500/595

SMD-1

Product Validation

Qualified to JANTXV screening flow according to MIL-PRF-19500 for high-reliability applications

Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heat sink. This improves thermal efficiency and reduces drain capacitance.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level
IRFN9140	SMD-1	COTS
JANTX2N7236U	SMD-1	JANTX
JANTXV2N7236U	SMD-1	JANTXV

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-18	A
I_{D2} @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-11	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	-72	A
P_D @ T_C = 25°C	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	500	mJ
I_{AR}	Avalanche Current [1]	-18	A
E_{AR}	Repetitive Avalanche Energy [1]	12.5	mJ
dv/dt	Peak Diode Reverse Recovery [3]	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5 s)	
	Weight	2.6 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = -25V, starting T_J = 25°C, L = 3.1mH, Peak I_L = -18A, V_{GS} = -10V

[3] I_{SD} ≤ -18A, di/dt ≤ -100A/µs, V_{DD} ≤ -100V, T_J ≤ 150°C

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D =-1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.087	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	V_{GS} = -10V, I_{D2} =-11A [1]
		—	—	0.22		V_{GS} = -10V, I_{D2} = -18A [1]
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
Gfs	Forward Transconductance	6.2	—	—	S	V_{DS} = -15V, I_{D2} = -11A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS} = -80V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	60	nC	I_{D1} = -18A V_{DS} = -50V V_{GS} = -10V
Q_{GS}	Gate-to-Source Charge	—	—	13		
Q_{GD}	Gate-to-Drain (‘Miller’) Charge	—	—	35.2		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	I_{D1} = -18A ** V_{DD} = -50V R_G = 9.1Ω V_{GS} = -10V
t_r	Rise Time	—	—	85		
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		
t_f	Fall Time	—	—	65		
L_s +L_D	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	1400	—	pF	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	600	—		
C_{rss}	Reverse Transfer Capacitance	—	200	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-18	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-72	A	
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J = 25°C, I_S = -18A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	280	ns	T_J = 25°C, I_F = -18A, V_{DD} ≤ -30V di/dt = -100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	2.4	—	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board (Soldered to a copper-clad PC board)	—	4.0	—	

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

3 Electrical Characteristics Curves

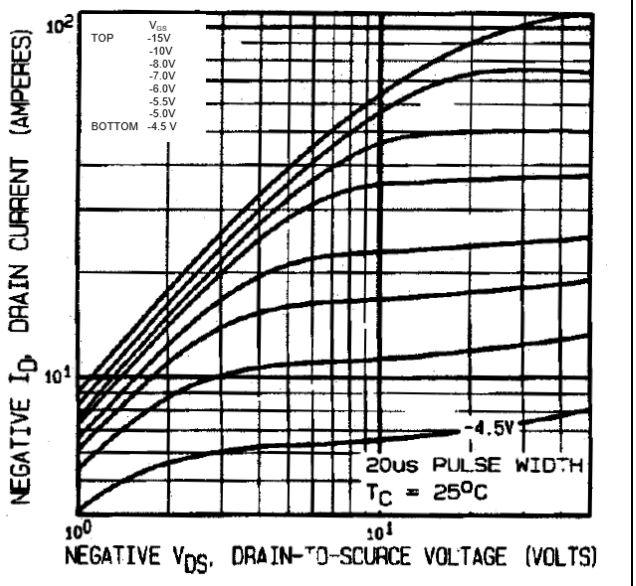


Figure 1 Typical Output Characteristics

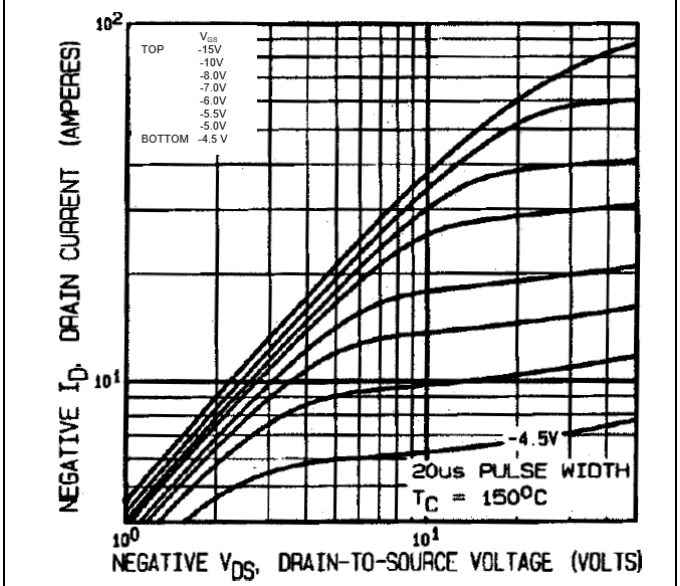


Figure 2 Typical Output Characteristics

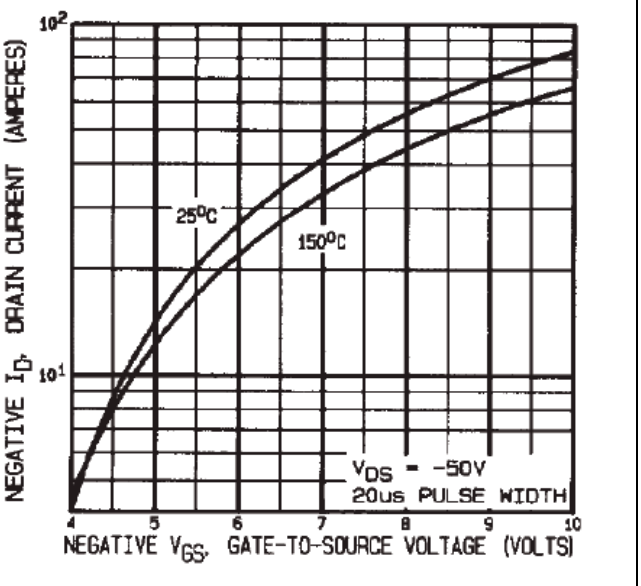


Figure 3 Typical Transfer Characteristics

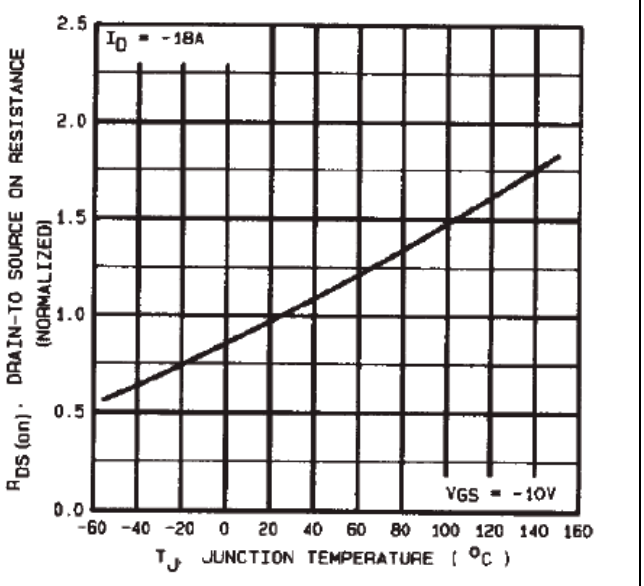


Figure 4 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves

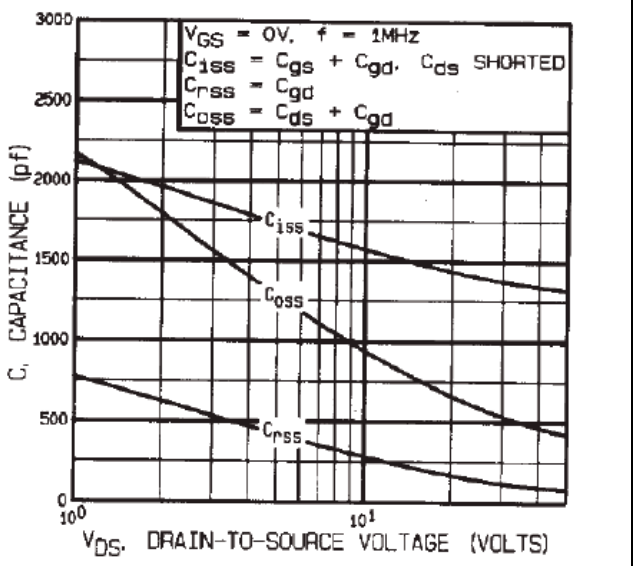


Figure 5 Typical Capacitance Vs. Drain-to-Source Voltage

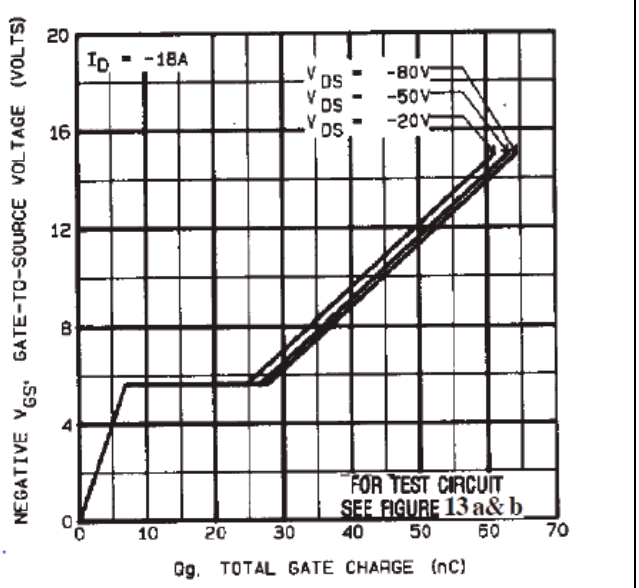


Figure 6 Typical Gate Charge Vs. Gate-to-Source Voltage

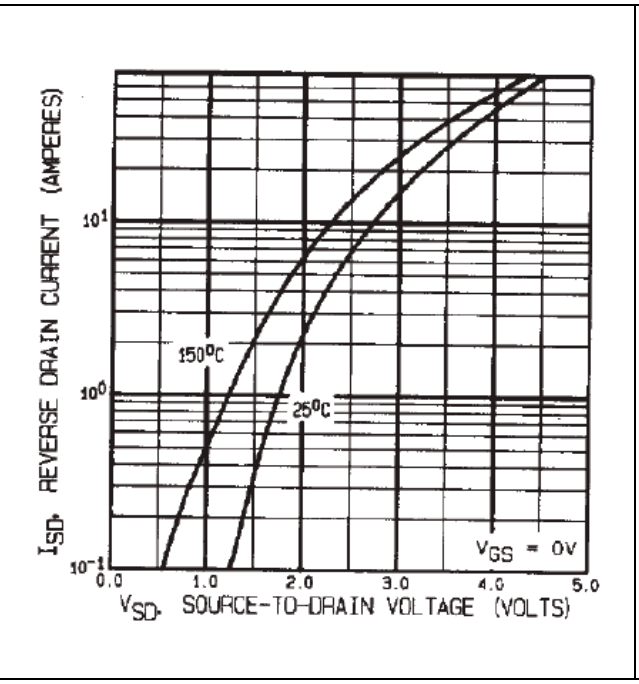


Figure 7 Typical Source-Drain Diode Forward Voltage

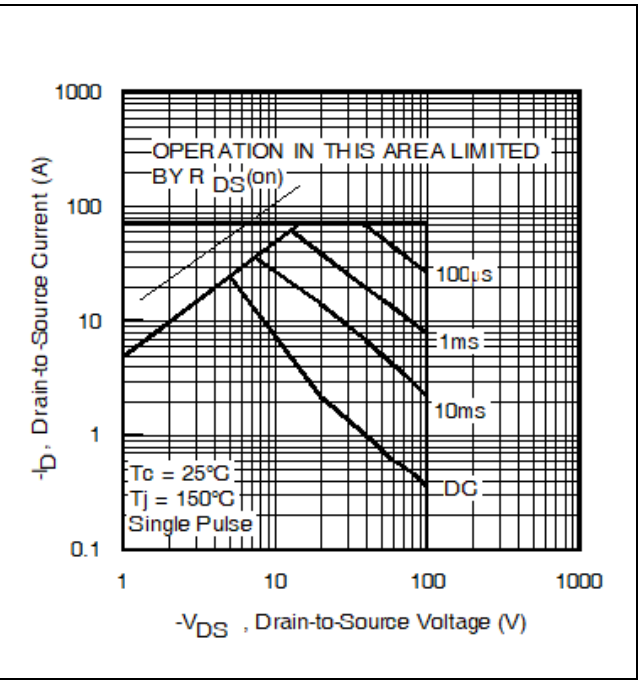


Figure 8 Maximum Safe Operating Area

Electrical Characteristics Curves

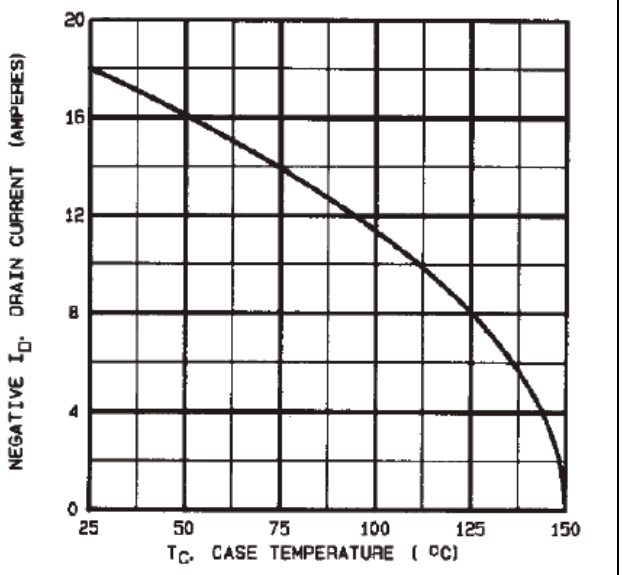


Figure 9 Maximum Drain Current Vs. Case Temperature

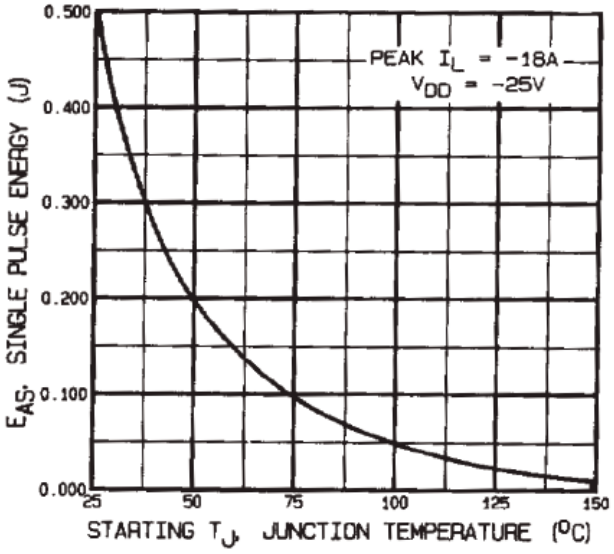


Figure 10 Maximum Avalanche Energy Vs. Junction Temperature

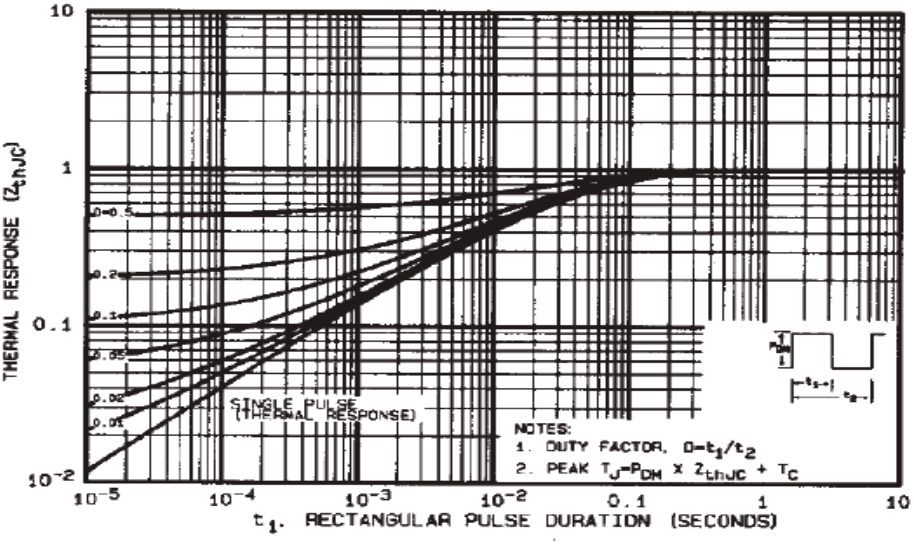


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits

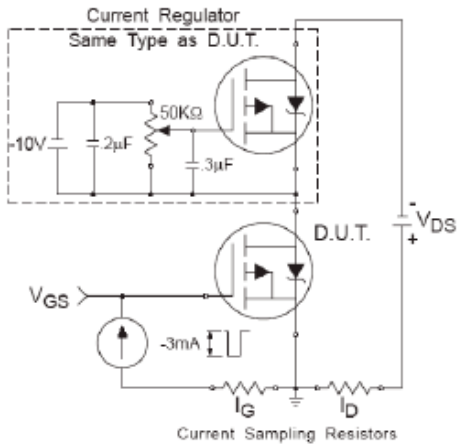


Figure 12 Gate Charge Test Circuit

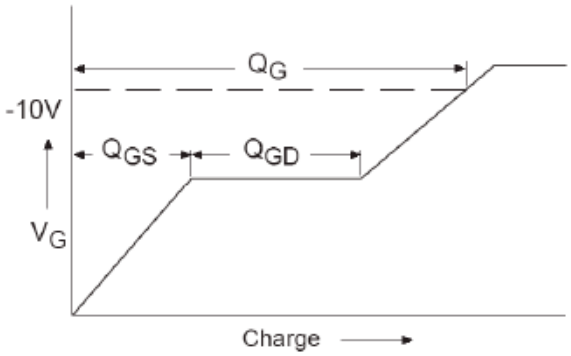


Figure 13 Gate Charge Waveform

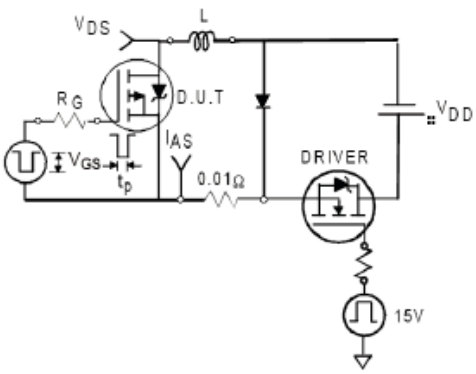


Figure 14 Unclamped Inductive Test Circuit

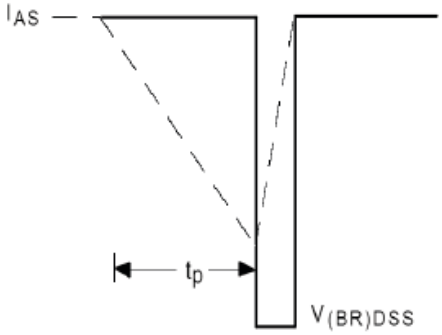


Figure 15 Unclamped Inductive Waveform

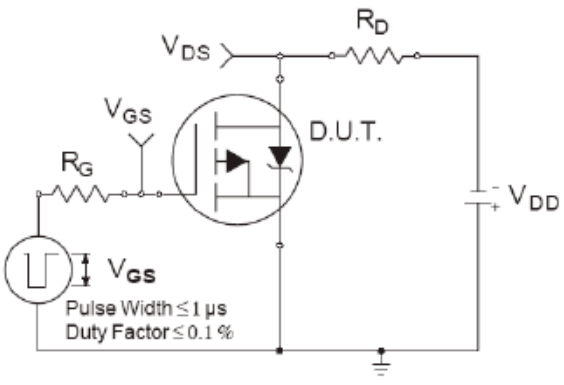


Figure 16 Switching Time Test Circuit

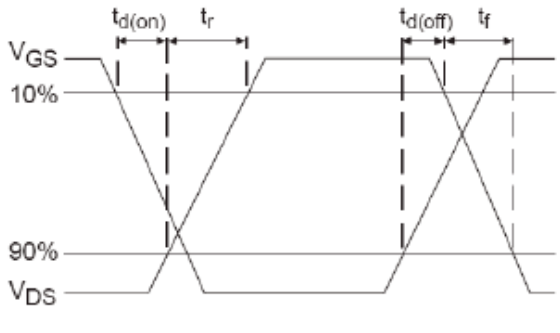
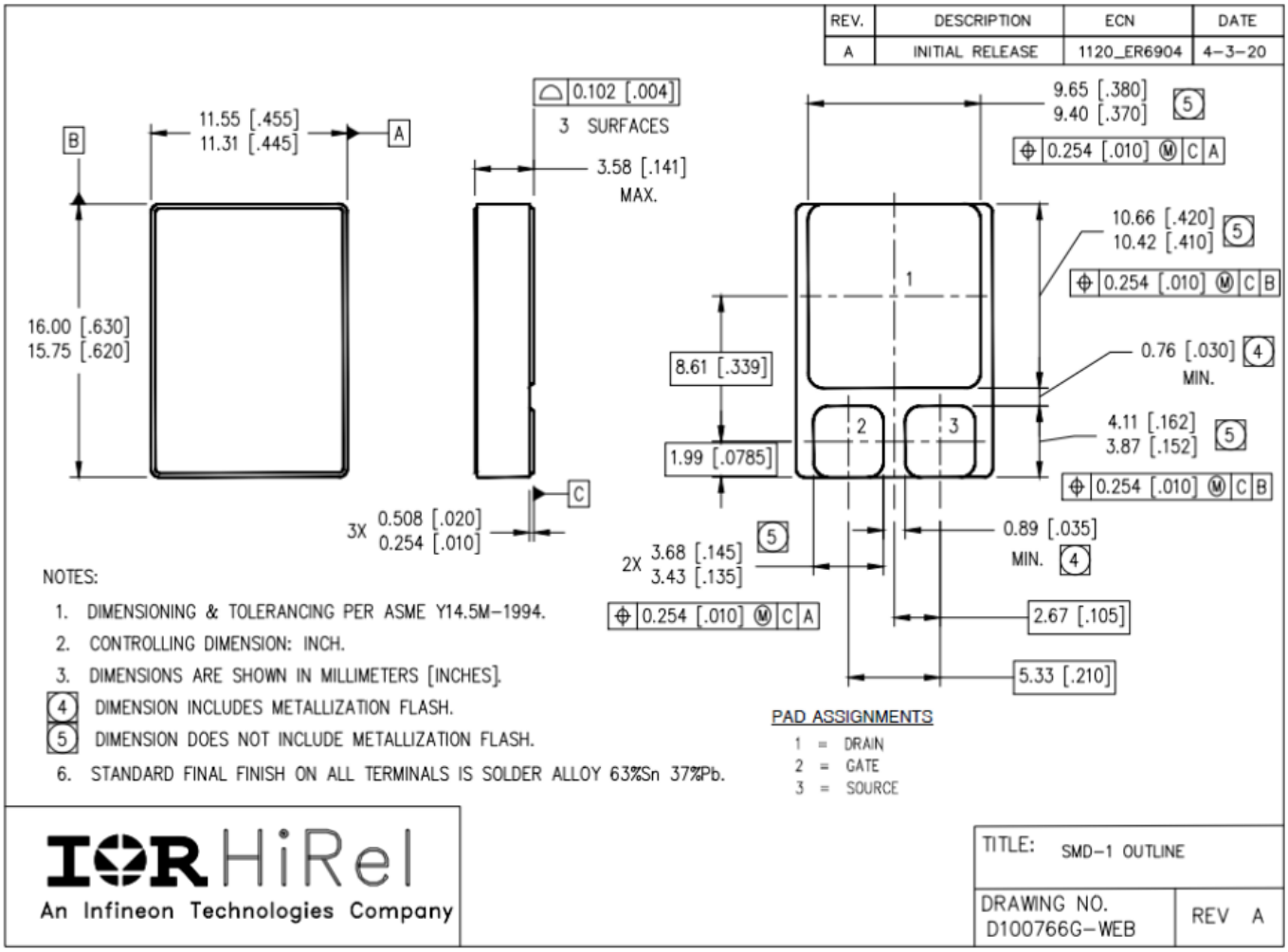


Figure 17 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: SMD-1



Revision history

Document version	Date of release	Description of changes
Rev	12/22/1999	Datasheet (PD-91553C)
Rev D	02/05/2002	ADDED Slash sheet # 595 -page1
Rev E	01/29/2002	Added Swichting test condition V_{GS}=-10V
Rev F	09/22/2003	Updated based on ECN-11069
Rev G	12/06/2024	Updated based on ECN-1120_10102

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