Description

The AL8859Q is an integrated two-phase SPI boost controller for high-power and high-efficiency power systems. It serves as primary stage in power architecture, such as adaptive LED lighting system that combines high beam, low beam, DRL (daytime running light), turn indicator, fog light, static cornering and other functionalities. In combination with second stage of high-current LED drivers, the AL8859Q delivers a complete LED lighting module solution capable of driving multiple LED strings. Its SPI-based digital programmable interface enables easy software updates and configuration changes, ensuring compatibility with diverse system architectures and application platforms.

The AL8859Q is a current-mode voltage boost controller that doubles as an input filter, requiring minimum external components. Output voltage is programmable via SPI. Two devices can operate in a multi-phase configuration (1-phase, 2-phases, 3-phases, 4-phases) to improve filtering and lower BOM cost for high-power applications.

The AL8859Q device is offered in the wettable flank V-QFN4040-24/SWP package (4mm × 4mm) for enhanced solder joint and reliability.

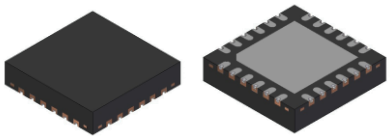
Features

- AEC-Q100 Grade 1
- Functional Safety-Capable
- Wide Input-Voltage Range 4.5V to 60V
- Output-Voltage Accuracy ±0.5% @50V typical
- Soft-Start and High Efficiency 95%
- SPI Programmable Features
  - Up to 4-Phase Control
  - Output-Voltage Regulation
  - Programmable Switching Frequency
  - Switching Current Limit, Overvoltage
  - Diagnostic and Protection Registers
  - One-Time Programming (OTP)
- Spread Spectrum to Improve EMI
- Fail-Safe Operating (FSO) Mode, Stand-Alone Mode
- Wettable V-QFN4040-24/SWP Package (4mm × 4mm)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AL8859Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

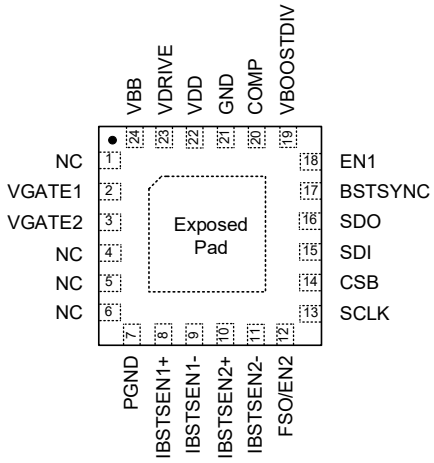
Applications

- Adaptive LED headlights, DRL, fog lamps
- Hybrid powertrains
- Actuators and pumps
- Integrated USB port systems (IUPS)
- Audio and infotainment
- Adas and radars

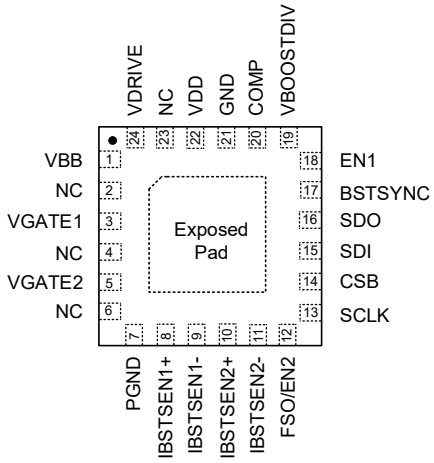
Pin Assignments



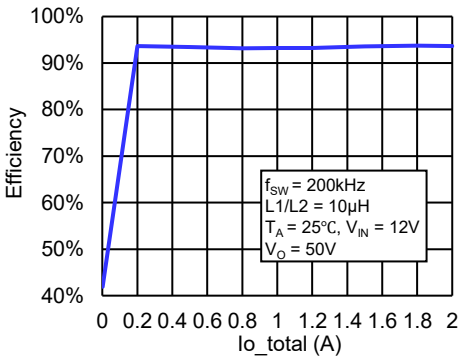
(Generic Package View – Not to Scale)
V-QFN4040-24/SWP (4mm × 4mm)



AL8859QA0DKCW24-13



AL8859QA1DKCW24-13



System Efficiency Performance

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

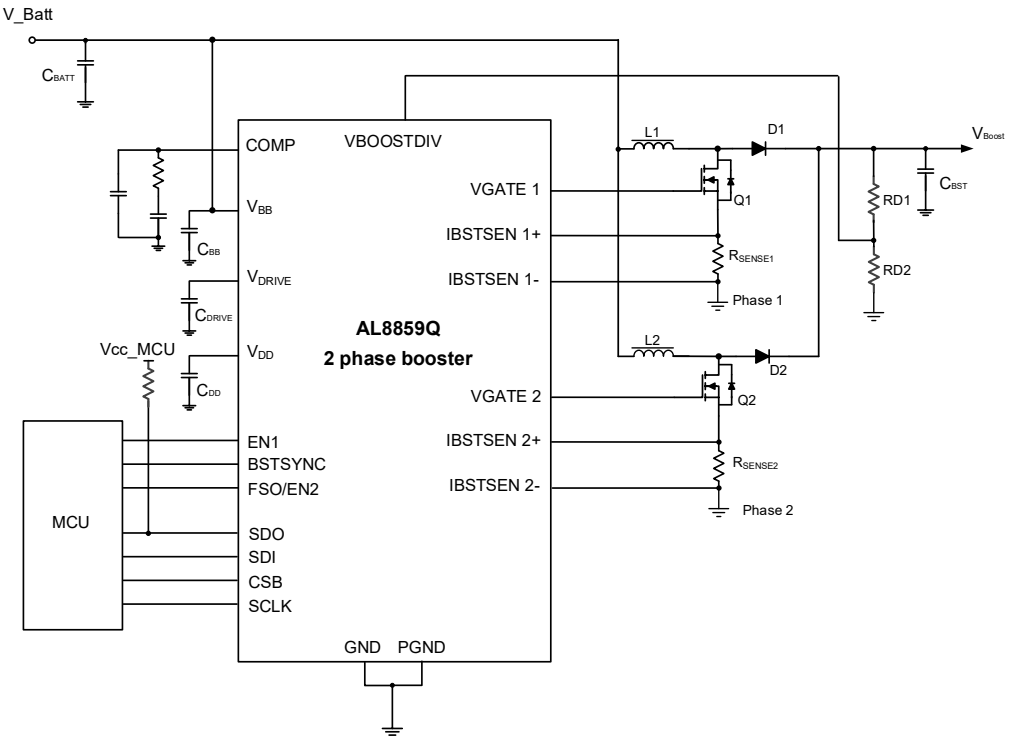


Figure 1. AL8859Q Typical Boost Application Using MOSFET

Functional Block Diagram

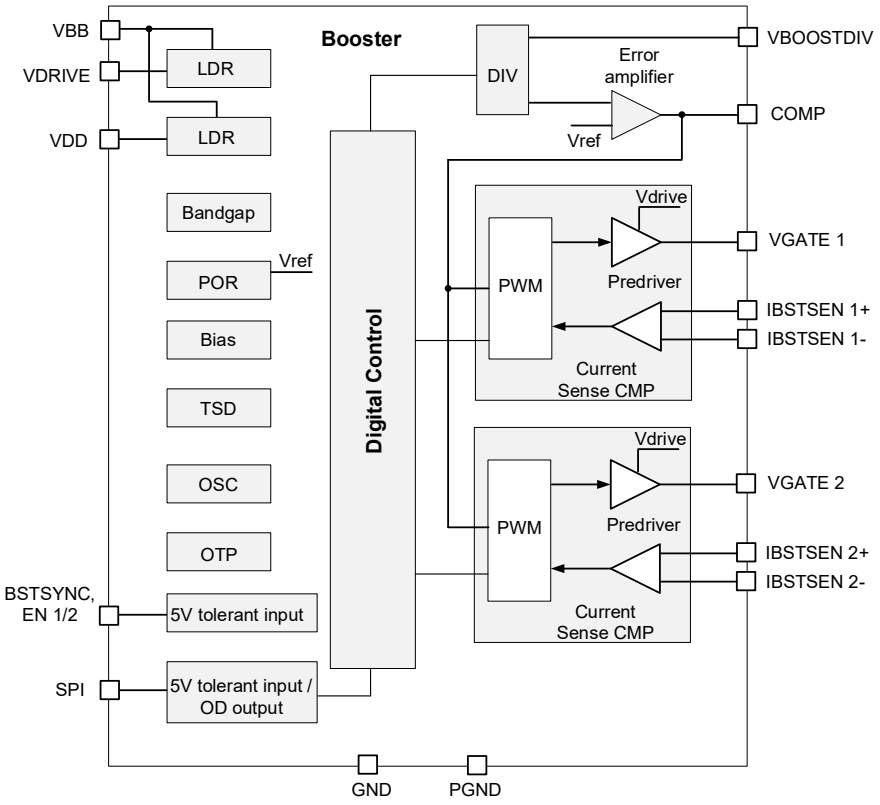


Figure 2. AL8859Q Functional Block Diagram

Pin Descriptions

Pin Name	Pin Number		Function
	AL8859QA0DKCW24-13	AL8859QA1DKCW24-13	
NC	1	23	No connection.
VGATE 1	2	3	Booster MOSFET gate pre-driver 1
VGATE 2	3	5	Booster MOSFET gate pre-driver 2
NC	4	2	No connection.
NC	5	4	No connection.
NC	6	6	No connection.
PGND	7	7	Power ground to internal low side MOSFET.
IBSTSEN1+	8	8	Coil 1 current positive feedback input
IBSTSEN1-	9	9	Coil 1 current negative feedback input
IBSTSEN2+	10	10	Coil 2 current positive feedback input
IBSTSEN2-	11	11	Coil 2 current negative feedback input
FSO/EN2	12	12	FSO/EN2 input
SCLK	13	13	SPI clock input
CSB	14	14	SPI chip select input
SDI	15	15	Serial data input, data is shifted in on the rising edge of SCK.
SDO	16	16	Serial data output, output data is clocked out on the falling edge of SCK.
BSTSYNC	17	17	Connect external clock to sync internal oscillator
EN1	18	18	Enable 1 input.
VBOOSTDIV	19	19	Booster high voltage feedback input
COMP	20	20	Compensation for the booster regulator
GND	21	21	Ground
VDD	22	22	3V logic supply
VDRIVE	23	24	10V supply
VBB	24	1	Battery supply
Exposed Thermal Pad	—	—	Connect to ground plane for adequate heat sinking and noise reduction.

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{VBB}, $V_{BSTSYNC/TST/TST1}$, $V_{BOOSTDIV}$	Voltage on VBB, BSTSYNC/TST/TST1, BOOSTDIV pins	-0.3 to +62	V
V_{VDD}, V_{COMP}	Voltage on VDD, COMP pins	-0.3 to +3.6	V
V_{VDRIVE}, V_{GATEx}	Voltage on VDRIVE, VGATEx pins	-0.3 to +12	V
$V_{IBSTSENx+}$, $V_{IBSTSENx-}$	Voltage on IBSTSENx+, IBSTSENx- pins	-1.0 to +12	V
$V_{SCLK/TST2}$, V_{CSB}, V_{SDI}, V_{SDO}, $V_{ENABLE1}$, $V_{FSO/ENABLE2}$	Voltage on SCLK/TST2, CSB, SDI, SDO, ENABLE1, FSO/ENABLE2 pins	-0.3 to +6.5	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{ST}	Storage Temperature	-65 to +150	°C
V_{ESD}	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	750	

Note: 4. Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Package Thermal Information (Note 5)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	31.2	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	27.2	°C/W
$R_{\theta JB}$	Junction-to-Board Thermal Resistance	11.1	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	0.18	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	10.78	°C/W
$R_{\theta JC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	1.13	°C/W

Note: 5. The device is mounted on JEDEC standard 4 layers (2s2p) PCB test board.

Recommended Operating Conditions (Over operating free-air temperature range, unless otherwise specified.) (Note 6)

Parameter	Min	Typ	Max	Unit
Battery Supply Voltages on VBB Pin	4.5	—	60	V
Logic Supply Voltage	3.1	—	3.5	V
VDD Supply Current	1	—	50	mA
Medium Voltage I/O Pins	0	—	5	V
Input Current-Sense Voltage	-0.1	—	1	V
Operating Junction Temperature Range, T_J	-40	—	+150	°C
Operating Ambient Temperature Range, T_A	-40	—	+125	°C

Note: 6. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For verified specifications, see *Electrical Characteristics*.

Electrical Characteristics (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

TEMPERATURE MEASUREMENTS (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TSD	Thermal Shutdown	—	+155	+165	+175	°C
TW	Thermal Warning	—	+145	+155	+165	°C
TEMP7	Thermal Output	ADC_TEMP_THR[2:0] = 111	+140	+150	+160	°C
TEMP6	Thermal Output	ADC_TEMP_THR[2:0] = 110	+130	+140	+150	°C
TEMP5	Thermal Output	ADC_TEMP_THR[2:0] = 101	+120	+130	+140	°C
TEMP4	Thermal Output	ADC_TEMP_THR[2:0] = 100	+110	+120	+130	°C
TEMP3	Thermal Output	ADC_TEMP_THR[2:0] = 011	+100	+110	+120	°C
TEMP2	Thermal Output	ADC_TEMP_THR[2:0] = 010	+90	+100	+110	°C
TEMP1	Thermal Output	ADC_TEMP_THR[2:0] = 001	+80	+90	+100	°C
TEMP0	Thermal Output	ADC_TEMP_THR[2:0] = 000	+70	+80	+90	°C
TEMP_HYST	Thermal Output Hysteresis	—	—	+3	—	°C

Note: 7. Guaranteed by bench measurement, not tested in production.

VDRIVE: 10V SUPPLY FOR BOOST FET GATE DRIVER CIRCUIT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDRV_15	VDRIVE Reg. Voltage from VBB (Note 8)	[VDRIVE_VSETPOINT =1111], V_{BB} − VDRIVE > 0.5V @IDRIVE = 90mA	9.7	10.1	10.7	V
VDRV_00	VDRIVE Reg. Voltage from VBB (Note 8)	[VDRIVE_VSETPOINT =0000], V_{BB} − VDRIVE > 0.5V @IDRIVE = 90mA	4.8	5	5.3	V
DVDRV	VDRIVE Increase per Code (Note 8)	Linear increase, 4 bits	—	0.34	—	V
VDRV_ILIM	DC Output Current Consumption	—	0	—	90	mA
VDRV_BB_IL	Output Current Limitation	—	90	—	500	mA
VDRIVE_NOK_ILOAD	Output Overload Condition for VDRIVE_NOK Detection (Note 9)	—	95	—	—	mA
VDRIVE_NOK_VBBLOW	Minimum VBB-VDRIVE Sufficient Voltage (Note 9)	—	0.5	—	—	V
VDRV_UV_[7]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 111]	83	87	91	%
VDRV_UV_[6]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 110]	79	83	87	%
VDRV_UV_[5]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 101]	75	79	84	%
VDRV_UV_[4]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 100]	71	75	79	%
VDRV_UV_[3]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 011]	63	67	71	%

Notes: 8. The VDRIVE voltage drop between VDRIVE and V_{BB} has to be sufficient (min 0.5V).
9. Both of these conditions have to be fulfilled otherwise SPI status bit VDRIVE_NOK is set.
10. Relative threshold to typical value of VDRIVE_VSETPOINT settings.

Electrical Characteristics (continued) (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

VDRIVE: 10V SUPPLY FOR BOOST FET GATE DRIVER CIRCUIT (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDRV_UV_[2]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 010]	54	58	62	%
VDRV_UV_[1]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 001]	46	50	54	%
VDRV_UV_[0]	VDRIVE UV Detection Threshold (Note 10)	Relative threshold to actual VDRIVE_VSETPOINT {VDRIVE_UV_THR = 000]	—	0	—	%
VDRV_UV_DL	VDRIVE UV Detection Delay	—	5	—	35	µs

Note: 10. Relative threshold to typical value of VDRIVE_VSETPOINT settings.

VDD: 3V LOW-VOLTAGE ANALOG AND DIGITAL SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	VDD Regulator Output Voltage	V_{BB} > 5V	3.135	—	3.465	V
VDD_IOUT	DC Output Current Consumption	V_{BB} > 5V, including 10mA self-current consumption	—	—	50	mA
VDD_ILIM	Output Current Limitation	—	60	—	350	mA

POR: POWER-ON RESET CIRCUIT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POR3VH	POR Toggle Level on VDD Rising	—	2.55	—	3.05	V
POR3V_L	POR Toggle Level on VDD Falling	—	2.3	—	2.8	V
POR3V_HYST	POR Hysteresis	—	—	0.15	—	V
POR_VBB_H	POR Threshold on VBB, VBB Rising	Applicable only during startup	3.8	4.15	4.3	V
POR_VBB_L	POR Threshold on VBB, VBB Falling	Applicable only during startup	—	4	—	V
I_{SD}	Shutdown Supply Current	EN = Low @ T_J = +25°C	—	—	1	µA

OTP MEMORY

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBB_OTP	Recommend VBB Range for OTP Zapping	—	7.65	—	7.71	V
VBB_OTP_L	VBB Pin Voltage Range for OTP_FAIL Flag During OTP Programming	—	6.37	6.8	7.23	V

OSC10M: SYSTEM OSCILLATOR CLOCK

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FOSC10M	System Oscillator Frequency	—	7	10	13	MHz

BOOSTER (Note 11)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BST_OV_127	Booster Overvoltage Shutdown	[BOOST_OVERVOLTSD_THR = 1111111], DC level	63.80	65.85	67.90	V
BST_OV_022	Booster Overvoltage Shutdown	[BOOST_OVERVOLTSD_THR = 0010110], DC level	11	11.5	12	V
DBST_OV	Booster Overvoltage Shutdown Increase per Code	Linear increase, 7 bits	—	0.518	0.718	V

Note: 11. All parameters are guaranteed for recommended external Vboost resistor divider (Rdiv) ratio 34 with ±1% tolerance.

Electrical Characteristics (continued) (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

BOOSTER (Note 11) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BST_RA_3	Booster Overvoltage Re-activation	[BOOST_OV_REACT = 11], DV to the Vboost reg. overvoltage protection, DC level	-1.9	-1.5	-1.1	V
BST_RA_0	Booster Overvoltage Re-activation	[BOOST_OV_REACT = 00], DV to the Vboost reg. overvoltage protection, DC level	—	0	—	V
DBST_RA	Booster Overvoltage Re-activation Decrease per Code	Linear decrease, 2 bits, DC level	-0.6	-0.5	—	V
BST_EA_UV	Booster Undervoltage Protection (External Divider Fail State Detection)	—	3.45	3.95	4.45	V
BST_EA_UV_HYST	Booster Undervoltage Protection (External Divider Fail State Detection) Hysteresis	—	—	0.6	—	V
BST_REG_125	Booster Regulation Level	[BOOST_VSETPOINT = 1111101], DC level	62.8	64.8	66.8	V
BST_REG_022	Booster Regulation Level	[BOOST_VSETPOINT = 0010110], DC level	11	11.5	12	V
DBST_REG	Booster Regulation Level Increase per Code	Linear increase, 7 bits	—	0.518	0.718	V
BST_EA_GM3	Transconductance Gain of Error Amplifier	[BOOST_OTA_GAIN = 11], seen from VBOOST, DC value	63	90	117	µA/V
BST_EA_GM2	Transconductance Gain of Error Amplifier	[BOOST_OTA_GAIN = 10], seen from VBOOST, DC value	42	60	78	µA/V
BST_EA_GM1	Transconductance Gain of Error Amplifier	[BOOST_OTA_GAIN = 01], seen from VBOOST, DC value	21	30	39	µA/V
BST_EA_GM0	Transconductance Gain of Error Amplifier	[BOOST_OTA_GAIN = 00], high impedance	—	0	—	µA/V
EA_IOUT_POS	EA Max Output Current	—	150	—	—	µA
EA_IOUT_NEG	EA Min Output Current	—	—	—	-150	µA
EA_ILEAK	Output Leakage Current in Tri-state	Output in tri-state (EA_GM0)	-1	—	1	µA
EA_ROUT	EA Output Resistance	—	—	2.0	—	MΩ
COMP_CLH_3	EA Max Output Voltage_3	BOOST_SLPCTRL[2] = 1, OR of all BOOST_VLIMTHx[1] = 1	2.1	2.26	—	V
COMP_CLH_2	EA Max Output Voltage_2	BOOST_SLPCTRL[2] = 1, OR of all BOOST_VLIMTHx[1] = 0	—	1.98	—	V
COMP_CLH_1	EA Max Output Voltage_1	BOOST_SLPCTRL[2] = 0, OR of all BOOST_VLIMTHx[1] = 1	—	1.64	—	V
COMP_CLH_0	EA Max Output Voltage_0	BOOST_SLPCTRL[2] = 0, OR of all BOOST_VLIMTHx[1] = 0	—	1.35	—	V
COMP_CLL	EA Min Output Voltage	—	—	—	0.4	V
BST_EA_DIV_INI	Booster VOOSTDIV Pin Input Pullup Current	Pull current source towards to VDD voltage	0.4	0.8	1.4	µA
COMP_DIV_15	Division of COMP on the Current Comparator Input	[P_DISTRIBUTIONx = 01111]	—	20	—	—
COMP_DIV_0	Division of COMP on the Current Comparator Input	[P_DISTRIBUTIONx = 00000]	—	6.81	—	—
COMP_DIV_−16	Division of COMP on the Current Comparator Input	[P_DISTRIBUTIONx = 11111]	—	4	—	—

Note: 11. All parameters are guaranteed for recommended external Vboost resistor divider (Rdiv) ratio 34 with ±1% tolerance.

Electrical Characteristics (continued) (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

BOOSTER (Note 11) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
COMP_VSF	Voltage Shift on COMP on Current Comparator Input	—	—	+0.5	—	V
BST_SKCL_3	Booster Skip Cycle for Low Currents (Note 12)	[BOOST_SKCL = 11], Booster disabled for lower V(COMP)	—	0.7/0.8	—	V
BST_SKCL_2	Booster Skip Cycle for Low Currents (Note 12)	[BOOST_SKCL = 10], Booster disabled for lower V(COMP)	—	0.625/0.7	—	V
BST_SKCL_1	Booster Skip Cycle for Low Currents (Note 12)	[BOOST_SKCL = 01], Booster disabled for lower V(COMP)	—	0.55/0.6	—	V
BST_VGATE_THR_1	VGATE Comparator to Start BST_TOFF Time	[VBOOST_VGATE_THR = 1]	—	1.2	—	V
BST_VGATE_THR_0	VGATE Comparator to Start BST_TOFF Time	[VBOOST_VGATE_THR = 0]	—	0.4	—	V
BST_TOFF_7	Booster Minimum OFF Time	[VBOOST_TOFF_SET = 111], time from VGATE below VBOOST_VGATE_THR	780	1200	1620	ns
BST_TOFF_6	Booster Minimum OFF Time	[VBOOST_TOFF_SET = 110], time from VGATE below VBOOST_VGATE_THR	300	460	620	ns
BST_TOFF_5	Booster Minimum OFF Time	[VBOOST_TOFF_SET = 101], time from VGATE below VBOOST_VGATE_THR	260	400	540	ns
BST_TOFF_4	Booster Minimum OFF Time	[VBOOST_TOFF_SET = 100], time from VGATE below VBOOST_VGATE_THR	220	340	460	ns
BST_TOFF_3	Booster Minimum OFF Time	VBOOST_TOFF_SET = 011], time from VGATE below VBOOST_VGATE_THR	180	280	380	ns
BST_TOFF_2	Booster Minimum OFF Time	VBOOST_TOFF_SET = 010], time from VGATE below VBOOST_VGATE_THR	140	220	300	ns
BST_TOFF_1	Booster Minimum OFF Time	VBOOST_TOFF_SET = 001], time from VGATE below VBOOST_VGATE_THR	100	160	220	ns
BST_TOFF_0	Booster Minimum OFF Time	VBOOST_TOFF_SET = 000], time from VGATE below VBOOST_VGATE_THR	60	100	140	ns
BST_TON_7	Booster Minimum ON Time	[VBOOST_TON_SET = 111], time from internal signal for VGATE drive	330	530	730	ns
BST_TON_6	Booster Minimum ON Time	[VBOOST_TON_SET = 110], time from internal signal for VGATE drive	300	480	660	ns
BST_TON_5	Booster Minimum ON Time	[VBOOST_TON_SET = 101], time from internal signal for VGATE drive	270	430	590	ns
BST_TON_4	Booster Minimum ON Time	[VBOOST_TON_SET = 100], time from internal signal for VGATE drive	240	380	520	ns
BST_TON_3	Booster Minimum ON Time	[VBOOST_TON_SET = 011], time from internal signal for VGATE drive	210	330	450	ns
BST_TON_2	Booster Minimum ON Time	[VBOOST_TON_SET = 010], time from internal signal for VGATE drive	180	280	380	ns
BST_TON_1	Booster Minimum ON Time	[VBOOST_TON_SET = 001], time from internal signal for VGATE drive	150	230	310	ns
BST_TON_0	Booster Minimum ON Time	[VBOOST_TON_SET = 000], time from internal signal for VGATE drive	120	180	240	ns

Notes: 11. All parameters are guaranteed for recommended external Vboost resistor divider (Rdiv) ratio 34 with ±1% tolerance.
12. Higher levels are valid if BST_VLIMTH value 2 or 3 (BOOST_VLIMTHx[1] = 1) is selected at least on one channel.

Electrical Characteristics (continued) (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

BOOSTER – CURRENT REGULATION AND LIMITATION

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BST_VLIMTHx_3	Current Comparator for Imax Detection	[BOOST_VLIMTHx = 11], DC level of threshold voltage	95	100	105	mV
BST_VLIMTHx_2	Current Comparator for Imax Detection	[BOOST_VLIMTHx = 10], DC level of threshold voltage	75	80	85	mV
BST_VLIMTHx_1	Current Comparator for Imax Detection	[BOOST_VLIMTHx = 01], DC level of threshold voltage	57	62.5	67	mV
BST_VLIMTHx_0	Current Comparator for Imax Detection	[BOOST_VLIMTHx = 00], DC level of threshold voltage	45	50	55	mV
BST_OFFS	Current Comparator for Vboost regulation, Offset Voltage (Note 15)	—	-10	—	10	mV
BST_SLPCTRL_7	Booster Slope Compensation	BOOST_SLPCTRL = 111], see *Power Distribution* section	—	290 / COMP_DIV	—	mV/µs
BST_SLPCTRL_6	Booster Slope Compensation	BOOST_SLPCTRL = 110], see *Power Distribution* section	—	190 / COMP_DIV	—	mV/µs
BST_SLPCTRL_5	Booster Slope Compensation	BOOST_SLPCTRL = 101], see *Power Distribution* section	—	120 / COMP_DIV	—	mV/µs
BST_SLPCTRL_4	Booster Slope Compensation	BOOST_SLPCTRL = 100], see *Power Distribution* section	—	85 / COMP_DIV	—	mV/µs
BST_SLPCTRL_3	Booster Slope Compensation	BOOST_SLPCTRL = 011], see *Power Distribution* section	—	50 / COMP_DIV	—	mV/µs
BST_SLPCTRL_2	Booster Slope Compensation	BOOST_SLPCTRL = 010], see *Power Distribution* section	—	35 / COMP_DIV	—	mV/µs
BST_SLPCTRL_1	Booster Slope Compensation	BOOST_SLPCTRL = 001], see *Power Distribution* section	—	17 / COMP_DIV	—	mV/µs
BST_SLPCTRL_0	Booster Slope Compensation	BOOST_SLPCTRL = 000], see *Power Distribution* section	—	0	—	mV/µs
CMVSENSE	Sense Voltage Common Mode (Note 15)	*Power Distribution* section over full operating range	-0.1	—	1	V

BOOSTER – PRE-DRIVER

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RONHI	High-Side Switch Impedance	T_J = +25°C	—	4.2	—	Ω
RONHI	High-Side Switch Impedance	T_J = +150°C	—	6	7	Ω
RONLO	Low-Side Switch Impedance	T_J = +25°C	—	4.2	—	Ω
RONLO	Low-Side Switch Impedance	T_J = +150°C	—	6	7	Ω
RPDOWN	Pulldown Resistor on VGATEx	—	—	10	—	kΩ

5V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, BSTSYNC, ENABLE1, FSO/ENABLE2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VINHI	High-Level Input Voltage	SDI, BSTSYNC, CSB and SCLK	2	—	—	V
VINLO	Low-Level Input Voltage	SDI, BSTSYNC, CSB and SCLK	—	—	0.8	V
Rpull	Pull Resistance (Note 13)	SDI, BSTSYNC, CSB and SCLK	40	—	160	kΩ
ENA_VINHI	High-Level Input Voltage	ENABLE1 and FSO/ENABLE2	2.35	—	—	V
ENA_VINLO	Low-Level Input Voltage	ENABLE1 and FSO/ENABLE2	—	—	0.7	V
ENA_Rpull	Pull Resistance (Notes 13 and 14)	ENABLE1 and FSO/ENABLE2	20	—	400	kΩ

Notes: 13. Internal pulldown resistor (Rpd) for SDI, ENABLE1, FSO/ENABLE2, BSTSYNC and SCLK, pull up resistor (Rpu) for CSB to VDD.
14. VDD > POR3V_H; ENA_Rpull > 20kW when VDD = 0 to 3.5V.
15. Tested parameters are guaranteed by design, not tested in production.

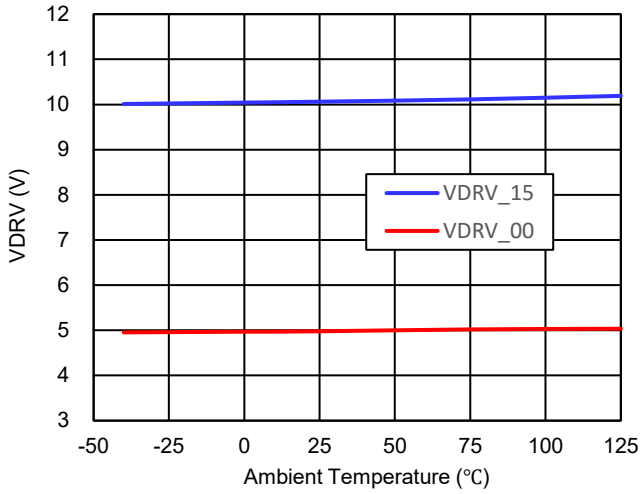
Electrical Characteristics (continued) (T_A = -40°C to +125°C, V_{BB} = 12V, unless otherwise specified.)

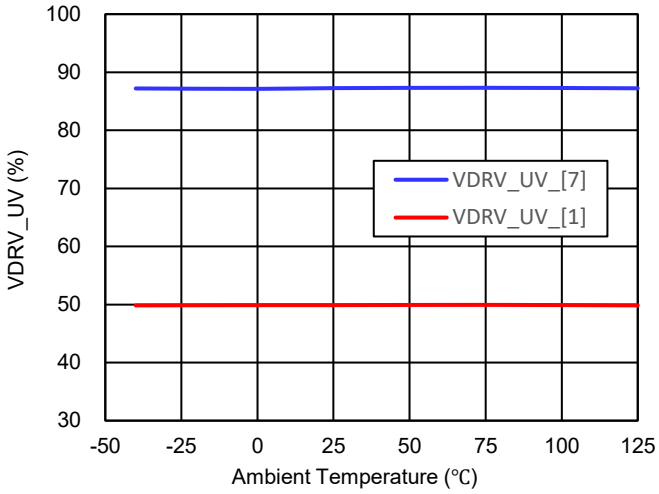
5V TOLERANT OPEN-DRAIN DIGITAL OUTPUT (SDO)

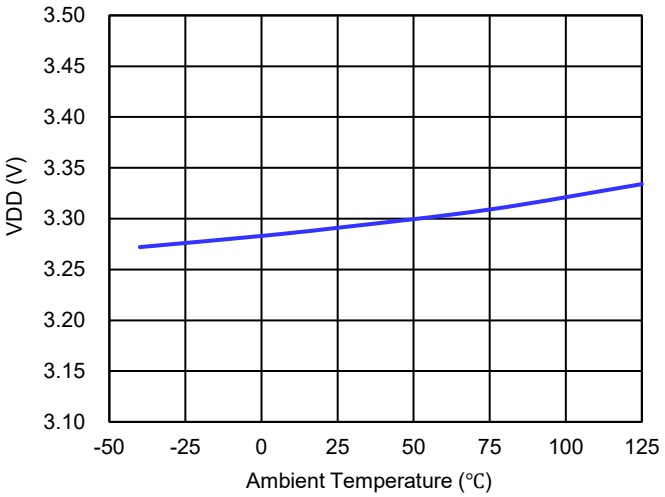
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOUTLO	Low-Voltage Output Voltage	Iout = -10mA (current flows into the pin)	—	—	0.4	V
RDSON	Equivalent Output Resistance	Low-side switch	—	20	40	Ω
SDO_ILEAK	SDO Pin Leakage Current	—	—	—	2	μA
SDO_C	SDO Pin Capacitance (Note 16)	—	—	—	10	pF
SDO_DL	CLK to SDO Propagation Delay (Note 15)	Low-side switch activation/deactivation time; @1k_ to 5V, 100pF to GND, for falling edge V(SDO) goes below 0.5Vklo-m	—	—	60	ns

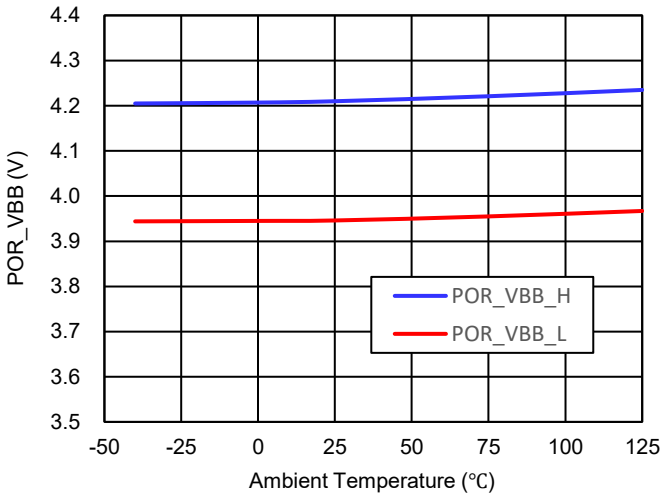
Notes: 15. Tested parameters are guaranteed by design, not tested in production.
16. This is guaranteed by bench measurement, not tested in production.

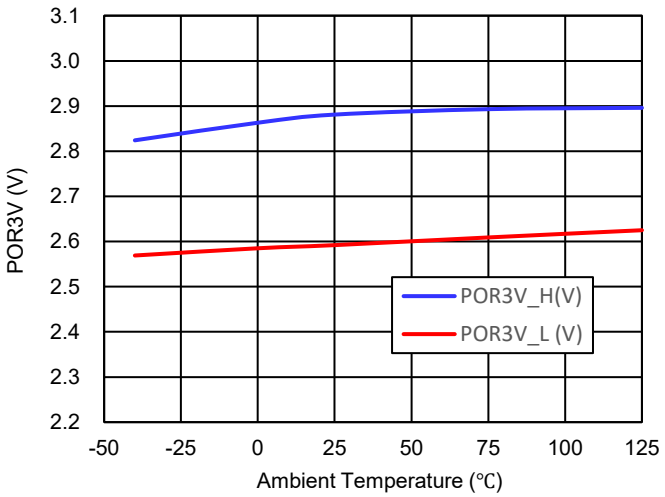
Typical Performance Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.)

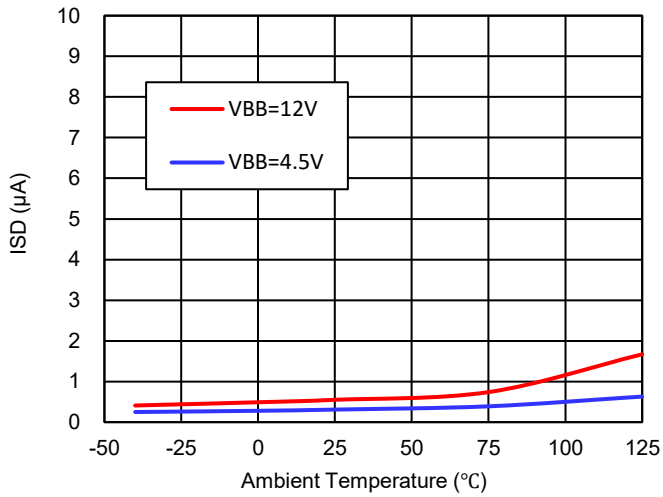




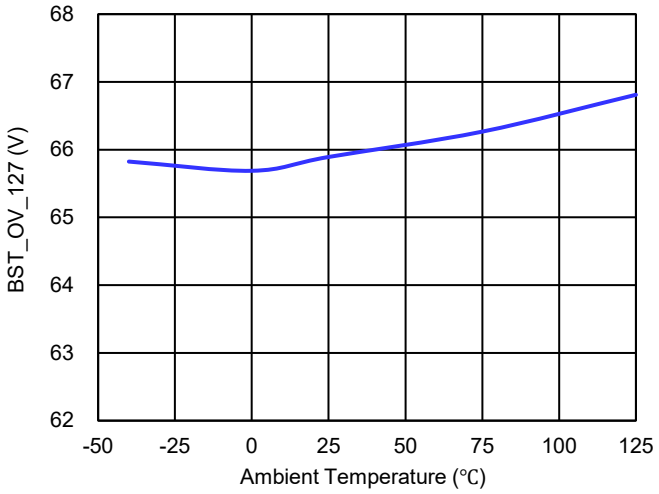


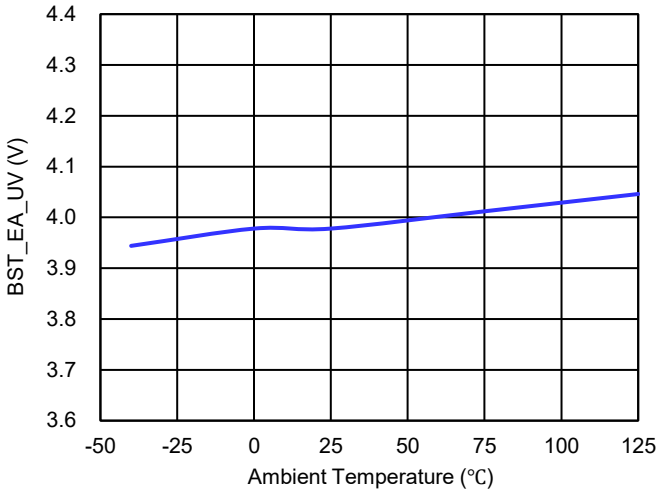


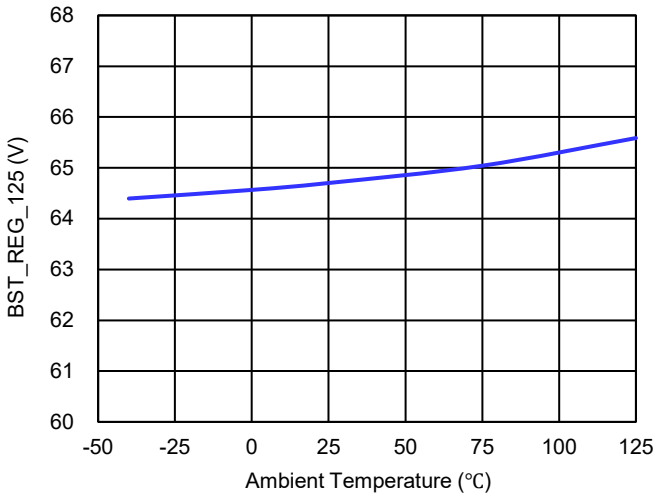


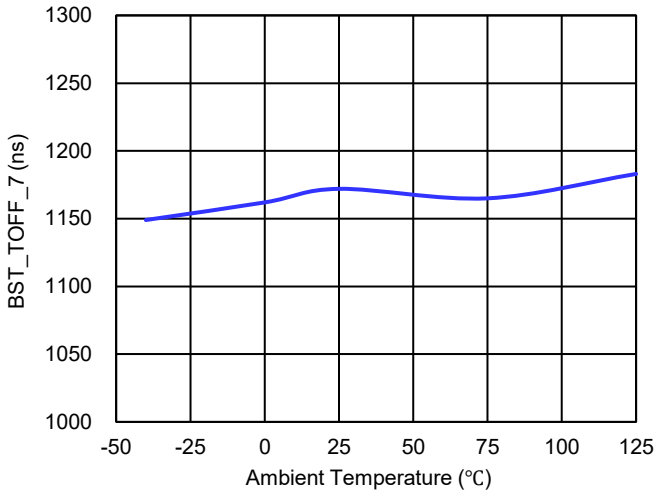


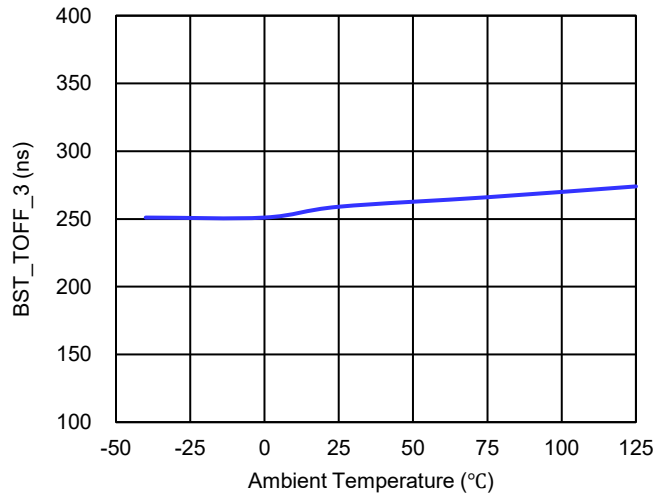
Typical Performance Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.) (continued)

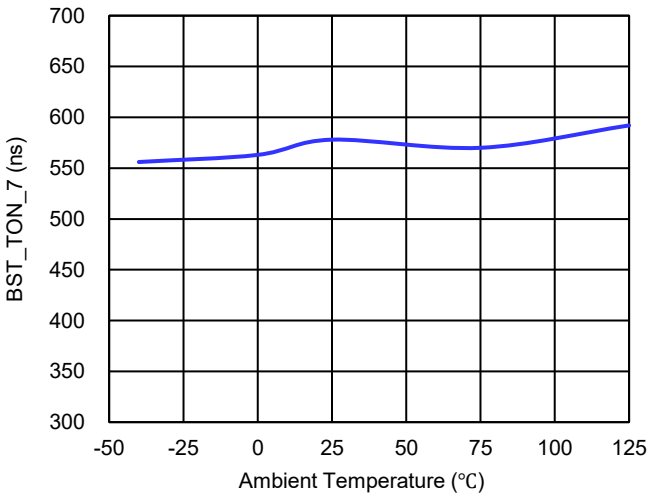




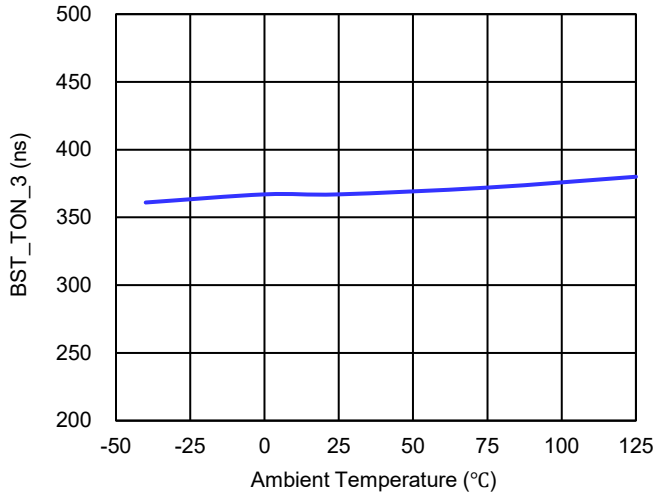


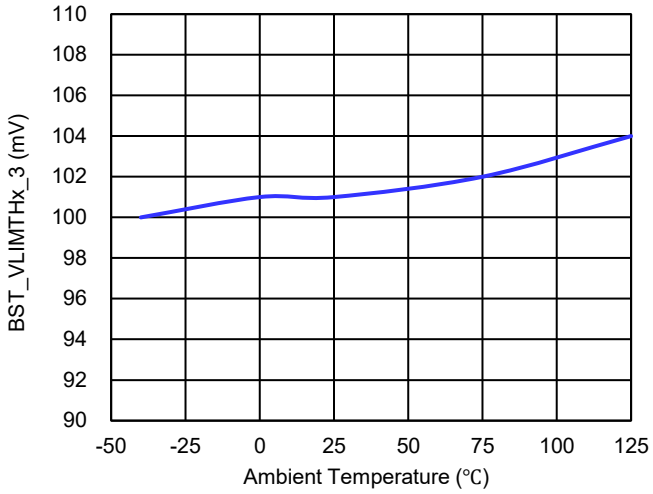


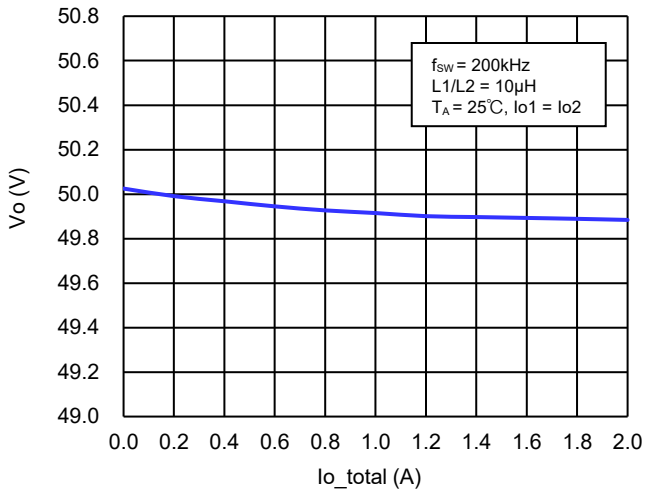


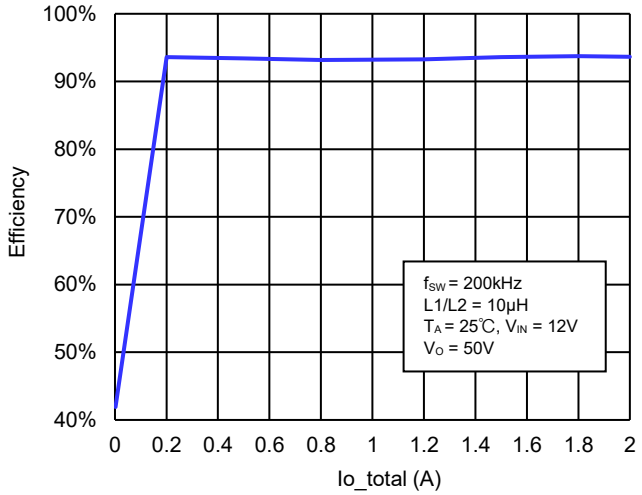


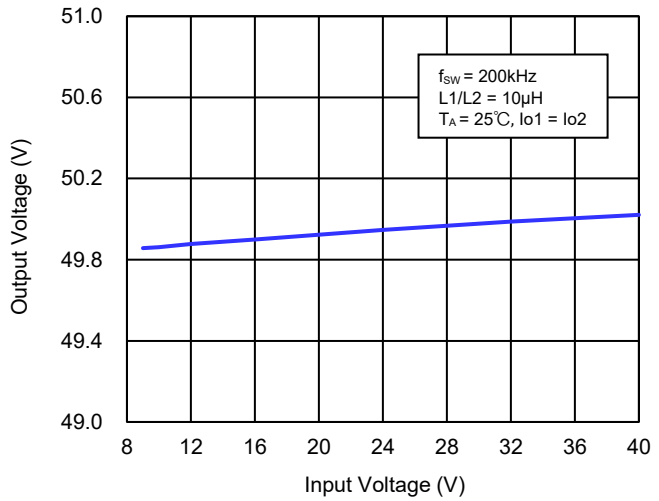
Typical Performance Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.) (continued)

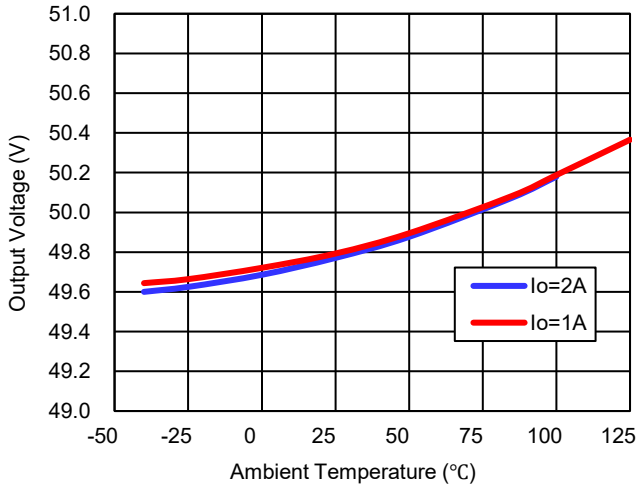












Functional Description and Application Information

VDD Supply

The VDD supply is the low-voltage digital and analog supply for the chip and derives energy from VBB. Due to the low dropout regulator design, VDD is guaranteed from low VBB voltages.

The power-on-reset circuit (POR) monitors the VDD and VBB voltages to control the out-of-reset condition at power-up. At least one ENABLE input is required to be in logic “1” to enable the VDD regulator and leave reset state.

When SPI register VDD_ENA is set to “1”, VDD regulator stays enabled and chip stays in normal mode, even if all ENABLEx (x = 1, 2) inputs are set to logic “0”. When SPI register VDD_ENA is set to “0” and all ENABLEx inputs are set to logic “0”, chip enters the reset state and VDD regulator is switched off.

VDRIVE Supply

The VDRIVE supply voltage represents the power for the complete booster pre-driver block which generates the VGATE, used to switch the booster MOSFETs. The voltage is programmable via SPI in 16 different values (register VDRIVE_VSETPOINT[3:0], ranging from a minimum of 5V typical to 10.1V typical: see *VDRIVE* Table). This feature allows having the best switching losses vs. resistive losses trade off, according to the MOSFET selection in the application, also versus the minimum required battery voltage.

VDRIVE supply takes energy from VBB battery voltage. Minimal VDRIVE regulator voltage drop is about 0.5V. To ensure that booster can be operated close to minimal VBB battery voltage, logic level MOSFETs should be considered. By efficiency reasons, it is important to select MOSFETs with low gate charge. External MOSFETs are controlled by the integrated pre-driver with slope control to reduce EMC emissions.

VDRIVE undervoltage lockout safety mechanism monitors sufficient voltage for MOSFETs and protects them by switching off the booster when VDRIVE voltage is too low. During initial 150µs after POR the detection is disabled to ensure that normal operating mode is entered. The detection level is set by VDRIVE_UV_THR[2:0] register relative to used VDRIVE voltage. Detection thresholds are summarized in *VDRIVE* Table. When VDRIVE_UV_THR[2:0] = 0, function is disabled.

Internal Clock Generation – OSC10M

An internal RC clock named OSC10M is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection (refer to OSC10M for details). All timings depend on OSC10M accuracy.

Boost Regulator

General

The booster stage provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in continuous mode of operation, thus maximizing the system power efficiency at the same time having the lowest possible input ripple current (with “continuous mode” it is meant that the supply current does not go to zero while the load is activated). Only in case of very low loads or low dimming duty cycle values, discontinuous mode can occur: this means the supply current can swing from zero when the switch is off, to the required peak value when the switch is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

On top of the using phases available in the device, the device can be combined with more AL8859Q devices in the application to gain even more phases. More details about the multichip-multiphase mode can be found in the dedicated section.

Booster Regulation Principles

The AL8859Q features a current-mode voltage boost controller, which regulates the VBOOST line used by backward stage converters. The regulation loop principle is shown in the following picture. The loop compares the reference voltage (BOOST_VSETPOINT) with the actual measured voltage at the VBOOST pin, thus generating an error signal which is treated internally by the error trans−conductance amplifier (block A1). This amplifier transforms the error voltage into current by means of the trans-conductance gain Gm. The amplifier’s output current is then fed into the external compensation network impedance (A2) so that it originates a voltage at the COMP pin, this last used as a reference by the current control block (B).

The current controller regulates the duty cycle based on the VCOMP reference, the sensed inductor peak current via the external resistor R_{SENSE} and the slope compensation used. The power converter (block C) represents the circuit formed by the boost converter externals (inductor, capacitors, MOSFET and forward diode). The load (usually the LED power supplied by the buck converters) is applied to the converter. The controlled variable is the boost voltage, measured directly at the device VBOOST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained inside the device. The regulation parameters are flexibly set by a series of SPI commands. A detailed internal boost controller block diagram is presented in the next section.

Functional Description and Application Information (continued)

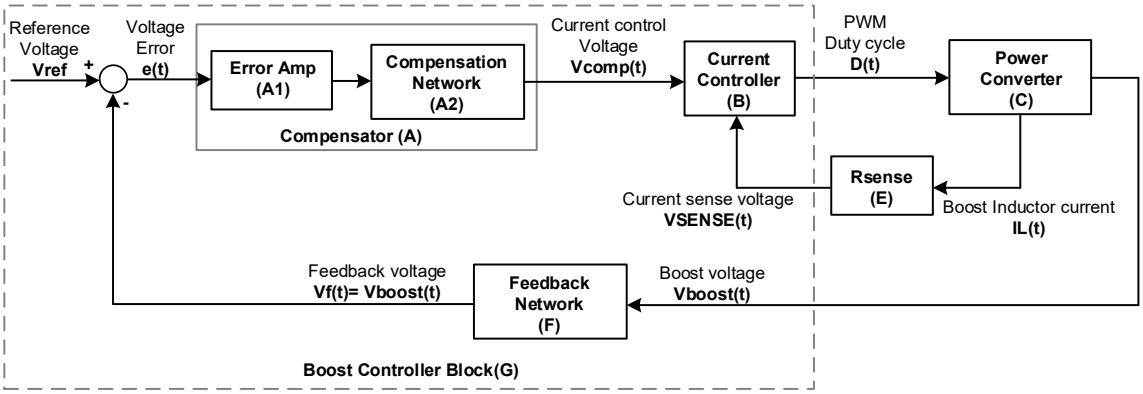


Figure 3. AL8859Q Boost Control Loop – Principle Block Diagram

Boost Controller Detailed Internal Block Diagram

A detailed AL8859Q boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the protection specific blocks can be found (see dedicated sections for details).

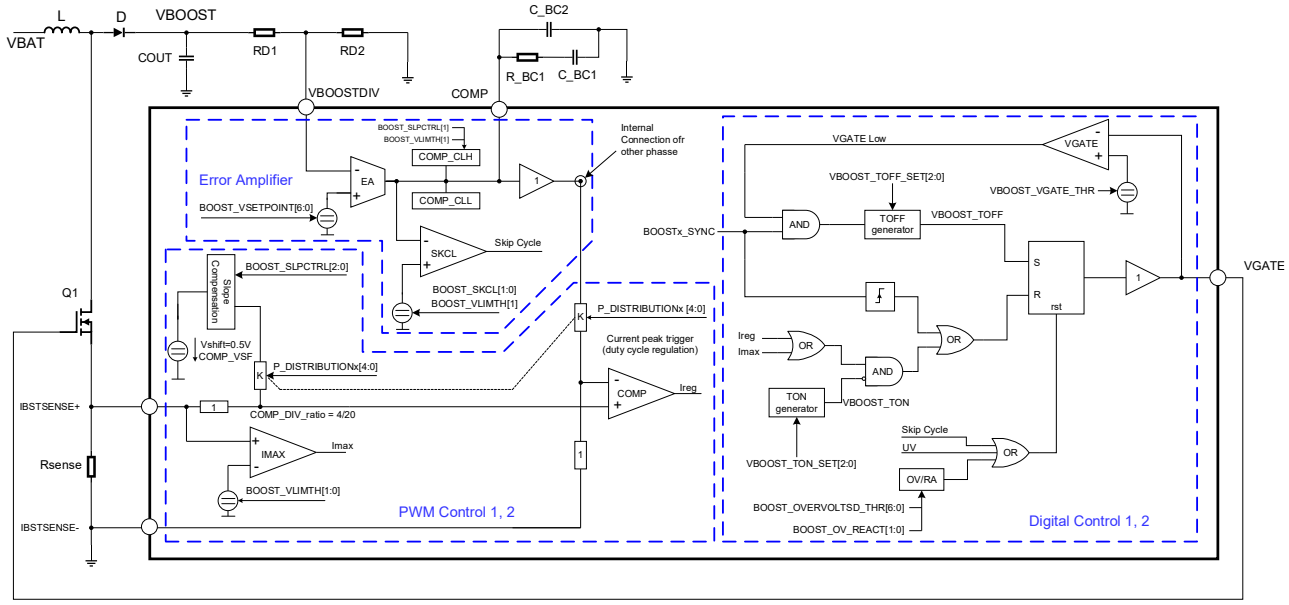


Figure 4. Boost Controller Internal Detailed Block Diagram

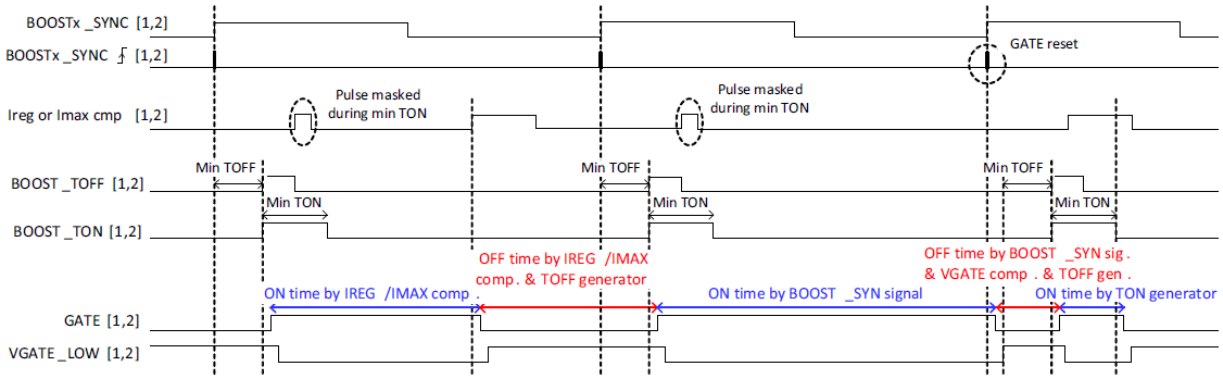


Figure 5. Boost Controller Internal Waveforms

Functional Description and Application Information (continued)

Booster Regulator Setpoint (BOOST_VSETPOINT)

The booster voltage VBOOST is regulated around the target programmable by the 7-bit SPI setting BOOST_VSETPOINT[6:0], ranging from a minimum of 11.5V to a maximum of typical 64.8V (refer to *Booster* Table for details). Due to the step-up characteristic of any boost converter, the boost voltage cannot obviously be lower than the supply battery voltage provided. Therefore, a target of 11.5V would be used only for systems that require the activation of the booster in case of battery drops below the nominal level. At power-up, the booster is disabled and the setpoint is per default the minimum (all zeroes).

Booster Soft-Start

The AL8859Q provides soft-start function to depress overshoot in startup sequence. After POR flag and ENx is active high, an internal constant current source will charge the capacitor on COMP pin. The voltage on COMP pin will ramp up slowly and the boost output voltage ramps consequently.

Booster Overvoltage Shutdown Protection

An integrated comparator monitors VBOOST in order to protect the external booster components from overvoltage. When the voltage rises above the threshold defined by the BOOST_OVERVOLTSD_THR[6:0], ranging from a minimum 11.5V to a maximum of typical 65.85V (refer to *Booster* Table for details), the MOSFET is switched-off at least for the current PWM cycle. At the same time, the boost overvoltage flag in the status register will be set (BOOST_OV = “1”), together with the BOOSTx_STATUS flags equal to zero. The PWM runs again as the moment the VBOOST will fall below the reactivation hysteresis defined by the BOOST_OV_REACT[1:0] SPI parameter. Therefore, depending on the voltage drop and the PWM frequency, it might be that more than one cycle will be skipped. A graphical interpretation of the protection levels is given in the figure below, followed by a summary table (Table 1).

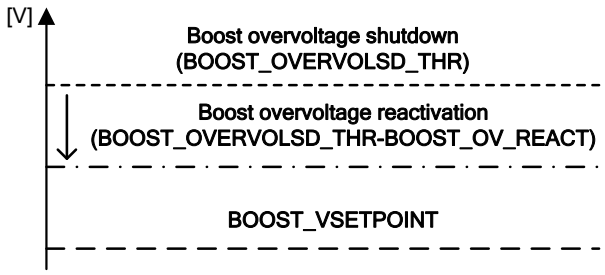


Figure 6. Booster Voltage Protection Levels with Respect to the Setpoint

Case	Condition	PWM Gate Control	SPI Flag BOOSTx_STATUS	SPI Flag BOOST_OV
A	V_{BOOST} < BOOST_VSETPOINT	Normal (not disabled)	1	0
B	V_{BOOST} > BOOST_OVERVOLTSD_THR	Disabled until case “C”	0	1 (latched)
C	V_{BOOST} < BOOST_OVERVOLTSD_THR − BOOST_OV_REACT	Re-enables the PWM, normal mode resumed if from case “B”	1	1 (latched, if read in this condition, it will go back to “0”

Table 1. Boost Overvoltage Protection Levels and Related Diagnostic

Booster Current Regulation Loop

The peak-current level of the booster is set by the voltage of the compensation pin COMP, which is output of the trans-conductance error amplifier, “block B” of Figure 3. This reference voltage is fed to the current comparator via a divider (divider ratio of which can be set by power sharing function for each phase independently, see *Power Distribution* section for more details). The comparator compares this reference voltage with the VSENSE sensed on the external sense resistor RSENSE, connected to the pins IBSTSENSE1/2+ and IBSTSENSE1/2−. The sense voltage is created by the booster inductor current when the MOSFET is switched on and is summed up to an additional offset of +0.5V (see COMP_VSF in *Booster* Table) and on top of that, a slope compensation voltage ramp is added. The slope compensation is programmable by SPI via the BOOST_SLPCTRL[2:0] register and can also be disabled. Due to the offset, current can start flowing in the circuit when VCOMP > COMP_VSF.

When booster is active, voltage at COMP pin is clamped to voltage between 0.4V (see *Booster* Table) and 1.35V to 2.26V depending on BOOST_VLIMTHx and BOOST_SLPCTRL settings (see Table *BOOSTER – CURRENT REGULATION AND LIMITATION*) to ensure quicker reaction of the system to load changes.

Functional Description and Application Information (continued)

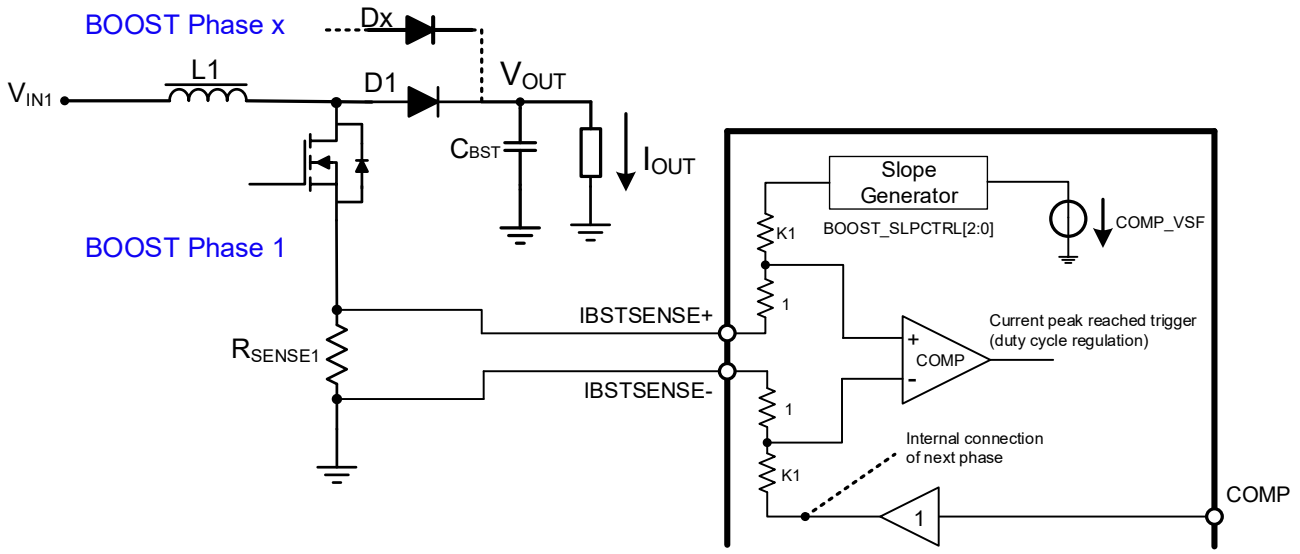


Figure 7. Booster Peak Current Regulator Involved in the Current Control Loop

Booster Current Limitation Protection

On top of the normal current regulation loop comparator, an additional comparator clamps the maximum current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (boost inductor from saturation, boost diode and boost MOSFET from overcurrent, etc.). The protection is active PWM cycle-by-cycle and switches off the MOSFET gate when VSENSE reaches its maximum threshold defined by the BOOST_VLIMTHx[1:0] register (see Table *BOOSTER – CURRENT REGULATION AND LIMITATION* for more details). Therefore, the maximum allowed peak current is defined by the ratio IPEAK_MAX = BOOST_VLIMTHx[1:0]/RSENSE. The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage.

Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de-rating of the LED light due to insufficient power.

Booster PWM Internal Generation

Internally generated booster PWM signal is used only in FSO modes. When FSO mode is entered, booster PWM source is switched automatically from the external BSTSYNC pin to the internally generated signal, which is derived from the internal oscillator OSC10M. A selection of the frequencies is enabled by the register FSO_BST_FREQ[2:0], typical ranging from 200kHz to 1MHz (Table *BOOSTER FREQUENCY IN FSO MODES*).

Booster PWM External Generation

In normal operation mode the booster PWM is taken directly from the BSTSYNC device pin. The maximum frequency at the BSTSYNC pin is 1MHz. There is no actual limitation in the resolution, apart from the system clock for the sampling and a debounce of two clock cycles on the signal edges. The gate PWM is synchronized with either the rising or falling edge of the external signal depending on the BOOST_SRCINV bit value. The default POR value is “0” and corresponds to synchronization to the rising edge. BOOST_SRCINV equals “1” selects falling edge synchronization. Thanks to the possibility to invert external clock in the chip by SPI, up to 6-phase systems with shifted clock are supported with only 1 external clock.

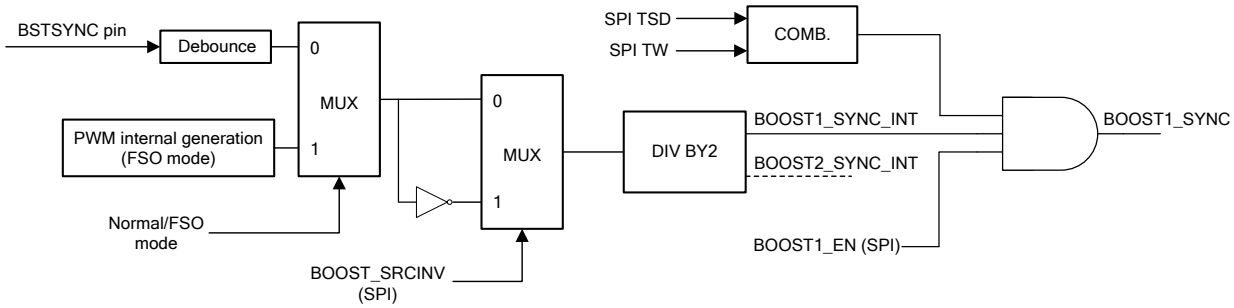


Figure 8. Generation of BOOSTx_SYNC

Functional Description and Application Information (continued)

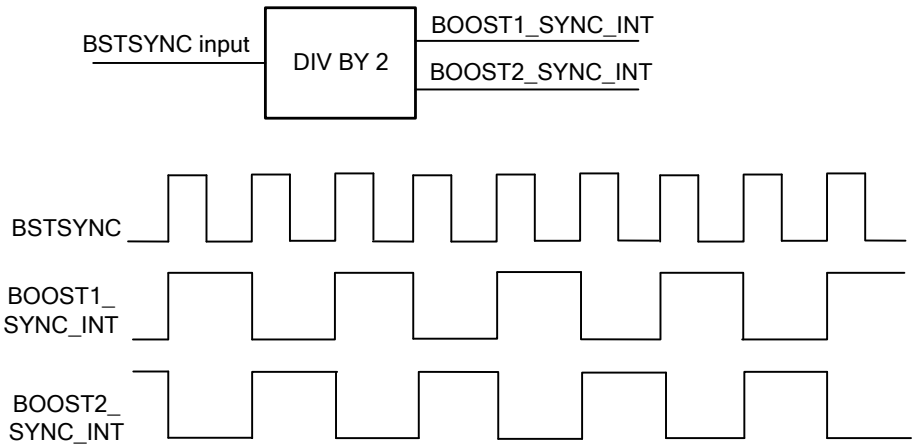


Figure 9. PWM Generation (2-Phase)

Booster PWM Min TOFF and Min TON Protection

As additional protection, the PWM duty cycle is constrained between a minimum and a maximum, defined per means of two parameters available in the device. The PWM minimum on-time is programmable via VBOOST_TON_SET[2:0]: its purpose is to guarantee a minimum activation interval for the booster MOSFET gate, to insure full drive of the component and avoiding switching in the linear region. Please note that this does not imply that the PWM is always running even when not required by the control loop, but means that whenever the MOSFET should be activated, then its on time would be at least the one specified. On the contrary when no duty cycle at all is required, then it will be zero.

The PWM minimum off-time is set via the parameter VBOOST_TOFF_SET[2:0]: this parameter is limiting the maximum duty cycle that can be used in the regulation loop for a defined period TPWM:

$$Duty_{MAX} = \frac{T_{PWM} - T_{OFFMIN}}{T_{PWM}}$$

The main aim of a maximum duty cycle is preventing MOSFET shoot-through in cases the (transient) duty cycle would get too close to 100% of the MOSFET real switch-off characteristics. In addition, as a secondary effect, a limit on the duty cycle may also be exploited to minimize the inrush current when the load is activated. Warning: a wrong setting of the duty cycle constraints may result in unwanted system behavior. In particular, a too big VBOOST_TOFF_SET[2:0] may prevent the system to regulate the VBOOST with low battery voltages (VBAT). This can be explained by the simplified formula for booster steady state continuous mode:

$$V_{BOOST} \cong \frac{V_{BAT}}{1 - Duty} \Leftrightarrow Duty \cong 1 - \frac{V_{BAT}}{V_{BOOST}}$$

So, in order to reach a desired VBOOST for a defined supply voltage, a certain duty cycle must be guaranteed.

Booster Compensator Model

A linear model of the booster controller compensator (block “A” Figure 3) is provided in this section. The protection mechanisms around are not considered. A type “2” network is considered at the VCOMP pin. The equivalent circuit is shown below:

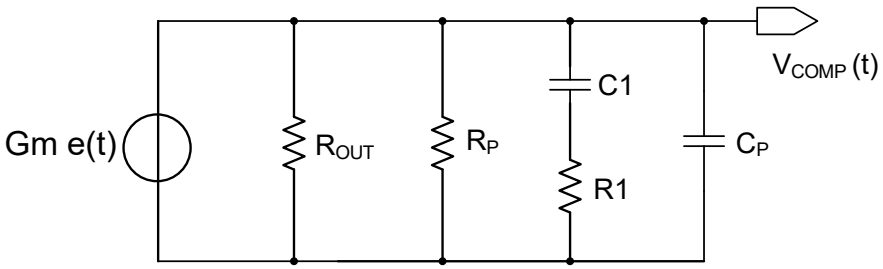


Figure 10. Booster Compensator Circuit with Type “2” Network

Functional Description and Application Information (continued)

In the figure, e(t) represents the control error, and equals to the difference BOOST_VSETPOINT(t) − VBOOST(t). “Gm” is the trans-conductance error amplifier gain, while “R_{OUT}” is the amplifier internal output resistance. The values of these two parameters can be found in *Booster* Table. By solving the circuit in Laplace domain, the following error to V_{COMP} transfer function is obtained:

$$H_{COMP} = \frac{V_{COMP}(s)}{e(s)}$$

$$= G_m \cdot R_T \frac{\tau_1 s + 1}{\tau_1 \tau_P s^2 + (\tau_P + \tau_{1P})s + 1}$$

The explanation of the parameters stated in the equation above follows:

$$R_T = \frac{R_P \cdot R_{OUT}}{R_P + R_{OUT}}$$

$$\tau_1 = R_1 C_1$$

$$\tau_P = R_T C_P$$

$$\tau_{1P} = (R_1 + R_T) C_1$$

This transfer function model can be used for closed loop stability calculations.

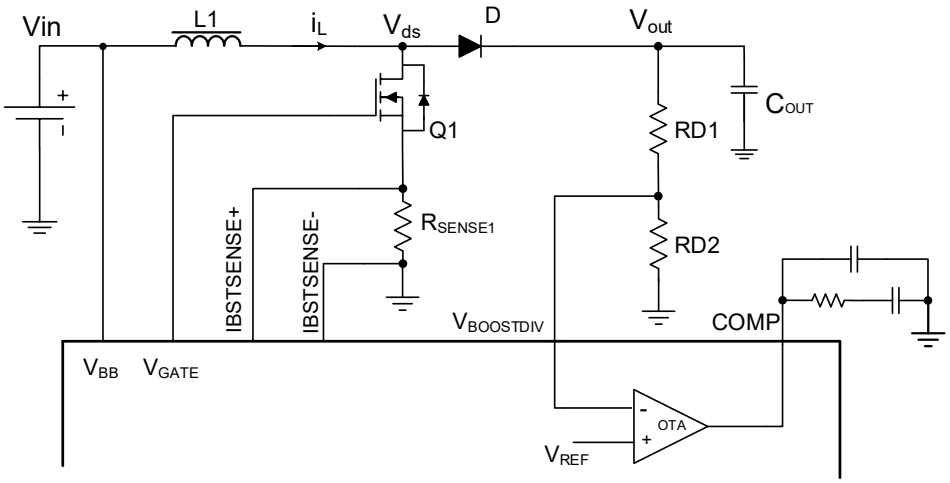


Figure 11. Voltage Divider and Compensation Network

Booster PWM Skip Cycles

In case of light load, it may be useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the “skip cycles” feature, programmable by SPI via BOOST_SKCL[1:0] (see *Booster* Table and SPI map). BOOST_SKCL[1:0] = “00” means skip cycle disabled.

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding VBOOST oscillations in a larger voltage window.

Booster Switching Frequency Spread Spectrum Function

The AL8859Q incorporates a spread spectrum frequency modulation technique for low EMI performance while the device is using an internal PWM generator. The switching frequency is modulated by ±13% of nominal frequency at a rate of 500Hz via a triangular waveform. In one modulation cycle, the switching frequency varies linearly from a minimum to a maximum, and to a minimum again.

Functional Description and Application Information (continued)

Booster Multiphase Mode Principles

The AL8859Q device supports two booster phases, which are connected to the same VBOOST node, sharing the boost capacitor block. Multiphase mode shows to be a cost-effective solution in case of mid to high power systems, where bigger external BOM components would be required to bear the total power in one phase only with the same performances and total board size. In particular, the boost inductor could become a critical item for very high-power levels, to guarantee the required minimum saturation current and RMS heating current.

Another advantage is the benefit from EMC point of view, due to the reduction in ripple current per phase and ripple voltage on the module input capacitor and boost capacitor. The picture below shows the (very) ideal case of 50% duty cycle. The ripple of the total module current (ILmp_sum = IL1mp + IL2mp) is reduced to zero. The equivalent single-phase current (ILsp) is provided as a graphical comparison.

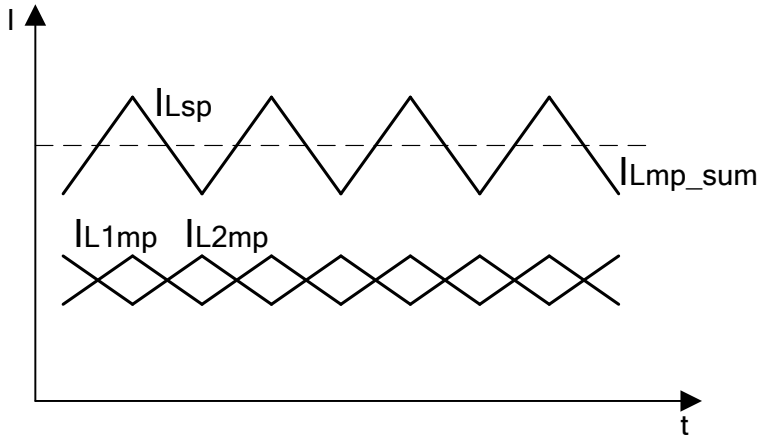


Figure 12. Booster Single Phase vs. Multiphase Example

Booster Multichip Connection Diagram and Programming

For high-power systems, more AL8859Q devices can be combined to gain even more synchronized booster phases. This section describes the steps both from hardware and SPI programming point of view to operate in multichip mode. Examples of physical connection of two devices is provided in this section. From a hardware point of view, it is assumed that in multiphase mode (N boosters), each stage has the same external components. The following features must be considered as well:

1. The compensation pin (COMP) of all boosters is connected together to the same compensation network, to equalize the power distribution of each booster (booster phases work with the equal peak current). For the best noise rejection, the compensation network area has to be surrounded by the GND plane.

2. Boosters are synchronized by using shared external clock, generated by MCU or external logic, according to the user-defined control strategy. The generic number of lines needed is equivalent to the number of devices. When two chips are combined, the slave device shall have BOOST_SRCINV bit at “1” (clock polarity internal inversion active), whereas the master device will keep the BOOST_SRCINV bit at “0” (= no inversion, default).

3. Only the master device’s error amplifier OTA must be active, while the other (slave) devices must have all their own OTA blocks disabled (BOOST_OTA_GAIN[1:0] = “00”). Master device should have the register BOOST_MULTI_PHASE_MD[1:0] set to “01” (Multiphase Mode − MASTER). This will ensure that error amplifier of this device drives COMP signal which is shared between all devices. Other (slave) devices should have BOOST_MULTI_PHASE_MD[1:0] set to “10” (Multiphase Mode − SLAVE), meaning that COMP pin is used only to sense the voltage.

4. Overvoltage settings of master and slave devices should be set to the same level. Each device senses boost voltage via VBOOSTDIV pin and reacts to the overvoltage situation independently. See also *Booster Overvoltage Shutdown Protection* for more details on the protection mechanism and threshold.

Functional Description and Application Information (continued)

Booster Multiple Devices 4-Phases Connection Example

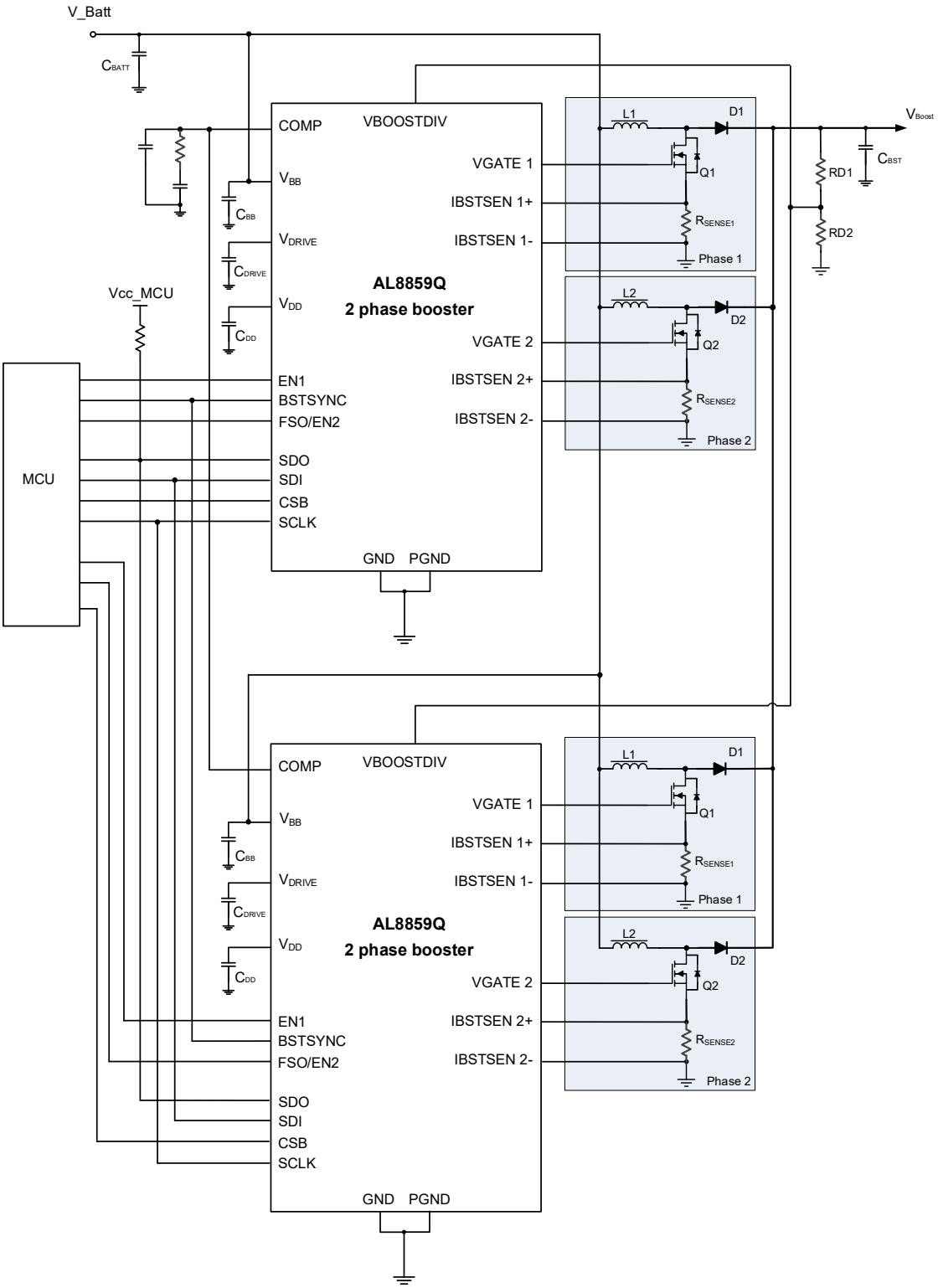


Figure 13. Booster Multichip Connection Example

Booster Enable and Disable Control

By means of FSO_ENABLE_SEL SPI registers, function of FSO/ENABLE2 pin can be selected. When FSO_ENABLE_SEL = “0”, FSO function is enabled (FSO mode can be entered by falling edge on this pin). In this case each phase of the booster can be enabled/disabled by corresponding BOOSTx_EN bit. The enable signal is the transition from “0” to “1”, the disable function is vice-versa.

Functional Description and Application Information (continued)

When FSO_ENABLE_SEL = "1", ENABLE function is enabled (independent control of booster phases). When the independent control of the phases is chosen, a booster x is activated only when SPI bit BOOSTx_EN is "1" and corresponding debounced ENABLEx pin is in logic "1". When BOOSTx_EN = "0", the corresponding channel is off and its GATE drive is disabled. Please note that even when all phases are off, the error amplifier is not shut off automatically and to avoid voltage generation on the VCOMP pin the Gm gain must be put to zero as well.

Power Distribution

Current peak regulation level I_{PEAK} in current regulation loop can be modified by changing of division ratio of the internal voltage divider in range from 4 to 20 (see COMP_DIV parameter in *Booster* Table and Table *Power Distribution*) for each phase individually by SPI registers P_DISTRIBUTIONx[4:0]. The same internal divider is also in path of slope compensation. Internal slope has to be translated into corresponding slope on sensing resistor RSENSE according to Table *BOOSTER – CURRENT REGULATION AND LIMITATION* and Table *Power Distribution*. Power distribution feature allows setting of the ratio between peak values of the currents in the individual booster channels. This can serve to:

• balance power sharing between booster phases which can differ because of external components tolerances and device specification.
• set different power levels to the individual phases without changing external components (RSENSE). As peak value of the current IPEAK is modified by power distribution setting, the average current IAVERAGE and corresponding power P have to be computed by the following formulas when operated in continuous mode:

$I_{AVERAGE} = I_{PEAK} – I_{RIPPLE}/2$, $P = I_{AVERAGE} \cdot V_{BAT}$.
Individual intermediate values of COMP_DIV are computed according to the following equation:

$$COMP\_DIV = \frac{1}{\frac{1}{20} + \frac{15 - P\_DISTRIBUTION[4:0](signed)}{155}}$$

Power Distribution

P_DISTRIBUTIONx[4:0] unsigned	—	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P_DISTRIBUTIONx[4:0] signed		-16	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1
COMP_DIV_ratio		4.00	4.11	4.22	4.34	4.46	4.59	4.73	4.88	5.04	5.21	5.39	5.59	5.79	6.02	6.26	6.53
—	Internal Slope [mV/µs]	—															
Slope_Comp_0 (mV/µs @Rsense)	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Slope_Comp_1 (mV/µs @Rsense)	17	4.25	4.14	4.03	3.92	3.81	3.70	3.59	3.48	3.37	3.26	3.15	3.04	2.94	2.82	2.72	2.60
Slope_Comp_2 (mV/µs @Rsense)	35	8.75	8.52	8.29	8.06	7.85	7.63	7.40	7.17	6.94	6.72	6.49	6.26	6.04	5.81	5.59	5.36
Slope_Comp_3 (mV/µs @Rsense)	50	12.50	12.17	11.85	11.52	11.21	10.89	10.57	10.25	9.92	9.60	9.28	8.94	8.64	8.31	7.99	7.66
Slope_Comp_4 (mV/µs @Rsense)	85	21.25	20.68	20.14	19.59	19.06	18.52	17.97	17.42	16.87	16.31	15.77	15.21	14.68	14.12	13.58	13.02
Slope_Comp_5 (mV/µs @Rsense)	120	30.00	29.20	28.44	27.65	26.91	26.14	25.37	24.59	23.81	23.03	22.26	21.47	20.73	19.93	19.17	18.38
Slope_Comp_6 (mV/µs @Rsense)	190	47.50	46.23	45.02	43.78	42.60	41.39	40.17	38.93	37.70	36.47	35.25	33.99	32.82	31.56	30.35	29.10
Slope_Comp_7 (mV/µs @Rsense)	290	72.50	70.56	68.72	66.82	65.02	63.18	61.31	59.43	57.54	55.66	53.80	51.88	50.09	48.17	46.33	44.41

P_DISTRIBUTIONx[4:0] unsigned	—	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
P_DISTRIBUTIONx[4:0] signed		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
COMP_DIV_ratio		6.81	7.13	7.47	7.85	8.27	8.73	9.25	9.84	10.51	11.27	12.16	13.19	14.42	15.9	17.71	20
—	Internal Slope [mV/µs]	—															
Slope_Comp_0 (mV/µs @Rsense)	0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
Slope_Comp_1 (mV/µs @Rsense)	17	2.5	2.38	2.28	2.17	2.06	1.95	1.84	1.73	1.62	1.51	1.4	1.29	1.18	1.07	0.96	0.85
Slope_Comp_2 (mV/µs @Rsense)	35	5.14	4.91	4.69	4.46	4.23	4.01	3.78	3.56	3.33	3.11	2.88	2.65	2.43	2.2	1.98	1.75
Slope_Comp_3 (mV/µs @Rsense)	50	7.34	7.01	6.69	6.37	6.05	5.73	5.41	5.08	4.76	4.44	4.11	3.79	3.47	3.14	2.82	2.5
Slope_Comp_4 (mV/µs @Rsense)	85	12.48	11.92	11.38	10.83	10.28	9.74	9.19	8.64	8.09	7.54	6.99	6.44	5.89	5.35	4.8	4.25
Slope_Comp_5 (mV/µs @Rsense)	120	17.62	16.83	16.06	15.29	14.51	13.75	12.97	12.20	11.42	10.65	9.87	9.10	8.32	7.55	6.78	6.00
Slope_Comp_6 (mV/µs @Rsense)	190	27.90	26.65	25.44	24.20	22.97	21.76	20.54	19.31	18.08	16.86	15.63	14.40	13.18	11.95	10.73	9.50
Slope_Comp_7 (mV/µs @Rsense)	290	42.58	40.67	38.82	36.94	35.07	33.22	31.35	29.47	27.59	25.73	23.85	21.99	20.11	18.24	16.37	14.50

Functional Description and Application Information (continued)

Diagnostics

The AL8859Q features a wide range of embedded diagnostic features. Their description follows.

• **Thermal Warning:** This mechanism detects a junction temperature which is in principle close, but lower, to the chip maximum allowed, thus providing the information that some action (power de-rating) is required to prevent overheating that would cause thermal shutdown. The thermal warning (TW) flag is given in status register 0x0A and is latched. Thermal warning threshold is typically +160°C (see Table *TEMPERATURE MEASUREMENTS*).

• **Thermal Shutdown:** This safety mechanism intends to protect the device from damage caused by overheating, by disabling the booster channels. The diagnostic is displayed per means of the TSD bit in status register 0x0A (latched). Once occurred, the thermal shutdown condition is exited when the temperature drops below the thermal warning level, thus providing hysteresis for thermal shutdown recovery process. Booster channels are re-enabled automatically if TSD_AUT_RCVR_EN = 1, respectively can be re-enabled by rising edge on BOOSTx_EN if TSD_AUT_RCVR_EN = 0. The application thermal design should be made as such to avoid the thermal shutdown in the worst-case conditions. The thermal shutdown level is not user-programmable and is factory-trimmed to typically +170°C (see Table *TEMPERATURE MEASUREMENTS*).

• **Temperature Output:** This allows to observe temperature of the chip by the means of the adjustable threshold ADC_TEMP_THR[2:0] (see Table *TEMPERATURE MEASUREMENTS*). When temperature exceeds the threshold, status flag TEMP_OUT is set.

• **SPI Error:** In case of SPI communication errors the SPIERR bit in status register 0x0A is set. The bit is latched. For more details, please refer to section *SPI Framing and Parity Error*.

• **HW Reset:** The out of reset condition is reported through the HWR bit (latched). This bit is set only at each power-on-reset (POR) and indicates the device is ready to operate.

• **Booster Overvoltage Shutdown:** Whenever the boost overvoltage detection triggers in the control loop, the BOOST_OV flag (latched, register 0x0A) is set and booster is switched off. The booster is automatically activated when voltage falls below the hysteresis defined by booster overvoltage re-activation parameter in *Booster* Table.

• **Booster Undervoltage Protection:** When voltage at booster divider pin VBOOSTDIV drops below BST_EA_UV level (see *Booster* Table) because of external divider failure, the VBSTDIV_UV flag (latched, 0x0B) is displayed and booster is switched off to protect external components from the overvoltage.

• **VDRIVE Out of Regulation:** Correct work of VDRIVE regulator is monitored by checking VBB - VDRIVE voltage difference which has to be at least 0.5V and by checking current drawn from the regulator. If one or both conditions are not met, VDRIVE_NOK flag is displayed (latched, 0x0B).

• **VDRIVE Undervoltage Lockout:** This safety mechanism monitors sufficient voltage for MOSFETs and protects them by switching off the booster when VDRIVE voltage is too low. During initial 150µs after POR, the detection is disabled to ensure that normal operating mode is entered. Detection level is set by VDRIVE_UV_THR[2:0] register relatively to used VDRIVE voltage (set by VDRIVE_VSETPOINT[3:0] register). Detection thresholds are summarized in Table *VDRIVE*. When VDRIVE_UV_THR[2:0] = 0, function is disabled.

• **Booster Status:** The physical activation of the booster phase is displayed by the BOOSTx_STATUS flag (non-latched, 0x0A). Please note this is different from the BOOSTx_EN control bit, which reports instead the willing to activate the booster. See also section *Booster Enable and Disable Control*.

• **Enable Pin Status:** The actual logic status read at ENABLEx pin is reported by the flag ENABLEx_STATUS (non-latched, 0x0B). Thanks to this diagnostic, the MCU can check proper logic level on the pin.

A short summary table of the main diagnostic bits related to the LED outputs follows.

Functional Description and Application Information (continued)

Diagnostic Summary

Flag	Description	Detection Level	Booster Output	Register Latched
TW	Thermal Warning	Factory trimmed	No change	Yes
TSD	Thermal Shutdown	Factory trimmed	Disabled. Re-enabled by rising edge on BOOSTx_EN after T_J < TW and TSD flag was cleared. Re-enabled automatically when TSD_AUT_RCVR_EN bit is set (in FSO/SA modes always).	Yes
TEMP_OUT	Temperature Output	See *Diagnostics* section	No change	No
SPIERR	SPI Error	See SPI section	No change	Yes
BOOST_OV	Overvoltage Shutdown	See *Electrical Characteristics*	Disabled. Re-enabled automatically below BOOST_RA threshold.	Yes
VBSTDIV_UV	Undervoltage Protection	See *Electrical Characteristics*	Disabled. Re-enabled by rising edge on BOOSTx_EN when VBOOSTDIV > BST_EA_UV / 34	Yes
VDRIVE_NOK	VDRIVE Out of Regulation	See *Electrical Characteristics*	No change	Yes
VDRIVE_UV*	VDRIVE UV Lockout	See *Diagnostics* section. Depends on SPI VDRIVE_VSETPOINT[3:0] and VDRIVE_UV_THR[2:0] settings.	Disabled. Re-enabled by rising edge on BOOSTx_EN after VDRIVE_UV condition disappears.	Yes
HWR	HW Reset	Set after POR	No change	Yes

* The flag not available in SPI map

TSD RECOVERY OVERVIEW

FSO_ENABLE_SEL SPI bit	TSD_AUT_RCVR_EN SPI bit	ENABLEx pin	BOOSTx_EN SPI bit	BOOSTERx status after TSD disappear
0	0	x	0	Disabled
0	0	x	1	Disabled
0	0	x	0 → 1 (Note 17)	Enabled
0	1	x	0	Disabled
0	1	x	1	Enabled
1	0	0	0	Disabled
1	0	0	1	Disabled
1	0	1	0	Disabled
1	0	1	1	Disabled
1	0	0 → 1 (Note 17)	1	Disabled
1	0	1	0 → 1 (Note 17)	Enabled
1	1	0	0	Disabled
1	1	0	1	Disabled
1	1	1	0	Disabled
1	1	1	1	Enabled

Note: 17. 0 → 1 … rising edge (after TW disappeared).

Functional Description and Application Information (continued)

Reset

POR always causes asynchronous reset − transition to reset state. The power-on-reset circuit (POR) monitors the VDD and VBB voltages to control the out-of-reset condition at power-up. Chip will leave the reset state and VDD regulator will be enabled when VBB > POR_VBB_H and VDD > POR3V_H and at least one ENABLE input is in logic “1”. When SPI register VDD_ENA is set to “1”, VDD regulator stays enabled and chip stays in normal mode, even if all ENABLE inputs are set to logic “0”. When SPI register VDD_ENA is set to “0” and all ENABLE inputs are set to logic “0”, chip enters the reset state and VDD regulator is switched off, current consumption from VBB is less than 1µA (for T_J = +30°C).

Init and Normal Mode

Normal mode is entered through Init state after internal delay of 150µs. In Init state, OTP Refresh is performed. If OTP bits for FSO_MD[2:0] register and OTP Lock Bit are programmed, transition to FSO/SA mode is possible. Device is fully started 500µs after rising edge on ENABLE pin.

FSO/Stand-Alone Mode

FSO (fail-safe operation)/stand-alone modes can be used for two main purposes:

- Default power-up operation of the chip (stand-alone functionality without external microcontroller or preloading of the registers with default content for default operation before microcontroller starts sending SPI commands for chip settings)
- Fail-safe functionality (chip functionality definition in fail-safe mode when the external microcontroller functionality is not guaranteed)

FSO/stand-alone function is controlled according to Table *FSO MODES DESCRIPTION*. Entrance into FSO/stand-alone mode is possible only after costumer OTP zapping when OTP Lock Bit is set. FSO/ENABLE2 pin serves to enter/exit FSO mode when SPI bit FSO_ENABLE_SEL = “0” (meaning that function of the pin is “FSO”). If FSO_ENABLE_SEL = “1”, FSO mode cannot be entered. Independent control of booster phases (FSO_ENABLE_SEL = “1”) is not available in FSO mode. When FSO_ENABLE_SEL is changed in FSO mode from “0” to “1”, the FSO mode is immediately exited. Actual value of SPI register FSO_MD[2:0] (preloaded from OTP only at power-up) is used for entrance into FSO mode and all FSO related functions are then controlled according to it. When FSO mode is entered, SPI status bit FSO is set. It is clear by read flag.

When FSO/stand-alone mode is activated, content of the following SPI registers is preloaded from OTP memory:

OTP Memory Map

BOOST_SKCL[1:0]
BOOST_OTA_GAIN[1:0]
VDRIVE_VSETPOINT[3:0]
VBOOST_VGATE_THR
BOOST_VLIMTH1[1:0]
BOOST_VLIMTH2[1:0]
BOOST_OV_REACT[1:0]
BOOST_SLPCTRL[2:0]
BOOST_OVERVOLTSD_THR[6:0]
BOOST_SRCINV
BOOST_MULTI_PHASE_MD[1:0]
BOOST_VSETPOINT[6:0]
FSO_BST_FREQ[2:0]
BOOST1_EN
BOOST2_EN
VDD_ENA
FSO_ENABLE_SEL
VBOOST_TOFF_SET[2:0]
VBOOST_TON_SET[2:0]
P_DISTRIBUTION1[4:0]
P_DISTRIBUTION2[4:0]
VDRIVE_UV_THR[2:0]

Functional Description and Application Information (continued)

In FSO (entered via falling edge on FSO/ENABLE2 pin) or stand-alone modes, internal booster PWM source with 50% duty cycle is used as booster frequency. Frequency at which booster runs is determined by value in FSO_BST_FREQ[2:0] register. Values which can be selected are shown in the following table.

BOOSTER FREQUENCY IN FSO MODES

FSO_BST_FREQ[2:0]	Booster Frequency [kHz]
0x0	200
0x1	294.1
0x2	416.7
0x3	500
0x4	625
0x5	714.3
0x6	833
0x7	1000

To achieve better EMC performance, in FSO or stand-alone modes, the AL8859Q provides fixed switching frequency dither function. The spread spectrum frequency modulation block modulates the oscillator frequency by ±13% of the nominal frequency switching frequency. The modulation frequency is 500Hz fixed.

TSD_AUT_RCVR_EN is kept high “1” in FSO or stand-alone modes, allowing automatic recovery when thermal shutdown occurs. TSD_AUT_RCVR_EN is loaded from OTP only when FSO_MD[2:0] = 1. BOOSTx_EN bits are kept high “1” in FSO modes (entered via falling edge on FSO pin), enabling booster phases. If BOOSTx_EN values preloaded from OTP’s are and remain “0”, corresponding booster phases will be disabled when FSO mode is exited.

FSO MODES OVERVIEW

FSO_MD[2:0]	FSO entered after startup	FSO entered after falling edge on FSO pin	SPI ctrl. Registers loaded with “00” after POR	SPI ctrl. Registers loaded with values from customer OTPs after POR	SPI registers update in FSO enabled	OTP programming needed
0	N	N	Y	N	N	N
1	N	N	N	Y	N	Y
2	N	Y	Y	N	N	Y
3	N	Y	Y	N	Y	Y
4	N	Y	N	Y	N	Y
5	N	Y	N	Y	Y	Y
6	Y	N	N	Y	N	Y
7	Y	Y*	N	Y	Y	Y

* after proper FSO_MD[2:0] register update

Functional Description and Application Information (continued)

FSO MODES DESCRIPTION

FSO_MD[2:0]	Description
000b = 0	**FSO mode disabled, registers are loaded with safe value = 0x00h after POR, default** • After the reset, control registers are loaded with 0x00h value. • Entrance into FSO mode is not possible.
001b = 1	**FSO mode disabled, registers are loaded with data from OTP memory after POR** • After the reset, control registers are loaded with data stored in OTP memory (device's OTP memory has to be programmed, OTP Lock Bit has to be set). It reduces number of SPI transfers needed to configure the device after the reset. • Entrance into FSO mode is not possible.
010b = 2	**FSO entered after falling edge on FSO pin, registers are loaded with safe value = 0x00h after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is disabled (SPI write operation is blocked; clearing of SPI registers is blocked; SPIERR flag is set in case of invalid SPI frame). • FSO/ENABLE2 pin serves to enter/exit FSO mode (when SPI bit FSO_ENABLE_SEL = 0). • Internal booster PWM source will be selected as the booster frequency after activation of FSO mode.
011b = 3	**FSO entered after falling edge on FSO pin, registers are loaded with safe value = 0x00h after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is enabled • FSO mode can be exited by writing FSO_MD[2:0] = 000 or 001 • FSO/ENABLE2 pin serves to enter/exit FSO mode (when SPI bit FSO_ENABLE_SEL = 0). • If SPI bit FSO_ENABLE_SEL is written with "1" in FSO mode, the FSO mode is immediately exited. • Internal booster PWM source will be selected as the booster frequency after activation of FSO mode.
100b = 4	**FSO entered after falling edge on FSO pin, registers are loaded with data from OTP memory after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is disabled (SPI write operation is blocked; clearing of SPI registers is blocked; SPIERR flag is set in case of invalid SPI frame). • FSO/ENABLE2 pin serves to enter/exit FSO mode (when SPI bit FSO_ENABLE_SEL = 0). • Internal booster PWM source will be selected as the booster frequency after activation of FSO mode.
101b = 5	**FSO entered after falling edge on FSO pin, registers are loaded with data from OTP memory after POR** • After FSO mode activation, control registers are loaded with data stored in OTP memory. • SPI register update (SPI write/read operation) in FSO mode is enabled. • FSO mode can be exited by writing FSO_MD[2:0] = 000 or 001. • FSO/ENABLE2 pin serves to enter/exit FSO mode (when SPI bit FSO_ENABLE_SEL = 0). • If SPI bit FSO_ENABLE_SEL is written with "1" in FSO mode, the FSO mode is immediately exited. • Internal booster PWM source will be selected as the booster frequency after activation of FSO mode.
110b = 6	**SA (stand-alone)/FSO entered after POR, registers are loaded with data from OTP memory** • After SA/FSO mode activation, control registers are loaded with data from OTP memory. • SPI register update (SPI write/read operation) in SA/FSO mode is disabled (SPI write operation is blocked; clearing of SPI registers is blocked; SPIERR flag is set in case of invalid SPI frame). • Internal booster PWM source will be selected as the booster frequency.
111b = 7	**SA (stand-alone)/FSO entered after POR, registers are loaded with data from OTP memory** • After SA/FSO mode activation, control registers are loaded with data from OTP memory. • SPI register update (SPI write/read operation) in SA/FSO mode is enabled. • FSO mode can be exited by writing FSO_MD[2:0] = 000 or 001. • If SPI bit FSO_ENABLE_SEL is written with "1" in FSO mode, the FSO mode is immediately exited. • Internal booster PWM source will be selected as the booster frequency.

Functional Description and Application Information (continued)

SPI Interface

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. The AL8859Q acts always as a slave, and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The AL8859Q SPI transfer size is 16 bits. During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCLK) synchronizes shifting and sampling of the information on the two serial data lines: SDO and SDI. The SDO signal is the output from the slave (AL8859Q), and the SDI signal is the output from the master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple-slave system.

The CSB line is active low. If an AL8859Q is not selected, SDO is in high impedance state and it does not interfere with SPI bus activities. Since the AL8859Q always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation. The implemented SPI allows connection to multiple slaves by means of star connection (CSB per slave) or by means of daisy chain. An SPI star connection requires a bus = (3 + N) total lines, where N is the number of slaves used, the SPI frame length is 16 bits per communication.

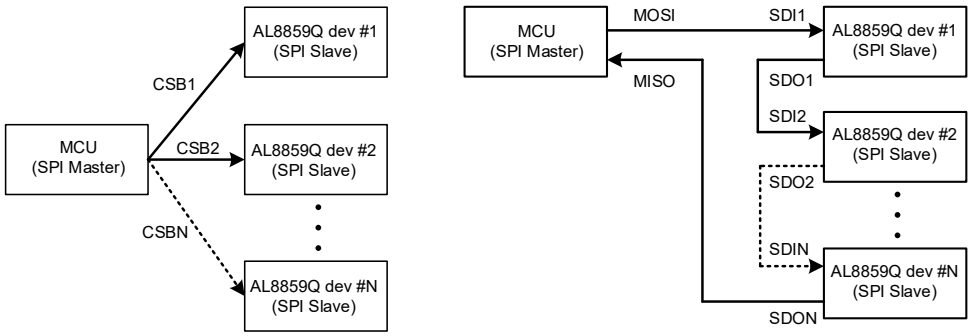


Figure 14. SPI Star vs. Daisy Chain Connection

SPI Daisy Chain Mode

SPI daisy chain connection bus width is always four lines independently on the number of slaves. However, the SPI transfer frame length will be a multiple of the base frame length so N x 16 bits per communication: the data will be interpreted and read in by the devices at the moment the CSB rises.

A diagram showing the data transfer between devices in daisy chain connection is given further: CMDx represents the 16-bit command frame on the data input line transmitted by the master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

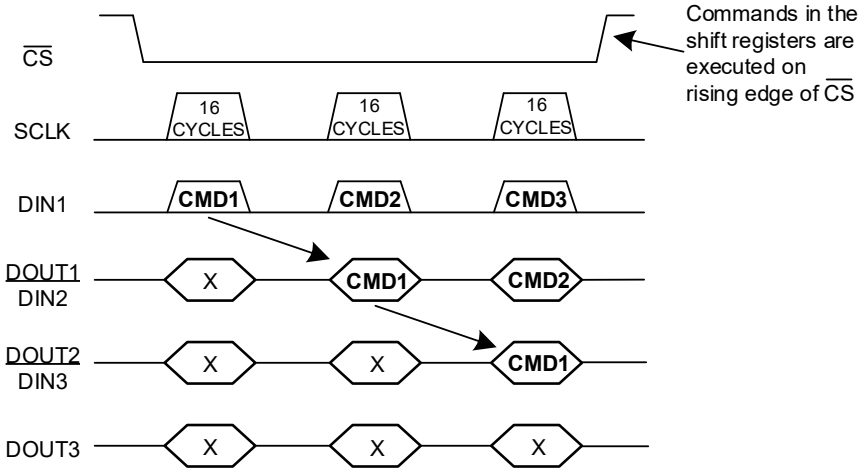


Figure 15. SPI Daisy Chain Data Shift Between Slaves

Functional Description and Application Information (continued)

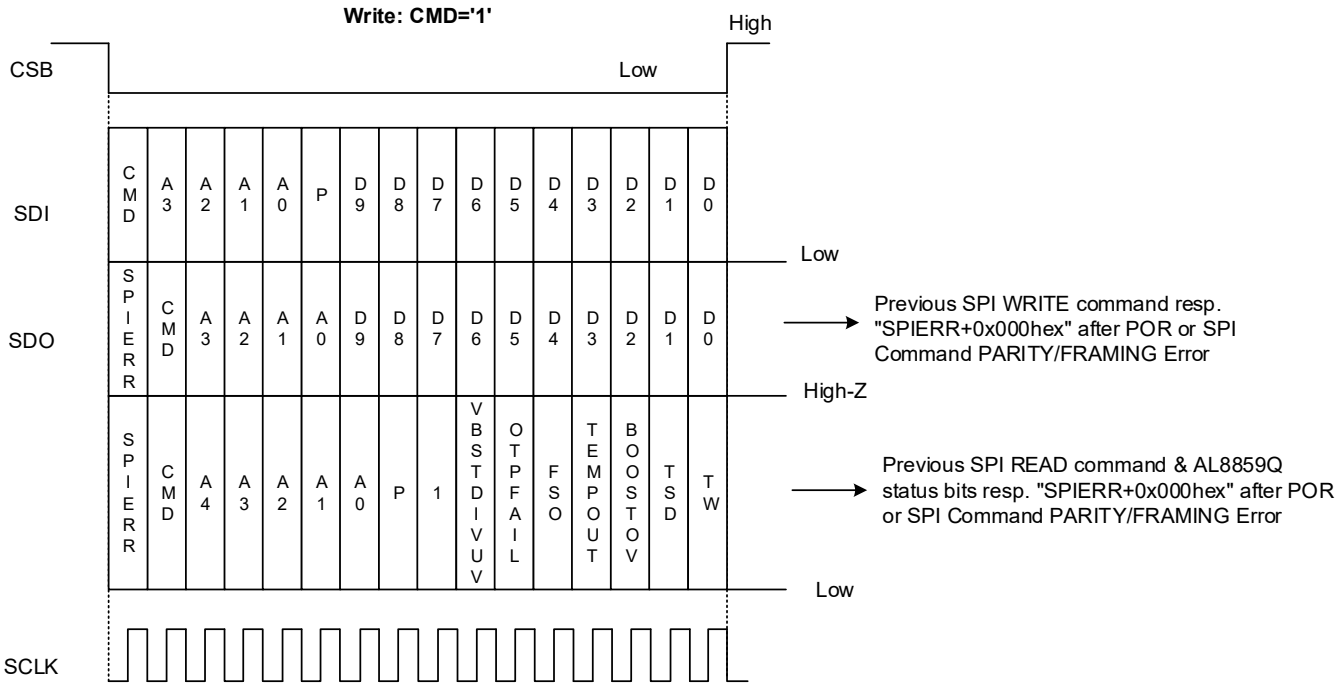
The symbol “x” represents the previous content of the SPI shift register buffer.

The AL8859Q default power up communication mode is “star”. In order to enable daisy chain mode, a multiple of 16 bits clock cycles must be sent to the devices, while the SDI line is left to zero.

Note: To come back to star mode the NOP register (address 0x0000) must be written with all ones, with the proper data parity bit and parity framing bit: see SPI protocol for details about parity and write operation.

SPI Transfer Format

Two types of SPI commands (to SDI pin of AL8859Q) from the micro controller can be distinguished: “Write to a control register” and “Read from register (control or status)”. The frame protocol for the write operation:



P = not (CMD xor A3 xor A2 xor A1 xor A0 xor D9 xor D8 xor D7 xor D6 xor D5 xor D4 xor D3 xor D2 xor D1 xor D0

Figure 16. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the SDI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 1 for write operation.
- Bits[14:11]: 4 bits WRITE ADDRESS field.
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame.
- Bits[9:0]: 10 bit DATA to write.

Device in the same time replies to the master (on the SDO):

- If the previous command was a write and no SPI error had occurred, a copy of the command, address and data written fields.
- If the previous command was a read, the response frame summarizes the address used and an overall diagnostic check (copy of the main detected errors, see Figure 16 and Figure 17 for details).
- In case of previous SPI error or after power-on-reset, only the MSB bit will be 1, followed by zeros. If parity bit in the frame is wrong, device will not perform command and <SPI> flag will be set.

Functional Description and Application Information (continued)

The frame protocol for the read operation:

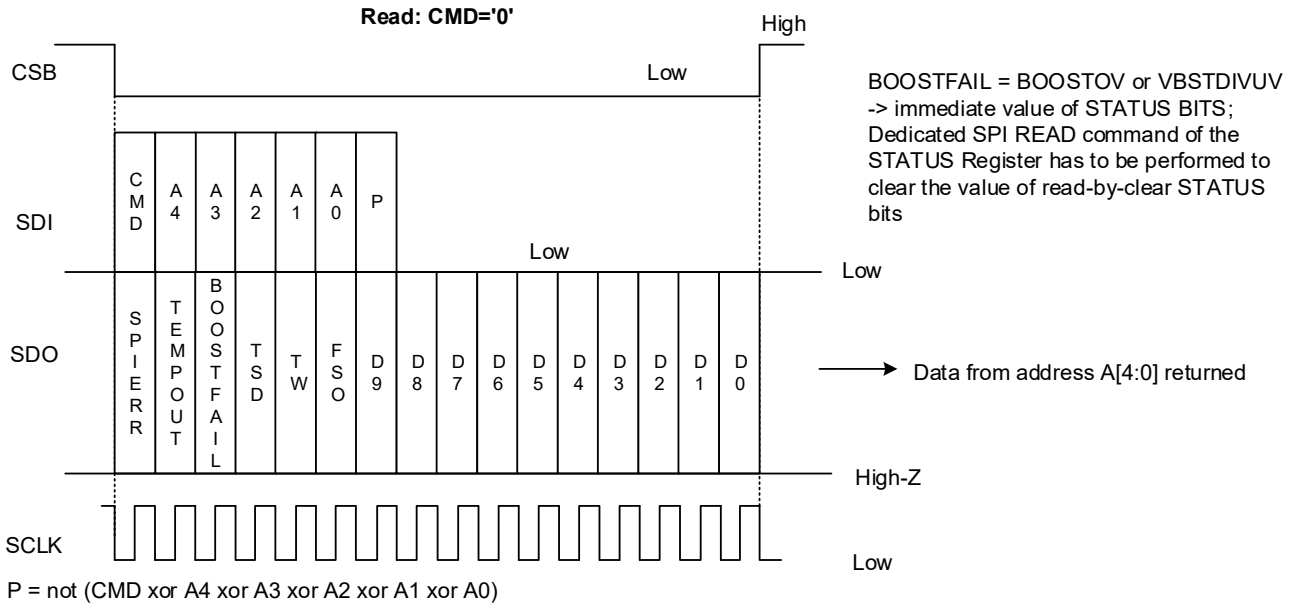


Figure 17. SPI Read Frame

Referring to the previous picture, the read frame coming from the master (into the SDI) is composed from the following fields:

- Bit[15] (MSB): CMD bit = 0 for read operation.
- Bits[14:10]: 5 bits READ ADDRESS field.
- Bit[10]: frame parity bit. It is ODD parity formed by the negated XOR of all other bits in the frame.
- Bits [8:0]: 9 bits zeroes field.

Device in the same frame provides to the master (on the SDO) data from the required address (in frame response), thus achieving the lowest communication latency.

SPI Framing and Parity Error

SPI communication framing error is detected by the AL8859Q in the following situations:

- Not an integer multiple of 16 CLK pulses are received during the active-low CSB signal.
- LSB bits (8...0) of a read command are not all zero.
- SPI parity errors, either on write or read operation.

Once an SPI error occurs, the <SPI> flag can be reset only by reading the status register in which it is contained (using in the read frame the right communication parity bit).

Functional Description and Application Information (continued)

SPI Interface Logic Electrical Characteristics (SCK, SDO, SDI, CSB) (Note 18)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CSS}	CSB Setup Time	—	0.5	—	—	μs
t_{CSH}	CSB Hold Time	—	0.25	—	—	μs
t_{WL}	SCLK Low Time	—	0.5	—	—	μs
t_{WH}	SCLK High Time	—	0.5	—	—	μs
t_{SU}	Data-In (DIN) Setup Time, Valid Data Before Rising Edge of CLK	—	0.25	—	—	μs
t_H	Data-In (DIN) Hold Time, Hold Data After Rising Edge of CLK	—	0.275	—	—	μs
t_{DIS}	Output (DOUT) Disable Time (Note 19)	—	0.07	—	0.32	μs
$t_{V1\to0}$	Output (DOUT) Valid (Note 19)	—	—	—	0.32	μs
$t_{V0\to1}$	Output (DOUT) Valid (Note 20)	—	—	—	$0.32+t_{(RC)}$	μs
t_{HO}	Output (DOUT) Hold Time (Note 19)	—	0.07	—	—	μs
t_{CS}	CSB High Time	—	1	—	—	μs

Notes: 18. These tested parameters are guaranteed by design, not tested in production.
19. SDO low-side switch activation time.
20. Time depends on the SDO load and pullup resistor.

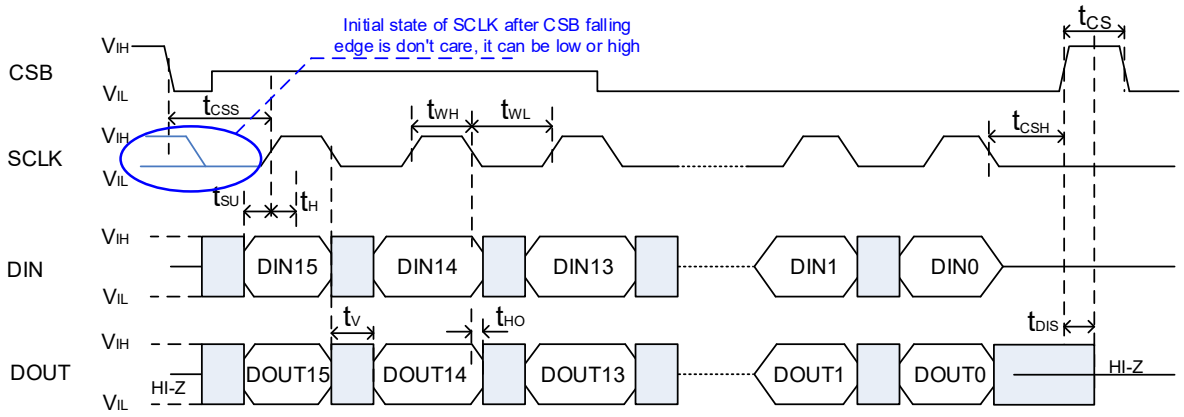


Figure 18. SPI Communication Timing

Register Definition

SPI ADDRESS MAP

ADDR	R/W	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	NA	NOP register (tead/write operation ignored)									
0x01	R/W	RESERVED	VBOOST_VGATE_THR	VDRIVE_VSETPOINT[3:0]				BOOST_OTA_GAIN[1:0]		BOOST_SKCL[1:0]	
0x02	R/W	0x0	BOOST_SLPCTRL[2:0]			RESERVED		BOOST_VLIMITH2[1:0]		BOOST_VLIMITH1[1:0]	
0x03	R/W	BOOST_MULTI_PHASE_MD[1:0]		BOOST_SRCINV	BOOST_OVERVOLTSD_THR[6:0]						
0x04	R/W	FSO_BST_FREQ[2:0]			BOOST_VSETPOINT[6:0]						
0x05	R/W	TSD_AUT_RCVR_EN	ADC_TEMP_THR[2:0]			FSO_MD[2:0]			RESERVED	BOOST2_EN	BOOST1_EN
0x06	R/W	BOOST_OV_REACT[1:0]		VBOOST_TON_SET[2:0]			VBOOST_TOFF_SET[2:0]			FSO_ENABLE_SEL	VDD_ENA
0x07	R/W	P_DISTRIBUTION2[4:0]					P_DISTRIBUTION1[4:0]				
0x08	R/W	0x0		VDRIVE_UV_THR[2:0]			RESERVED				
0x09	R/W	0x0			OTP_BIAS_H	OTP_BIAS_L	OTP_ADDR[2:0]			OTP_OPERATION[1:0]	
0x0A	R	HWR	ODD PARITY	RESERVED	BOOST2_STATUS	BOOST1_STATUS	BOOST_OV	TEMP_OUT	UARTE	TSD	TW
0x0B	R	0x0	ODD PARITY	RESERVED	ENABLE2_STATUS	ENABLE1_STATUS	VDRIVE_NOK	VBSTDIV_UV	OTP_ACTIVE	OTP_FAIL	FSO
0x0C	R	OTP_DATA[9:0]									
0x0D	R	0x0		REVID[7:0]							
OTHER	R	0x0									

Bit Definition

Symbol	MAP Position	Description
REGISTER 0x00(CR): NOP Register, Reset Value (POR) = 0000000000_2		
NOP	Bits [9:0]-ADDR_0x00	NOP Register (read/write operation ignored)
REGISTER 0x01(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
VBOOST_VGATE_THR	Bit 8-ADDR_0x01	Adjustment of Gate Threshold Voltage for Booster Transistor
VDRIVE_VSETPOINT[3:0]	Bits [7:4]-ADDR_0x01	VDRIVE Voltage
BOOST_OTA_GAIN[1:0]	Bits [3:2]-ADDR_0x01	Error Amplifier Gain
BOOST_SKCL[1:0]	Bits [1:0]-ADDR_0x01	Booster Skip Cycle Settings
REGISTER 0x02(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
BOOST_SLPCTRL[2:0]	Bits [8:6]-ADDR_0x02	Booster Slope Control
BOOST_VLIMTH2[1:0]	Bits [3:2]-ADDR_0x02	Booster phase Current Limitation
BOOST_VLIMTH1[1:0]	Bits [1:0]-ADDR_0x02	Booster phase Current Limitation
REGISTER 0x03(CR): Booster Settings, Reset Value (POR) = 0001111111_2		
BOOST_MULTI_PHASE_MD[1:0]	Bits [9:8]-ADDR_0x03	Stand Alone/Master/Slave Selection
BOOST_SRCINV	Bit 7-ADDR_0x03	Booster Clock Inversion
BOOST_OVERVOLTSD_THR[6:0]	Bits [6:0]-ADDR_0x03	Booster Overvoltage Threshold
REGISTER 0x04(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
FSO_BST_FREQ[2:0]	Bits [9:7]-ADDR_0x04	Booster Frequency
BOOST_VSETPOINT[6:0]	Bits [6:0]-ADDR_0x04	Booster Voltage Setpoint
REGISTER 0x05(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
TSD_AUT_RCVR_EN	Bit 9-ADDR_0x05	Thermal Shutdown Automatic Recovery
ADC_TEMP_THR[2:0]	Bits [8:6]-ADDR_0x05	Temperature Output Threshold
FSO_MD[2:0]	Bits [5:3]-ADDR_0x05	Fail-Safe Operation Mode Selection
BOOST2_EN	Bit 1 -ADDR_0x05	Booster Phase 2 Enable
BOOST1_EN	Bit 0-ADDR_0x05	Booster Phase 1 Enable
REGISTER 0x06(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
BOOST_OV_REACT[1:0]	Bits [9:8]-ADDR_0x06	Booster Overvoltage Reaction
VBOOST_TON_SET[2:0]	Bits [7:5]-ADDR_0x06	Booster Minimal TON
VBOOST_TOFF_SET[2:0]	Bits [4:2]-ADDR_0x06	Booster Minimal TOFF
FSO_ENABLE_SEL	Bit 1-ADDR_0x06	Function of FSO/ENABLE2 Pin
VDD_ENA	Bit 0-ADDR_0x06	VDD Active without Enable Pin
REGISTER 0x07(CR): Booster Settings, Reset Value (POR) =0000000000_2		
P_DISTRIBUTION2[4:0]	Bits [9:5]-ADDR_0x07	Power Distribution phase 2
P_DISTRIBUTION1[4:0]	Bits [4:0]-ADDR_0x07	Power Distribution phase 1

Bit Definition (continued)

Symbol	MAP position	Description
REGISTER 0x08(CR): Booster Settings, Reset Value (POR) = 0000000000_2		
VDRIVE_UV_THR[2:0]	Bits [9:5]-ADDR_0x08	VDRIVE Undervoltage Threshold
REGISTER 0x09(CR): OTP Operations, Reset Value (POR) = 0000000000_2		
OTP_BIAS_H	Bit 6-ADDR_0x09	OTP Bias High
OTP_BIAS_L	Bit 5-ADDR_0x09	OTP Bias Low
OTP_ADDR[2:0]	Bits [4:2]-ADDR_0x09	OTP Address
OTP_OPERATION[1:0]	Bits [1:0]-ADDR_0x09	OTP Operation
REGISTER 0x0A (SR): Booster Status, Reset Value (POR) = $1x000xxxxx_2$		
HWR	Bit 9-ADDR_0x0A	Hardware Reset Flag
ODD PARITY	Bit 8-ADDR_0x0A	Odd Parity Over Data
BOOST2_STATUS	Bit 6-ADDR_0x0A	Booster Phase 2 Status
BOOST1_STATUS	Bit 5-ADDR_0x0A	Booster Phase 1 Status
BOOST_OV	Bit 4-ADDR_0x0A	Booster Overvoltage Flag
TEMP_OUT	Bit 3-ADDR_0x0A	Temperature Output
SPIERR	Bit 2-ADDR_0x0A	SPI Error
TSD	Bit 1-ADDR_0x0A	Thermal Shutdown
TW	Bit 0-ADDR_0x0A	Thermal Warning
REGISTER 0x0B(SR): Booster Status, Reset Value (POR) = $0x0xxxx00x_2$		
ODD PARITY	Bit 8-ADDR_0x0B	Odd Parity Over Data
ENABLE2_STATUS	Bit 6-ADDR_0x0B	Enable Pin 2 Status
ENABLE1_STATUS	Bit 5-ADDR_0x0B	Enable Pin 1 Status
VDRIVE_NOK	Bit 4-ADDR_0x0B	VDRIVE Voltage Not OK
VBSTDIV_UV	Bit 3-ADDR_0x0B	VBOOST Divider Undervoltage Flag
OTP_ACTIVE	Bit 2-ADDR_0x0B	OTP Active Flag
OTP_FAIL	Bit 1-ADDR_0x0B	OTP Fail Flag
FSO	Bit 0-ADDR_0x0B	Fail-Safe Operation Mode Active Flag
REGISTER 0x0C (SR): OTP Data, Reset Value (POR) = 0000000000_2		
OTP_DATA[9:0]	Bits [9:0] -ADDR_0x0C	OTP Data Register
REGISTER 0x0D (SR): Revision ID, Reset Value (POR) = $00xxxxxxxx_2$		
REVID[7:0]	Bits [7:0]-ADDR_0x0D	Revision ID

POR values of status registers are shown in situation that FSO mode is not entered after POR. All latched flags are “cleared by read”. “x” means that value after reset is defined during reset phase (diagnostics) or is trimmed during manufacturing process.
SPI register SPI_REVID[7:0] is used to track the silicon version, following encoding mechanism is used:

- SPI_REVID[7] : 1 for AL8859Q
- SPI_REVID[6:4] : Full Mask Version <0 to 7>
- SPI_REVID[3:0] : Metal Tune <0 to 15>
- REVID[7:0] for N702-0 device is 91hex (AL8859Q = 1, Full Mask Version = 1, Metal Tune = 1)

Functional Description and Application Information (continued)

OTP Memory

Description

The OTP (one-time programmable) memory contains 75 bits which bear the most important application dependent parameters and is user-programmable via SPI interface. The programming of these bits is typically done at the end of the module manufacturing line. OTP memory serves to store configuration data for fail-safe or stand-alone functionality or default configuration of the chip after power-up.

The OTP bits can be programmed only once. This is ensured by dedicated OTP Lock Bit which is set during programming.

OTP MAP

OTP bits	Connection to SPI register
OTP[1:0]	BOOST_SKCL[1:0]
OTP[3:2]	BOOST_OTA_GAN[1:0]
OTP[7:4]	VDRIVE_VSETPOINT[3:0]
OTP[8]	VBOOST_VGATE_THR
OTP[9]	SPARE = “0”
OTP[11:10]	BOOST_VLIMTH1[1:0]
OTP[13:12]	BOOST_VLIMTH2[1:0]
OTP[15:14]	SPARE[1:0] = “00”
OTP[17:16]	BOOST_OV_REACT[1:0]
OTP[20:18]	BOOST_SLPCTRL[2:0]
OTP[27:21]	BOOST_OVERVOLTSD_THR[6:0]
OTP[28]	BOOST_SRCINV
OTP[30:29]	BOOST_MULTI_PHASE_MD[1:0]
OTP[37:31]	BOOST_VSETPOINT[6:0]
OTP[40:38]	FSO_BST_FREQ[2:0]
OTP[41]	BOOST1_EN
OTP[42]	BOOST2_EN
OTP[43]	SPARE = “0”
OTP[46:44]	FSO_MD[2:0]
OTP[47]	TSD_AUT_RCVR_EN
OTP[48]	VDD_ENA
OTP[49]	FSO_ENABLE_SEL
OTP[52:50]	VBOOST_TOFF_SET[2:0]
OTP[55:53]	VBOOST_TON_SET[2:0]
OTP[60:56]	P_DISTRIBUTION1[4:0]
OTP[65:61]	P_DISTRIBUTION2[4:0]
OTP[70:66]	SPARE[4:0] = “00000”
OTP[73:71]	VDRIVE_UV[2:0]
OTP[74]	OTP Lock Bit

Functional Description and Application Information (continued)

The OTP bits addressed by SPI register OTP_ADDR[2:0] are accessible (read only) in the SPI register OTP_DATA[9:0] after OTP Refresh operation (OTP_OPERATION[1:0] = 0x1) in the following way:

OTP_ADDR[2:0] = 0x0: OTP_DATA[9:0] = OTP[9:0]

OTP_ADDR[2:0] = 0x1: OTP_DATA[9:0] = OTP[19:10]

OTP_ADDR[2:0] = 0x2: OTP_DATA[9:0] = OTP[29:20]

OTP_ADDR[2:0] = 0x3: OTP_DATA[9:0] = OTP[39:30]

OTP_ADDR[2:0] = 0x4: OTP_DATA[9:0] = OTP[49:40]

OTP_ADDR[2:0] = 0x5: OTP_DATA[9:0] = OTP[59:50]

OTP_ADDR[2:0] = 0x6: OTP_DATA[9:0] = OTP[69:60]

OTP_ADDR[2:0] = 0x7: OTP_DATA[9:0] = {00000 &OTP[74:70]}

OTP Operations

The AL8859Q supports following operations with OTP memory:

- OTP_OPERATION[1:0] = 0x0 or 0x3: **NOP** (no operation)
- OTP_OPERATION[1:0] = 0x1: **OTP Refresh** – refresh of the whole OTP memory (75 bits). Data addressed by SPI register OTP_ADDR[2:0] are available in SPI register OTP_DATA[9:0] after the end of OTP Refresh operation. Duration of OTP Refresh operation should be 46µs measured from CSB rising edge.
- OTP_OPERATION[1:0] = 0x2: **OTP Zap** – data from SPI register (those listed in Table *OTP MAP*) and OTP Lock Bit are programmed into OTP memory. OTP Zap operation is allowed to be performed only once − when OTP Lock Bit is unprogrammed. Duration of OTP Zap operation should be 15ms measured from CSB rising edge. SPI status bit OTP_ACTIVE is set to “log. 1” when an OTP operation is in progress.

OTP Programming Procedure

Following procedure should be applied to program OTP memory:

- VBB voltage has to be higher than 7.65V with current capability at least 50mA. The user has to insure that the right voltage is available in the application. Remark: Lower VBB voltage does not prevent OTP zapping.
- SPI registers listed in Table *OTP MAP* have to be written with required content.
- Content of the SPI registers (those listed in Table *OTP MAP*) is programmed into the OTP memory by OTP_OPERATION[1:0] = 0x2 SPI write command. OTP Lock Bit is programmed automatically at the same time to prevent any further OTP programming.

OTP Programming Verification

OTP_FAIL bit in the SPI status register is set when VBB undervoltage (VBB < VBB_OTP_L) is detected during OTP Zap operation. It is clear by read flag. The OTP_BIAS_H and OTP_BIAS_L registers are used to check proper OTP programming. After OTP programming, the OTP content has to be the same as programmed when OTP is read with OTP_BIAS_H = 1 and OTP_BIAS_L = 1.

Following procedures should be applied to verify OTP content:

- VDD voltage has to be kept in range for normal mode operation.
- Write SPI registers OTP_BIAS_L = 1 and OTP_BIAS_H = 0.
- Write SPI register OTP_OPERATION[1:0] = 0x1 (OTP Refresh) for all OTP_ADDR[2:0] values and check corresponding OTP_DATA[9:0] content which has to match with previously programmed data.
- Write SPI registers OTP_BIAS_L = 0 and OTP_BIAS_H = 1.
- Write SPI register OTP_OPERATION[1:0] = 0x1 (OTP Refresh) for all OTP_ADDR[2:0] values and check corresponding OTP_DATA[9:0] content which has to match with previously programmed data.
- Programming is considered as successful when no mismatch is observed and OTP_FAIL flag is not set.

Design Tools (https://www.diodes.com/design/tools/)

- AL8859Q Demo Board & User Guide
- Demo Board Gerber File for PCB Layout Reference
- PSPICE Digital Simulation

Functional Description and Application Information (continued)

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	+150°C +200°C 60 to 120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max
Liquidous temperature (TL) Time at liquidous (tL)	+217°C 60 to 150 seconds
Peak package body temperature (Tp)*	Max +260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max
Time +25°C to peak temperature	8 minutes max

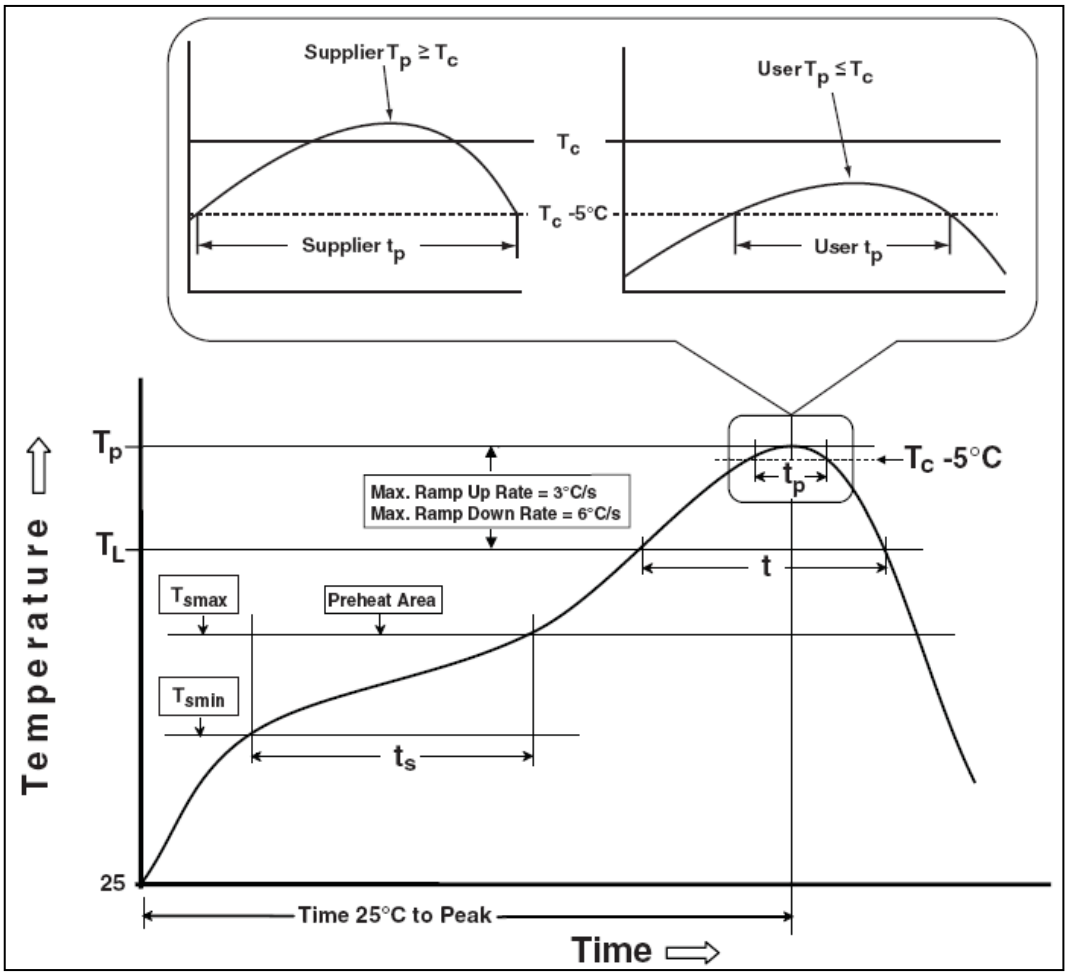
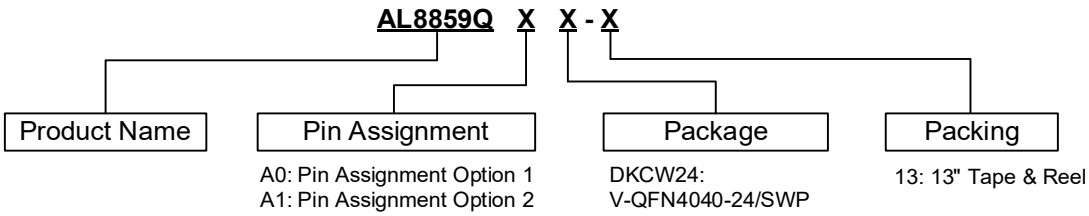


Figure 19. Classification Profile

Ordering Information (Note 21)



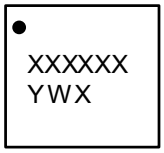
Orderable Part Number	Package	Packing	
		Qty.	Carrier
AL8859QA0DKCW24-13	V-QFN4040-24/SWP	3000	13'' Tape and Reel
AL8859QA1DKCW24-13	V-QFN4040-24/SWP	3000	13'' Tape and Reel

Note: 21. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

Package: V-QFN4040-24/SWP

(Top View)



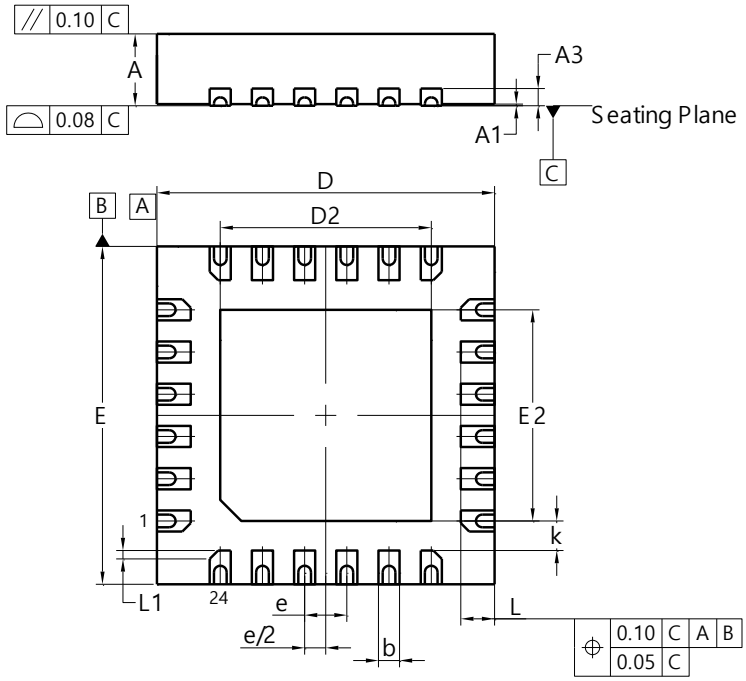
XXXXXX: Identification Code
Y : Year : 0~9
W : Week : A~Z : week 1~26;
a~z : week 27~52; z represents
week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AL8859QA0DKCW24-13	V-QFN4040-24/SWP	59Q-A0
AL8859QA1DKCW24-13	V-QFN4040-24/SWP	59Q-A1

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN4040-24/SWP

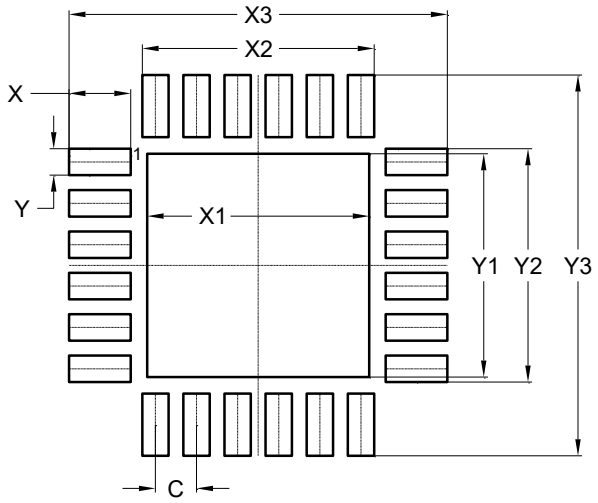


V-QFN4040-24/SWP			
Dim	**Min**	**Max**	**Typ**
A	0.80	0.90	0.85
A1	--	0.05	--
A3	--	--	0.203
b	0.20	0.30	0.25
D	3.90	4.10	4.00
D2	2.40	2.60	2.50
E	3.90	4.10	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
k	0.25	--	--
L	0.35	0.45	0.40
L1	0.05	0.15	0.10
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN4040-24/SWP



Dimensions	Value (in mm)
C	0.500
X	0.750
X1	2.700
X2	2.820
X3	4.600
Y	0.320
Y1	2.700
Y2	2.820
Y3	4.600

Please see https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf for tape and reel details.

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 (e3)
- Weight: 0.0304 grams (Approximate)

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

www.diodes.com