NVIDIA BlueField-3 DPU Controller User Manual

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About This Manual

This User Manual describes NVIDIA® BlueField®-3 BF3220SH DPU Controller cards. It provides details as to the interfaces of the board, specifications, required software and firmware for operating the card, hardware installation, driver installation and bring-up instructions.

Ordering Part Numbers

The below table provides the ordering part numbers (OPN) for the available BlueField BF3220SH DPU Controllers.

Model	NVIDIA SKU		Heatsink	Lifecycle
B3220SH	**900-9D3C6-00CV-GA0**	NVIDIA BlueField-3 B3220SH E-Series **No heatsink** FHHL Storage Controller, 200GbE (default mode) / NDR200 IB, Dual-port QSFP112, PCIe Gen5.0 x16 with x16 PCIe extension option, 16 Arm cores, 48GB on-board DDR, integrated BMC, Crypto Enabled, Secure Boot	No Heatsink	Mass Production
	900-9D3C6-00CV-DA0	NVIDIA BlueField-3 B3220SH E-Series FHHL Storage Controller, 200GbE (default mode) / NDR200 IB, Dual-port QSFP112, PCIe Gen5.0 x16 with x16 PCIe extension option, 16 Arm cores, 48GB on-board DDR, integrated BMC, Crypto Enabled, Secure Boot	✓	Mass Production
	900-9D3C6-00SV-DA0	NVIDIA BlueField-3 B3220SH E-Series FHHL Storage Controller, 200GbE (default mode) / NDR200 IB, Dual-port QSFP112, PCIe Gen5.0 x16 with x16 PCIe extension option, 16 Arm cores, 48GB on-board DDR, integrated BMC, Crypto Disabled, Tall Bracke	✓	Mass Production

Intended Audience

This manual is intended for the installer and user of these cards. The manual assumes basic familiarity with InfiniBand/Ethernet network and architecture specifications.

Technical Support

Customers who purchased NVIDIA products directly from NVIDIA are invited to contact us through the following methods:

- URL: www.nvidia.com → Support
- E-mail: enterprisesupport@nvidia.com

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Customers who purchased NVIDIA products through an NVIDIA-approved reseller should first seek assistance through their reseller.

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Related Documentation

Related Documentation

InfiniBand Architecture Specification	InfiniBand Trade Association (IBTA) InfiniBand® specification Release 1.3.1, November 2, 2016 and Vol. 2, Release 1.4 , and Vol 2 - Release 1.5.
IEEE Std 802.3 Specification	IEEE Ethernet specification.
PCI Express Specifications	Industry Standard PCI Express Base and Card Electromechanical Specifications.
NVIDIA LinkX Interconnect Solutions	The NVIDIA® LinkX® product family of cables and transceivers provide the industry's broadest portfolio of QDR/FDR10 (40Gb/s), FDR (56Gb/s), EDR/HDR100 (100Gb/s), HDR (200Gb/s) and NDR (400Gb/s) cables, including Direct Attach Copper cables (DACs), copper splitter cables, Active Optical Cables (AOCs) and transceivers in a wide range of lengths from 0.5m to 10km. In addition to meeting IBTA standards, NVIDIA tests every product in an end-to-end environment ensuring a Bit Error Rate of less than 1E-15.
BlueField DPU Platform BSP Documentation	This guide provides product release notes as well as information on the BSP and how to develop and/or customize applications, system software, and file system images for the BlueField platform.
DOCA SDK Software Documentation	NVIDIA DOCA SDK software.

Document Conventions

When discussing memory sizes, GB and GBytes are used in this document to mean size in giga Bytes. The use of Gb or Gbits (small b) indicates size in giga bits. In this document PCIe is used to mean PCI Express.

Revision History

A list of the changes made to this document are provided in Document Revision History.

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1 Introduction

The NVIDIA® BlueField®-3 data processing unit (DPU) Controller is the 3rd-generation data center infrastructure-on-a-chip that enables organizations to build software-defined, hardware-accelerated IT infrastructures from cloud to core data center to edge. With 200Gb/s Ethernet or NDR200 200Gb/s InfiniBand network connectivity, BlueField-3 DPU Controller offloads, accelerates, and isolates software-defined networking, storage, security, and management functions in ways that profoundly improve data center performance, efficiency, and security. Providing powerful computing, and a broad range of programmable acceleration engines in the I/O path, BlueField-3 is perfectly positioned to address the infrastructure needs of the most demanding applications, while delivering full software backward compatibility through the NVIDIA DOCA™ software framework.
BlueField-3 DPU Controllers are highly optimized for NVMe storage systems, Network Functions Virtualization (NFV), Cloud and Machine Learning workloads. BlueField-3 integrates all the discrete components of a storage system appliance into a single chip making it the premier solution for building Just-a-Bunch-Of-Flash (JBOF) systems, All-Flash-Array and storage appliances for NVMe over Fabrics. With an integrated NVMe-oF and NVMe/TCP offload accelerator, the BlueField-3 DPU Controller has a superior performance advantage over existing JBOF systems, significantly reducing storage transaction latency, while increasing IOPs (I/O operations per second).

1.1 System Requirements

Motherboard	**In PCIe x16 Configuration** PCIe Gen 5.0 (32GT/s) through x16 edge connector. **In PCIe x16 Extension Option - Switch DSP (Data Stream Port)** • PCIe Gen 5.0 SERDES @32GT/s through edge connector • PCIe Gen 5.0 SERDES @32GT/s through PCIe Auxiliary Connection Card
System Power Supply	The maximum power consumption is up to **150W** and is split between the two power sources as follows: • Up to 66W from the PCIe golden fingers (12V) • The rest of the consumed power is drawn from a supplementary 8-pin ATX power supply connector ⚠ NOTE: The power cable is not included in the package. It should be part of the system wiring or ordered separately as an accessory.
Operating System	The BlueField-3 DPU Controller is shipped with Ubuntu – a Linux commercial operating system – which includes the NVIDIA OFED stack (MLNX_OFED), and is capable of running all customer-based Linux applications seamlessly. For more information, please refer to the DOCA SDK documentation or NVIDIA BlueField-3 Software User Manual.
Connectivity	• Interoperable with 1/10/25/40/50/100/200 Gb/s Ethernet switches and SDR/DDR/EDR/HDR100/HDR/NDR200 InfiniBand switches • Passive copper cable with ESD protection • Powered connectors for optical and active cable support

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1.2 Package Contents

Prior to unpacking your DPU Controller, it is important to make sure your server meets all the system requirements listed above for a smooth installation. Be sure to inspect each piece of equipment shipped in the packing box. If anything is missing or damaged, contact your reseller.

1.2.1 Card Package

Cards	1x BlueField-3 DPU Controller
Accessories	1x tall bracket (shipped assembled on the card)

1.2.2 Accessories Kit

> This is an optional accessories kit used for debugging purposes and can be ordered separately.

Kit OPN	Contents
MBF35-DKIT	4-pin USB to female USB Type-A cable
	20-pin shrouded connector to USB Type-A cable

1.2.3 PCIe Auxiliary Card Package

> This is an optional kit.

The PCIe auxiliary kit can be purchased separately to operate selected DPU Controllers in a dual-socket server. For package contents, refer to PCIe Auxiliary Card Kit.

For more detailed information, refer to Specifications.

1.3 Features and Benefits

This section describes hardware features and capabilities. Please refer to the relevant driver and/or firmware release notes for feature availability.

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<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>InfiniBand Architecture Specification v1.5 compliant</td><td>The DPU Controller delivers low latency, high bandwidth, and computing efficiency for high-performance computing (HPC), artificial intelligence (AI), and hyperscale cloud data centers applications.
The DPU Controller is InfiniBand Architecture Specification v1.5 compliant.
InfiniBand Network Protocols and Rates:
<table>
<tr><th rowspan="2">Protocol</th><th rowspan="2">Standard</th><th colspan="2">Rate (Gb/s)</th><th rowspan="2">Comments</th></tr>
<tr><th>4x Port (4 Lanes)</th><th>2x Ports (2 Lanes)</th></tr>
<tr><td>NDR/ NDR200</td><td>IBTA Vol2 1.5</td><td>425</td><td>212.5</td><td>PAM4 256b/ 257b encoding and RS-FEC</td></tr>
<tr><td>HDR/ HDR100</td><td>IBTA Vol2 1.4</td><td>212.5</td><td>106.25</td><td>PAM4 256b/ 257b encoding and RS-FEC</td></tr>
<tr><td>EDR</td><td>IBTA Vol2 1.3.1</td><td>103.125</td><td>51.5625</td><td>NRZ 64b/66b encoding</td></tr>
<tr><td>FDR</td><td>IBTA Vol2 1.2</td><td>56.25</td><td>N/A</td><td>NRZ 64b/66b encoding</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>Up to 200 Gigabit Ethernet</td><td>The DPU Controller complies with the following IEEE 802.3 standards:
200GbE / 100GbE / 50GbE / 40GbE / 25GbE / 10GbE
<table>
<tr><th>Protocol</th><th>MAC Rate</th></tr>
<tr><td>IEEE802.3ck</td><td>200/100 Gigabit Ethernet
(Include ETC enhancement)</td></tr>
<tr><td>IEEE802.3cd
IEEE802.3bs
IEEE802.3cm
IEEE802.3cn
IEEE802.3cu</td><td>200/100 Gigabit Ethernet
(Include ETC enhancement)</td></tr>
<tr><td>IEEE 802.3bj
IEEE 802.3bm</td><td>100 Gigabit Ethernet</td></tr>
<tr><td>IEEE 802.3by
Ethernet Technology Consortium</td><td>25/50 Gigabit Ethernet</td></tr>
<tr><td>IEEE 802.3ba</td><td>40 Gigabit Ethernet</td></tr>
<tr><td>IEEE 802.3ae</td><td>10 Gigabit Ethernet</td></tr>
<tr><td>IEEE 802.3cb</td><td>2.5/5 Gigabit Ethernet
(For 2.5: support only 2.5 x1000BASE-X)</td></tr>
<tr><td>IEEE 802.3ap</td><td>Based on auto-negotiation and KR startup</td></tr>
<tr><td>IEEE 802.3ad
IEEE 802.1AX</td><td>Link Aggregation</td></tr>
<tr><td>IEEE 802.1Q
IEEE 802.1P VLAN tags and priority</td><td></td></tr>
<tr><td>IEEE 802.1Qau (QCN) Congestion Notification
IEEE 802.1Qaz (ETS)
EEE 802.1Qbb (PFC)
IEEE 802.1Qbg
IEEE 1588v2
IEEE 802.1AE (MACSec)
Jumbo frame support (9.6KB)</td><td></td></tr>
</table></td></tr>
</table>

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Feature	Description

On-board Memory	• Quad SPI NOR FLASH - includes 256Mbit for Firmware image.
	• UVPS EEPROM - includes 2Mbit.
	• FRU EEPROM - Stores the parameters and personality of the card. The EEPROM capacity is 128Kbit. FRU I2C address is (0x50) and is accessible through the PCIe SMBus.
	• DPU_BMC Flashes:
	  • 2x 64MByte for BMC Image
	  • 512MByte for Config Data
	• eMMC pSLC 40GB with 30K Write Cycles eMMC for SoC BIOS and OS.
	• SSD (onboard BGA) 128GByte for user SoC OS, logs and application SW.
	• DDR5 SDRAM - 48GB @5200MT/s dual-channel DDR5 SDRAM memory. Solder down on-board 128bit + 16bit ECC.

BlueField-3 SoC	The DPU Controller integrates x16 Armv8.2+ A78 Hercules cores (64-bit) is interconnected by a coherent mesh network, one DRAM controller, an RDMA intelligent network adapter supporting up to 400Gb/s, an embedded PCIe switch with endpoint and root complex functionality, and up to 32 lanes of PCIe Gen 5.0.
RDMA and RDMA over Converged InfiniBand/Ethernet (RoCE)	The DPU Controller, utilizing IBTA RDMA (Remote Data Memory Access) and RoCE (RDMA over Converged InfiniBand/Ethernet) technology, delivers low-latency and high-performance over InfiniBand/Ethernet networks. Leveraging data center bridging (DCB) capabilities as well as advanced congestion control hardware mechanisms, RoCE provides efficient low-latency RDMA services over Layer 2 and Layer 3 networks.
Storage Acceleration	• A consolidated compute and storage network achieves significant cost-performance advantages over multi-fabric networks. Standard block and file access protocols can leverage RDMA for high-performance storage access: NVMe over Fabric offloads for the target machine • The DPU Controller may operate as a co-processor offloading specific storage tasks from the host, isolating part of the storage media from the host, or enabling abstraction of software-defined storage logic using the NVIDIA BlueField-3 Arm cores. On the storage initiator side, the DPU Controller can prove an efficient solution for hyper-converged systems to enable the host CPU to focus on compute while all the storage interface is handled through the Arm cores.
NVMe-oF and NVMe/TCP Accelerations	Non-volatile Memory Express (NVMe) over Fabrics or over TCP are protocols for communicating block storage IO requests over RDMA or TCP to transfer data between a host computer and a target solid-state storage device or system over a network. The DPU Controller may operate as a co-processor offloading specific storage tasks from the host using its powerful NVMe Offload accelerator.
SR-IOV	The DPU Controller SR-IOV technology provides dedicated adapter resources and guaranteed isolation and protection for virtual machines (VM) within the server.

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Feature	Description
GPU Direct	GPUDirect RDMA is a technology that provides a direct P2P (Peer-to-Peer) data path between the GPU Memory directly to/from the NVIDIA HCA devices. This provides a significant decrease in GPU-GPU communication latency and completely offloads the CPU, removing it from all GPU-GPU communications across the network. The DPU Controller uses high-speed DMA transfers to copy data between P2P devices resulting in more efficient system applications
Cryptography Accelerations	From IPsec and TLS data-in-motion inline encryption to AES-XTS block-level data-at-rest encryption and public key acceleration, the DPU Controller hardware-based accelerations offload the crypto operations and free up the CPU, reducing latency and enabling scalable crypto solutions. BlueField-3 “host-unaware” solutions may transmit and receive data, while BlueField-3 acts as a bump-in-the-wire for crypto.
Security Accelerators	A consolidated compute and network solution based on the DPU Controller achieves significant advantages over a centralized security server solution. Standard encryption protocols and security applications can leverage NVIDIA BlueField-3 compute capabilities and network offloads for security application solutions such as Layer4 Statefull Firewall.
Out-of-Band Management	The DPU Controller incorporates a 1GbE RJ45 out-of-band port that allows the network operator to establish trust boundaries in accessing the management function to apply it to network resources. It can also be used to ensure management connectivity (including the ability to determine the status of any network component) independent of the status of other in-band network components.
BMC	The DPU Controller incorporate local NIC BMC (Baseboard Management Controller) hardware on the board. The BMC SoC (system on a chip) can utilize either shared or dedicated NICs for remote access. The BMC node enables remote power cycling, board environment monitoring, BlueField-3 chip temperature monitoring, board power and consumption monitoring, and individual interface resets. The BMC also supports the ability to push a bootstream to BlueField-3. Having a trusted on-board BMC that is fully isolated for the host server ensures highest security for the DPU boards.

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2 BlueField-3 Administrator Quick Start Guide

This page is tailored for system administrators wishing to install BlueField and perform sample administrative actions on it. For a quick start guide aimed at software developers wishing to develop applications on the BlueField card using the DOCA framework, please refer to the *NVIDIA DOCA Developer Quick Start Guide*.

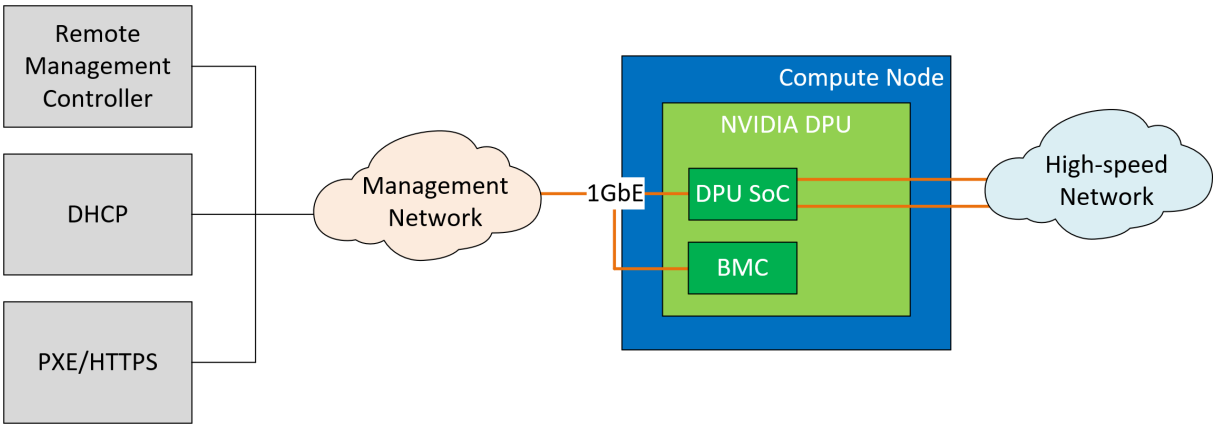
> Not sure which guide to follow? For more details on the different BlueField user types, please refer to the NVIDIA BlueField and DOCA User Types document.

2.1 Prerequisites for Initial BlueField-3 Deployment

- DPU BMC 1GbE interface connected to the management network via ToR
- Remote Management Controller (RMC) connected to DPU BMC 1GbE via ToR

  > RMC is the platform for data center infrastructure managers to manage DPUs.

- DHCP server existing in the management network
- An NVQual certified server



2.2 First-time Installation Procedure

Content:

- 2.3 Step 1 - DPU SoC Boots
- 2.4 Step 2 - DHCP Discover
- 2.5 Step 3 - Change Default Password
- 2.6 Step 4 - Upgrade DPU BMC Firmware
  - 2.6.1 Update BMC Firmware
  - 2.6.2 Update eROT Firmware
  - 2.6.3 Possible Error Codes During BMC/eROT Upgrade
- 2.7 Step 5 - Upgrade DPU Firmware Components and BSP
  - 2.7.1 Transferring BFB Image
    - 2.7.1.1 Redfish Interface

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- 2.7.1.2 Direct SCP
- 2.8 Step 6 – Verify Software Component Versions
- 2.9 Step 7 – Relate DPU to DPU BMC and NIC Data Ports on Same Machine
- 2.10 Step 8 – (Optional) Change Mode of Operation from DPU Mode to NIC Mode
- 2.11 Step 9 – (Optional) Change Mode of Operation to Zero-trust Mode
- 2.12 Step 10 – (Optional) Disable Secure Boot

The following illustrates the sequence of events and actions from first time power-up of the NVIDIA® BlueField® DPU in the data center environment through provisioning and maintenance.

> The numbers indicated in the sequence diagram map to the steps below the diagram.

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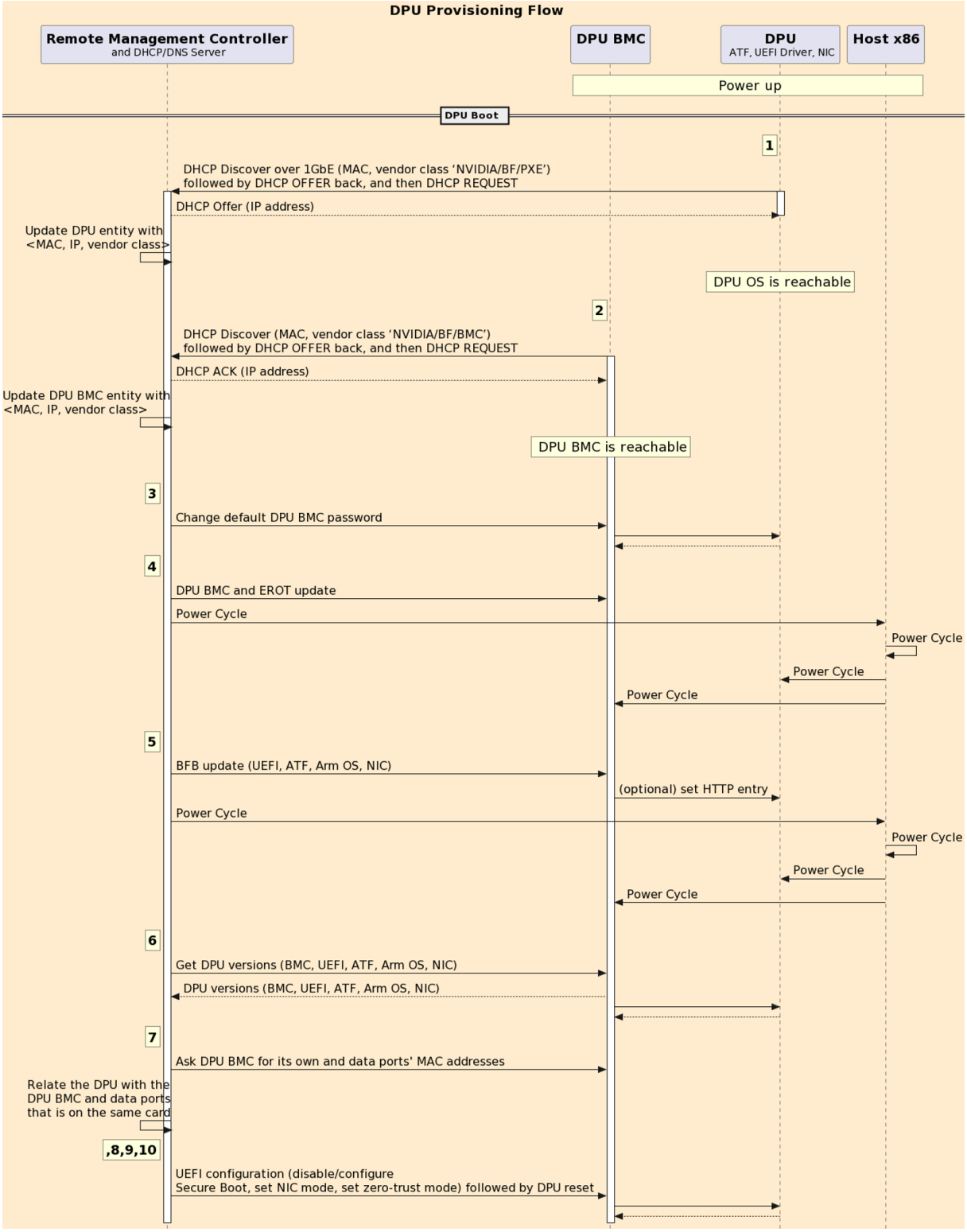

At the end of this procedure, the DPU should be configured with an IP address, all required settings, has up-to-date software component versions, and is ready to use.

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2.3 Step 1 – DPU SoC Boots

The DPU SoC boots to DPU UEFI BIOS and DHCP DISCOVER is sent

1. DPU SoC runs UEFI/PXE which sends a DHCP DISCOVER over the 1GbE OOB interface, including vendor class (`"NVIDIA/BF/PXE"`) for DPU SoC (to allow customer's server to differentiate between DPU SoC and DPU BMC), and MAC for identification and discovery (see Appendix A for more information).
2. A customer's DHCP server inspects the MAC address and the vendor class, allocates IP, and continues the standard DHCP.
3. DHCP server updates RMC of the new DPU discovered with detailed information (e.g., MAC, IP address, vendor class).

2.4 Step 2 – DHCP Discover

DPU BMC issues DHCP DISCOVER over the 1GbE OOB interface, including vendor class (`"NVIDIA/BF/BMC"`) for DPU-BMC, and MAC for identification and discovery. Example of DPU BMC DHCP DISCOVER packet structure (note `"NVIDIA/BF/BMC"` in line 13):

```
1   root@dpu-bmc:~# 18:18:10.563269 IP (tos 0xc0, ttl 64, id 0, offset 0, flags [none], proto UDP (17),
    length 320)
2   0.0.0.0.bootpc > 255.255.255.255.bootps: [udp sum ok] BOOTP/DHCP, Request from b8:3f:d2:ca:4b:26 (oui
    Unknown), length 292, xid 0xfc2acdec, secs 1, Flags [none] (0x0000)
3   Client-Ethernet-Address b8:3f:d2:ab:cd:ef (oui Unknown)
4   Vendor-rfc1048 Extensions
5   Magic Cookie 0x63825363
6   DHCP-Message (53), length 1: Discover
7   Client-ID (61), length 7: ether b8:3f:d2:ab:cd:ef
8   Parameter-Request (55), length 9:
9   Subnet-Mask (1), Default-Gateway (3), Domain-Name-Server (6), Hostname (12)
10  Domain-Name (15), Static-Route (33), NTP (42), Unknown (120)
11  Classless-Static-Route (121)
12  MSZ (57), length 2: 576
13  Hostname (12), length 7: "dpu-bmc" Vendor-Class (60), length 13: "NVIDIA/BF/BMC" END (255), length 0
14  18:18:10.565261 IP (tos 0x0, ttl 63, id 0, offset 0, flags [DF], proto UDP (17), length 353)
15  (example) dhcp01.XX.YY > ldev-platform-13-043-bmc.bootpc: [no cksum] BOOTP/DHCP, Reply, length 325,
    hops 1, xid 0xfc2acdec, secs 1, Flags [none] (0x0000)
16  (example) Your-IP ldev-platform-13-043-bmc.XX.YY
17  (example) Server-IP l-pxe02.XX.YY
18  Gateway-IP 10.237.0.255
19  Client-Ethernet-Address b8:3f:d2:ab:cd:ef (oui Unknown)
20  file "pxelinux.0" Vendor-rfc1048 Extensions
21  Magic Cookie 0x63825363
22  DHCP-Message (53), length 1: Offer
23  Server-ID (54), length 4: (example) dhcp01.XX.YY
24  Lease-Time (51), length 4: 43200
25  Subnet-Mask (1), length 4: 255.255.0.0
26  Default-Gateway (3), length 4
27  (example) GW.XX.YY
28  Hostname (12), length 24: "ldev-platform-13-043-bmc" Domain-Name (15), length 13: "<local domain name>"
     NTP (42), length 4: (example) NTP.XX.YY
29  END (255), length 0
30  18:18:10.565261 IP (tos 0x0, ttl 62, id 0, offset 0, flags [DF], proto UDP (17), length 353)
31  dhcp01.XX.YY > ldev-platform-13-043-bmc.<local domain name>: [no cksum] BOOTP/DH
```

1. DHCP server inspects the MAC address and the vendor class, allocates IP and continues the standard DHCP flow.
2. DHCP server updates RMC of the new DPU BMC discovered with detailed information: MAC, IP address, vendor classes, etc.

2.5 Step 3 – Change Default Password

To communicate with the DPU BMC, change the default password (`0penBmc`) by sending the following Redfish schema to the DPU BMC:

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```
curl -k -u root:OpenBmc -H "Content-Type: application/json" -X PATCH https://<DPU-BMC-IP>/redfish/v1/
AccountService/Accounts/root -d '{"Password" : "<user-password>"}'
```

Where `<DPU-BMC-IP>` is the IP address for the DPU BMC (e.g., 10.10.1.2), and `<user-password>` is the chosen password to log into the DPU BMC with root privileges.

The new password must comply with the following policy parameters:

- Minimum length: 13
- Maximum length: 20
- Minimum number of upper-case characters: 1
- Minimum number of lower-case characters: 1
- Minimum number of digits: 1
- Minimum number of special characters: 1

  > List of special characters:
  > - `$` (dollar sign)
  > - `%` (percent sign)
  > - `^` (caret/circumflex)
  > - `&` (ampersand)
  > - `*` (asterisk)
  > - `-` (minus)
  > - `+` (plus)
  > - `=` (equal)
  > - `|` (pipe)
  > - `~` (tilde)
  > - `_` (underscore)
  > - `,` (comma)
  > - `.` (period/full stop)
  > - `;` (semicolon)
  > - `:` (colon)
  > - `"` (quotation mark)
  > - `'` (apostrophe)
  > - `/` (forward slash)
  > - `\` (backslash)

- Maximum number of consecutive character pairs: 4

  > Two characters are consecutive if `|hex(char_1)-hex(char_2)|=1`.
  >
  > Examples of passwords with 5 consecutive character pairs (invalid): `DcB` `a123456AbCd!`; `ab1XbcYcdZdeGef!`; `Testing_123abcgh!`.

The following is a valid example password:

- `HelloNvidia3D!`

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> The root account locks after four consecutive failed attempts and automatically unlocks after 10 minutes.

For example:

```
[redfish_scripts] $ curl -k -u root:0penBmc -H "Content-Type: application/json" -X PATCH https://<DPU-BMC-IP>/
redfish/v1/AccountService/Accounts/root -d '{"Password" : "HelloNvidia3D!"}'
Response:
{
  "@Message.ExtendedInfo": [
    {
      "@odata.type": "#Message.v1_1_1.Message",
      "Message": "The request completed successfully.",
      "MessageArgs": [],
      "MessageId": "Base.1.15.0.Success",
      "MessageSeverity": "OK",
      "Resolution": "None"
    }
  ]
}
```

2.6 Step 4 – Upgrade DPU BMC Firmware

Upgrade DPU BMC firmware via the Redfish "update service schema" through the 1GbE OOB.

- If a BlueField-2 DPU is in your possession, follow the instructions in Appendix A
- If a BlueField-3 DPU is in your possession, follow the steps in the following subsections

> Make sure to download the latest DPU BMC image available from the BlueField Runtime and Driver Downloader.

2.6.1 Update BMC Firmware

1. Run the following Redfish command over the 1GbE out-of-band interface on the DPU BMC to trigger a secure DPU BMC firmware update:

   ```
   curl -k -u root:'<password>' -H "Content-Type: application/octet-stream" -X POST -T <package_path> https://
   <DPU-BMC-IP>/redfish/v1/UpdateService/update
   ```

   Where:

   - `<password>` - DPU BMC password
   - `<package_path>` - BMC firmware update package path pointing to BMC `*.fwpkg` binary (e.g., `bf3-bmc-23.09-6_opn.fwpkg`)
   - `<DPU-BMC-IP>` - BMC IP address

   After pushing the image to the DPU BMC, a new task is created. Example:

   ```
   {
     "@odata.id": "/redfish/v1/TaskService/Tasks/0",
     "@odata.type": "#Task.v1_4_3.Task",
     "Id": "0",
     "TaskState": "Running"
   }
   ```

   > BMC firmware update takes ~12 minutes.

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2. To track the progress of the update, use the task `Id` received in the response above (i.e., 0) in your query and monitor the value of the task's `PercentComplete` field:

```
curl -k -u root:'<password>' -X GET https://<DPU-BMC-IP>/redfish/v1/TaskService/Tasks/<task_id> | jq -r
' .PercentComplete'
```

Where:

- `<password>` - DPU BMC password
- `<DPU-BMC-IP>` - BMC IP address
- `<task_id>` - task ID of the update process as received in the response under the `Id` v alue

  Example output:

```
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current Dload  Upload
Total   Spent    Left  Speed
100  2123  100  2123    0     0  38600      0 --:--:-- --:--:-- --:--:-- 37910
20
```

  See `PercentComplete` is at 20 percent.

3. Proceed to the next step when the process reaches 100%.

2.6.2 Update eROT Firmware

1. Trigger a secure firmware update:

```
curl -k -u root:'<password>' -H "Content-Type: application/octet-stream" -X POST -T <package_path> https://
<DPU-BMC-IP>/redfish/v1/UpdateService/update
```

Where:

- `<password>` - DPU BMC password
- `<package_path>` - eROT firmware update package path pointing to eROT `*.fwpkg` binary (e.g. `cec1736-ecfw-00.02.0127.0000-n02-rel-prod.fwpkg`)
- `<DPU-BMC-IP>` - BMC IP address

  After initiating the eROT secure update, a new task is created. Example:

```
{
  "@odata.id": "/redfish/v1/TaskService/Tasks/0",
  "@odata.type": "#Task.v1_4_3.Task",
  "Id": "0",
  "TaskState": "Running"
}
```

> eROT firmware update takes ~20 seconds.

2. To track the progress of the update, use the task `Id` received in the response above (i.e., 0) in your query and monitor the value of the task's `PercentComplete` field:

```
curl -k -u root:'<password>' -X GET https://<DPU-BMC-IP>/redfish/v1/TaskService/Tasks/<task_id> | jq -r
' .PercentComplete'
```


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> Run this command several times until `PercentComplete` shows 100 before proceeding to other operations.

Where:

- `<password>` - DPU BMC password
- `<DPU-BMC-IP>` - BMC IP address
- `<task_id>` - task ID of the update process as received in the response under the `Id` value

> For the firmware of the BMC and CEC to apply and to allow new Redfish APIs which are required for the following steps, a power cycle of the DPU is required. The BlueField-3 DPU is installed in the host's PCIe slot. To initiate the power cycle sequence for the DPU, the entire server on which it is installed must be power cycled.

2.6.3 Possible Error Codes During BMC/eROT Upgrade

Fault	Diagnosis and Possible Solution
Connection to BMC breaks during firmware package transfer	• Redfish task URI is not returned by the Redfish server • The Redfish server (if operational) is in idle state • After a reboot of BMC, or restart/recovery of the Redfish server, the Redfish server is in idle state A new firmware update can be attempted by the Redfish client.

Connection to BMC breaks during firmware update	• Redfish task URI previously returned by the Redfish server is no longer accessible
	• The Redfish server (if operational) is in one of the following states:
	  • In idle state, if the firmware update has completed
	  • In update state, if the firmware update is still ongoing
	• After a BMC reboot, or the restart/recovery of the Redfish server, the Redfish server is in idle state
	A new firmware update can be attempted by the Redfish client.

Two firmware update requests are initiated	The Redfish server blocks the second firmware update request and returns the following: • HTTP code 400 "Bad Request" • Redfish message based on standard registry entry UpdateInProgress Check the status of the ongoing firmware update by looking at the TaskCollection resource.
Redfish task hangs	• Redfish task URI that previously returned by the Redfish server is no longer accessible • PLDM-based firmware update progresses • After a reboot of BMC, or restart/recovery of the Redfish server, the Redfish server us in idle state A new firmware update can be attempted by the Redfish client.

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Fault	Diagnosis and Possible Solution
BMC-EROT communication failure during image transfer	The Redfish task monitoring the firmware update indicates a failure: • TaskState is set to Exception • TaskStatus is set to Warning • Messages array in the task includes an entry based on the standard registry Update.1.0.0.TransferFailed indicating the components that failed during image transfer The Redfish client may retry the firmware update.
Firmware update fails	The Redfish task monitoring the firmware update indicates a failure: • TaskState is set to Exception • TaskStatus is set to Warning • Messages array in the task includes an entry describing the error The Redfish client may retry the firmware update.
ERoT failure (not responding)	The Redfish task monitoring the firmware update indicates a failure: • TaskState is set to Canceled • TaskStatus is set to Warning • Messages array in the task includes an entry describing the error • The Redfish client reports the error The Redfish client may retry the firmware update.
Firmware image validation failure	The Redfish task monitoring the firmware update indicates a failure: • TaskState is set to Exception • TaskStatus is set to Warning • Messages array in the task includes an entry based on the standard registry Update.1.0.0.VerificationFailed to indicate the component for which verification failed • The Redfish client reports the error The Redfish client might retry the firmware update.
Power loss before activation command is sent	• The Redfish server is in idle state A new firmware update can be attempted by the Redfish client.
Firmware activation failure	The Redfish task monitoring the firmware update indicates a failure: • TaskState is set to Exception • TaskStatus is set to Warning • Messages array in the task includes an entry based on the standard registry Update.1.0.ActivateFailed The Redfish client may retry the firmware update.
Push to BMC firmware package greater than 200 MB	• No Redfish task is created • Messages array in the task includes an entry based on the standard registry Base.1.8.1.ResourceExhaustion and a request to retry the operation is given

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2.7 Step 5 – Upgrade DPU Firmware Components and BSP

Upgrade the DPU firmware components (i.e., ATF, UEFI, NIC-firmware) and the BSP using the BFB image.

> ⓘ Make sure to download the latest DOCA image (BFB file) available from the BlueField Runtime and Driver Downloader.

The BFB installation procedure consists of the following main stages:

1. Enabling RShim on the BMC. See section "Enable RShim on DPU BMC" for instructions.
2. Initiating the BFB update procedure by transferring the BFB image using one of the following options:
    - Direct SCP
        i. Running an SCP command.
    - Redfish interface
        i. Confirming the identity of the host and BMC—required only during first-time setup or after BMC factory reset.
        ii. Sending a Simple-Update request.

2.7.1 Transferring BFB Image

Since the BFB is too large to store on the BMC flash or tmpfs, the image must be written to the RShim device. This can be done by either running SCP directly or using the Redfish interface.

2.7.1.1 Redfish Interface

The following is a simple sequence diagram illustrating the flow of the BFB installation process.

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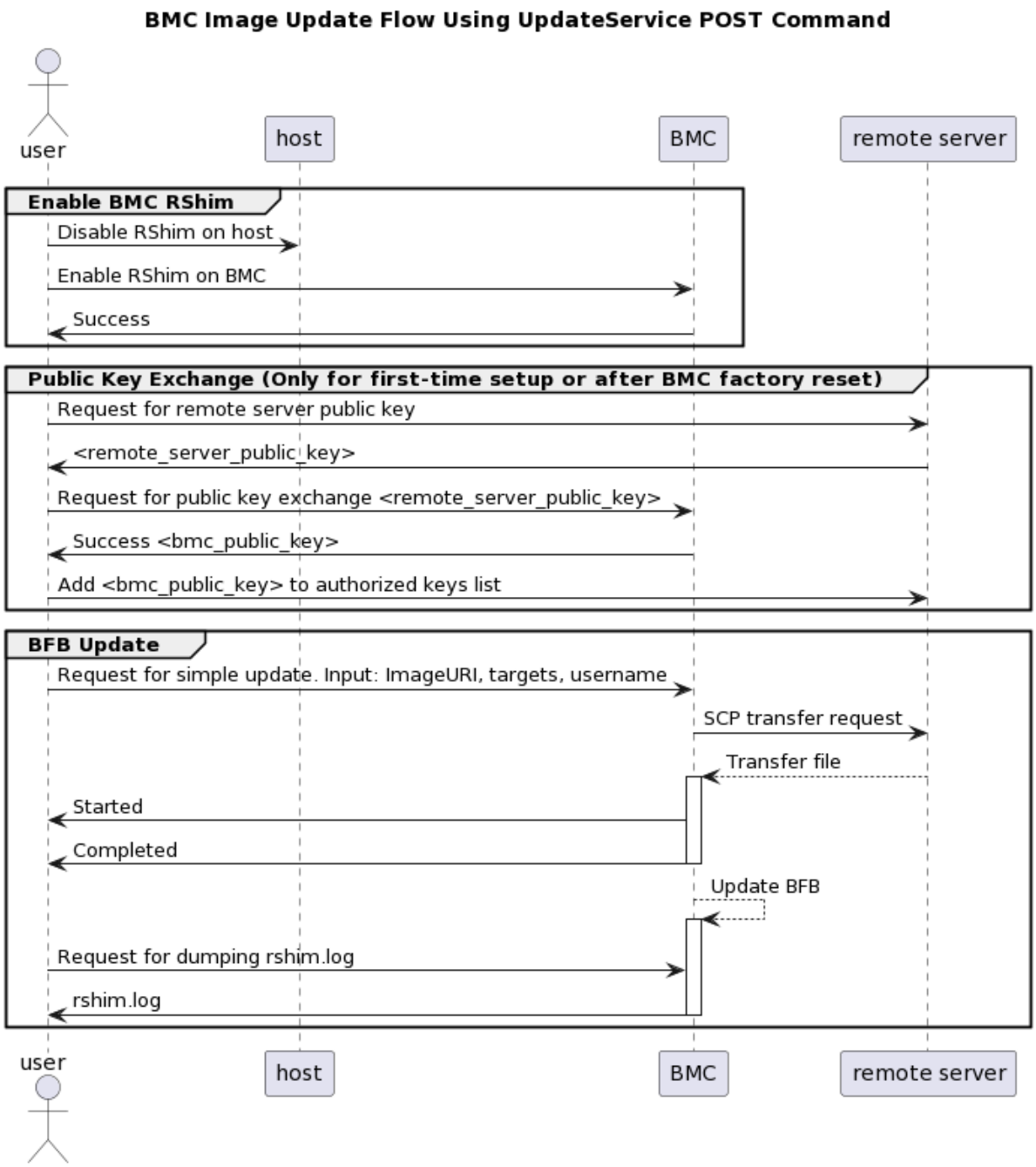

The following are detailed instructions outlining each step in the diagram:

1. Confirm the identity of the remote server (i.e., host holding the BFB image) and BMC.

   > ⓘ Required only during first-time setup or after BMC factory reset.

   a. Run the following on the remote server:

   ```
   ssh-keyscan -t <key_type> <remote_server_ip>
   ```

   Where:

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- `key_type` - the type of key associated with the server storing the BFB file (e.g., ed25519)
- `remote_server_ip` - the IP address of the server hosting the BFB file

b. Retrieve the public key of the host holding the BFB image from the response and provide the remote server's credentials to the DPU using the following command:

```
curl -k -u root:'<password>' -H "Content-Type: application/json" -X POST -d
'{"RemoteServerIP":"<remote_server_ip>", "RemoteServerKeyString":"<remote_server_public_key>"}'
https://<bmc_ip>/redfish/v1/UpdateService/Actions/Oem/NvidiaUpdateService.PublicKeyExchange
```

Where:

- `remote_server_ip` - the IP address of the server hosting the BFB file
- `remote_server_public_key` - remote server's public key from the `ssh-keyscan` response, which contains both the type and the public key with a space between the two fields (i.e., "`<type> <public_key>`").
- `bmc_ip` - BMC IP address

c. Extract the BMC public key information (i.e., "`<type> <bmc_public_key> <username>@<hostname>`") from the `PublicKeyExchange` response and append it to the `authorized_keys` file on the host holding the BFB image. This enables passwordless key-based authentication for users.

```
{
  "@Message.ExtendedInfo": [
    {
      "@odata.type": "#Message.v1_1_1.Message",
      "Message": "Please add the following public
       key info to ~/.ssh/authorized_keys on the
       remote server",
      "MessageArgs": [
        "<type> <bmc_public_key> root@dpu-bmc"
      ]
    },
    {
      "@odata.type": "#Message.v1_1_1.Message",
      "Message": "The request completed
       successfully.",
      "MessageArgs": [],
      "MessageId": "Base.1.15.0.Success",
      "MessageSeverity": "OK",
      "Resolution": "None"
        }
    ]
   }
```

d. If the remote server public key must be revoked, use the following command before repeating the previous step:

```
curl -k -u root:'<password>' -H "Content-Type: application/json" -X POST -d
'{"RemoteServerIP":"<remote_server_ip>"}' https://<bmc_ip>/redfish/v1/UpdateService/Actions/Oem/
NvidiaUpdateService.RevokeAllRemoteServerPublicKeys
```

Where:

- `remote_server_ip` - remote server's IP address
- `bmc_ip` - BMC IP address

2. Start BFB image transfer using the following command on the remote server:

```
curl -k -u root:'<password>' -H "Content-Type: application/json" -X POST -d '{"TransferProtocol":"SCP",
"ImageURI":"<image_uri>","Targets":["redfish/v1/UpdateService/FirmwareInventory/DPU_OS"],
"Username":"<username>"}' https://<bmc_ip>/redfish/v1/UpdateService/Actions/UpdateService.SimpleUpdate
```


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> After the BMC boots, it may take a few seconds (6-8 in NVIDIA® BlueField®-2, and 2 in BlueField-3) until the DPU BSP (`DPU_OS`) is up.

> This command uses SCP for the image transfer, initiates a soft reset on the BlueField and then pushes the boot stream. For Ubuntu BFBs, the eMMC is flashed automatically once the bootstream is pushed. On success, a "running" message is received with the current task ID.

Where:

- `image_uri` - the image URI format should be `<remote_server_ip>/<path_to_bfb>`

  > `image_uri` path is in reference to the user. For instance, if the BFB image is in `/root/image.bfb` , the user must use `image_uri=<ip>/image.bfb` (not `image_uri=<ip>/root/image.bfb`).

- `username` - username on the remote server
- `bmc_ip` - BMC IP address

  Examples:

  - If RShim is disabled:

```
{
  "error": {
    "@Message.ExtendedInfo": [
      {
        "@odata.type": "#Message.v1_1_1.Message",
        "Message": "The requested resource of type Target named '/dev/rshim0/boot' was not
found.",
        "MessageArgs": [
          "Target",
          "/dev/rshim0/boot"
        ],
        "MessageId": "Base.1.15.0.ResourceNotFound",
        "MessageSeverity": "Critical",
        "Resolution": "Provide a valid resource identifier and resubmit the request."
      }
    ],
    "code": "Base.1.15.0.ResourceNotFound",
    "message": "The requested resource of type Target named '/dev/rshim0/boot' was not
found."
}
```

  - If a username or any other required field is missing:

```
{
  "Username@Message.ExtendedInfo": [
    {
      "@odata.type": "#Message.v1_1_1.Message",
      "Message": "The create operation failed because the required property Username was
missing from the request.",
      "MessageArgs": [
        "Username"
      ],
      "MessageId": "Base.1.15.0.CreateFailedMissingReqProperties",
      "MessageSeverity": "Critical",
      "Resolution": "Correct the body to include the required property with a valid value
and resubmit the request if the operation failed."
    }
  ]
}
```

  - If the request is valid and a task is created:

```
{
  "@odata.id":
   "/redfish/v1/TaskService/Tasks/<task_id>",
  "@odata.type": "#Task.v1_4_3.Task",
```


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```
  "Id": "<task_id>",
  "TaskState": "Running",
  "TaskStatus": "OK"
}
```

3. Wait 2 seconds and run the following on the host to track image transfer progress:

```
curl -k -u root:'<password>' -X GET https://<bmc_ip>/redfish/v1/TaskService/Tasks/<task_id>
```

> The transfer takes ~8 minutes for BlueField-3, and ~40 minutes for BlueField-2. During the transfer, the `PercentComplete` value remains at 0. If no errors occur, the `TaskState` is set to `Running`, and a keep-alive message is generated every 5 minutes with the content "Transfer is still in progress (X minutes elapsed). Please wait". Once the transfer is completed, the `PercentComplete` is set to 100, and the `TaskState` is updated to `Completed`.
>
> Upon failure, a message is generated with the relevant resolution.

Where:

a. `bmc_ip` - BMC IP address

b. `task_id` - task ID

Troubleshooting:

- If host identity is not confirmed or the provided host key is wrong:

```
{
      "@odata.type": "#MessageRegistry.v1_4_1.MessageRegistry",
      "Message": "Transfer of image '<file_name>' to '/dev/rshim0/boot' failed.",
      "MessageArgs": [
        "<file_name>,
        "/dev/rshim0/boot"
      ],
      "MessageId": "Update.1.0.TransferFailed",
      "Resolution": " Unknown Host: Please provide server's public key using
PublicKeyExchange ",
      "Severity": "Critical"
    }
…
"PercentComplete": 0,
  "StartTime": "<start_time>",
  "TaskMonitor": "/redfish/v1/TaskService/Tasks/<task_id>/Monitor",
  "TaskState": "Exception",
  "TaskStatus": "Critical"
```

> In this case, revoke the remote server key (step 1.d.), and repeat steps 1.a. to 1.c.

- If the BMC identity is not confirmed:

```
{
      "@odata.type": "#MessageRegistry.v1_4_1.MessageRegistry",
      "Message": "Transfer of image '<file_name>' to '/dev/rshim0/boot' failed.",
      "MessageArgs": [
        "<file_name>",
        "/dev/rshim0/boot"
      ],
      "MessageId": "Update.1.0.TransferFailed",
      "Resolution": "Unauthorized Client: Please use the PublicKeyExchange action to
receive the system's public key and add it as an authorized key on the remote server",
      "Severity": "Critical"
      }
…
"PercentComplete": 0,
  "StartTime": "<start_time>",
  "TaskMonitor": "/redfish/v1/TaskService/Tasks/<task_id>/Monitor",
  "TaskState": "Exception",
  "TaskStatus": "Critical"
```


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> In this case, verify that the BMC key has been added correctly to the `authorized_key` file on the remote server.

- If SCP fails:

```
{
      "@odata.type": "#MessageRegistry.v1_4_1.MessageRegistry",
      "Message": "Transfer of image '<file_name>' to '/dev/rshim0/boot' failed.",
      "MessageArgs": [
        "<file_name>",
        "/dev/rshim0/boot"
      ],
      "MessageId": "Update.1.0.TransferFailed",
      "Resolution": "Failed to launch SCP",
      "Severity": "Critical"
      }
…
"PercentComplete": 0,
  "StartTime": "<start_time>",
  "TaskMonitor": "/redfish/v1/TaskService/Tasks/<task_id>/Monitor",
  "TaskState": "Exception",
  "TaskStatus": "Critical"
```

- The keep-alive message:

```
{
      "@odata.type": "#MessageRegistry.v1_4_1.MessageRegistry",
      "Message": " <file_name>' is being transferred to '/dev/rshim0/boot'.",
      "MessageArgs": [
        " <file_name>",
        "/dev/rshim0/boot"
      ],
      "MessageId": "Update.1.0.TransferringToComponent",
      "Resolution": "Transfer is still in progress (5 minutes elapsed): Please wait",
      "Severity": "OK"
    }
…
"PercentComplete": 0,
  "StartTime": "<start_time>",
  "TaskMonitor": "/redfish/v1/TaskService/Tasks/<task_id>/Monitor",
  "TaskState": "Running",
  "TaskStatus": "OK"
```

- Upon completion of transfer of the BFB image to the DPU, the following is received:

```
{
      "@odata.type": "#MessageRegistry.v1_4_1.MessageRegistry",
      "Message": "Device 'DPU' successfully updated with image '<file_name>'.",
      "MessageArgs": [
        "DPU",
        "<file_name>"
      ],
      "MessageId": "Update.1.0.UpdateSuccessful",
      "Resolution": "None",
      "Severity": "OK"
    },
…
"PercentComplete": 100,
  "StartTime": "<start_time>",
  "TaskMonitor": "/redfish/v1/TaskService/Tasks/<task_id>/Monitor",
  "TaskState": "Completed",
  "TaskStatus": "OK"
```

4. Apply the new BFB image:
   BlueField must be restarted to apply the new firmware. To restart BlueField:
   a. Perform a graceful shutdown of the BlueField Arm OS.
   b. Power cycle the server to complete the restart.

   Alternatively, a server reboot may be done instead of power cycle by following these steps:
   a. Graceful shutdown the BlueField Arm OS.

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> ⓘ Without graceful shutdown of BlueField Arm OS during server reboot, the BlueField Arm side does not undergo a restart process (so only NIC firmware is applied).

b. Wait until completed.
c. Reboot the server (ATF, UEFI, BlueField Arm OS, NIC firmware is applied).

> ⓘ Server reboot will not restart the BlueField BMC (CEC not applied).

d. Log into BlueField BMC via Redfish and issue a restart (BlueField BMC and CEC is applied).

5. Verify that the new BFB is running by checking its version:

```
curl -k -u root:'<password>' -H "Content-Type: application/json" -X GET https://<bmc_ip>/redfish/v1/
UpdateService/FirmwareInventory/DPU_OS
```

2.7.1.2 Direct SCP

```
scp <path_to_bfb> root@<bmc_ip>:/dev/rshim0/boot
```

2.8 Step 6 – Verify Software Component Versions

Verify BlueField BSP, BlueField BMC and BlueField NIC firmware versions are up to date according to the NVIDIA BlueField BMC Software User Manual and NVIDIA BlueField DPU BSP Release Notes.

1. Use the Redfish `FirmwareInventory` schema over the 1GbE OOB interface to the DPU's BMC:

```
[redfish_scripts] $ curl -k -u root:<password> -H "Content-Type: application/octet-stream" -X GET https://
<DPU-BMC-IP>/redfish/v1/UpdateService/FirmwareInventory
{
  "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory",
  "@odata.type": "#SoftwareInventoryCollection.SoftwareInventoryCollection",
  "Members": [
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/9f7ec75a_BMC_Firmware"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/Bluefield_FW_ERoT"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_ATF"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_BOARD"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_BSP"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_NIC"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_NODE"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_OFED"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_OS"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_SYS_IMAGE"
    },
    {
      "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_UEFI"
    }
  ],
  "Members@odata.count": 11,
```


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```
  "Name": "Software Inventory Collection"
}
```

Response example for `DPU_ATF`:

```
> curl -k -u root:<password> -H "Content-Type: application/octet-stream" -X GET https://<DPU-BMC-IP>/
redfish/v1/UpdateService/FirmwareInventory/DPU_ATF
{
  "@odata.id": "/redfish/v1/UpdateService/FirmwareInventory/DPU_ATF",
  "@odata.type": "#SoftwareInventory.v1_4_0.SoftwareInventory",
  "Description": "Host image",
  "Id": "DPU_ATF",
  "Members@odata.count": 1,
  "Name": " "Software Inventory",
  "RelatedItem": [
    {
      "@odata.id": "/redfish/v1/Systems/Bluefield/Bios"
    }
  ],
  "SoftwareId": "",
  "Status": {
    "Health": "OK",
    "HealthRollup": "OK",
    "State": "OK",
  },
  "Updateable": true,
  "Version": "v2.2(release):4.0.2-33-gd9f4ad5"
```

> This request may also be used to query some of the other previously mentioned components (e.g., `9f7ec75a_BMC_Firmware`, `Bluefield_FW_ERoT`).

2. If the versions are not as expected, upgrade as needed:
   a. Download the latest DOCA (BFB file) versions from the downloader at the bottom of the DOCA product page.
   b. DOCA (BFB) upgrade options (upgrading UEFI, ATF, Arm OS, NIC firmware components):
      - Recommended—BFB upgrade from remote management controller using Redfish `UpdateService` schema over 1GbE to DPU BMC:

```
export token=`curl -k -H "Content-Type: application/json" -X POST https://<bmc_ip>/login -d
'{"username":"root", "password":"<password>"}' | grep token | awk '{print $2;}' | tr -d
'"'`
```

For more information on deploying BlueField software from the BMC, refer to the "Deploying BlueField Software Using BFB from BMC" page of the NVIDIA BlueField DPU BSP document.

2.9 Step 7 – Relate DPU to DPU BMC and NIC Data Ports on Same Machine

1. Get the DPU's BMC MAC address using the following Redfish command over the 1GbE OOB port to the DPU BMC:

```
curl -k -u root:<password> -H 'Content-Type: application/json' -X GET https://<DPU-BMC-IP>/redfish/v1/
Managers/Bluefield_BMC/EthernetInterfaces/eth0
 {
   "@odata.id": "/redfish/v1/Managers/Bluefield_BMC/EthernetInterfaces/eth0",
   "@odata.type": "#EthernetInterface.v1_6_0.EthernetInterface",
   "DHCPv4": {
     "DHCPEnabled": true,
     "UseDNSServers": true,
     "UseDomainName": true,
     "UseNTPServers": true
   },
   "DHCPv6": {
     "OperatingMode": "Stateful",
     "UseDNSServers": true,
     "UseDomainName": true,
     "UseNTPServers": true
```


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```
    },
    "Description": "Management Network Interface",
    "FQDN": "dpu-bmc",
    "HostName": "dpu-bmc",
    "IPv4Addresses": [
      {
        "Address": "10.237.40.179",
        "AddressOrigin": "DHCP",
        "Gateway": "0.0.0.0",
        "SubnetMask": "255.255.0.0"
      }
    ],
    "IPv4StaticAddresses": [],
    "IPv6AddressPolicyTable": [],
    "IPv6Addresses": [
      {
        "Address": "fdfd:fdfd:10:237:966d:aeff:fe17:9f5f",
        "AddressOrigin": "DHCPv6",
        "AddressState": null,
        "PrefixLength": 64
      },
      {
        "Address": "fe80::966d:aeff:fe17:9f5f",
        "AddressOrigin": "LinkLocal",
        "AddressState": null,
        "PrefixLength": 64
      }
    ],
    "IPv6DefaultGateway": "fe80::445b:ed80:5f97:8900",
    "IPv6StaticAddresses": [],
    "Id": "eth0",
    "InterfaceEnabled": true,
    "LinkStatus": "LinkUp",
    "MACAddress": "94:6d:ae:17:9f:5f",
    "MTUSize": 1500,
    "Name": "Manager Ethernet Interface",
    "NameServers": [
      "fdfd:fdfd:7:77:250:56ff:fe8b:e4f9"
    ],
    "SpeedMbps": 0,
    "StaticNameServers": [],
    "Status": {
      "Health": "OK",
      "HealthRollup": "OK",
      "State": "Enabled"
    },
    "VLANs": {
      "@odata.id": "/redfish/v1/Managers/Bluefield_BMC/EthernetInterfaces/eth0/VLANs"
    }
  }
```


2. Get the DPU's high-speed port's MAC addresses using the following Redfish command over the 1GbE OOB port to the DPU BMC:

```
curl -k -u root:<password> -H "Content-Type: application/octet-stream" -X GET https://<bmc_ip>/redfish/v1/
Chassis/Card1/NetworkAdapters/NvidiaNetworkAdapter/NetworkDeviceFunctions/eth0f0
{
  "@odata.id": "/redfish/v1/Chassis/Card1/NetworkAdapters/NvidiaNetworkAdapter/NetworkDeviceFunctions/
eth0f0",
  "@odata.type": "#NetworkDeviceFunction.v1_9_0.NetworkDeviceFunction",
  "Ethernet": {
    "MACAddress": "02:b1:b6:12:39:05",
    "MTUSize": 1500
  },
  "Id": "eth0f0",
  "Links": {
    "OffloadSystem": {
      "@odata.id": "/redfish/v1/Systems/Bluefield"
    },
    "PhysicalPortAssignment": {
      "@odata.id": "/redfish/v1/Chassis/Card1/NetworkAdapters/NvidiaNetworkAdapter/Ports/eth0"
    }
  },
  "Name": "NetworkDeviceFunction",
  "NetDevFuncCapabilities": [
    "Ethernet"
  ],
  "NetDevFuncType": "Ethernet"
}
```

2.10 Step 8 – (Optional) Change Mode of Operation from DPU Mode to NIC Mode

To change from DPU mode to NIC mode (or vice versa):

1. To enable NIC mode:

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```
curl -k -u root:<password> -H 'content-type: application/json' -d '{ "Attributes": { "NicMode":
"NicMode" } }' -X PATCH https://<DPU-BMC-IP>/redfish/v1/Systems/Bluefield/Bios/Settings
```

2. To disable NIC mode:

```
curl -k -u root:<password> -H 'content-type: application/json' -d '{ "Attributes": { "NicMode":
"DpuMode" } }' -X PATCH https://<DPU-BMC-IP>/redfish/v1/Systems/Bluefield/Bios/Settings
```

3. To check that the BMC recorded the change for the next UEFI reboot to apply it:

```
curl -k -u root:<password> -H 'content-type: application/json' -X GET https://<DPU-BMC-IP>/redfish/v1/
Systems/Bluefield/Bios/Settings
```

> ⚠ Reset the DPU (Arm and NIC) for the mode change to take effect.

4. To verify that the NIC mode has updated accordingly:

```
curl -k -u root:<password> -H 'content-type: application/json' -X GET https://<DPU-BMC-IP>/redfish/v1/
Systems/Bluefield/Bios/
```

2.11 Step 9 – (Optional) Change Mode of Operation to Zero-trust Mode

1. Use Redfish BIOS settings schema over the 1GbE OOB to the DPU BMC:

```
curl -k -X PATCH -d '{"Attributes":{"Internal CPU Model": "Restricted"}}' -u root:<password> https://<DPU-
BMC-IP>/redfish/v1/Systems/<SystemID>/Bios/Settings | python3 -m json.tool
```

   The available BlueField host privilege levels are `Restricted` and `Privileged`. The default is `Privileged`, where the host has access to DPU.

2. Change the privilege level to `Restricted`.

> ⚠ Changing host privilege level requires DPU reset for the change to take effect.

> ⓘ For more information on BlueField Operational modes, refer to this page.

2.12 Step 10 – (Optional) Disable Secure Boot

As part of the default settings of the DPU, UEFI Secure Boot is enabled and requires no special configuration to use it with the bundled Ubuntu OS shipped with the BlueField DPU. Disabling UEFI Secure Boot may be necessary when running an unsigned Arm OS image, such as a customer OS. Using Redfish Secure Boot schema over 1GbE to DPU BMC, run:

```
curl -k -u root:<password> -H "Content-Type: application/octet-stream" -X GET https://<DPU-BMC-IP>/redfish/v1/
Systems/Bluefield/SecureBoot
{
  "@odata.id": "/redfish/v1/Systems/Bluefield/SecureBoot",
  "@odata.type": "#SecureBoot.v1_1_0.SecureBoot",
  "Description": "The UEFI Secure Boot associated with this system.",
  "Id": "SecureBoot",
  "Name": "UEFI Secure Boot",
  "SecureBootCurrentBoot": "Enabled",
```


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```
  "SecureBootEnable": true,
  "SecureBootMode": "SetupMode"
}
curl -k -u root:<password> -X PATCH https://<DPU-BMC-IP>/redfish/v1/Systems/Bluefield/SecureBoot -H 'Content-Type:
application/json' -d '{"SecureBootCurrentBoot": "Enabled", "SecureBootEnable": true, "SecureBootMode":
"SetupMode"}'
```

For more information on user management, review this page.

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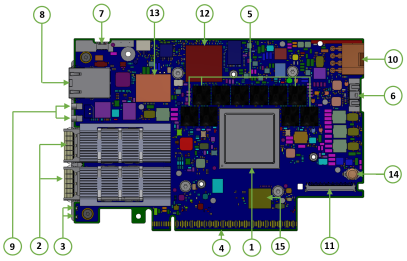
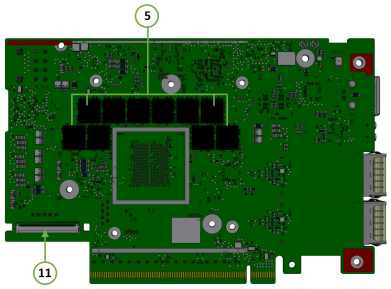
3 Supported Interfaces

This section describes the DPU Controller supported interfaces. Each numbered interface referenced in the figures is described in the following table with a link to detailed information.

> The below figures are for illustration purposes only and might not reflect the current revision of the DPU Controller.

3.1 FHHL DPU Controller Layout and Interface Information

OPN	*DPU Controller Component Side*	*DPU Controller Print Side*
900-9D3C6-00CV-GA0 **900-9D3C6-00CV-DA0**		

Item	Interface	Description
1	System-on-Chip (SoC)	16 Arm-Cores SoC
2	Networking Interface	The network traffic is transmitted through the DPU Controller QSFP112 connectors. The QSFP112 connectors allow the use of modules and optical and passive cable interconnect solutions
3	Networking Ports LEDs Interface	One bi-color I/O LEDs **per port** to indicate link and physical status
4	PCI Express Interface	PCIe Gen 5.0 through an x16 edge connector
5	DDR5 SDRAM On-Board Memory	20 units of DDR5 SDRAM for a total of 48GB @ 5200MT/s. 128bit + 16bit ECC, solder-down memory
6	NC-SI Management Interface	NC-SI 20 pins BMC connectivity for remote management
7	USB 4-pin RA Connector	Used for OS image loading
8	1GbE OOB Management Interface	1GbE BASE-T OOB management interface

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Item	Interface	Description
9	MMCX RA PPS IN/OUT	Allows PPS IN/OUT
10	External PCIe Power Supply Connector	An external 12V power connection through an 8-pin ATX connector
11	Cabline CA-II Plus Connectors	Two Cabline CA-II plus connectors are populated to allow connectivity to an additional PCIe x16 Auxiliary card
12	Integrated BMC	DPU BMC
13	SSD Interface	128GB
14	RTC Battery	Battery holder for RTC
15	eMMC	x8 NAND flash

3.2 Interfaces Detailed Description

3.2.1 System-on-Chip (SoC)

NVIDIA BlueField-3 DPU Controller is a family of advanced DPU Controller IC solutions that integrate a coherent mesh of 64-bit Armv8.2+ A78 Hercules cores, an NVIDIA® ConnectX®-7 network adapter front-end, and a PCI Express switch into a single chip. The powerful DPU Controller IC architecture includes an Armv multicore processor array, enabling customers to develop sophisticated applications and highly differentiated feature sets. Leverages the rich Arm software ecosystem and introduces the ability to offload the x86 software stack.

At the heart of BlueField-3, the ConnectX-7 network offload controller with RDMA and RDMA over Converged Ethernet (RoCE) technology delivers cutting-edge performance for networking and storage applications such as NVMe over Fabrics. Advanced features include an embedded virtual switch with programmable access lists (ACLs), transport offloads, and stateless encaps/decaps of NVGRE, VXLAN, and MPLS overlay protocols.

3.2.1.1 Encryption

DPU Controller addresses the concerns of modern data centers by combining hardware encryption accelerators with embedded software and fully integrated advanced network capabilities, making it an ideal platform for developing proprietary security applications. It enables a distributed security architecture by isolating and protecting each workload and providing flexible control and visibility at the server and workload level; controlling risk at the server access layer builds security into the DNA of the data center and enables prevention, detection, and response to potential threats in real-time. DPU Controller can deliver powerful functionality, including encryption of data-in-motion, bare-metal provisioning, stateful L4 firewall, and more.

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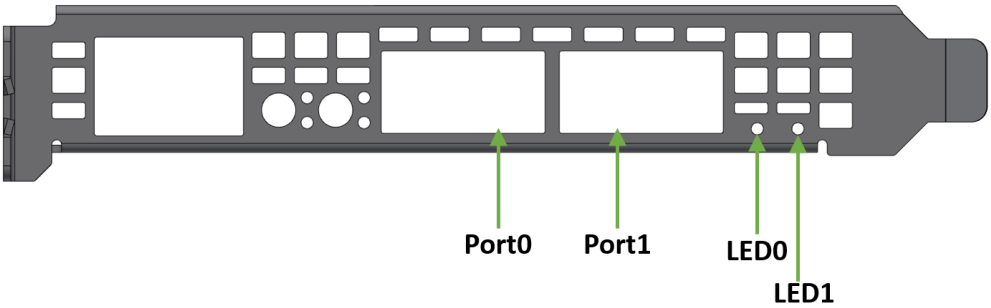
3.2.2 Networking Interface

> ⚠ The DPU Controller includes special circuits to protect the card/server from ESD shocks when plugging copper cables.

The network ports are compliant with the InfiniBand Architecture Specification, Release 1.5. InfiniBand traffic is transmitted through the cards' QSFP112 connectors.

3.2.3 Networking Ports LEDs Interface



One bicolor (Yellow and Green) I/O LED per port indicates speed and link status.

Link Indications

State	Bi-Color LED (Yellow/Green)	
Beacon command for locating the adapter card	1Hz blinking Yellow	
Error	4Hz blinking Yellow Indicates an error with the link. The error can be one of the following:	

Error Type	Description	LED Behavior
I^2C	I^2C access to the networking ports fails	Blinks until error is fixed
Over-current	Over-current condition of the networking ports	Blinks until error is fixed

Physical Activity	Blinking Green	
Link Up	Solid Green	
Physical Up (InfiniBand Mode Only)	Solid Yellow	

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3.2.4 PCI Express Interface

The DPU Controller supports PCI Express Gen 5.0/4.0 through x16 edge connectors. Some cards allow connectivity to an additional PCIe x16 Auxiliary card through the Cabline CA-II Plus connectors.

The following lists PCIe interface features:

- PCIe Gen 5.0, 4.0, 3.0, 2.0 and 1.1 compatible
- 2.5, 5.0, or 8.0, 16.0 or 32.0 GT/s link rate x16 lanes
- Auto-negotiates to x16, x8, x4, x2, or x1

3.2.5 DDR5 SDRAM On-Board Memory

The DPU Controllers incorporate 20 units of DDR5 SDRAM for a total of 48GB @ 5200MT/s single or dual channels. 64/128bit + 8bit ECC per channel, solder-down memory.

3.2.6 NC-SI Management Interface

The DPU Controller enables the connection of a Baseboard Management Controller (BMC) to a set of Network Interface Controller (NICs) to enable out-of-band remote manageability. The NC-SI management is supported over RMII and has a connector on the DPU Controller. Please refer to NC-SI Management Interface for pins.

The maximum trace length on the board is 5.7inch.

> The USB to UART cable is not used for NC-SI management purposes.

3.2.7 UART Interface Connectivity

The UART debug interface on BlueField-3 boards can be accessed through a 20-pin NC-SI connector, which is associated with the NIC BMC device. The connectivity is shown in the following table:

NC-SI Connector Pin #	Signal on Board
12	GND
14	UART_TX
16	UART_RX

> It is prohibited to connect any RS-232 cable directly! Only TTL 3.3V voltage level cables are supported.
>
> Do not use the USB-to-UART cable for NC-SI management purposes.

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3.2.8 USB 4-pin RA Connector

The USB 4-pin RA USB connector is used to load operating system images. Use a 4-pin male connector to a male Type-A cable to connect to the board.

It is prohibited to connect male-to-male to host, it is only used for a disk on key.

The male connector to the male Type-A cable is not included in the shipped DPU Controller card box and should be ordered separately as part of the accessories kit (P/N: MBF35-DKIT).

3.2.9 1GbE OOB Management Interface

The DPU Controller incorporates a 1GbE RJ45 out-of-band port that allows the network operator to establish trust boundaries in accessing the management function to apply it to network resources. It can also be used to ensure management connectivity (including the ability to determine the status of any network component) independent of other in-band network components' status.

For DPU Controllers with integrated BMC: 1GbE OOB Management can be performed via the integrated BMC.

3.2.9.1 1GbE OOB Management LEDs Interface

Two OOB management LEDs, one Green and one Yellow, behave as described in the table below.

Green LED	Yellow LED	Link/Activity
OFF	OFF	Link off
ON	OFF	1 Gb/s link / No activity
Blinking	OFF	1 Gb/s link / Activity (RX,TX)
OFF	ON	Not supported
OFF	Blinking	
ON	ON	
Blinking	Blinking	

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3.2.10 PPS IN/OUT Interface

The DPU Controller incorporates an integrated Hardware Clock (PHC) that allows the DPU Controller to achieve sub-20u Sec accuracy and also offers many timing-related functions such as time-triggered scheduling or time-based SND accelerations (time-based ASAP^2). Furthermore, 5T technology enables the software application to transmit fronthaul (ORAN) at high bandwidth. The PTP part supports the subordinate clock, master clock, and boundary clock.

The DPU Controller PTP solution allows you to run any PTP stack on your host.

With respect to testing and measurements, selected NVIDIA DPU Controllers allow you to use the PPS-out signal from the onboard MMCX RA connecter. The DPU Controller also allows measuring PTP in scale with the PPS-In signal. The PTP HW clock on the Network adapter is sampled on each PPS-In signal, and the timestamp is sent to the SW.

3.2.11 External PCIe Power Supply Connector

> ⚠ The external ATX power cable is not supplied with the DPU Controller package; however, this is a standard cable usually available in servers.

To power up the above-mentioned DPUs, it is necessary to use a supplementary 8-pin ATX power cable. Since the power provided by the PCIe golden fingers is limited to 66W, a total maximum of up to 150W is enabled through the ATX 8-pin connector and the PCIe x16 golden fingers.

The maximum power consumption which does not exceed 150W, is in accordance with the mode of operation of the DPU, and is split between the two power sources as follows:

- Up to 66W from the PCIe golden fingers (12V)
- The rest of the consumed power is drawn from the external PCIe power supply connector

Important Notes and Warnings

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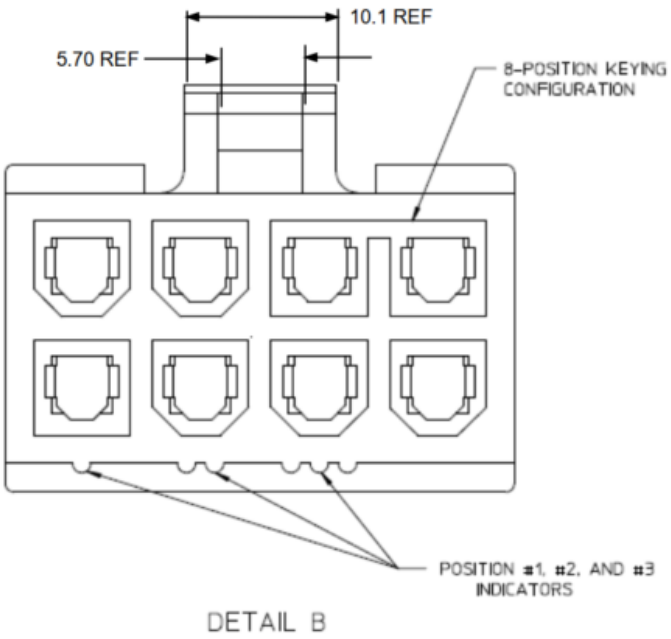
- The BlueField-3 DPU requires a standard PCIe ATX power connection. However, certain servers may require a custom setup to enable ATX power compatibility.
- Consult the manufacturer's manuals and specifications to ensure proper connectivity.
- Before connecting the ATX power cable, make sure you are using a PCIe-compliant 8-pin ATX cable from the server power supply kit.
- Do not link the CPU power cable to the BlueField-3 DPU PCIe ATX power connector, as their pin configurations differ. Using the CPU power cable in this manner is strictly prohibited and can potentially damage the BlueField-3 DPU. Please refer to External PCIe Power Supply Connector Pins for the external PCIe power supply pins.
- Avoid using non-standard cables that do not comply with the DPU, unnecessary adapter cables, or storing the cables near heat sources.
- It is preferable that the x16 PCIe golden fingers and the PCI ATX power supply draw from the same power source. For more information on how to power up the card, refer to Power-Up Instructions.
- The PCIe ATX 8-pin connector is not compatible with an EPS12V power cable source. Ensure that the appropriate PCIe auxiliary power source is available, not an EPS12V power source.
- If you are uncertain about your server's compatibility with the PCI ATX connection, please contact your NVIDIA representative for assistance.

Mechanical Keys of the 8-pin ATX Power Cable (PCIe CEM Specification Rev 5.0)



3.2.12 Cabline CA-II Plus Connectors

The Cabline CA-II connectors on the DPU Controller enable connectivity to an additional PCIe x16 bus in addition to the PCIe x16 bus available through the golden-fingers. The Cabline CA-II Plus connectors allow connectivity to flash cards and NVMe SSD drives.

Specific applications have an interest in direct connectivity to the far end of the Cabline CA-II cables, through the two 60-pin Cabline CA-II connectors, directly to the motherboard, in order to cut the insertion loss and/or the additional space associated with a PCIe x16 Flash Auxiliary Board.

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The Cabline CA-II connectors mate with two 60-pin Cabline CA-II cables that can be distinguished by their black or white external insulators and connector pinouts. The black Cabline CA-II cable mates with the DPU Controller's component (top) side, whereas the white Cabline CA-II cable mates with the DPU Controller print (bottom) side. The Cabline CA-II cables are offered in three standard lengths; 150mm and 350mm. For connector pinouts, please refer to Cabline CA-II Plus Connectors Pinouts.

3.2.13 Integrated BMC Interface

The DPU Controller incorporates an onboard integrated NIC BMC and an Ethernet switch. The BMC becomes available once the host server powers up the card. The NIC BMC can control the DPU Controller's power and enables DPU Controller shutdown and power-up.

3.2.14 NVMe SSD Interface

> ⚠ The Self Encrypting Disk (SED) capability is not supported.

The on-board 128GB NVMe SSD is utilized for the storage of user applications and logs. It is important to note that all SSD devices come with a limitation on the total number of write operations they can handle throughout their lifespan. This limit is influenced significantly by the software use case and specific parameters like block size and the pattern of data access (whether it is sequential or random).

It is the customer's responsibility to oversee the rate at which the SSD ages during both the validation of the code and its usage in the field, ensuring that it aligns with the intended use case.

3.2.15 RTC Battery

BlueField-3 incorporates a coin type Lithium battery CR621 for RTC (Real Time Clock).

3.2.16 eMMC Interface

The eMMC is an x8 NAND flash used for Arm boot and operating system storage. Memory size is 128GB, where it is effectively pSLC 40GB.

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4 Pinouts Description

Unknown macro: 'easy-heading-free'

4.1 PCI Express Interface

The below tables lists the PCI Express pins description. For further details, please refer to PCI Express Interface.

DPU PCI Express x16 Pin Description

Pin #	Signal Name	Description	Pin #	Signal Name	Description
A1	PRSNT1#	Mechanical Present	B1	12V	
A2	12V		B2	12V	
A3	12V		B3	12V	
A4	GND		B4	GND	
A5	TCK	JTAG - Not Connected	B5	SMCLK	Host SMBus
A6	TDI	JTAG - Not Connected	B6	SMDAT	Host SMBus
A7	TDO	JTAG - Not Connected	B7	GND	
A8	TMS	JTAG - Not Connected	B8	3.3V	3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only)
A9	3.3V	3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only)	B9	TRST#	JTAG - Not Connected
A10	3.3V	3.3V - (Connected in 900-9D3B4-00CC-EA0 & 900-9D3B4-00SC-EA0 only)	B10	3.3V_AUX	
A11	PERST#	PCIe Reset	B11	WAKW#/RSVD	
A12	GND		B12	SER_DI	
A13	REFCLK+	Host Reference Clock	B13	GND	
A14	REFCLK-	Host Reference Clock	B14	PETP0	
A15	GND		B15	PETN0	
A16	PERP0		B16	GND	
A17	PERN0		B17	RSVD	
A18	GND		B18	GND	
A19	SER_DO		B19	PETP1	
A20	GND		B20	PETN1	
A21	PERP1		B21	GND	
A22	PERN1		B22	GND	
A23	GND		B23	PETP2	
A24	GND		B24	PETN2	

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Pin #	Signal Name	Description	Pin #	Signal Name	Description
A25	PERP2		B25	GND	
A26	PERN2		B26	GND	
A27	GND		B27	PETP3	
A28	GND		B28	PETN3	
A29	PERP3		B29	GND	
A30	PERN3		B30	RSVD	
A31	GND		B31	RSVD	
A32	SER_CLK		B32	GND	
A33	SER_CAPTURE		B33	PETP4	
A34	GND		B34	PETN4	
A35	PERP4		B35	GND	
A36	PERN4		B36	GND	
A37	GND		B37	PETP5	
A38	GND		B38	PETN5	
A39	PERP5		B39	GND	
A40	PERN5		B40	GND	
A41	GND		B41	PETP6	
A42	GND		B42	PETN6	
A43	PERP6		B43	GND	
A44	PERN6		B44	GND	
A45	GND		B45	PETP7	
A46	GND		B46	PETN7	
A47	PERP7		B47	GND	
A48	PERN7		B48	RSVD	
A49	GND		B49	GND	
A50	RSVD		B50	PETP8	
A51	GND		B51	PETN8	
A52	PERP8		B52	GND	
A53	PERN8		B53	GND	
A54	GND		B54	PETP9	
A55	GND		B55	PETN9	
A56	PERP9		B56	GND	
A57	PERN9		B57	GND	
A58	GND		B58	PETP10	
A59	GND		B59	PETN10	

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Pin #	Signal Name	Description	Pin #	Signal Name	Description
A60	PERP10		B60	GND	
A61	PERN10		B61	GND	
A62	GND		B62	PETP11	
A63	GND		B63	PETN11	
A64	PERP11		B64	GND	
A65	PERN11		B65	GND	
A66	GND		B66	PETP12	
A67	GND		B67	PETN12	
A68	PERP12		B68	GND	
A69	PERN12		B69	GND	
A70	GND		B70	PETP13	
A71	GND		B71	PETN13	
A72	PERP13		B72	GND	
A73	PERN13		B73	GND	
A74	GND		B74	PETP14	
A75	GND		B75	PETN14	
A76	PERP14		B76	GND	
A77	PERN14		B77	GND	
A78	GND		B78	PETP15	
A79	GND		B79	PETN15	
A80	PERP15		B80	GND	
A81	PERN15		B81	PRSNT2#	Mechanical Present
A82	GND		B82	GND	

4.2 External Power Supply Connector

The below table provides the External Power Supply pins of the external power supply interfaces on the DPU. For further details, please refer to External PCIe Power Supply Connector.

> The mechanical pinout of the 8-pin external +12V power connector is shown below. The +12V connector is a GPU power PCIe standard connector. Care should be taken to ensure the power is applied to the correct pins as some 8-pin ATX-type connectors can have different pinouts.

Pin Number	Description
1	12V
2	12V

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Pin Number	Description
3	12V
4	Sense1
5	GND
6	Sense0
7	GND
8	GND

4.3 NC-SI Management Interface

The below tables list the NC-SI management interface pinout descriptions. For further details, please refer to NC-SI Management Interface.

Pin #	Signal Name	I/O	Signal Description
1	GND	GND	Ground
2	PKG_ID1	Input (to BlueField-3)	NC-SI PKG_ID Should be connected to the Primary controller NC-SI PKG_ID pins to set the appropriate package ID. PKG_ID0 should be connected to the endpoint device GPIO associated with Package ID[0]. PKG_ID1 should be associated with Package ID[1]. Baseboard should connect to GND or leave floating. DPU should have a 4.7k PU.
3	RBT_RXD0	Output (from BlueField-3)	Receive data. Data signals from the network controller to the BMC. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
4	RBT_REF_CLK	Input	RBT Reference clock. Synchronous clock reference for receive, transmit and control interface. The clock should have a typical frequency of 50MHz ±50 ppm. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the DPU cable connector. The RBT_REF_CLK should not be driven until 3.3V AUX is present on the DPU. The RBT_REF_CLK should be continuous once it has started. For DPUs, this pin should be connected between the connector and the RBT PHY. No external termination is required.
5	RBT_RXD1	Output	Receive data. Data signals from the network controller to the BMC. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no card is installed. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
6	GND	GND	Ground

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Pin #	Signal Name	I/O	Signal Description
7	RBT_CRS_DV	Output	Carrier sense/receive data valid. This signal is used to indicate to the baseboard that the carrier sense/receive data is valid. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor on the baseboard between the BMC and the RBT isolator to prevent the signal from floating when no DPU is installed. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
8	RBT_ISOLATE_N	Output	This signal is used to indicate the DPU has powered and is ready for NC-SI physical layer connection to be present. When low the baseboard circuitry will isolate the NC-SI connection to the DPU. When high normal NC-SI RBT connectivity is available. Baseboards should terminate this with a 47K-100K PD resistor. DPUs should terminate with a 10k PU resistor.
9	GND	GND	Ground
10	PKG_ID0	Input	NC-SI PKG_ID should be connected to the Primary controller NC-SI PKG_ID pins to set the appropriate package ID. PKG_ID0 should be connected to the endpoint device GPIO associated with Package ID[0]. PKG_ID1 should be associated with Package ID[1]. Baseboard should connect to GND or leave floating. DPU should have a 4.7k PU.
11	RBT_TX_EN	Input	Transmit enable. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to ground on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
12	GND	GND	Ground
13	RBT_TXD0	Input	Transmit data. Data signals from the BMC to the network controller. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
14	UART_TX	Input	3.3V UART TX signal from the baseboard
15	RBT_TXD1	Input	Transmit data. Data signals from the BMC to the network controller. For baseboards, this pin should be connected between the baseboard NC-SI over RBT PHY and the connector. This signal requires a 100 kΩ pull down resistor to GND on the baseboard between the RBT isolator and the DPU cable connector to prevent the card-side signals from floating when the RBT signals are isolated. For DPUs, this pin should be connected between the connector and the RBT PHY. External termination determined by the DPU RBT PHY requirements.
16	UART_RX	Output	3.3V UART RX signal to the baseboard

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Pin #	Signal Name	I/O	Signal Description
17	PRESENCE_N		Presence of DPU. Baseboard should implement a 200 Ω series resistor and 4.7kohm pull-up resistor to 3.3V AUX. DPU should tie this to GND.
18	GND	GND	Ground
19	RBT_ARB_OUT	Input	NC-SI hardware arbitration output. If the baseboard supports multiple DPUs cards connected to the same RBT interface, it should implement logic that connects the RBT_ARB_OUT pin of the first populated DPU card to its RBT_ARB_IN pin if it is the only card present or to the RBT_ARB_IN pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic should bypass slots that are not populated or powered off.
20	RBT_ARB_IN	Output	NC-SI hardware arbitration input. If the baseboard supports multiple DPUs cards connected to the same RBT interface, it should implement logic that connects the RBT_ARB_IN pin of the first populated DPU card to its RBT_ARB_OUT pin if it is the only card present or to the RBT_ARB_OUT pin of the next populated card and so on sequentially for all cards on the specified RBT bus to ensure the arbitration ring is complete. This logic should bypass slots that are not populated or powered off.

4.4 Cabline CA-II Plus Connectors Pinouts

4.4.1 Component Side

Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
1	GND	GND BAR		1
2	PCIE_REFCLK1_P	Micro coax	38	2
3	PCIE_REFCLK1_N	Micro coax	38	3
4	GND	GND BAR		4
5	PCIE_CPU_CX_15N	Micro coax	38	5
6	PCIE_CPU_CX_15P	Micro coax	38	6
7	GND	GND BAR		7
8	PCIE_CPU_CX_14N	Micro coax	38	8
9	PCIE_CPU_CX_14P	Micro coax	38	9
10	GND	GND BAR		10
11	PCIE_CPU_CX_13N	Micro coax	38	11
12	PCIE_CPU_CX_13P	Micro coax	38	12
13	GND	GND BAR		13
14	PCIE_CPU_CX_12N	Micro coax	38	14

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Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
15	PCIE_CPU_CX_12P	Micro coax	38	15
16	GND	GND BAR		16
17	PCIE_CPU_CX_11N	Micro coax	38	17
18	PCIE_CPU_CX_11P	Micro coax	38	18
19	GND	GND BAR		19
20	PCIE_CPU_CX_10N	Micro coax	38	20
21	PCIE_CPU_CX_10P	Micro coax	38	21
22	GND	GND BAR		22
23	PCIE_CPU_CX_9N	Micro coax	38	23
24	PCIE_CPU_CX_9P	Micro coax	38	24
25	GND	GND BAR		25
26	PCIE_CPU_CX_8N	Micro coax	38	26
27	PCIE_CPU_CX_8P	Micro coax	38	27
28	GND	GND BAR		28
29	PCIE_CPU_CX_7N	Micro coax	38	29
30	PCIE_CPU_CX_7P	Micro coax	38	30
31	GND	GND BAR		31
32	CIE_CPU_CX_6N	Micro coax	38	32
33	PCIE_CPU_CX_6P	Micro coax	38	33
34	GND	GND BAR		34
35	PCIE_CPU_CX_5N	Micro coax	38	35
36	PCIE_CPU_CX_5P	Micro coax	38	36
37	GND	GND BAR		37
38	PCIE_CPU_CX_4N	Micro coax	38	38
39	PCIE_CPU_CX_4P	Micro coax	38	39
40	GND	GND BAR		40
41	PCIE_CPU_CX_3N	Micro coax	38	41
42	PCIE_CPU_CX_3P	Micro coax	38	42
43	GND	GND BAR		43
44	PCIE_CPU_CX_2N	Micro coax	38	44
45	PCIE_CPU_CX_2P	Micro coax	38	45
46	GND	GND BAR		46
47	PCIE_CPU_CX_1N	Micro coax	38	47
48	PCIE_CPU_CX_1P	Micro coax	38	48
49	GND	GND BAR		49
50	PCIE_CPU_CX_0N	Micro coax	38	50

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Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
51	PCIE_CPU_CX_0P	Micro coax	38	51
52	GND	GND BAR		52
53	No wire	Micro coax	38	53
54	No wire	Micro coax	38	54
55	AUX_PGOOD	Micro coax	38	55
56	No wire	Micro coax	38	56
57	I2C_AUX_SCL	Micro coax	38	57
58	I2C_AUX_SDA	Micro coax	38	58
59	S_PRSNT1_L	Micro coax	38	59
60	No wire			60

4.4.2 Print Side

Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
1	No wire	Micro coax	38	1
2	No wire	Micro coax	38	2
3	No wire	Micro coax	38	3
4	No wire	Micro coax	38	4
5	No wire	Micro coax	38	5
6	Reserved_06	Micro coax	38	6
7	Reserved_07	Micro coax	38	7
8	Reserved_08	Micro coax	38	8
9	GND	GND BAR		9
10	PCIE_CPU_CX_0P	Micro coax	38	10
11	PCIE_CPU_CX_0N	Micro coax	38	11
12	GND	GND BAR		12
13	PCIE_CPU_CX_1P	Micro coax	38	13
14	PCIE_CPU_CX_1N	Micro coax	38	14
15	GND	GND BAR		15
16	PCIE_CPU_CX_2P	Micro coax	38	16
17	PCIE_CPU_CX_2N	Micro coax	38	17
18	GND	GND BAR		18
19	PCIE_CPU_CX_3P	Micro coax	38	19
20	PCIE_CPU_CX_3N	Micro coax	38	20
21	GND	GND BAR		21

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Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
22	PCIE_CPU_CX_4P	Micro coax	38	22
23	PCIE_CPU_CX_4N	Micro coax	38	23
24	GND	GND BAR		24
25	PCIE_CPU_CX_5P	Micro coax	38	25
26	PCIE_CPU_CX_5N	Micro coax	38	26
27	GND	GND BAR		27
28	PCIE_CPU_CX_6P	Micro coax	38	28
29	PCIE_CPU_CX_6N	Micro coax	38	29
30	GND	GND BAR		30
31	PCIE_CPU_CX_7P	Micro coax	38	31
32	PCIE_CPU_CX_7N	Micro coax	38	32
33	GND	GND BAR		33
34	PCIE_CPU_CX_8P	Micro coax	38	34
35	PCIE_CPU_CX_8N	Micro coax	38	35
36	GND	GND BAR		36
37	PCIE_CPU_CX_9P	Micro coax	38	37
38	PCIE_CPU_CX_9N	Micro coax	38	38
39	GND	GND BAR		39
40	PCIE_CPU_CX_10P	Micro coax	38	40
41	PCIE_CPU_CX_10N	Micro coax	38	41
42	GND	GND BAR		42
43	PCIE_CPU_CX_11P	Micro coax	38	43
44	PCIE_CPU_CX_11N	Micro coax	38	44
45	GND	GND BAR		45
46	PCIE_CPU_CX_12P	Micro coax	38	46
47	PCIE_CPU_CX_12N	Micro coax	38	47
48	GND	GND BAR		48
49	PCIE_CPU_CX_13P	Micro coax	38	49
50	PCIE_CPU_CX_13N	Micro coax	38	50
51	GND	GND BAR		51
52	PCIE_CPU_CX_14P	Micro coax	38	52
53	PCIE_CPU_CX_14N	Micro coax	38	53
54	GND	GND BAR		54
55	PCIE_CPU_CX_15P	Micro coax	38	55
56	PCIE_CPU_CX_15N	Micro coax	38	56
57	GND	GND BAR		57

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Pin#	Signal Name	Wire Type	AWG#	Pin# on other end
58	S_PERST1_CONN_L	Micro coax	38	58
59	No wire	No Wire		59
60	S_PRSNT2_L	Micro coax	38	60

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5 Hardware Installation and PCIe Bifurcation

Installation and initialization of the DPU Controller require attention to the mechanical attributes, power specification, and precautions for electronic equipment.

5.1 Safety Warnings

> Safety warnings are provided here in the English language.

Please observe all safety warnings to avoid injury and prevent damage to system components. Note that not all warnings are relevant to all models.

Note that not all warnings are relevant to all models.

	General Installation Instructions Read all installation instructions before connecting the equipment to the power source.
	Jewelry Removal Warning Before you install or remove equipment that is connected to power lines, remove jewelry such as bracelets, necklaces, rings, watches, and so on. Metal objects heat up when connected to power and ground and can meltdown, causing serious burns and/or welding the metal object to the terminals.
	Over-temperature This equipment should not be operated in an area with an ambient temperature exceeding the maximum recommended: 55°C (131°F). An airflow of 200LFM at this maximum ambient temperature is required for HCA cards and NICs. To guarantee proper airflow, allow at least 8cm (3 inches) of clearance around the ventilation openings.
	During Lightning - Electrical Hazard During periods of lightning activity, do not work on the equipment or connect or disconnect cables.
	Copper Cable Connecting/Disconnecting Some copper cables are heavy and not flexible, as such, they should be carefully attached to or detached from the connectors. Refer to the cable manufacturer for special warnings and instructions.
	Equipment Installation This equipment should be installed, replaced, or serviced only by trained and qualified personnel.
	Equipment Disposal The disposal of this equipment should be in accordance to all national laws and regulations.
	Local and National Electrical Codes This equipment should be installed in compliance with local and national electrical codes.
	Hazardous Radiation Exposure • Caution – Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.For products with optical ports. • CLASS 1 LASER PRODUCT and reference to the most recent laser standards: IEC 60 825-1:1993 + A1:1997 + A2:2001 and EN 60825-1:1994+A1:1996+ A2:20

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5.2 Installation Procedure Overview

The installation procedure of DPU involves the following steps:

Step	Procedure	Direct Link
1	Check the system's requirements.	Refer to System Requirements
2	Pay attention to the airflow consideration within the host system	Refer to Airflow Requirements
3	Follow the safety precautions	Refer to Safety
4	Unpack the package	Refer to Unpacking
5	Follow the pre-installation checklist	Refer to Pre-Installation Checklist
7	Install the DPU according to the form-factor you have purchased.	Refer to DPU Installation
8	Connect cables or modules to the DPU	Refer to Cables and Modules
9	Power-up the DPU	Refer to DPU Power-Up Instructions

5.3 System Requirements

5.3.1 Hardware Requirements

Unless otherwise specified, products are designed to work in an environmentally controlled data center with low levels of gaseous and dust (particulate) contamination.

The operating environment should meet severity level G1 as per ISA 71.04 for gaseous contamination and ISO 14644-1 class 8 for cleanliness level.

The below table lists the motherboard and power supply requirements per DPU series.

Power Supply Requirement
Require a supplementary 8-pin ATX power supply connectivity available through the external power supply connector.

5.3.2 Airflow Requirements

The DPU Controller is offered with one airflow direction: from the heatsink to the network ports.

Any use of the product in the opposite airflow direction (from network ports to heatsink) must be validated thermally to ensure proper cooling of the product.

Please refer to the Specifications section for airflow numbers per DPU model.

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5.3.3 Software Requirements

- Refer to System Requirements section under the Introduction section.
- Software Stacks -BlueField-3 DPU Controller is shipped with Ubuntu – a Linux commercial operating system – which includes the NVIDIA OFED stack (MLNX_OFED), and is capable of running all customer-based Linux applications seamlessly. For more information, please refer to the DOCA SDK documentation or NVIDIA BlueField DPU BSP.

5.4 Safety Precautions

The DPU Controller is being installed in a system that operates with voltages that can be lethal. Before opening the case of the system, observe the following precautions to avoid injury and prevent damage to system components.

- Remove any metallic objects from your hands and wrists.
- Make sure to use only insulated tools.
- Verify that the system is powered off and is unplugged.
- It is strongly recommended to use an ESD strap or other antistatic devices.

5.5 Unpacking

Check against the package contents list that all the parts have been sent. Check the parts for visible damage that may have occurred during shipping. Please note that the DPU Controllers must be placed on an antistatic surface.

> Please note that if the DPU is removed hastily from the antistatic bag, the plastic ziplock may harm the EMI fingers on the networking connector. Carefully remove the DPU Controller from the antistatic bag to avoid damaging the EMI fingers.

For package contents, please refer to Package Contents.

5.6 Pre-Installation Checklist

1. Verify that your system meets the hardware and software requirements stated above.
2. Shut down your system if active.
   Turn off the power to the system, and disconnect the power cord. Refer to the system documentation for instructions. Before you install the DPU, make sure that the system is disconnected from power.

5.7 Installation Instructions

This section provides detailed instructions on how to install your DPU Controller in a system. Choose the installation instructions according to the configuration you would like to use.

Installation Instructions
PCIe x16 DPU Controller Installation Instructions

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Installation Instructions
[Optional] PCIe Extension Connection (2x PCIe x16) Installation Instructions

5.8 Cables and Modules

5.8.1 Networking Cable Installation

1. All cables can be inserted or removed with the unit powered on.
2. To insert a cable, press the connector into the port receptacle until the connector is firmly seated.
   a. Support the weight of the cable before connecting the cable to the DPU Controller. Do this by using a cable holder or tying the cable to the rack.
   b. Determine the correct orientation of the connector to the DPU Controller before inserting the connector. Do not try and insert the connector upside down. This may damage the DPU Controller.
   c. Insert the connector into the DPU Controller . Be careful to insert the connector straight into the cage. Do not apply any torque, up or down, to the connector cage in the DPU Controller.
   d. Make sure that the connector locks in place.

   > When installing cables make sure that the latches engage.

   > Always install and remove cables by pushing or pulling the cable and connector in a straight line with the DPU.

3. After inserting a cable into a port, the Green LED indicator will light when the physical connection is established (that is, when the unit is powered on and a cable is plugged into the port with the other end of the connector plugged into a functioning port). See Networking Ports LEDs interface under the Supported Interfaces section.
4. After plugging in a cable, lock the connector using the latching mechanism particular to the cable vendor. When data is being transferred the Green LED will blink.
5. Make sure not to impede the air exhaust flow through the ventilation holes. Use cable lengths that allow for routing horizontally around to the side of the chassis before bending upward or downward in the rack.
6. To remove a cable, disengage the locks and slowly pull the connector away from the port receptacle. LED indicator will turn off when the cable is unseated.

5.8.2 8-pin ATX Power Supply Cable

> The 8-pin ATX power supply cable is mandatory when powering-up the following DPUs. Without a connection to the power supply cable, the DPU will not complete the power on procedure and will not function properly.

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The BlueField-3 DPU Controller includes an 8-pin PCIe ATX power connector that provides additional power supply. While the PCIe slot feeds 66W, the 8-pin PCIe ATX power supply cable provides additional power.

Important Notes and Warnings

- The BlueField-3 DPU Controller requires a standard PCIe ATX power connection. However, certain servers may require a custom setup to enable ATX power compatibility.
- Consult the manufacturer's manuals and specifications to ensure proper connectivity.
- Before connecting the ATX power cable, make sure you are using a PCIe-compliant 8-pin ATX cable from the server power supply kit.
- Do not link the CPU power cable to the BlueField-3 DPU Controller PCIe ATX power connector, as their pin configurations differ. Using the CPU power cable in this manner is strictly prohibited and can potentially damage the BlueField-3 DPU Controller. Please refer to External Power Supply Connector for the external PCIe power supply pins.
- Avoid using non-standard cables that do not comply with the DPU Controller, unnecessary adapter cables, or storing the cables near heat sources.
- It is preferable that the x16 PCIe golden fingers and the PCI ATX power supply draw from the same power source. For more information on how to power up the card, refer to DPU Controller Power-Up Instructions.
- The PCIe ATX 8-pin connector is not compatible with an EPS12V power cable source. Ensure that the appropriate PCIe auxiliary power source is available, not an EPS12V power source.
- If you are uncertain about your server's compatibility with the PCI ATX connection, please contact your NVIDIA representative for assistance.

5.8.3 Cable Installation Instructions

- Ensure both the system and card are completely powered off for at least 20 seconds before inserting the power connector.
- DO NOT force the connector into place; the connectors are “keyed” to fit only one way. Refer to the mechanical keys below for further information.
- Connect the power supply end of the 8-pin connector to the appropriate receptor on the power supply unit.
- Apply parallel force when plugging the cable into the power supply connector. Do not bend or twist the cables when plugging or unplugging it.
- Ensure the cable is fully and securely connected to your DPU Controller and the connector lock is secured.

Mechanical Keys of the 8-pin ATX Power Cable (PCIe CEM Specification Rev 5.0)

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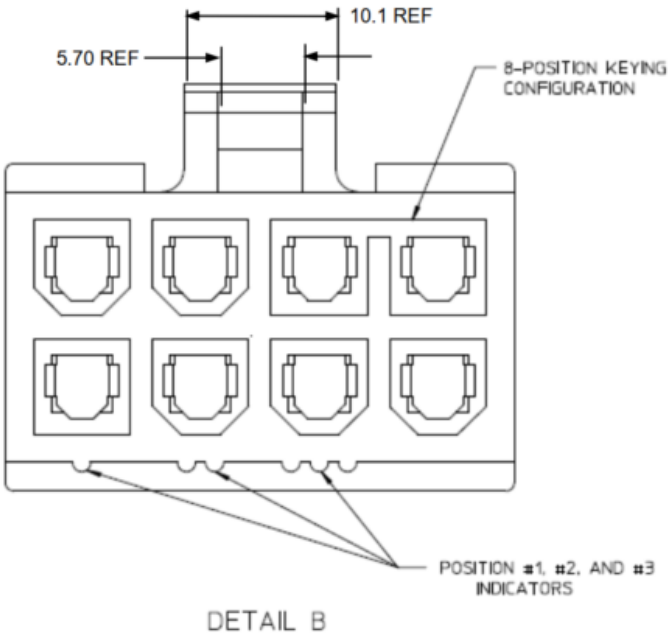
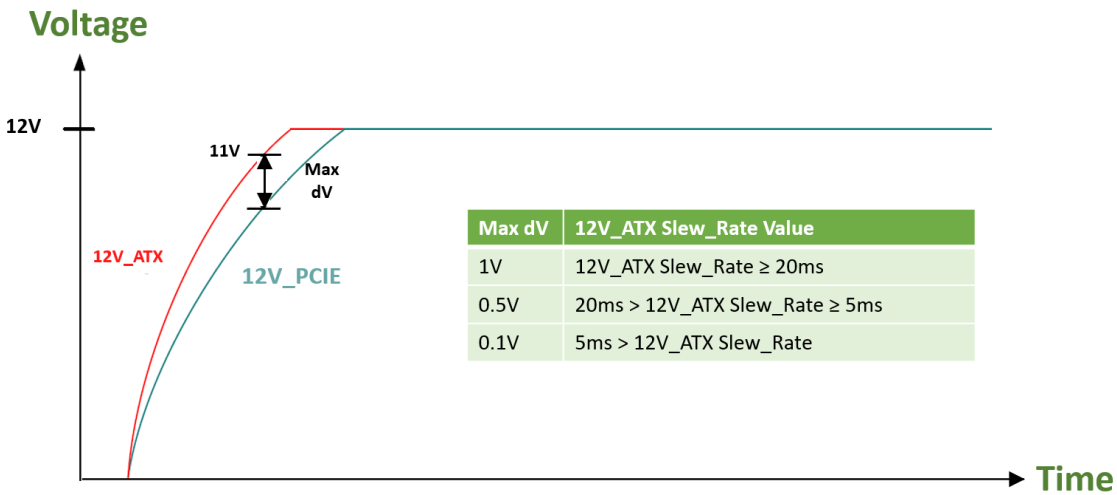


5.9 DPU Controller Power-Up and Power-Down Sequences

5.9.1 Power-Up Sequence

1. The 12V_ATX voltage can exceed the 12V_PCIE voltage by a maximum allowable voltage difference (dV) when the 12V_ATX reaches 11V. See below graph and table describing the dV between the 12V_ATX and 12V_PCIE voltages.



Max dV	12V_ATX Slew_Rate Value
1V	12V_ATX Slew_Rate ≥ 20ms
0.5V	20ms > 12V_ATX Slew_Rate ≥ 5ms
0.1V	5ms > 12V_ATX Slew_Rate

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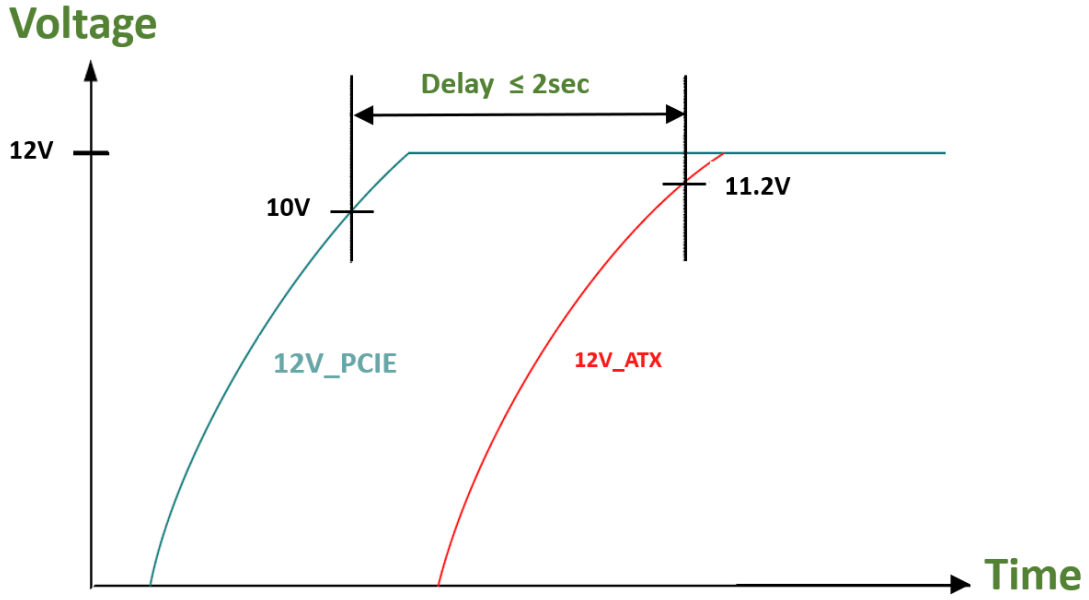
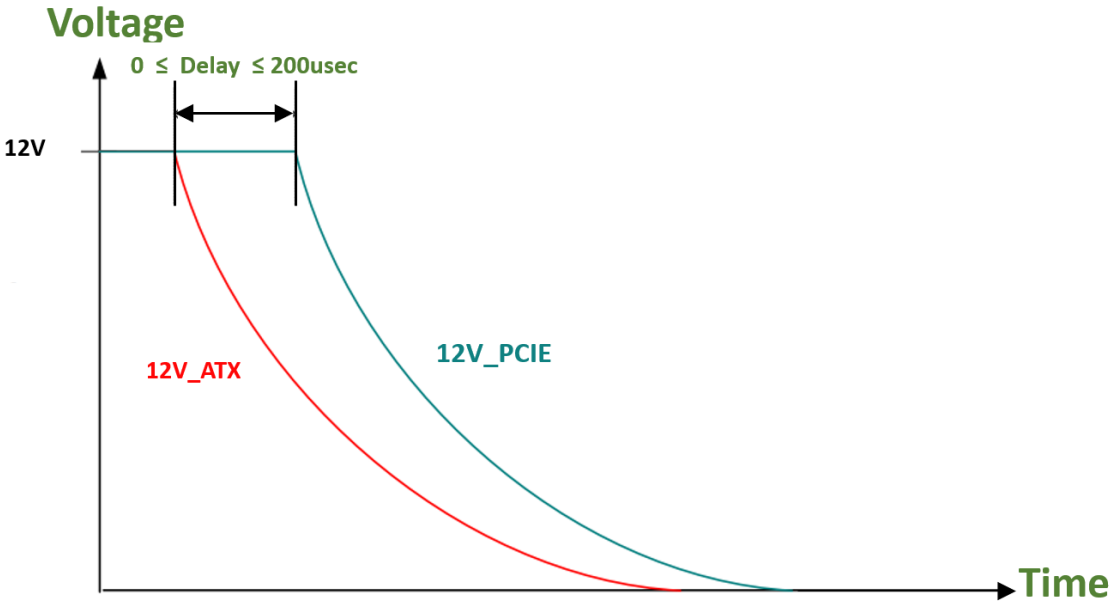
2. The 12V_ATX can be powered up after the 12V_PCIE, with a maximum delay of 2 seconds. The below graph illustrates the delay between the 12V_ATX and 12V_PCIE voltages at power-up.



5.9.2 Power-Down Sequence

1. The 12V_PCIE voltage can be powered down simultaneously with the 12V_ATX voltage, or within a maximum delay of 200usec. The below graph illustrates the delay between the 12V_ATX and 12V_PCIE voltages at power-down.



2. The 12V_PCIE voltage must not be powered down while the 12V_ATX voltage is powered up.

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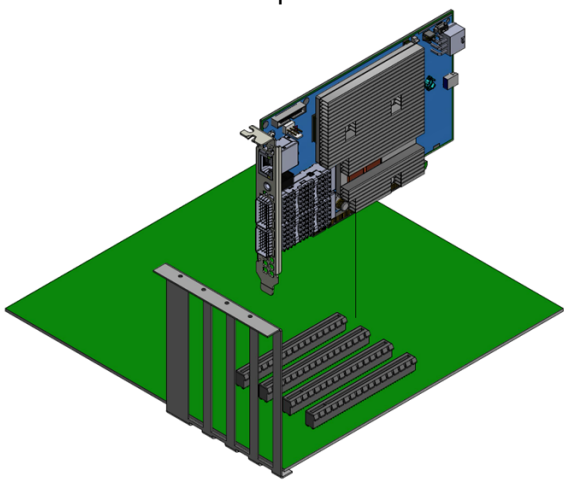
5.10 PCIe x16 DPU Controller Installation Instructions

5.10.1 Installation Instructions

This section provides detailed instructions on how to install your BlueField-3 card in a system.

> Please note that the following figures are for illustration purposes only.

1. Open the system case.
2. Locate an available PCI Express slot.



3. Hold the card by its edges and bracket, avoiding contact with the top surface. Apply even pressure to both edges of the card and gently insert the BlueField-3 card into the PCI Express slot.

> Exercise caution to avoid touching the components on the top surface of the card. Do not use excessive force when seating the card, as this may damage the system or the card's components.

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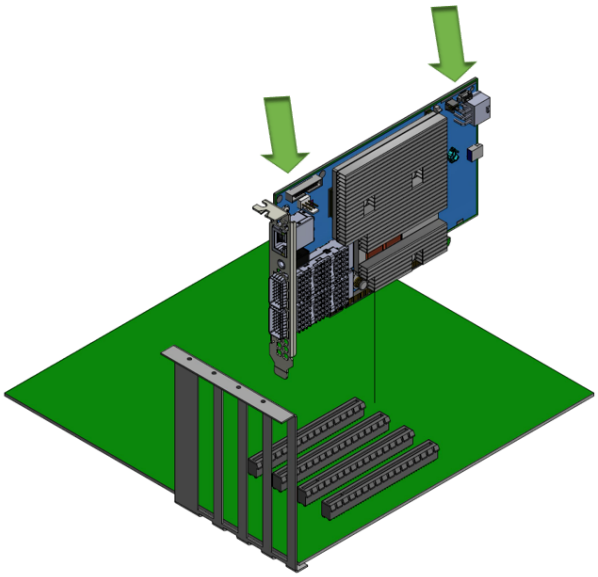
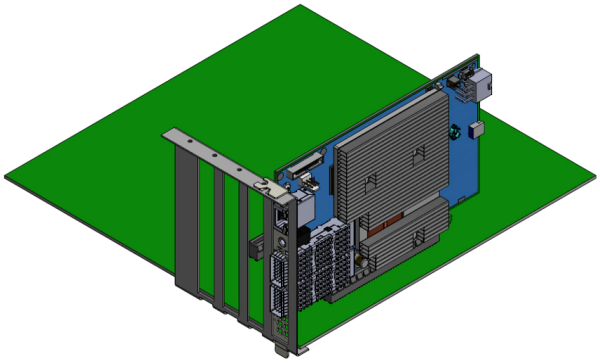
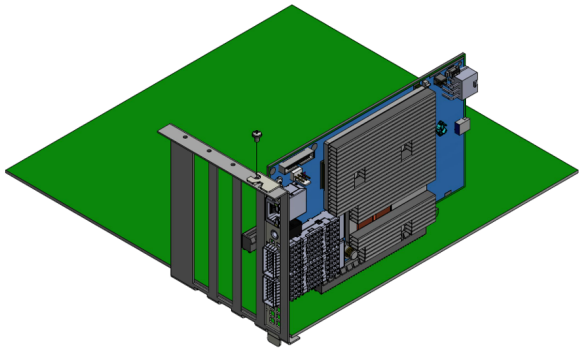


4. When the BlueField-3 card is properly seated, the port connectors are aligned with the slot opening, and the card's faceplate is visible against the system chassis.



5. Secure the card with the screw.



6. Close the system case.
7. Install the networking cables. For instructions, please refer to Networking Cable Installation.

5.10.2 Uninstalling the BlueField-3 Card

Safety Precautions

Downloaded from Arrow.com.

The card is installed in a system that operates with voltages that can be lethal. Before uninstalling the board, please observe the following precautions to avoid injury and prevent damage to system components.

1. Remove any metallic objects from your hands and wrists.
2. It is strongly recommended to use an ESD strap or other antistatic devices.
3. Turn off the system and disconnect the power cord from the server.

Card Removal

Please note that the following images are for illustration purposes only.

1. Verify that the system is powered off and unplugged.
2. Wait 30 seconds.
3. To remove the card, disengage the retention mechanism on the bracket (screws).
4. Holding the board from its center, gently pull the board out of the PCI Express slot.
5. When the port connectors reach the top of the chassis window, gently pull the board in parallel to the motherboard.

5.11 [Optional] PCIe Extension Connection (2x PCIe x16) Installation Instructions

The socket-direct functionality is currently not supported by firmware.

This section relevant when the DPU controller is used in Socket Direct mode in dual-socket servers:

For more information on the PCIe Auxiliary Kit, refer to PCIe Auxiliary Card Kit.

The below images are for illustration purposes only.

The hardware installation section uses the terminology of white and black harnesses to differentiate between the two supplied cables. Due to supply chain variations, some DPUs may be supplied with two black harnesses instead. To clarify the difference between these two harnesses, one black harness was marked with a “WHITE” label and the other with a “BLACK” label.

The Cabline harness marked with "WHITE" label should be connected to the connector on the DPU and Auxiliary PCIe card engraved with “White Cable” while the one marked with "BLACK" label should be connected to the connector on the DPU and Auxiliary PCIe card engraved with “Black Cable”.

The harnesses' minimal bending radius is 10[mm].

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5.11.1 Installing the DPU

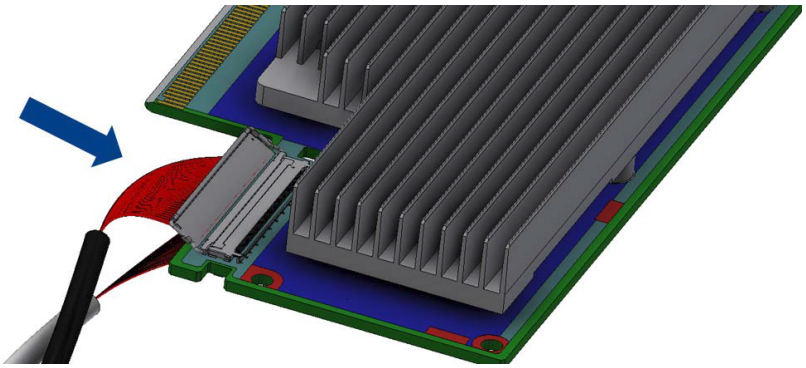
> ⚠ The installation instructions include steps that involve a retention clip to be used while connecting the Cabline harnesses to the DPUs. Please note that this is an optional accessory.

> ⚠ Please make sure to install the DPU cards in a PCIe slot capable of supplying the required power and airflow as stated in Specifications.

Connect the DPU Controller with the Auxiliary connection card using the supplied Cabline CA-II Plus harnesses.

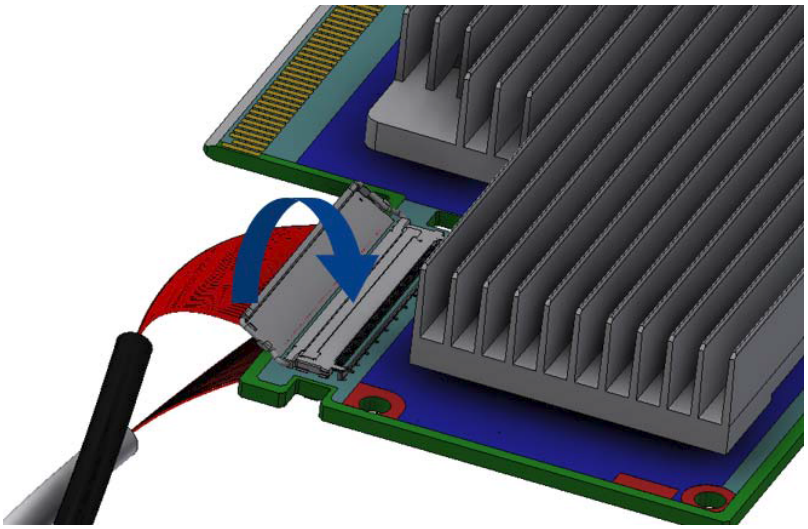
Step 1: Slide the black and white Cabline CA-II Plus harnesses through the retention clip while making sure the clip opening is facing the plugs.

Step 2: Plug the Cabline CA-II Plus harnesses on the DPU while paying attention to the color-coding. As indicated on both sides of the card; plug the black harness to the component side and the white harness to the print side.



Step 3: Verify the plugs are locked.

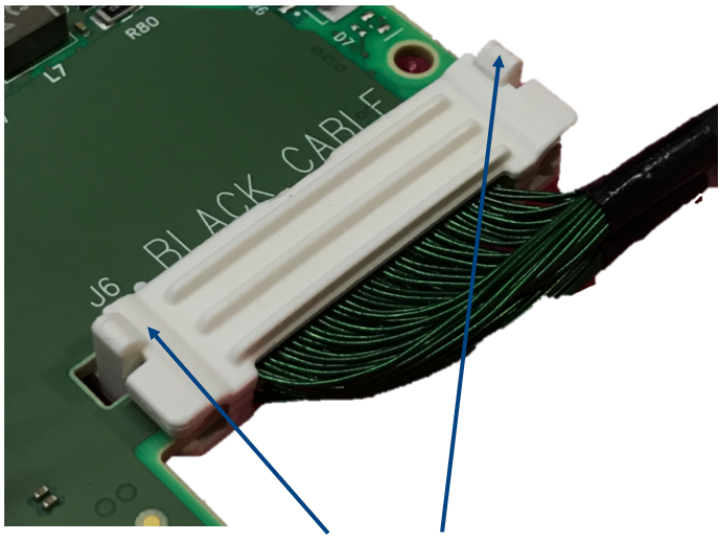
Downloaded from Arrow.com.



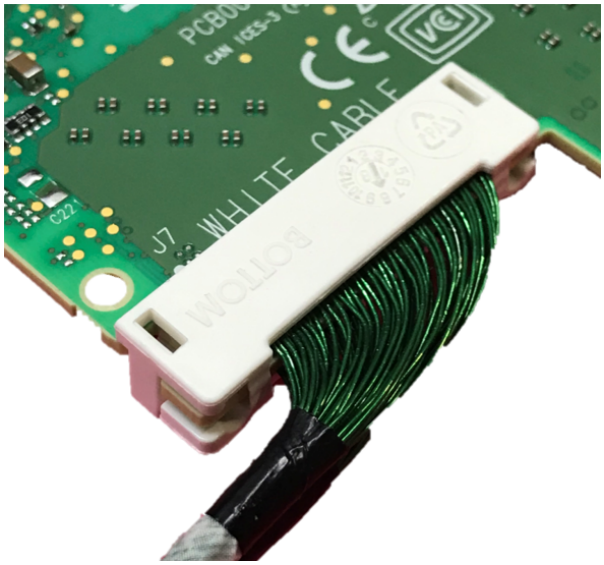
Step 4: Slide the retention clip latches through the cutouts on the PCB. The latches should face the annotation on the PCB.

Step 4: Clamp the retention clip. Verify both latches are firmly locked.

Downloaded from Arrow.com.



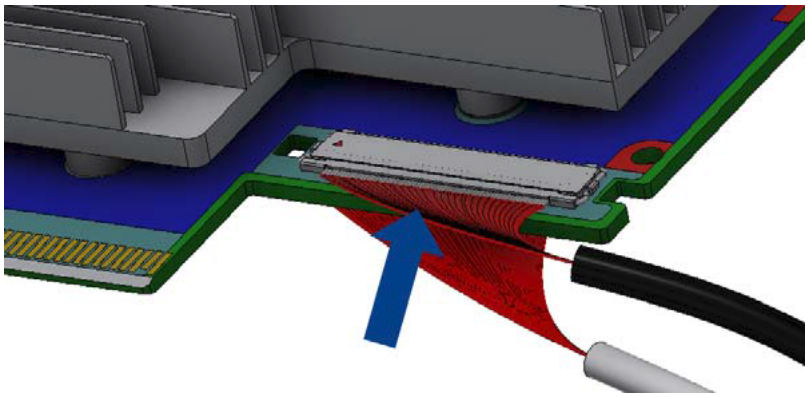
Verify that both latches are firmly snapped



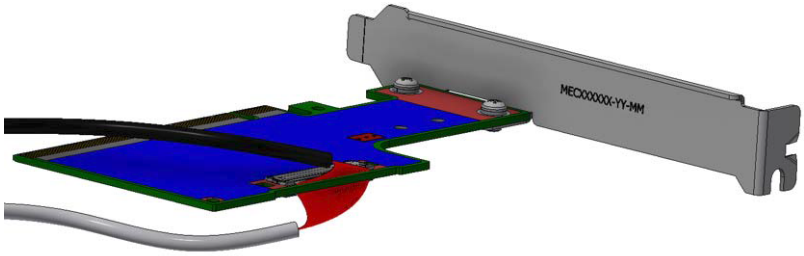
Step 5: Slide the Cabline CA-II Plus harnesses through the retention clip. Make sure that the clip opening is facing the plugs.

Downloaded from Arrow.com.

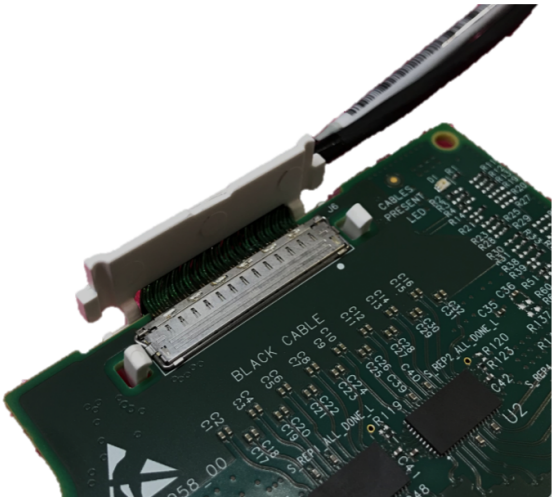
Step 6: Plug the Cabline CA-II Plus harnesses on the PCIe Auxiliary Card. As indicated on both sides of the Auxiliary connection card; plug the black harness to the component side and the white harness to the print side.



Step 7: Verify the plugs are locked.

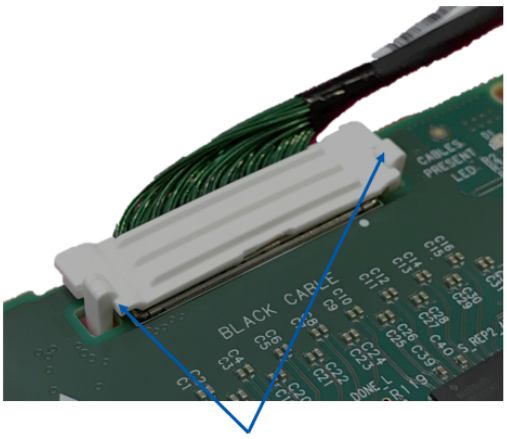


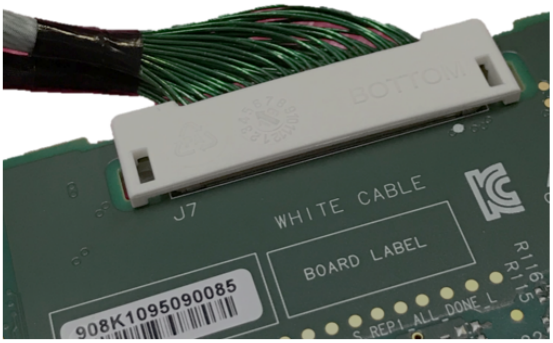
Step 8: Slide the retention clip through the cutouts on the PCB. Make sure latches are facing "Black Cable" annotation as seen in the below picture.



Step 9: Clamp the retention clip. Verify both latches are firmly locked.

Downloaded from Arrow.com.





Verify that both latches are firmly snapped

➢ Connect the DPU Controller and PCIe Auxiliary Connection cards in available PCI Express x16 slots in the chassis.

Step 1: Locate two available PCI Express x16 slots.

Step 2: Applying even pressure at both corners of the cards, insert the DPU in the PCI Express slots until firmly seated.

> Do not use excessive force when seating the cards, as this may damage the system or the cards.

Step 3: Applying even pressure at both corners of the cards, insert the Auxiliary Connection card in the PCI Express slots until firmly seated.

➢ Secure the DPU Controller and PCIe Auxiliary Connection Cards to the chassis.

Secure the brackets to the chassis with the bracket screws.

➢ Install the PCIe external power cable.

Connect the 8-pin power connector from the power supply to the power connector on the top edge of the DPU. Note that the connector and socket on the graphics card have a unique shape and connect one way only. For further instructions, please refer to the cable vendor documentation. Please refer to the pinout description in External Power Supply Connector.

➢ Close the system case.

5.11.2 Uninstalling the Cards

Safety Precautions

The DPU Controller is installed in a system that operates with voltages that can be lethal. Before uninstalling the DPU, please observe the following precautions to avoid injury and prevent damage to system components.

1. Remove any metallic objects from your hands and wrists.
2. It is strongly recommended to use an ESD strap or other antistatic devices.
3. Turn off the system and disconnect the power cord from the server.

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Card Removal

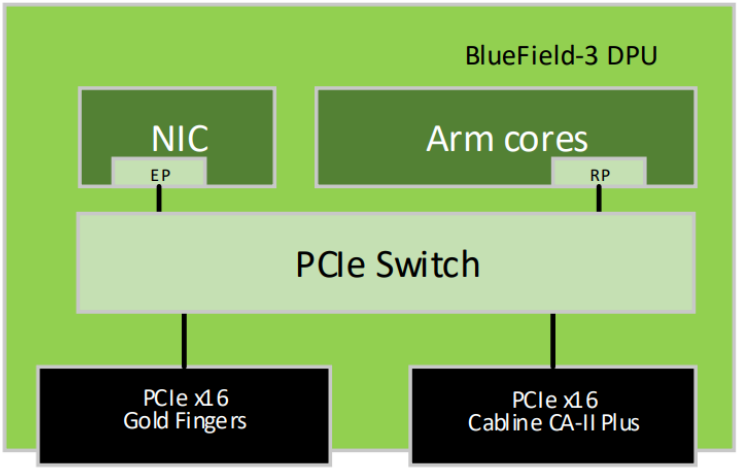
> Please note that the following images are for illustration purposes only.

1. Verify that the system is powered off and unplugged.
2. Wait 30 seconds.
3. To remove the card, disengage the retention mechanisms on the brackets (clips or screws).
4. Holding the DPU from its center, gently pull the DPU and Auxiliary Connections card out of the PCI Express slot.

5.12 PCIe Bifurcation Configuration Options

> PCIe bifurcation is supported starting from DOCA 2.5 with BlueField BSP 4.5.0 (released December 2023).

NVIDIA BlueField-3 Self-Hosted DPU Controller provides a range of configuration scenarios to meet the demands of environments and deployments. This section describes the various connectivity options for peripherals on the PCIe, such as NVMe SSDs as PCIe endpoints. While this list of scenarios is not exhaustive, it highlights the tested and verified options. Customers seeking to support unlisted configurations should contact NVIDIA Support.



> Before setting the desired configuration, take note of the following warnings:
>
> - Any customer-set configuration overrides the previous configuration values.
> - WARNING: Misconfiguration may harm the system.
> - It is recommended to establish out-of-band connectivity to the BlueField DPU Arm OS before setting any of these configurations for the first time. This enables you to reset the NVConfig parameters to their default values in case of misconfiguration.

The following table summarizes the available configuration scenarios.

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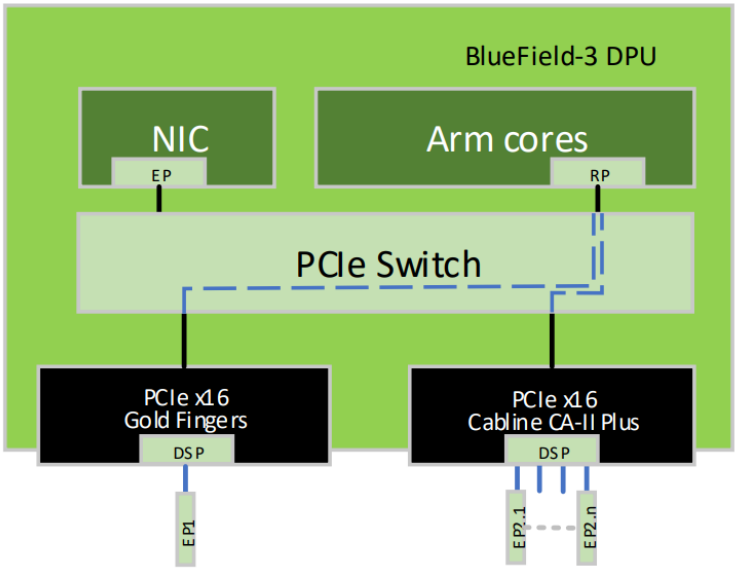
Configuration	Root Port Arm	DPU PCIe Golden Fingers Bifurcation	DPU PCIe Auxiliary Connection Bifurcation
Default	DPU Arm	1 x Gen 5.0/4.0 x16 PCIe lanes as down-stream-port	1 x Gen 5.0/4.0 x16 PCIe lanes as down-stream-port
Bifurcated to Eight x4 PCIe	DPU Arm	4 x Gen 5.0/4.0 x4 PCIe lanes as down-stream-port	4 x Gen 5.0/4.0 x4 PCIe lanes as down-stream-port
Bifurcated to One x16 PCIe and Eight x2 PCIe	DPU Arm	1 x Gen 5.0/4.0 x16 PCIe lanes as down-stream-port	8 x Gen 5.0/4.0 x2 PCIe lanes as down-stream-port

5.12.1 Bifurcated to Eight x4 PCIe

In this scenario, the x16 PCIe Goldfingers of the BlueField-3 DPU are bifurcated into four PCIe links, where each link comprises x4 PCIe lanes, while the additional x16 PCIe lanes are accessible via the Cabline CA-II Plus connector, bifurcated into four PCIe links, where each link comprises x4 PCIe lanes.

As seen in the below visual representation of this configuration, the DPU's Arm cores function as Root Port of all devices connected to both the Gold Fingers and the Cabline CA-II Plus connector.



Important Notes:

- mlxconfig can be configured either through the host in NIC Mode and DPU Mode, or directly from the DPU's Arm running OS.
- This configuration is persistent even following resets and NIC firmware updates.

The required set of configurations to implement this bifurcation is outlined below.

```
mlxconfig -d <device> s PCI_BUS00_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS00_WIDTH=3
mlxconfig -d <device> s PCI_BUS00_SPEED=4
mlxconfig -d <device> s PCI_BUS02_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS02_WIDTH=3
mlxconfig -d <device> s PCI_BUS02_SPEED=4
```

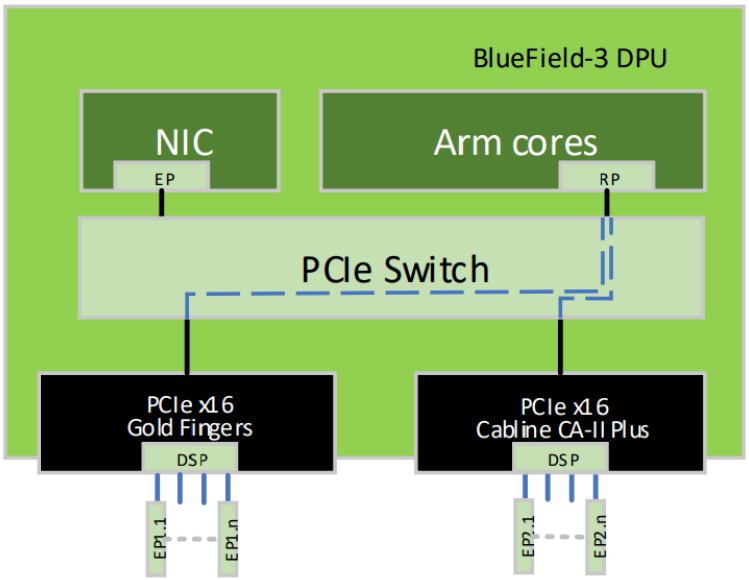

Downloaded from Arrow.com.

```
mlxconfig -d <device> s PCI_BUS04_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS04_WIDTH=3
mlxconfig -d <device> s PCI_BUS04_SPEED=4
mlxconfig -d <device> s PCI_BUS06_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS06_WIDTH=3
mlxconfig -d <device> s PCI_BUS06_SPEED=4
mlxconfig -d <device> s PCI_BUS10_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS10_WIDTH=3
mlxconfig -d <device> s PCI_BUS10_SPEED=4
mlxconfig -d <device> s PCI_BUS12_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS12_WIDTH=3
mlxconfig -d <device> s PCI_BUS12_SPEED=4
mlxconfig -d <device> s PCI_BUS14_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS14_WIDTH=3
mlxconfig -d <device> s PCI_BUS14_SPEED=4
mlxconfig -d <device> s PCI_BUS16_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS16_WIDTH=3
mlxconfig -d <device> s PCI_BUS16_SPEED=4
```

5.12.2 Bifurcated to One x16 PCIe and Eight x2 PCIe

In this scenario, the x16 PCIe Goldfingers of the BlueField-3 DPU are bifurcated to one PCIe link with x16 PCIe lanes, while the additional x16 PCIe lanes are accessible via the Cabline CA-II Plus connector, bifurcated into eight PCIe links, where each link comprises x2 PCIe lanes.

As seen in the below visual representation of this configuration, the DPU's Arm cores function as Root Port of all downstream devices connected to both the Goldfingers and the Cabline CA-II Plus connector.



Important Notes:

- mlxconfig can be configured either through the host in NIC Mode and DPU Mode, or directly from the DPU's Arm running OS.
- This configuration is persistent even following resets and NIC firmware updates.

The required set of configurations to implement this bifurcation is outlined below:

```
mlxconfig -d <device> s PCI_BUS00_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS00_WIDTH=5
mlxconfig -d <device> s PCI_BUS00_SPEED=4
mlxconfig -d <device> s PCI_BUS10_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS10_WIDTH=2
mlxconfig -d <device> s PCI_BUS10_SPEED=4
mlxconfig -d <device> s PCI_BUS11_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS11_WIDTH=2
mlxconfig -d <device> s PCI_BUS11_SPEED=4
```


Downloaded from Arrow.com.

```
mlxconfig -d <device> s PCI_BUS12_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS12_WIDTH=2
mlxconfig -d <device> s PCI_BUS12_SPEED=4
mlxconfig -d <device> s PCI_BUS13_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS13_WIDTH=2
mlxconfig -d <device> s PCI_BUS13_SPEED=4
mlxconfig -d <device> s PCI_BUS14_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS14_WIDTH=2
mlxconfig -d <device> s PCI_BUS14_SPEED=4
mlxconfig -d <device> s PCI_BUS15_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS15_WIDTH=2
mlxconfig -d <device> s PCI_BUS15_SPEED=4
mlxconfig -d <device> s PCI_BUS16_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS16_WIDTH=2
mlxconfig -d <device> s PCI_BUS16_SPEED=4
mlxconfig -d <device> s PCI_BUS17_HIERARCHY_TYPE=2
mlxconfig -d <device> s PCI_BUS17_WIDTH=2
mlxconfig -d <device> s PCI_BUS17_SPEED=4
```


Downloaded from Arrow.com.

6 Setting High-Speed-Port Link Type

The following table lists the BlueField-3 supported speeds and the default networking port link type per OPN.

OPN	Data Transmission Rate	Default Protocol and Rate
900-9D3C6-00CV-GA0 900-9D3C6-00CV-DA0 900-9D3C6-00SV-DA0	InfiniBand: NDR200 200Gb/s Ethernet: 200GbE	Ethernet 200GbE

To configure the networking high-speed ports mode, you can either use the mlxconfig or the UEFI tools.

UEFI can configure the DPU device before the operating system is up, while mlxconfig configures the card once the operating system is up. According to your preference, use one of the below tools:

6.1 mlxconfig

The mlxconfig tool allows users to change device configurations without burning the firmware. The configuration is also kept after reset. By default, mlxconfig shows the configurations that will be loaded in the next boot. For more information and instructions, refer to Using mlxconfig to Set IB/ETH Parameters.

6.2 UEFI

PreBoot drivers initialize the adapter device, check the port protocol type – Ethernet or InfiniBand - and bring up the port. Then it connects to a DHCP server to obtain its assigned IP address and network parameters and obtain the source location of the kernel/OS to boot from. The DHCP server instructs the PreBoot drivers to access the kernel/OS through a TFTP server, an iSCSI target, or some other service. For more information and instructions, refer to UEFI.

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7 Troubleshooting

7.1 General Troubleshooting

Server unable to find the DPU	• Ensure that the DPU is placed correctly • Make sure the DPU slot and the DPU are compatible Install the DPU in a different PCI Express slot • Use the drivers that came with the DPU or download the latest • Make sure your motherboard has the latest BIOS • Try to reboot the server
The DPU no longer works	• Reseat the DPU in its slot or a different slot, if necessary • Try using another cable • Reinstall the drivers for the network driver files may be damaged or deleted • Reboot the server
DPUs stopped working after installing another DPU	• Try removing and re-installing all DPUs • Check that cables are connected properly • Make sure your motherboard has the latest BIOS
Link indicator light is off	• Try another port on the switch • Make sure the cable is securely attached • Check you are using the proper cables that do not exceed the recommended lengths • Verify that your switch and DPU port are compatible
Link light is on, but with no communication established	• Check that the latest driver is loaded • Check that the DPU and its link are set to the same speed, and duplex settings
Forgot password needed to install/upgrade the DPU image	Refer to the latest version of BlueField DPU SW Manual and follow the instructions under "Upgrading NVIDIA BlueField DPU Software" section.

Downloaded from Arrow.com.

8 Specifications

> The DPU Controller maximum power consumption does not exceed 150W and is split between the two power sources as follows:
> - Up to 66W from the PCIe golden fingers (12V)
> - The rest of the consumed power is drawn from the external PCIe power supply connector

8.1 900-9D3C6-00CV-GA0 / 900-9D3C6-00CV-DA0 / 900-9D3C6-00SV-DA0 Specifications

BlueField-3 IC	BlueField-3 E-Series - 16 Arm-Cores - 505MHz/2000MHz		
	Crypto Enabled with integrated BMC		
Physical	Single-Slot FHHL Card Dimensions: 111.15mm x 167.65mm Tall Bracket Dimensions: 121.0mm x 21.6mm 900-9D3C6-00CV-DA0 Only: Heatsink Dimensions (Length, Width, Height): 139.6mm x 92.7mm x 10.2mm		
Interfaces	See Supported Interfaces		
	PCI Express Interface	Gen 5.0 SERDES @ 32.0GT/s, 16 lanes (4.0, 3.0, 2.0 and 1.1 compatible)	
		Optional: Additional PCIe x16 Gen 5.0 @ SERDES 32GT/s through the PCIe auxiliary passive card and Cabline SA-II Plus harnesses	
	On-Board Memory	• Dual-channel with 20 DDR5 + ECC (128bit + 16bit ECC) for a total of 48GB @ 5200MT/s • 40GB pSLC eMMC memory + 128GB SSD	
	Networking Connector	Dual-port QSFP112 (copper and optical)	
Data Rate	InfiniBand	NDR200/HDR/HDR100/EDR/FDR/SDR	
	Ethernet (Default Speed)	200/100/50/25/10 Gb/s	
Protocol Support	InfiniBand: IBTA v1.5a Auto-Negotiation: NDR200 (2 lanes x 100Gb/s per lane) port, HDR (50Gb/s per lane) port, HDR100 (2 lane x 50Gb/s per lane), EDR (25Gb/s per lane) port, FDR (14.0625Gb/s per lane), 1X/2X/4X SDR (2.5Gb/s per lane).		
	Ethernet: 200GAUI-4 C2M, 200GAUI-2 C2M, 200GBASE-CR4, 100GAUI-2 C2M, 100GBASE-CR4, 100GBASE-CR2, 100GBASE-CR1, 50GAUI-2 C2M, 50GAUI-1 C2M, 50GBASE-CR, 50GBASE-R2 , 40GBASE-CR4, 40GBASE-R2, 25GBASE-R, 10GBASE-R, 10GBASE-CX4, 1000BASE-CX, CAUI-4 C2M, 25GAUI C2M, XLAUI C2M , XLPPI, SFI		
Electrical and Thermal Specifications	Voltage: 12V		
	Electrical and thermal specifications are provided in "*NVIDIA BlueField-3 DPUs and SuperNICs Electrical and Thermal Specifications*" document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.		
Environmental	Temperature	Operational	0°C to 55°C
		Non-operational	-40°C to 70°C[a]
	Humidity	Operational	10% to 85% relative humidity

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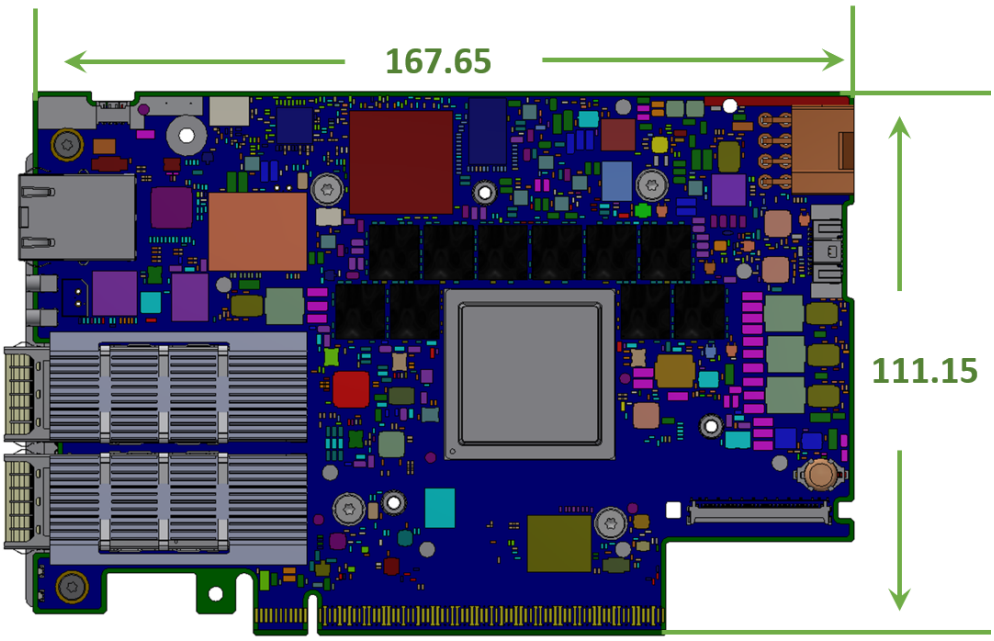
		Non-operational	10% to 90% relative humidity
	Altitude (Operational)	3050m	
Regulatory	Safety	CB / cTUVus / CE	
	EMC	CE / FCC / VCCI / ICES / RCM	
	RoHS	RoHS compliant	

a. The non-operational storage temperature specifications apply to the product without its package.

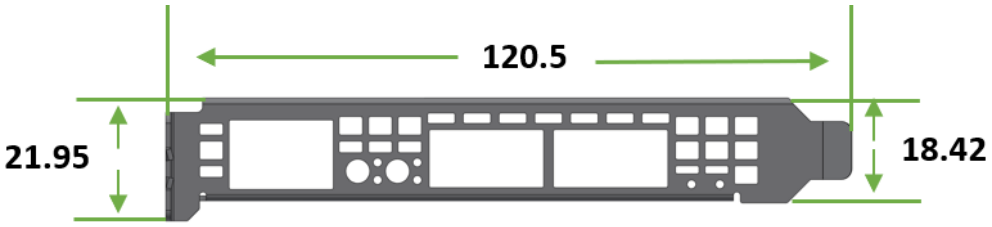
8.1.1 DPU Controller Mechanical Drawing and Dimensions

All dimensions are in millimeters. The PCB mechanical tolerance is +/- 0.13mm.

The diagrams may differ for different cards and are provided here for illustration purposes only.



8.1.1.1 Tall Bracket Mechanical Drawing and Dimensions



Downloaded from Arrow.com.

9 Monitoring

9.1 Thermal Sensors

The thermal threshold definitions are described in the "*NVIDIA BlueField-3 Networking Platforms Electrical and Thermal Specifications*" document. You can access the document either by logging into NVOnline or by contacting your NVIDIA representative.

9.2 Heatsink

> ⚠ This section applies to 900-9D3C6-00CV-DA0 only, 900-9D3C6-00CV-GA0 is shipped without a heatsink.

The heatsink is attached to the DPU by three screws to dissipate the heat from the IC.
The DPU IC has a thermal shutdown safety mechanism that automatically shuts down the DPU in cases of high-temperature events, improper thermal coupling, or heatsink removal.

Refer to the below table for heatsink details per card configuration. For the required airflow (LFM) per OPN, please refer to Specifications.

Maximum Dimensions
Length, Width, Height: 139.6mm x 92.7mm x 10.2mm

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10 Finding the GUID/MAC and Serial Number on the Card

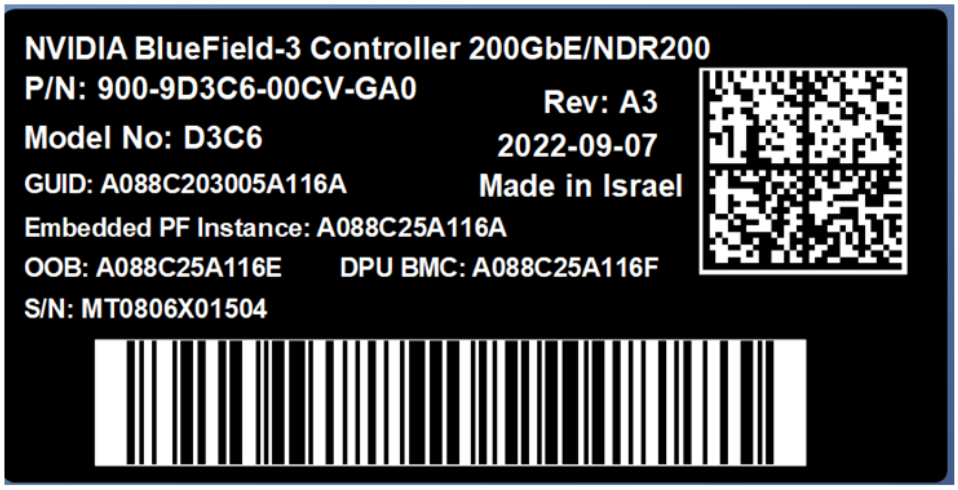
Each BlueField-3 platform is uniquely identified to facilitate efficient management and configuration. This section aims to guide you through identifying your BlueField-3 platform by using the information provided on the board label.

The board label includes unique identifiers essential for network communication—specifically, a primary GUID address for InfiniBand protocols or MAC addresses for Ethernet protocols. If your BlueField-3 board supports both InfiniBand and Ethernet protocols, the label will feature a primary GUID along with five 'base' MAC addresses derived from the GUID address: Host, ECPF, MPF, DPU BMC, and OOB.

Refer to the board label example and a table listing the different MAC addresses, offering examples and additional information to enhance clarity.

10.1 DPU Controller Board Label Example

Note: The product revisions ("Rev") indicated on the label do not necessarily represent the latest revisions of the cards.



Item on Label	Description	Example/Additional Information
GUID (Global Unique Identifier)	GUIDs is a unique 16 byte identifier of the BlueField in an InfiniBand network, the GUID never changes.	The GUID on the label is assigned to the **System GUID** of the BlueField HCA. The System GUID represents the HCA hardware with all its ports. Each HCA port is assigned a dedicated Node GUID. The **Node GUID** of **port 0** is equal to the System GUID. The **Node GUID** of **port 1** is equal to the System GUID+1

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Item on Label	Description	Example/Additional Information
HOST (Base MAC)	Represents the base MAC address for high-speed data port 0	DPUs with more than one high-speed port will use incremental (+1) MAC addresses against the base HOST MAC on the label. For instance: From the label - HOST: 94 6D AE F5 A1 CC **Port 0:** 94 6D AE F5 A1 CC (same as label) **Port 1:** 94 6D AE F5 A1 CD (+1 from base) **Port 2:** 94 6D AE F5 A1 CE (+2 from base) **Port 3:** 94 6D AE F5 A1 CF (+3 from base)
OOB (Out-of-Band)	OOB represents the MAC address of the 1GbE out-of-band management port of the DPU's embedded Arm system.	Network traffic for the "OOB" (DPU embedded Arm system) and "DPU BMC" traverse through the 1GbE RJ-45 connector located on the front panel of the DPU card.
DPU BMC (Baseboard Management Controller)	Represents the MAC address for the 1GbE OOB management port of the DPU BMC. Note: The base MAC address for DPU BMC is +1 from the OOB MAC address.	
S/N (Serial Number)	A unique serial number that distinguishes your DPU from others. The S/N is used for tracking and support purposes.	N/A

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11 PCIe Auxiliary Card Kit

Down Stream Port (DSP)

The self-hosted BlueField-3 DPU controllers with downstream port extension option integrate a single network adapter silicon on a primary board, and an auxiliary PCIe connection card and Cabline SA-II Plus Harness connecting the two. Utilizing the Down Stream Port (DSP) extension option, where the PCIe extension card is connected to the BlueField-3 DPU, used as a root complex for storage devices.

This enables direct access from each CPU to the network through its dedicated PCIe interface as the card's 32-lane PCIe bus is split into two 16-lane buses, with one bus accessible through a PCIe x16 edge connector and the other bus through an x16 Auxiliary PCIe Connection card. The two cards should be installed into two PCIe x16 slots and connected using two Cabline SA-II Plus harnesses.

The PCIe auxiliary kit can be purchased separately to allow downstream port extension. The table below lists the available PCIe auxiliary kit ordering part numbers, depending on the desired length of the Cabline SA-II Plus harnesses and the PCI Express interface, Gen 4.0 or Gen 5.0.

OPN	Description
930-9DAX5-0015-000	NVIDIA BlueField-3 Auxiliary Kit for additional self-hosted PCIe Gen **5.0/4.0** x16 connection, two 150mm Cabline SA-II Plus Harnesses
930-9DAX4-0035-000	NVIDIA BlueField-3 Auxiliary Kit for additional self-hosted PCIe Gen 4.0 x16 connection, two 350mm Cabline SA-II Plus Harnesses
930-9DHAR-0001-000	NVIDIA BlueField-3 150mm Gen **5.0** FRU harness, Cabline SA-II Plus 60-pin micro coax 38AWG

11.1 PCIe Auxiliary Card Package Contents

Category	Qty	Item
Cards	1	930-9DAX5-0015-000: PCIe x16 Gen 5.0/4.0 Auxiliary Connection Card 930-9DAX4-0035-000: PCIe x16 Gen 4.0 Auxiliary Connection Card
Harnesses	1	Cabline CA-II Plus harness (white) - Length according to kit OPN
	1	Cabline CA-II Plus harness (black) - Length according to kit OPN
Accessories	2	Retention Clip for Cabeline harness (shipped assembled on the harnesses - optional)
	1	PCIe Auxiliary card short bracket
	1	PCIe Auxiliary card tall bracket (shipped assembled on the Auxiliary card)

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11.2 Channel Insertion Loss

Channel insertion loss is the loss of signal power resulting from the insertion of a device in a transmission line or optical fiber and is usually expressed in decibels (dB).

The following table describes the BlueField-3 DPU channel insertion loss budget for PCIe Gen 5.0 architecture (32 GT/s).

The total PCIe channel insertion loss approved by PCI-SIG Gen5.0 spec is 36dB @16GHz.

The total BlueField-3 DPU board insertion loss of the PCIe lanes (PCORE1) routed to the Cabline CA-II Plus is 6dB (@16GHz).

The Passive PCIe Auxiliary Card Loss is 1.5dB (@16Ghz).

The Cabline CA-II Plus harness loss at 16GHz:

Harness Length	Channel Loss at Gen 5.0
15cm	3.8dB
35cm	7.6dB
55cm	11.4dB

The above is measured data; it is recommended to add 0.5dB margins for your system (some loss variations are possible).

The Cabline CA-II Plus harnesses loss = 0.24dB/cm for Gen 5.0.

The above loss includes the Cabline CA-II Plus harnesses and connectors on both sides.

The PCI-SIG Gen5 SPEC also defines the total loss for AIC (bump to Golden-Fingers) to be 9.5dB @16Ghz.

The BlueField-3 AIC, together with a 15cm Cabline CA-II Plus harnesses and the Passive PCIe Auxiliary Card loss is: 3dB+2dB+3.8dB+1.5dB=10.3dB > 9.5dB

11.3 Cabline CA-II Plus Harness Pinouts

11.3.1 Cabline CA-II Plus Harness - Component Side

Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
1	GND	GND BAR			1

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
2	PCIE_REFCLK1_P	Micro coax	Primary PCIe clock from the motherboard to the Network Adapter Main card, to be used for the x16 Cabline harness PCIe interface. This clock must meet all the PCIe SIG spec requirements. It should be driven from the motherboard side.	38	2
3	PCIE_REFCLK1_N	Micro coax	Primary PCIe clock from the motherboard to the Network Adapter Main card, to be used for the x16 Cabline harness PCIe interface. This clock must meet all the PCIe SIG spec requirements. It should be driven from the motherboard side.	38	3
4	GND	GND BAR			4
5	PCIE_CPU_CX_15N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	5
6	PCIE_CPU_CX_15P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	6
7	GND	GND BAR			7
8	PCIE_CPU_CX_14N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	8

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
9	PCIE_CPU_CX_14P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	9
10	GND	GND BAR			10
11	PCIE_CPU_CX_13N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	11
12	PCIE_CPU_CX_13P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	12
13	GND	GND BAR			13
14	PCIE_CPU_CX_12N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	14
15	PCIE_CPU_CX_12P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	15
16	GND	GND BAR			16
17	PCIE_CPU_CX_11N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	17
18	PCIE_CPU_CX_11P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	18

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
19	GND	GND BAR			19
20	PCIE_CPU_CX_10N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	20
21	PCIE_CPU_CX_10P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	21
22	GND	GND BAR			22
23	PCIE_CPU_CX_9N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	23
24	PCIE_CPU_CX_9P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	24
25	GND	GND BAR			25
26	PCIE_CPU_CX_8N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	26
27	PCIE_CPU_CX_8P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	27
28	GND	GND BAR			28

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
29	PCIE_CPU_CX_7N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	29
30	PCIE_CPU_CX_7P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	30
31	GND	GND BAR			31
32	PCIE_CPU_CX_6N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	32
33	PCIE_CPU_CX_6P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	33
34	GND	GND BAR			34
35	PCIE_CPU_CX_5N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	35
36	PCIE_CPU_CX_5P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	36
37	GND	GND BAR			37
38	PCIE_CPU_CX_4N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	38

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
39	PCIE_CPU_CX_4P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	39
40	GND	GND BAR			40
41	PCIE_CPU_CX_3N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	41
42	PCIE_CPU_CX_3P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	42
43	GND	GND BAR			43
44	PCIE_CPU_CX_2N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	44
45	PCIE_CPU_CX_2P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	45
46	GND	GND BAR			46
47	PCIE_CPU_CX_1N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	47
48	PCIE_CPU_CX_1P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	48

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
49	GND	GND BAR			49
50	PCIE_CPU_CX_0N	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	50
51	PCIE_CPU_CX_0P	Micro coax	Connect from the Black Cabline CA-II Plus cable through 220nF capacitors to the x16 PCIe Tx lanes of the CPU/ GPU/End-Point	38	51
52	GND	GND BAR			52
53	No wire	Micro coax		38	53
54	No wire	Micro coax		38	54
55	Reserved_01	Micro coax		38	55
56	No wire	Micro coax		38	56
57	I2C_AUX_SCL	Micro coax	The ConnectX-7 silicon serves as the I2C bus master on this bus. An I2C EEPROM at I2C address 0x57 needs to be mounted on the motherboard side to report to the Cabline CA-II Plus interface parameters to the main-card network adapter silicon, like Cabline CA-II Plus cables length (contact NVIDIA for the format of this EEPROM). If additional optional I2C slave devices need to be managed by the main-card network adapter silicon, they need to be included on this I2C bus as well.	38	57

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Pin#	Signal Name	Wire Type	Detailed Description	AWG#	Pin# on the other end
58	I2C_AUX_SDA	Micro coax	The ConnectX-7 silicon serves as the I2C bus master on this bus. An I2C EEPROM at I2C address 0x57 needs to be mounted on the motherboard side to report to the Cabline CA-II Plus interface parameters to the main-card network adapter silicon, like Cabline CA-II Plus cables length (contact NVIDIA for the format of this EEPROM). If additional optional I2C slave devices need to be managed by the main-card network adapter silicon, they need to be included on this I2C bus as well.	38	58
59	S_PRSNT1_L	Micro coax	Connect this pin to GND No wires are connected to these pins to ensure they do not interfere with the operation of S_PRSNT2_L for the detection when the two Cabline harnesses are installed.	38	59
60		No Wire			60

11.3.2 Cabline CA-II Plus Harness - Print Side

Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
1	No wire	Micro coax	38		1
2	No wire	Micro coax	38		2
3	No wire	Micro coax	38		3
4	No wire	Micro coax	38		4

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
5	No wire	Micro coax	38		5
6	Reserved_06	Micro coax	38		6
7	Reserved_07	Micro coax	38	Reserved for future expansion	7
8	Reserved_08	Micro coax	38	Reserved for future expansion	8
9	GND	GND BAR			9
10	PCIE_CX_CPU_0P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	10
11	PCIE_CX_CPU_0N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	11
12	GND	GND BAR			12
13	PCIE_CX_CPU_1P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	13
14	PCIE_CX_CPU_1N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	14
15	GND	GND BAR			15

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
16	PCIE_CX_CPU_2P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	16
17	PCIE_CX_CPU_2N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	17
18	GND	GND BAR			18
19	PCIE_CX_CPU_3P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	19
20	PCIE_CX_CPU_3N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	20
21	GND	GND BAR			21
22	PCIE_CX_CPU_4P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	22

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
23	PCIE_CX_CPU_4N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	23
24	GND	GND BAR			24
25	PCIE_CX_CPU_5P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	25
26	PCIE_CX_CPU_5N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	26
27	GND	GND BAR			27
28	PCIE_CX_CPU_6P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	28
29	PCIE_CX_CPU_6N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	29
30	GND	GND BAR			30

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
31	PCIE_X_CPU_7P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	31
32	PCIE_CX_CPU_7N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	32
33	GND	GND BAR			33
34	PCIE_CX_CPU_8P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	34
35	PCIE_CX_CPU_8N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	35
36	GND	GND BAR			36
37	PCIE_CX_CPU_9P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	37

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
38	PCIE_CX_CPU_9N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	38
39	GND	GND BAR			39
40	PCIE_CX_CPU_10P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	40
41	PCIE_CX_CPU_10N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	41
42	GND	GND BAR			42
43	PCIE_CX_CPU_11P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	43
44	PCIE_CX_CPU_11N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	44
45	GND	GND BAR			45

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
46	PCIE_CX_CPU_12P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	46
47	PCIE_CX_CPU_12N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	47
48	GND	GND BAR			48
49	PCIE_CX_CPU_13P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	49
50	PCIE_CX_CPU_13N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	50
51	GND	GND BAR			51
52	PCIE_CX_CPU_14P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	52

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
53	PCIE_CX_CPU_14N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	53
54	GND	GND BAR			54
55	PCIE_CX_CPU_15P	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	55
56	PCIE_CX_CPU_15N	Micro coax	38	Connect from the White Cabline CA-II Plus harness to the PCIe x16 Rx lanes of the CPU/GPU/End-Point. 220nF caps are required on this signal on the ConnectX-7 card.	56
57	GND	GND BAR			57

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
58	S_PERST1_CONN_L	Micro coax	38	PCIe compliant PERST_L (active low PCI Reset) signal for the PCIe Cabline CA-II Plus Connectors. The direction of this PERST_L signal depends on the implementation: When connecting a CPU root complex to the PCIe Cabline CA-II Plus interface, this signal is driven from the motherboard side (from the CPU), to the network adapter. When connecting a GPU or an end point to the PCIe Cabline CA-II Plus interface, this signal is driven from the network adapter side (which operates as a PCIe switch in this case), to the GPU or end-point on the motherboard side.	58
59	No wire	No Wire			59

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Pin#	Signal Name	Wire Type	AWG#	Detailed Description	Pin# on the other end
60	S_PRSNT2_L	Micro coax	38	Connect to a 4.7K pull-up resistor to 3.3V on the motherboard side, to detect if both the Cabline harnesses are connected or not. This signal is connected to S_PRSNT1_L on the network adapter main card. In the motherboard side, read logic low if both Cabline harnesses are connected. Read logic 1 (3.3V) if one or both the Cabline harnesses are not connected. No wires are connected to these pins to ensure they do not interfere with the operation of S_PRSNT1_L for the detection when the two Cabline harnesses are installed.	60

11.4 Technical Specifications

Physical	PCIe Auxiliary Card Size: 5.09 in. x 2.32 in. (129.30mm x 59.00mm) Two Cabline CA-II Plus harnesses (white and black) Length: 15, 25 or 35cm		
Power Consumption	**Voltage**: 12V, 3.3V_AUX **Maximum current:** 100mA for the 3.3V_AUX voltage rail		
PCIe Connectivity	930-9DAX5-0015-000	PCI Express Gen 5.0/4.0: SERDES @ 16/32 GT/s, x16 lanes (Gen 3.0 compatible)	
	930-9DAX4-0035-000	PCI Express Gen 4.0: SERDES @ 16GT/s, x16 lanes (Gen 3.0 compatible)	
Environmental	**Temperature**	**Operational**	0°C to 55°C
		Non-operational	-40°C to 70°C
	Humidity	**Operational**	10% to 85% relative humidity
		Non-operational	10% to 90% relative humidity
	Altitude (Operational)	3050m	
Regulatory	**Safety**: CB / cTUVus / CE		
	EMC: CE / FCC / VCCI / ICES / RCM / KC		

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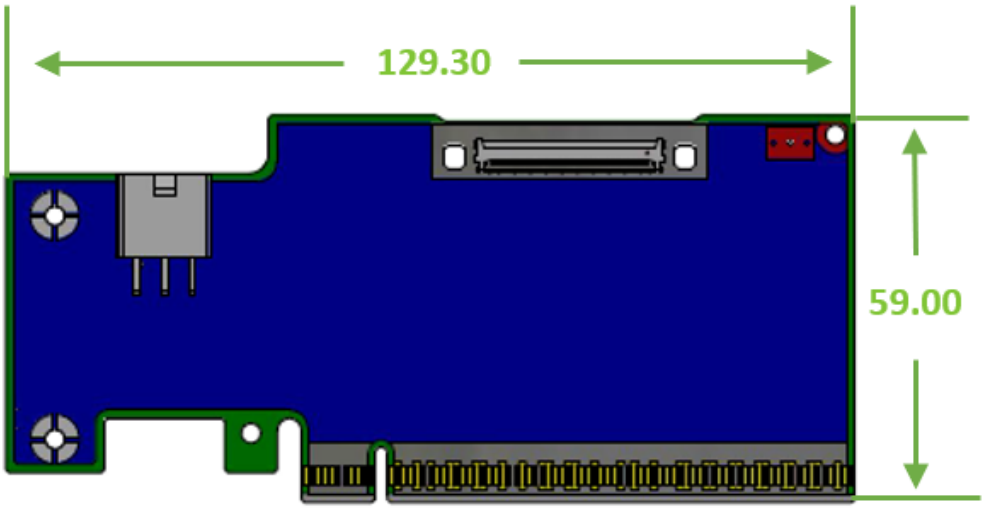
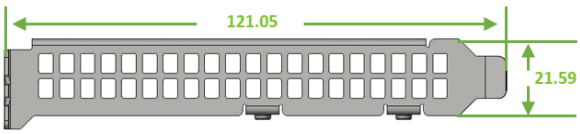
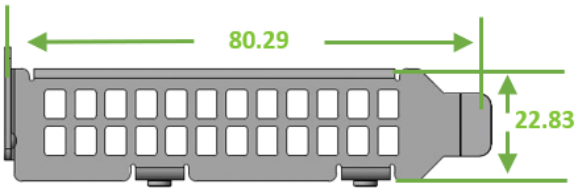
Physical	PCIe Auxiliary Card Size: 5.09 in. x 2.32 in. (129.30mm x 59.00mm) Two Cabline CA-II Plus harnesses (white and black) Length: 15, 25 or 35cm
Power Consumption	**Voltage**: 12V, 3.3V_AUX **Maximum current:** 100mA for the 3.3V_AUX voltage rail
	RoHS: RoHS Compliant

11.4.1 PCIe Auxiliary Card Mechanical Drawings and Dimensions

All dimensions are in millimeters. The PCB mechanical tolerance is +/- 0.13mm.



11.4.2 Bracket Mechanical Drawings and Dimensions

Auxiliary PCIe Connection Card Tall Bracket	Auxiliary PCIe Connection Card Short Bracket
	

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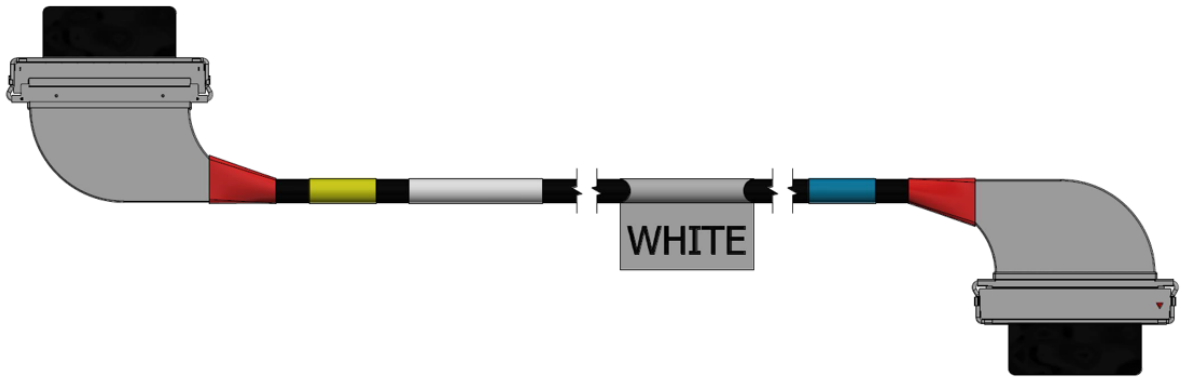
11.4.3 Cabline CA-II Plus Harnesses Mechanical Drawing



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12 Cables and Cabling Configurations

12.1 RJ45 Cable for the 1GbE OOB Management Interface

12.2 USB Interface Cabling

Debugging and loading new versions of the operating systems and firmware requires the use of Type A to Type B USB 2.0 Cable. The following figure shows an example of Type A to Type V USB Cable.

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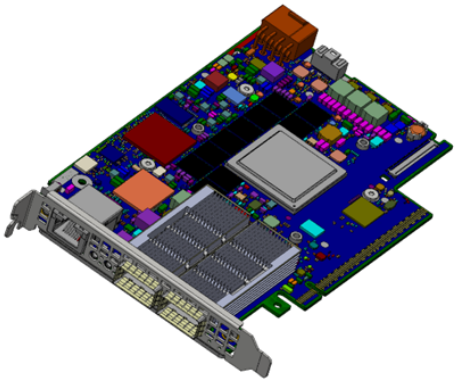
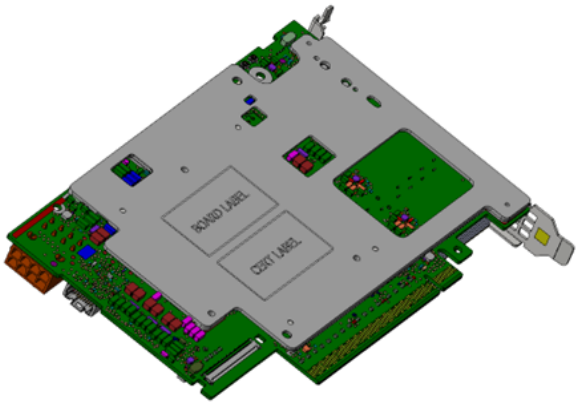
13 General Cooling Recommendations for Heatsink-less DPU Controllers

This section offers general cooling recommendations to NVIDIA customers who have acquired a heatsink-less DPU Controller (OPN: 900-9D3C6-00CV-GA0).

IMPORTANT NOTES:

1. The customer holds exclusive responsibility for the thermal design and for ensuring all board components never exceed their designated thermal operating limits.
2. The recommendations provided in this section are based on an air-cooled thermal design.
3. If the customer's environment has low or no airflow (e.g., liquid cooling) where the DPU Controller is to be installed, the customer must ensure proper cooling for all the other board components that are not covered by the recommendations of this chapter or in the product's thermal model. The customer must guarantee those components do not exceed their thermal operating limits as well.

Isometric view of the heatsink-less DPU Controller:

Component Side	Print Side (with Stiffener)
	

13.1 General Notes

1. The Thermal Transfer Plate (TTP) may encompass an internal liquid cooling system within a cold plate.
2. The M3 screws maximum protrusion length according to stiffener thread depth is listed in Mechanical Interfaces.
3. Recommended torque values: M3: 0.35~0.4 Nm. Use a locking mechanism.
4. To ensure unobstructed access for replacement, ensure that the battery is not blocked. Refer to Encapsulation and Battery on SFG.

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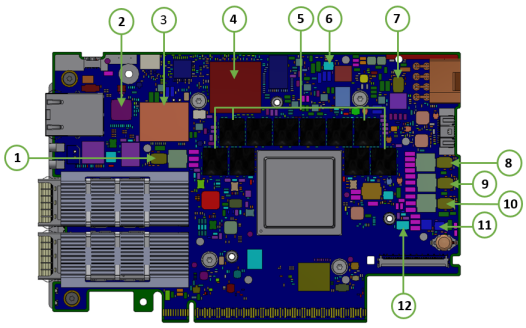
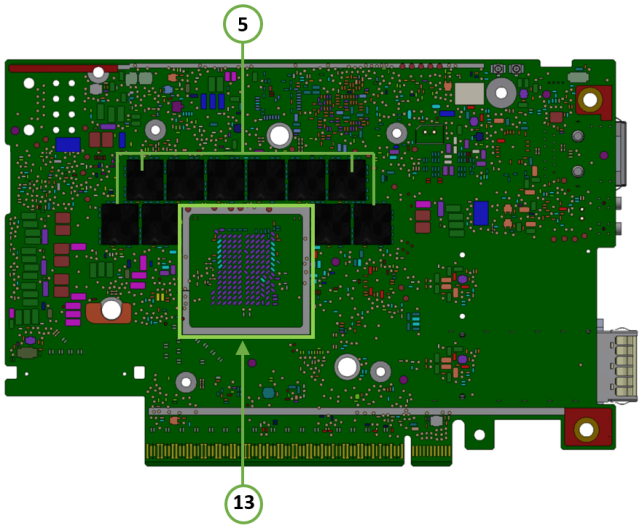
5. When considering encapsulation, ensure there is no interference with the TTP. The encapsulation is presented as the maximum tolerance on the SFG and is labeled with ENC. Refer to Encapsulation and Battery on SFG.

13.2 Components that Require Cooling

It is the responsibility of the customer to ensure proper cooling and thermal regulation for all components on the board. The provided guidelines are minimal and are based on NVIDIA's air-cooling thermal solution. Note the following:

- The DPU controller SoC require contact with TTP on the component side of the product.
- Within the air-cooled thermal solution, the cooling of components on the print side of the DPU controller is achieved via attachment to the board's bottom stiffener with the thermal interface material. See example in the board print side isometric view above.
- The battery's thermal limitation is the maximum ambient temperature of 60°C.
- The acceptable pressure on the SoC adheres to the following specifications:
    - 35 psi (SoC area 761.5 mm^2).
    - The center force should be applied at the center of the SoC.

Component Side	Print Side (without Stiffener)
	

Item #	Board Components
1	U63
2	U44
3	M1394
4	U99
5	M111-M115, M221-M225, M331-M335, M441-M445
6	U30
7	U66
8	U62

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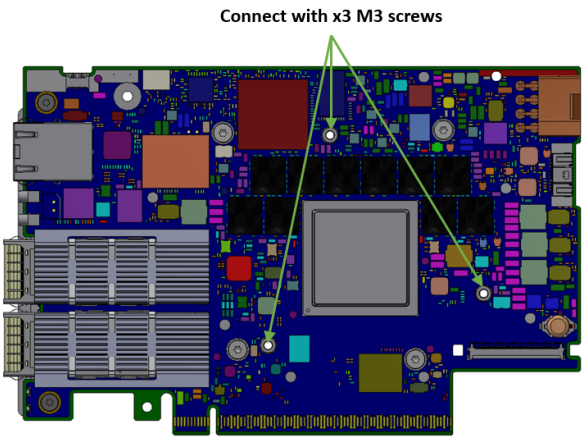
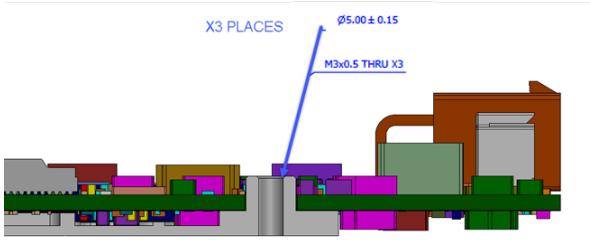
Item #	Board Components
9	U64
10	U65
11	U32
12	U33
13	See marked square

13.2.1 Mechanical Interfaces

The following figure lists the mechanical interfaces of the DPU controller.

Mechanical Interface	
	

13.2.2 Encapsulation and Battery on SFG

Ensure that the battery remains unobstructed to allow access for replacement. Furthermore, avoid any interference with the TTP. Note that the encapsulation is depicted as the maximum tolerance in the SFG and is labeled as ENC.

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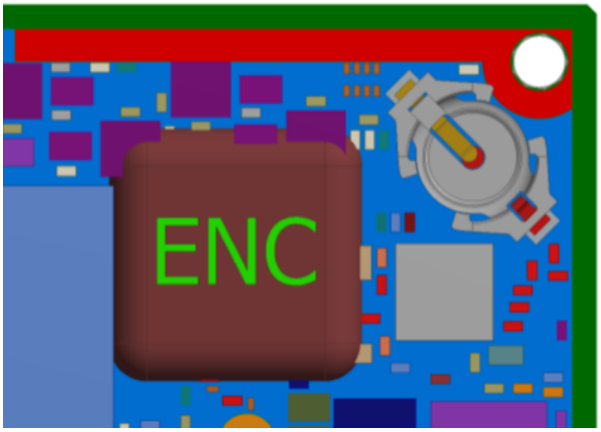

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14 Document Revision History

Date	Comments/Changes
Aug. 2024	Added support for the 900-9D3C6-00SV-DA0 Storage Controller
Apr. 2024	• Removed the "Securing Workloads" feature from Features and Benefits • Updated the important notes and warnings in External PCIe Power Supply Connector • Added 8-pin ATX Power Supply Cable installation instructions • Updated Cabline CA-II Plus Harness Pinouts • Updated PCIe Auxiliary Card Kit • Added notes across the document stating that the Socket-Direct functionality is currently not supported by firmware
Nov. 2023	• Updated PCIe Auxiliary Card Kit
Oct. 2023	• Updated NVMe SSD Interface • Updated DPU Power-Up and Power-Down Instructions
Aug. 2023	• Added General Cooling Recommendations for Heatsink-less DPU Controllers • Updated Cabline CA-II Plus Connectors Pinouts. • Added a note to NVMe SSD Interface.
May. 2023	First release

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