# Synchronous Buck PWM Switcher - Integrated FETs

## 6 A

# NCP1592

NCP1592 is a low input voltage 6 A synchronous buck converter that integrates both 30 mΩ high side and low side MOSFETs. NCP1592 is designed for space sensitive and high efficiency applications. The main features include: a high performance voltage error amplifier; an under−voltage−lockout circuit to prevent start−up until the input voltage reaches 3 V; an internally or externally programmable soft−start circuit to limit inrush currents; and a power good output monitor signal. NCP1592 is available in thermally enhanced 28−pin TSSOP package.

### Features

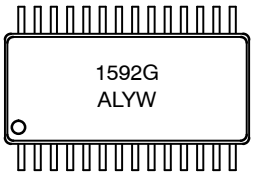
- 30 mΩ, 12 A Peak MOSFET Switches for High to Efficiency at 6 A Continuous Output Source or Sink Current
- Adjustable Output Voltage Down to 0.891 V With 1.0% Accuracy
- Wide PWM Frequency: Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz
- Synchronizable to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Component Count
- This is a Pb−Free Device

### Application

- Low−Voltage, High−Density Distributed Power Systems
- High Performance Point of Load Regulation for DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure
- Portable Computing/Notebook PCs

TSSOP−28 EP
CASE 948BG

**MARKING DIAGRAM**




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

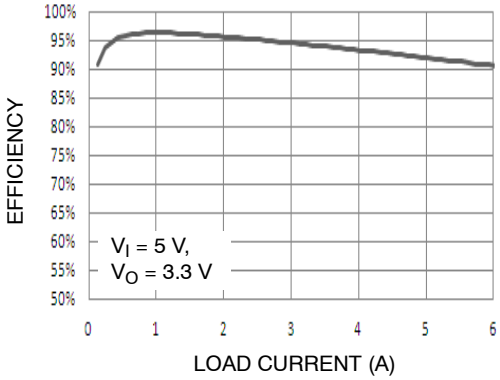



**Figure 1. Efficiency at 350 kHz**

### ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

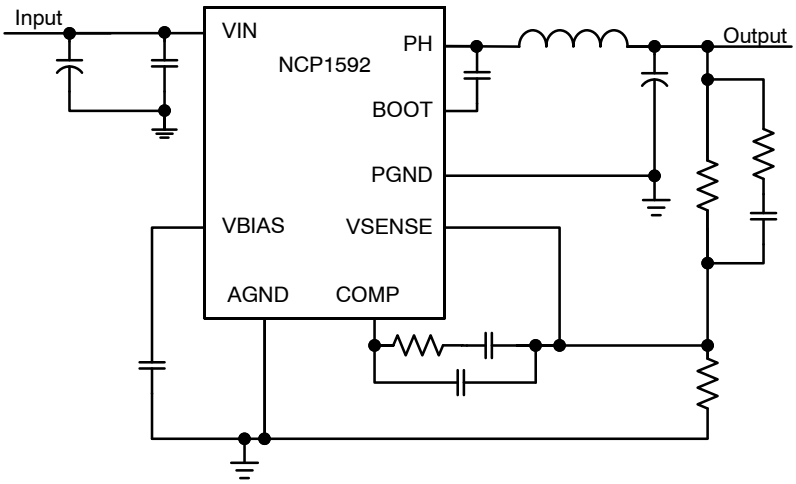



**Figure 2. Typical Application Circuit**

© Semiconductor Components Industries, LLC, 2014


Downloaded from Arrow.com.

## BLOCK DIAGRAM

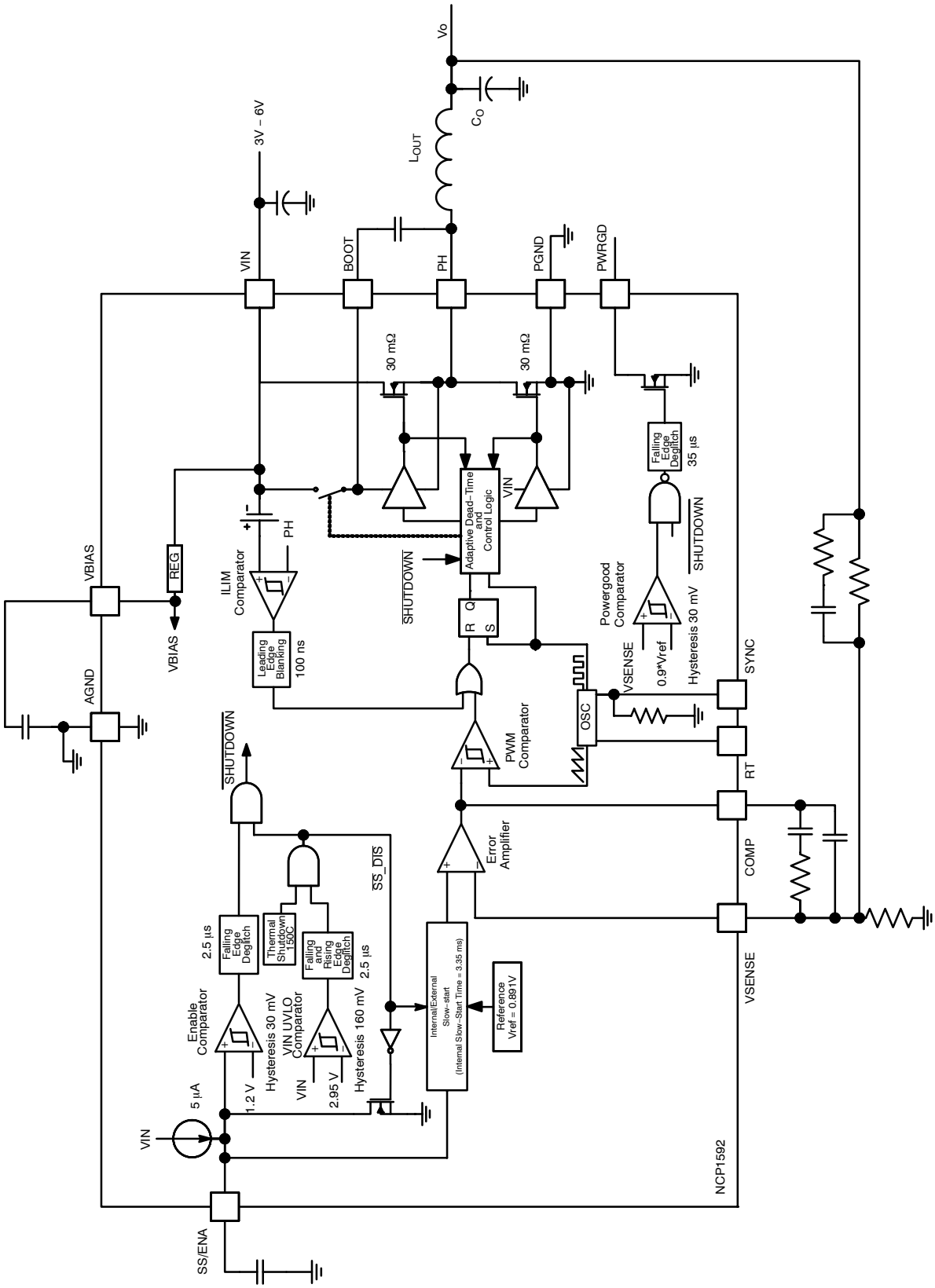



**Figure 3. Typical Application Circuit**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

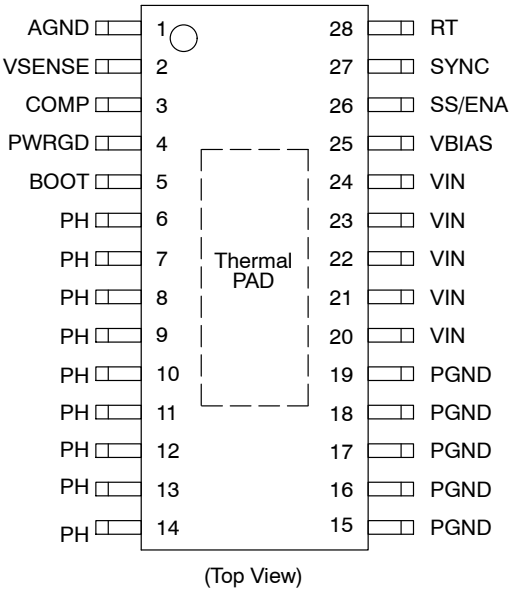



**Figure 4. Pin Connections**

## PIN DESCRIPTION

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | AGND | Analog ground. Return for compensation network/output divider, slow−start capacitor. VBIAS capacitor, RT resistor, and SYNC pin. Connect PowerPAD to AGND. |
| 2 | VSENSE | Error amplifier inverting input. Connect to output voltage through compensation network/output divider. |
| 3 | COMP | Error amplifier output. Connect frequency compensation network from COMP to VSENSE. |
| 4 | PWRGD | Power good open drain output. High when VSENSE ≥ 90% $V_{ref}$ otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active. |
| 5 | BOOT | Bootstrap output. 0.022 μF ~ 0.1 μF ceramic capacitor is recommended to connect between BOOT and PH generates floating drive for the high−side FET drive. |
| 6 ~ 14 | PH | Phase output. Junction of the internal high−side and low−side power MOSFETs, and output inductor. |
| 15 ~ 19 | PGND | Power ground. High current return for the low−side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended. |
| 20 ~ 24 | VIN | Input supply for the power MOSFET switches and internal bias regulator . Bypass VIN pins to PGND with X5R or higher quality 10 μF ceramic capacitors. |
| 25 | VBIAS | Internal bias voltage output. 0.1 μF ~ 1.0 μF low ESR ceramic capacitor is recommended to connect between VBIAS to AGND. |
| 26 | SS/ENA | Soft start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start−up time. |
| 27 | SYNC | Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin. |
| 28 | RT | Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the SYNC pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency. |



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

**MAXIMUM RATINGS** Over operating free−air temperature range unless otherwise noted

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Main supply voltage input | $V_{IN}$ | −0.3 | 7 | V |
| Soft start and enable voltage | SS / ENA | −0.3 | 7 | V |
| Synchronization voltage | SYNC | −0.3 | 7 | V |
| Frequency setting voltage | RT | −0.3 | 6 | V |
| Output divided voltage sense | VSENSE | −0.3 | 4 | V |
| High side drive supply voltage | BOOT | −0.3 | PH+7 | V |
| Output voltage range | VBIAS | −0.3 | 7 | V |
| Compensation Voltage | COMP | −0.3 | 7 | V |
| Power Good open collector voltage | PWRGD | −0.3 | 7 | V |
| Power Switching Node Transient voltage excursion | PH (Note 4) | −3 | 10 | V |
| Power Switching Node Source current | PH | Internally Limited | | A |
| Compensation Source current | COMP | 0 | 6 | mA |
| Regulated voltage Source current | VBIAS | 0 | 6 | mA |
| Power Switching node sink current | PH | 0 | 12 | A |
| Compensation Sink current | COMP | 0 | 6 | mA |
| Soft start and enable Sink current | SS/ENA | 0 | 10 | mA |
| Power Good open collector Sink current | PWRGD | 0 | 10 | mA |
| Voltage differential | AGND to PGND | −0.3 | 0.3 | V |
| Operating Junction Temperature Range (Note 1) | $T_J$ | −40 | 150 | °C |
| Operating Ambient Temperature Range | $T_A$ | −40 | 85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 | 150 | °C |
| Thermal Characteristics (Note 2)<br>TSSOP 28−pin EP Plastic Package<br>Maximum Power Dissipation @ $T_A$ = 25°C<br>Thermal Resistance Junction−to−Air with Solder<br>Thermal Resistance Junction−to−Air without Solder | <br><br>$P_D$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br><br>5.49<br>18.2<br>40.5 | | <br><br>W<br>°C/W<br>°C/W |
| Lead Temperature Soldering (10 sec):<br>Reflow (SMD styles only) Pb−Free (Note 3) | RF | 260 peak | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 1: The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. The value of θJA is measured with the device mounted on a 3in x 3in, 4 layer, 0.062 inch FR−4 board with 1.5 oz. copper on the top and bottom layers and 0.5 ounce copper on the inner layers, in a still air environment with $T_A$ = 25°C. The PCB part layout had 12 thermal vias (see Recommended Land Pattern in applications section of this data sheet
3. 60−180 seconds minimum above 237°C.
4. 10 V transients allowed for , 10 ns.

**RECOMMENDED OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input voltage | $V_I$ | 3 | | 6 | V |
| Operating junction temperature | $T_J$ | −40 | | 125 | °C |



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

**ELECTRICAL CHARACTERISTICS** Over operating free−air temperature range unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | MAX | Unit |
|---|---|---|---|---|---|---|
| **Power Supply, VIN** | | | | | | |
| VIN Operation Voltage | $V_{IN}$ | | 3 | | 6 | V |
| Quiescent Current | $I_{(QSW\ 350)}$ | Fs = 350 kHz, SYNC ≤ 0.8 V, RT open, PH pin open | 3.5 | | 11.2 | mA |
| | $I_{(QSW\ 550)}$ | Fs = 550 kHz, SYNC ≥ 2.5 V, RT open, PH pin open | 4.0 | | 16 | mA |
| | $I_{(QSD)}$ | Shutdown, SS / ENA = 0 V | | 1 | 1.4 | mA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| Start Threshold | UVLOR | | | 2.95 | 3.0 | V |
| Stop Threshold | UVLOF | | 2.7 | 2.8 | | V |
| UVLO Hysteresis | UVLOHYST | | 110 | 160 | | mV |
| Rising and falling edge deglitch (Note 5) | UVLORTD | | | 2.5 | | μs |
| **BIAS VOLTAGE** | | | | | | |
| Output Voltage | $V_{bias}$ | $I_{Vbias}$ = 0 | 2.7 | 2.8 | 2.90 | V |
| Output Current (Note 6) | $I_{Vbias}$ | | | | 100 | μA |
| **CUMULATIVE REFERENCE** | | | | | | |
| Reference Voltage Accuracy | $V_{ref}$ | | 0.882 | 0.891 | 0.900 | V |
| **REGULATION** | | | | | | |
| Line regulation (Notes 6 and 7) | | $I_L$ = 3 A, $F_s$ = 350 kHz, $T_J$ = 85°C | | | 0.04 | %/V |
| | | $I_L$ = 3 A, $F_s$ = 550 kHz, $T_J$ = 85°C | | | 0.04 | |
| Load regulation (Notes 5 and 7) | | $I_L$ = 0 A to 6 A, $F_s$ = 350 kHz, TJ = 85°C | | | 0.03 | %/A |
| | | $I_L$ = 0 A to 6 A, $f_s$ = 550 kHz, $T_J$ = 85°C | | | 0.03 | |
| **OSCILLATOR** | | | | | | |
| Internally set | FREQSYNC_LOW | SYNC ≤ 0.8 V, RT open | 280 | 350 | 420 | kHz |
| | FREQ_HIGH | SYNC ≥ 2.5 V, RT open | 440 | 550 | 660 | |
| Externally set | FREQ180RT | RT = 180 kΩ (1% resistor to AGND) (Note 5) | 252 | 280 | 308 | kHz |
| | FREQ100RT | RT = 100 kΩ (1% resistor to AGND) | 460 | 500 | 540 | |
| | FREQ68RT | RT = 68 kΩ (1% resistor to AGND) (Note 5) | 663 | 700 | 762 | |
| High level threshold | SYNCH | | 2.5 | | | V |
| Low level threshold | SYNCL | | | | 0.8 | V |
| External synchronization pulse duration (Note 5) | SYNCMIN | | 50 | | | ns |
| Frequency range (Note 5) | SYNCFREQ | | 330 | | 700 | kHz |
| Ramp valley (Note 5) | RAMP_Bot | | | 0.441 | | V |
| Peak−to−peak ramp amplitude (Note 5) | RAMP_AMP | | | 1 | | V |

5. Guaranteed by design.
6. Static resistive loads only.
7. Specified by the circuit used in Figure 14.
8. Matched MOSFETs low−side $R_{DS(on)}$ production tested, high−side $R_{DS(on)}$ specified by design.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

**ELECTRICAL CHARACTERISTICS** Over operating free−air temperature range unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | MAX | Unit |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| Minimum controllable on time (Note 5) | MIN_COT | | | | 200 | ns |
| Maximum duty cycle | DMAX | | 90% | | | |
| **ERROR AMPLIFIER** | | | | | | |
| Open loop voltage gain | OLG | 1 kΩ COMP to AGND (Note 5) | 90 | 110 | | dB |
| Unity gain bandwidth | UGBW | Parallel 10 kΩ, 160 pF COMP to AGND (Note 5) | 3 | 5 | | MHz |
| Common mode input voltage range | CMIVR | Powered by internal LDO (Note 5) | 0 | | $V_{BIAS}$ | V |
| Input bias current | IVSENSE | VSENSE = $V_{ref}$ | | 60 | 250 | nA |
| Output voltage slew rate (Positives) | EASRP | | 3.0 | 4.5 | | V/μs |
| Output voltage slew rate (Negatives) | EASRN | | 2.07 | 3.0 | | V/μs |
| **PWM COMPARATOR** | | | | | | |
| PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime) | COMPDLY | 10 mV overdrive (Note 5) | | 70 | 85 | ns |
| **SLOW−START/ENABLE** | | | | | | |
| Enable threshold voltage | ENTH | | 0.82 | 1.20 | 1.40 | V |
| Enable hysteresis voltage | ENHYS | | | 0.03 | | V |
| Falling edge deglitch (Note 5) | EN_DLY | | | 2.5 | | μs |
| Internal soft−start time | SSI | | 2.18 | 3.35 | 4.1 | ms |
| Charge current | EN_ICH | SS/ENA = 0 V | 3 | 5 | 8 | μA |
| Discharge current | EN_IDSCH | SS/ENA = 1.2 V, $V_I$ = 2.7 V | 2.3 | 3.1 | 5.4 | mA |
| **POWER GOOD** | | | | | | |
| Power good threshold voltage | | VSENSE falling | | 90 | | %$V_{ref}$ |
| Power good hysteresis voltage (Note 5) | | | | 3 | | %$V_{ref}$ |
| Power good falling edge deglitch (Note 5) | | | | 39 | | μs |
| Output saturation voltage | PWRGD | $I_{(sink)}$ = 2.5 mA | | 166 | 225 | mV |
| Leakage current | PWRGD | $V_I$ = 5.5 V | | | 3 | μA |
| **CURRENT LIMIT** | | | | | | |
| Current limit trip point | | $V_I$ = 3 V, output shorted (Note 5) | 7.2 | 10 | | A |
| | | $V_I$ = 6 V, Output shorted (Note 5) | 10 | 12 | | |
| Current limit leading edge blanking time (Note 5) | | | | 100 | | ns |
| Current limit total response time (Note 5) | | | | 200 | | ns |

5. Guaranteed by design.
6. Static resistive loads only.
7. Specified by the circuit used in Figure 14.
8. Matched MOSFETs low−side $R_{DS(on)}$ production tested, high−side $R_{DS(on)}$ specified by design.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

**ELECTRICAL CHARACTERISTICS** Over operating free−air temperature range unless otherwise noted

| Parameter | Symbol | Test Conditions | Min | Typ | MAX | Unit |
|---|---|---|---|---|---|---|
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal shutdown trip point (Note 5) | | | 135 | 150 | 165 | °C |
| Hysteresis (Note 5) | | | | 10 | | |
| **OUTPUT POWER MOSFETs** | | | | | | |
| Power MOSFETs $R_{DS(on)}$ High Side | | $V_I$ = 6 V (Note 8) | | 26 | 47 | mΩ |
| | | $V_I$ = 3 V (Note 8) | | 30 | 61 | mΩ |

5. Guaranteed by design.
6. Static resistive loads only.
7. Specified by the circuit used in Figure 14.
8. Matched MOSFETs low−side $R_{DS(on)}$ production tested, high−side $R_{DS(on)}$ specified by design.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## TYPICAL CHARACTERISTICS

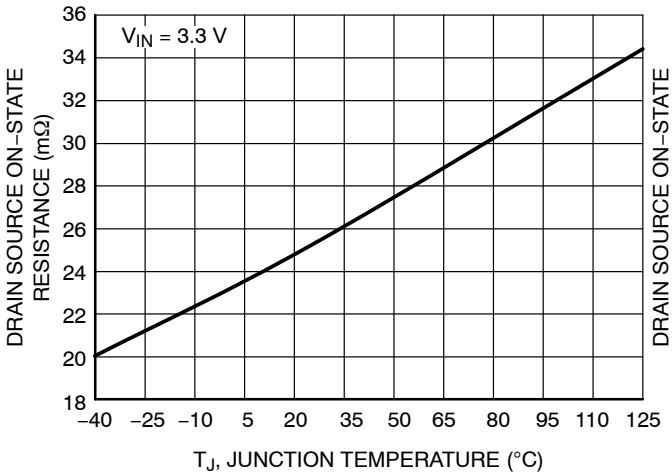



**Figure 5. Drain−Source ON−State Resistance vs Junction Temperature**

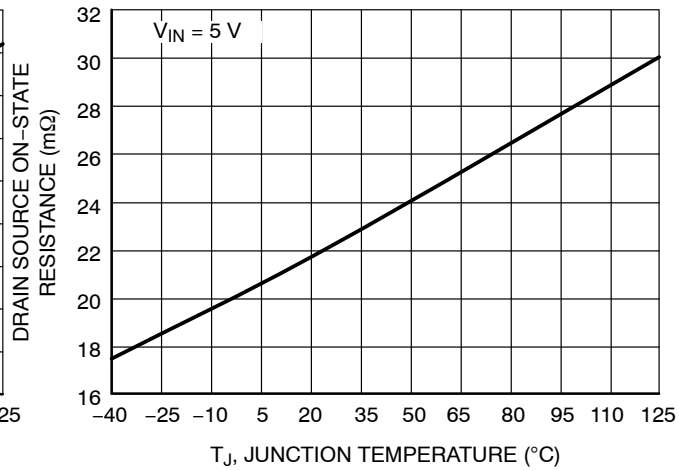



**Figure 6. Drain−Source ON−State Resistance vs Junction Temperature**

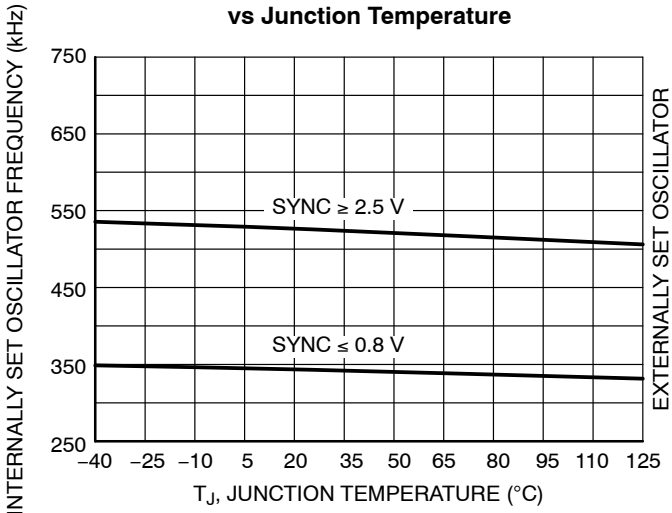



**Figure 7. Internally Set Oscillator Frequency vs Junction Temperature**

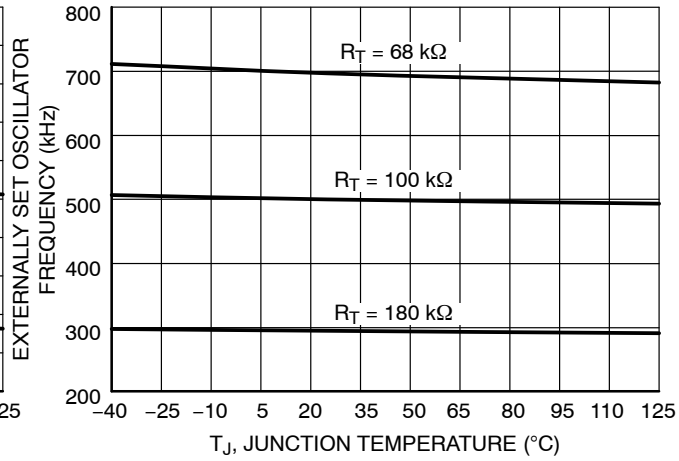



**Figure 8. Externally Set Oscillator Frequency vs Junction Temperature**

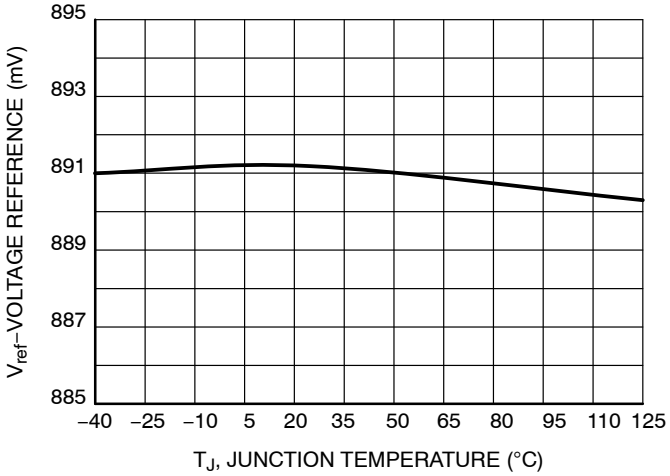



**Figure 9. Voltage Reference vs Junction Temperature**

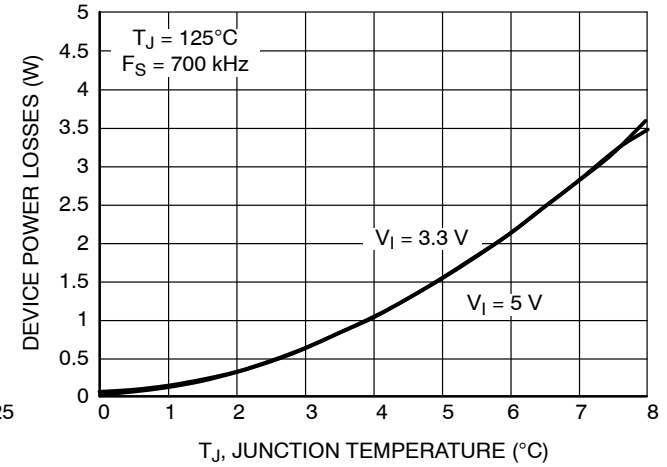



**Figure 10. Device Power Losses at $T_J$ = 125°C vs Load Current**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## TYPICAL CHARACTERISTICS

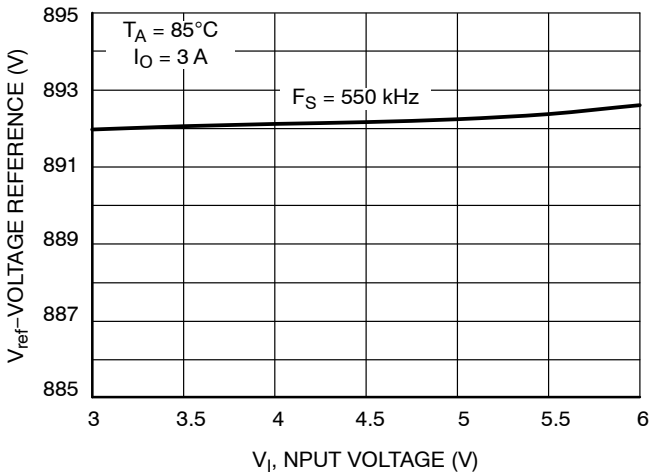



**Figure 11. Output Voltage Regulation vs. Input Voltage**

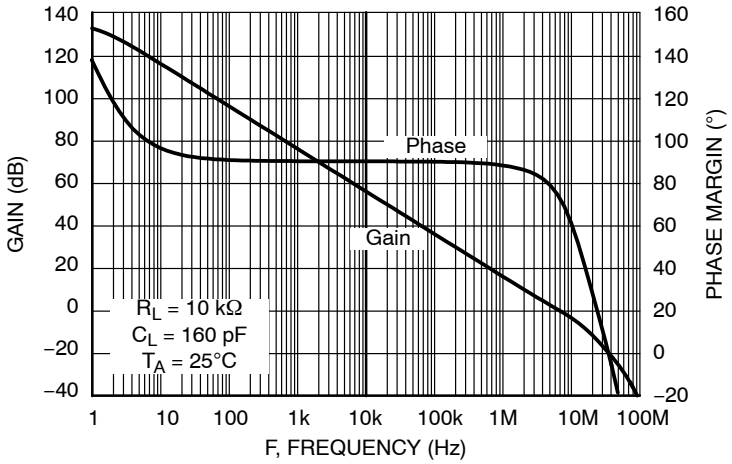



**Figure 12. Error Amplifier Open Loop Response**

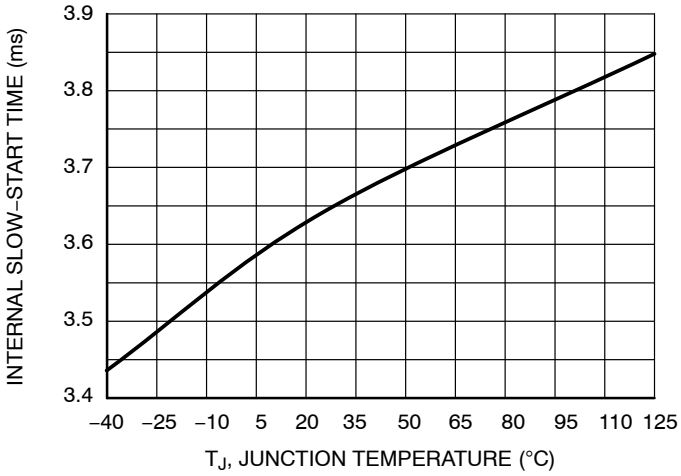



**Figure 13. Internal Slow–Start Time vs Junction Temperature**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## APPLICATION INFORMATION

Figure 14 shows the schematic diagram for a typical NCP1592 application. The NCP1592 (U1) can provide greater than 6 A of output current at a nominal output voltage of 3.3 V. For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit package must be soldered to the printed−circuit board.

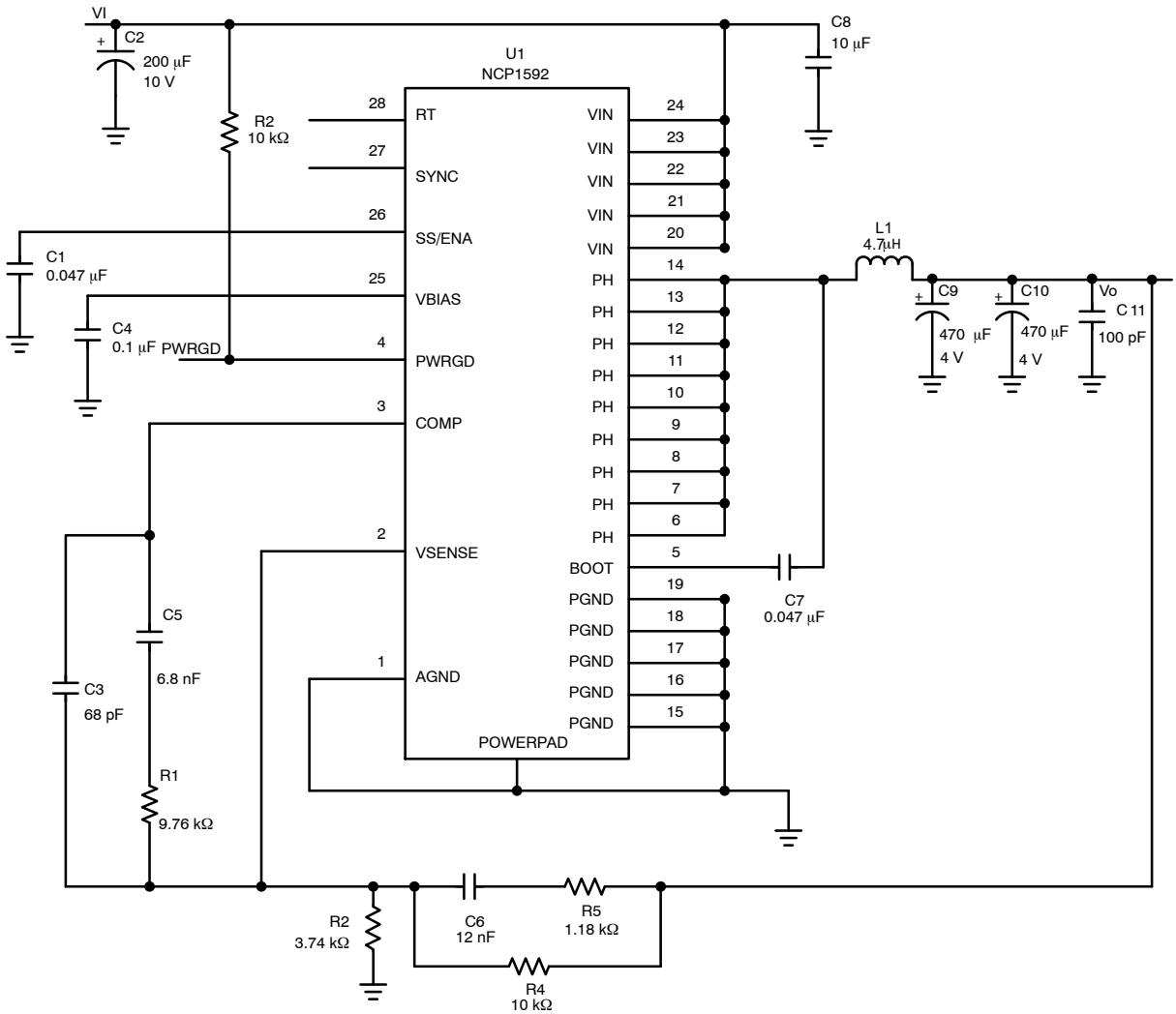



**Figure 14. Application Circuit**

## COMPONENT SELECTION

### INPUT FILTER

The input to the circuit is a nominal 5 VDC. The input filter C2 is a 220 µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 provides high frequency decoupling of the NCP1592 from the input supply and must be located as close as possible to the device. Ripple current is carried in both C2 and C8, and the return path to PGND must avoid the current circulating in the output capacitors C9 and C10.

### FEEDBACK CIRCUIT

The resistor divider network of R3 and R4 sets the output voltage for the circuit at 3.3 V. R4, along with R1, R5, C3, C5, and C6 form the loop compensation network for the circuit. For this design, a Type 3 topology is used.

### OPERATING FREQUENCY

In the application circuit, the 350 kHz operation is selected by leaving RT and SYNC open. Connecting a 180 kΩ to 68 kΩ resistor between RT (pin 28) and analog ground can be used to set the switching frequency to



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

280 kHz to 700 kHz. To calculate the RT resistor, use the equation below:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ [\text{k}\Omega] \qquad \text{(eq. 1)}$$

## OUTPUT FILTER

The output filter is composed of a 4.7 μH inductor and two 470 μF capacitors. The inductor is a low dc resistance (12 mΩ) type, Coiltronics UP3B−4R7. The capacitors used are 4 V POSCAP types with a maximum ESR of 0.040 Ω. The feedback loop is compensated so that the unity gain frequency is approximately 25 kHz.

## PCB LAYOUT

Figure 15 shows a generalized PCB layout guide for NCP1592.

The VIN pins are connected together on the printed−circuit board (PCB) and bypassed with a low−ESR ceramic−bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the NCP1592 ground pins. The minimum recommended bypass capacitance is 10 mF ceramic capacitor with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.

The NCP1592 has two internal grounds (analog and power). Inside the NCP1592, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the NCP1592, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. Therefore, separate analog and power ground traces are recommended. There is an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Additional vias are also used at the ground side of the input and output filter capacitors. The AGND and PGND pins are tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the NCP1592. Use a separate wide trace for the analog ground signal path. The analog ground is used for the voltage set point divider, timing resistor RT, slow−start capacitor and bias capacitor grounds. Connect this trace directly to AGND (Pin 1).

The PH pins are tied together and routed to the output inductor. Since the PH connection is the switching node, the inductor is located close to the PH pins. The area of the PCB conductor is minimized to prevent excessive capacitive coupling. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, LOUT, COUT and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pin−out, they must be routed close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow−start capacitor or RT resistor is used, or if the SYNC pin is used to select 350 kHz operating frequency, connect them to this trace.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

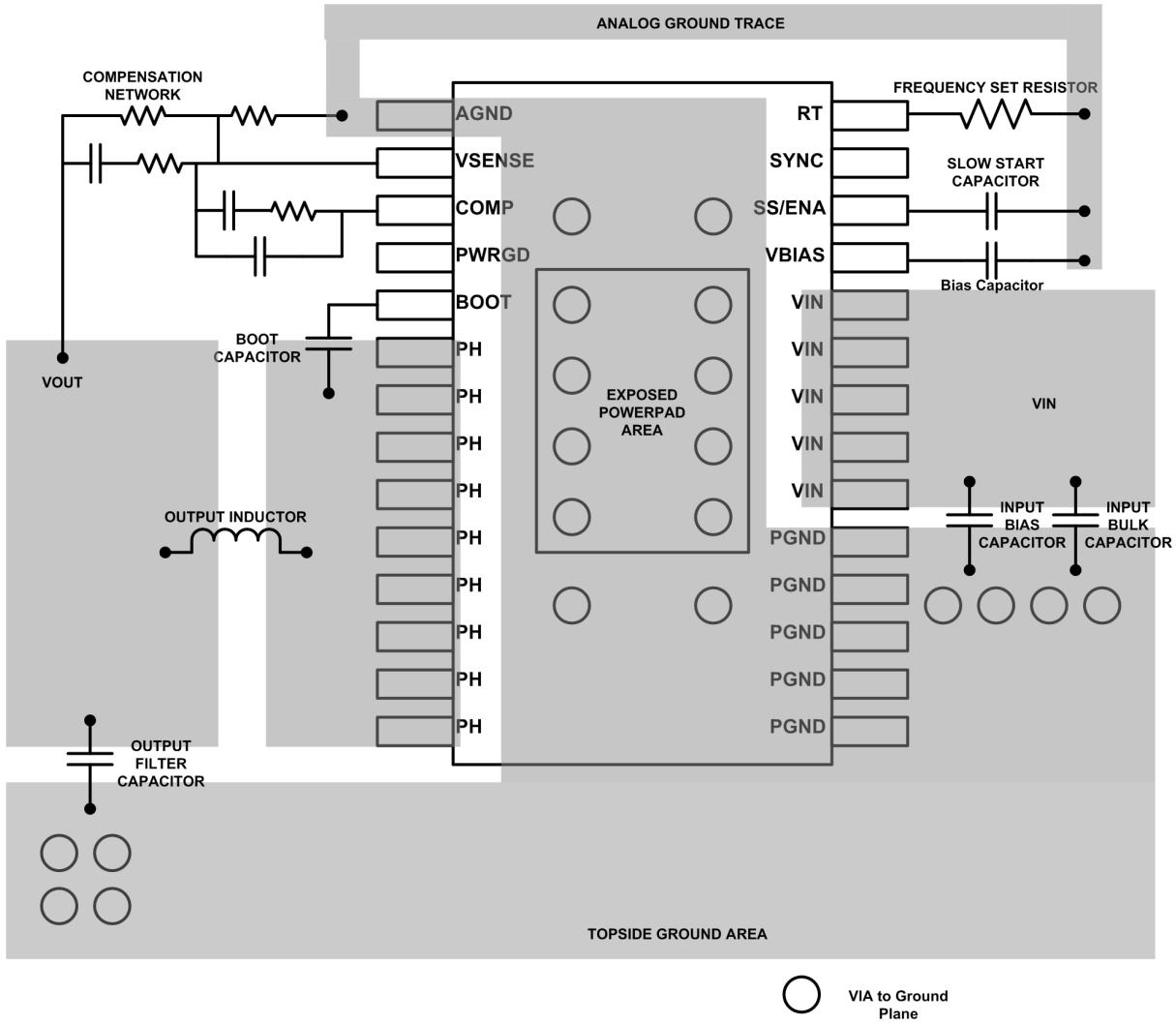



**Figure 15. Recommended Land Pattern For 28−Pin PowerPAD**

## LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3−inch by 3−inch plane of 1 copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground

plane layer must be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

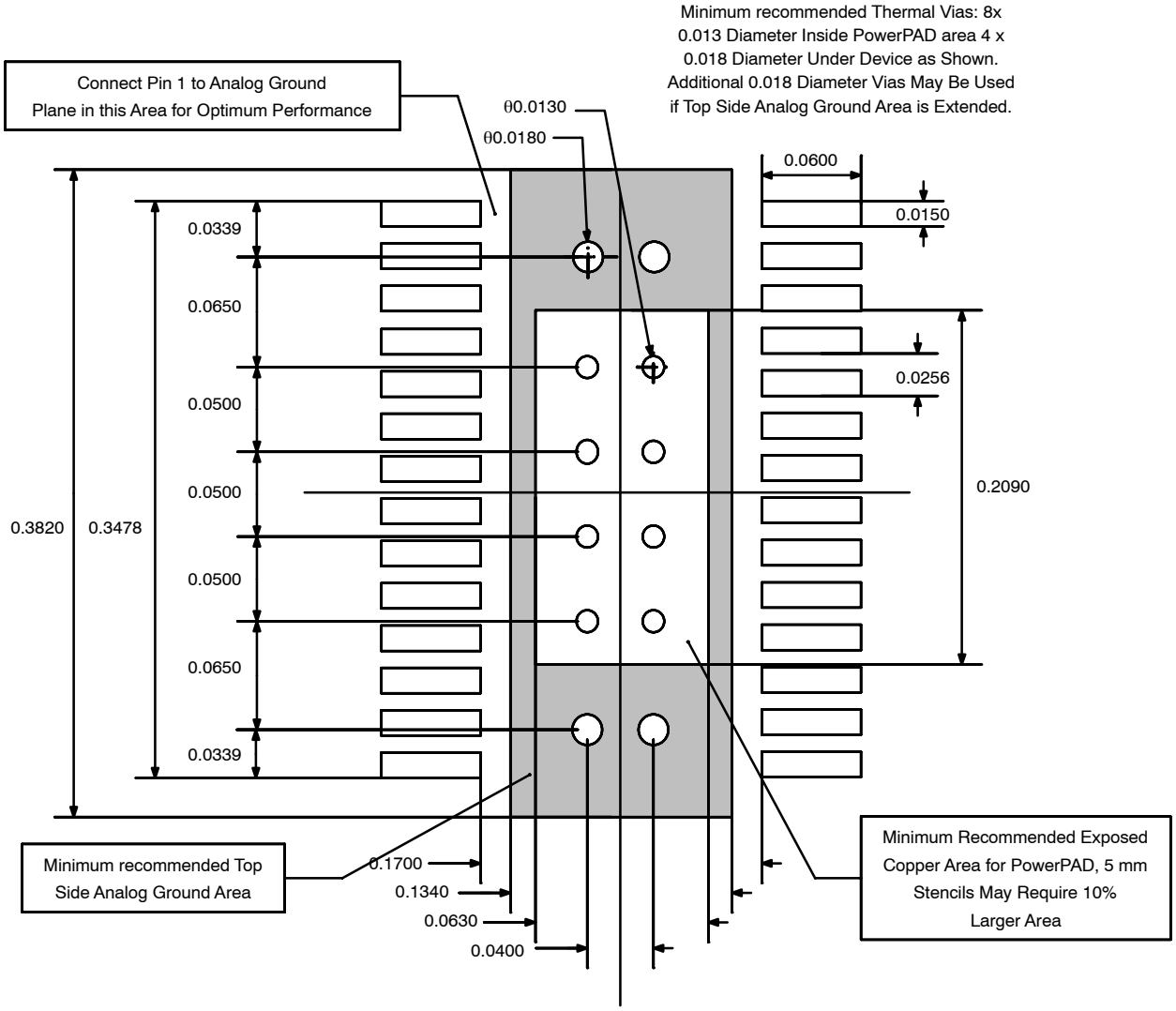



**Figure 16. Recommended Land Pattern For 28−Pin PowerPAD**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## PERFORMANCE GRAPHS

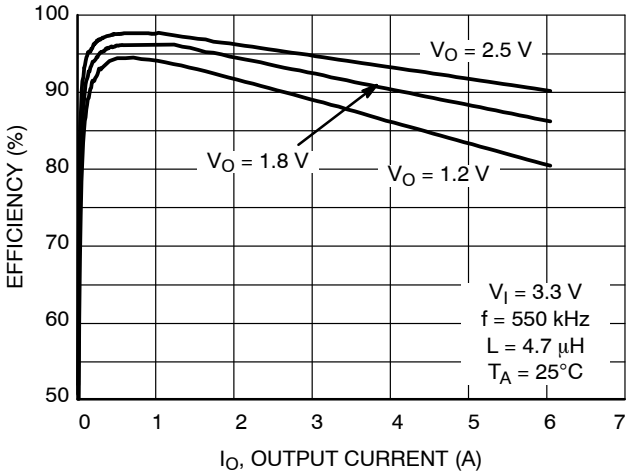



**Figure 17. Efficiency vs Output Current**

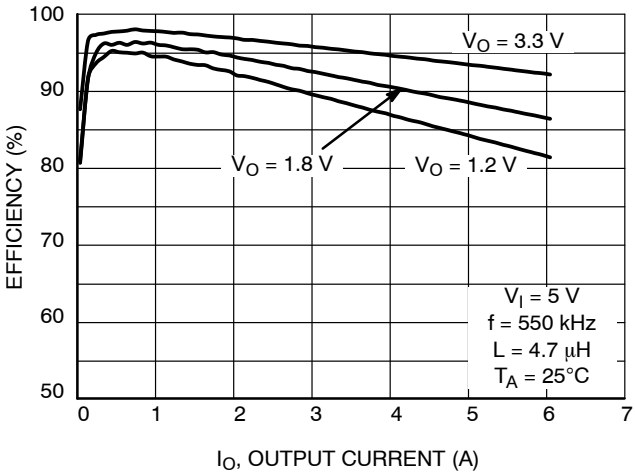



**Figure 18. Efficiency vs Output Current**

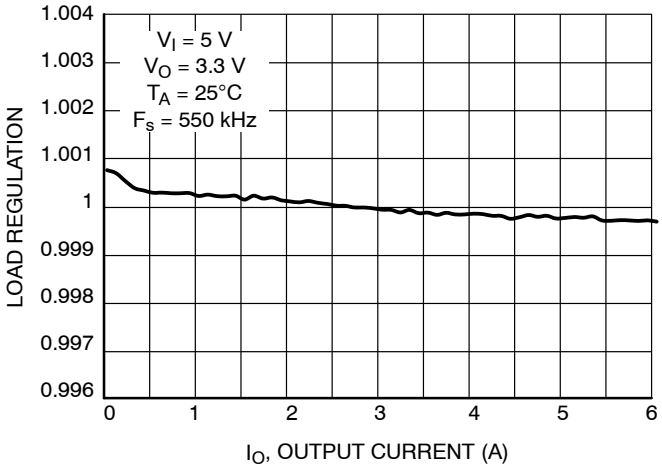



**Figure 19. Load Regulation vs Input Voltage**

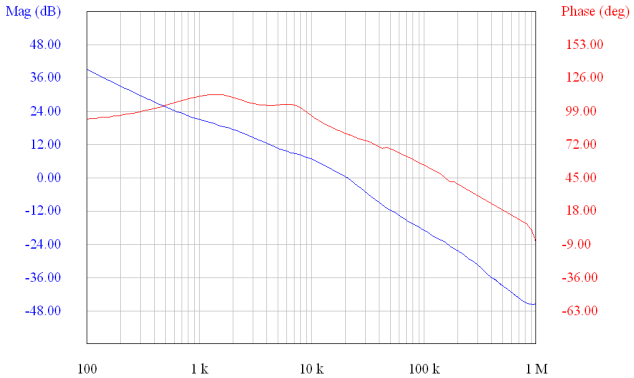



**Figure 20. Loop Response**

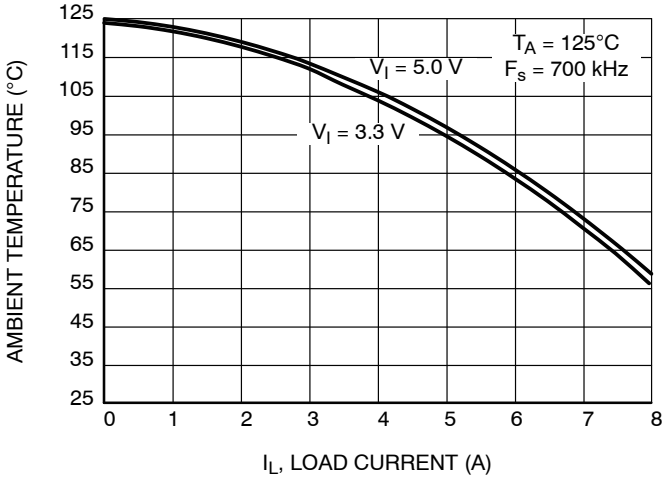



**Figure 21. Ambient Temperature vs Load Current**

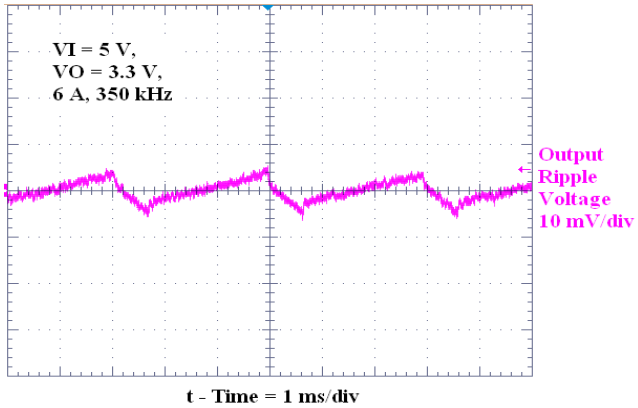



**Figure 22. Output Ripple Voltage**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## PERFORMANCE GRAPHS

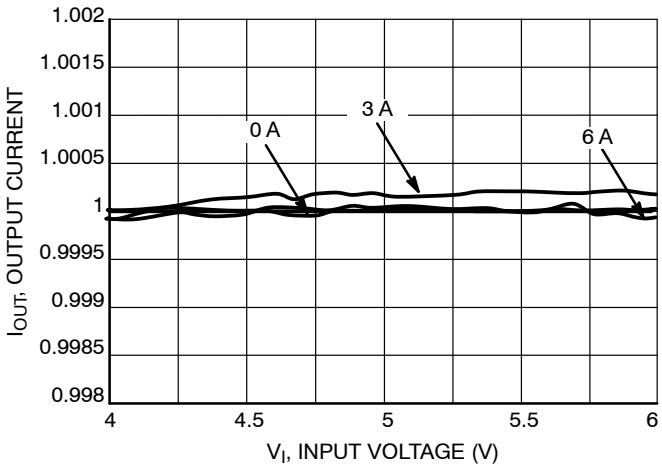



**Figure 23. Line Regulation vs Output Current**

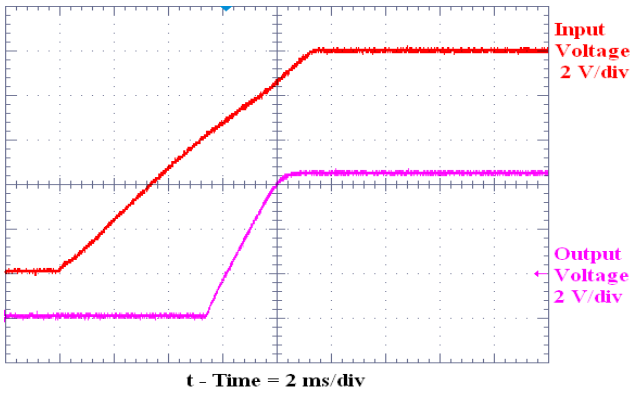



**Figure 24. Load Transient Response**

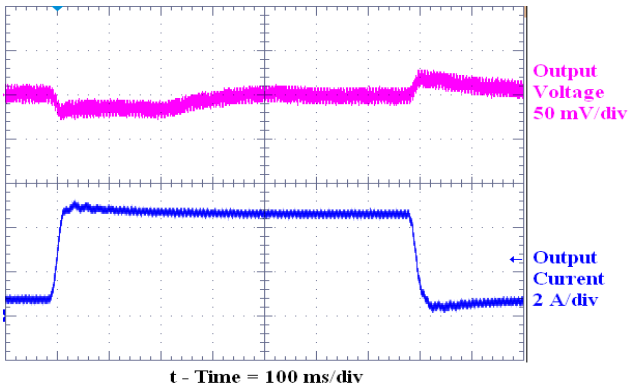



**Figure 25. Slow Start Timing**

Figure 26 shows the schematic diagram for a reduced size, high frequency application using the NCP1592. The NCP1592 (U1) can provide up to 6 A of output current at a nominal output voltage of 1.8 V. A small size 0.56 μH inductor is used and the switching frequency is set to 680 kHz by R1. The compensation network is optimized for fast transient response as shown in Figure 27. For good thermal performance, the PowerPAD underneath the integrated circuit NCP1592 needs to be soldered well to the printed−circuit board.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

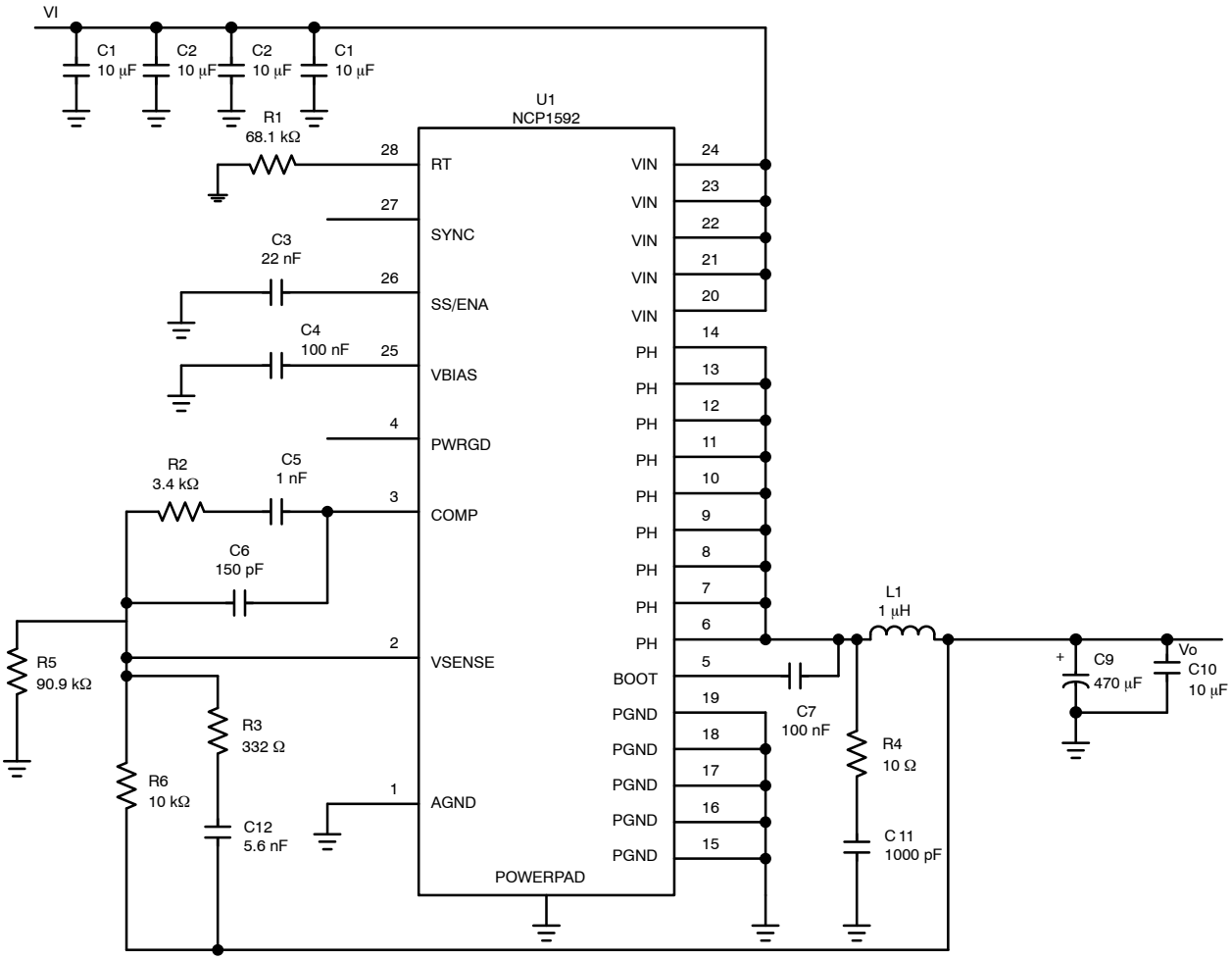



**Figure 26. Small Size, High Frequency Design**

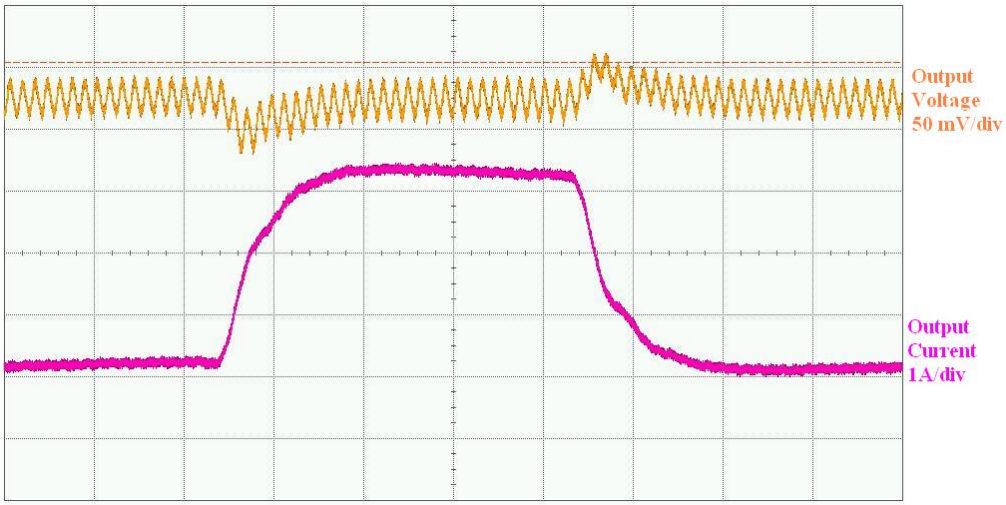



**Figure 27. Transient Response, 1.5 to 4.5 A Step**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## DETAILED DESCRIPTION

### UNDERVOLTAGE LOCK OUT (UVLO)

The NCP1592 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start−up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5 μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

### SLOW−START/ENABLE (SS/ENA)

The slow−start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start−up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms.

Voltage hysteresis and a 2.5−μs falling edge deglitch circuit reduce the likelihood of triggering the enable

due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow−start time with a low−value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start−up. First, a delay occurs between release of the SS/ENA pin and start−up of the output. The delay is proportional to the slow−start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start−up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \qquad \text{(eq. 2)}$$

Second, as the output becomes active, a brief ramp−up at the internal slow−start rate may be observed before the externally set slow−start rate takes control and the output rises at a rate proportional to the slow−start capacitor. The slow−start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \qquad \text{(eq. 3)}$$

The actual slow−start time is likely to be less than the above approximation due to the brief ramp−up at the internal rate.

During the soft−start period the output voltage is closed loop regulated from 0V to the output set voltage by slewing the reference voltage from 0 V to 0.891 V. If output voltage is not at 0 V during startup (pre-biased startup), output capacitor will be discharged by the control loop. The energy from the capacitors will flow from the output to ground and input through the low-side and High side MOSFETs. Under extreme conditions where pre-biased voltage is high with large output capacitance MOSFETs can be damaged.

### VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage.

A high quality, low−ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

### VOLTAGE REFERENCE

The voltage reference system produces a precise $V_{ref}$ signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the NCP1592, since it cancels offset errors in the scale and error amplifier circuits.

### 0SCILLATOR AND PWM RAMP

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin and AGND and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ k\Omega}{R} \times 500\ [kHz] \qquad \text{(eq. 4)}$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. The following table summarizes the frequency selection configurations:



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

| Switching Frequency | Sync Pin | RT Pin |
|---|---|---|
| 350 kHz, internally set | Float or AGND | Float |
| 550 kHz, internally set | ≥2.5 V | Float |
| Externally set 280 kHz to 700 kHz | Float | R= 180 kΩ to 68 kΩ |
| Externally synchronized frequency | Synchronization signal | R = RT value for 80% of external synchronization frequency |

## ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the NCP1592 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

## PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead−time and control logic block. During steady−state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low−side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low−side FET turns off and high−side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high−side FET and turning on the low−side FET. The low−side FET remains on until next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high−side FET remains on until the oscillator pulse signals the control logic to turn the high−side FET off and the low−side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set−point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high−side FET does not turn on. The low−side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The NCP1592 is capable of sinking current continuously until the output reaches the regulation set−point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high−side FET turns off and low−side FET turns on to decrease the energy in the output inductor and consequently output current. This process is repeated each cycle in which the current limit comparator is tripped.

## DEAD−TIME CONTROL AND MOSFET DRIVERS

Adaptive dead−time control prevents shoot−through current from flowing in both N−channel power MOSFETs during the switching transitions by actively controlling the turn−on times of the MOSFET drivers. The high−side driver does not turn on until the voltage at the gate of the low−side FET is below 2 V. While the low−side driver does not turn on until the voltage at the gate of the high−side MOSFET is below 2 V.

The high−side and low−side drivers are designed with 300 mA source and sink capability to quickly drive the power MOSFETs gates. The low−side driver is supplied from VIN, while the high−side driver is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5 Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

## OVERCURRENT PROTECTION

The cycle−by−cycle current limiting is achieved by sensing the current flowing through the high−side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100 ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

## THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the low thermal shutdown trip point, and starts up under control of the slow−start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft−start circuit, heating up due to the fault condition, and then shutting down upon reaching



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

### POWER−GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open−drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low, or a thermal shutdown occurs. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of $V_{ref}$, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of $V_{ref}$ and a 35 μs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

### ORDERING INFORMATION

| Device | Temperature Range (°C) | Package | Shipping† |
|---|---|---|---|
| NCP1592PAR2G | −40 to +125 | TSSOP−28 EP (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



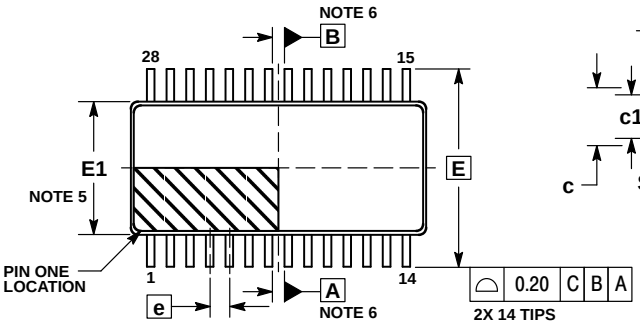
Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

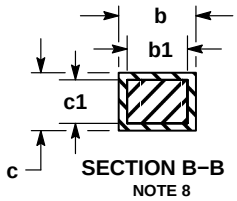
SCALE 1:1

**TSSOP28 9.7x4.4 EP**
CASE 948BG
ISSUE O

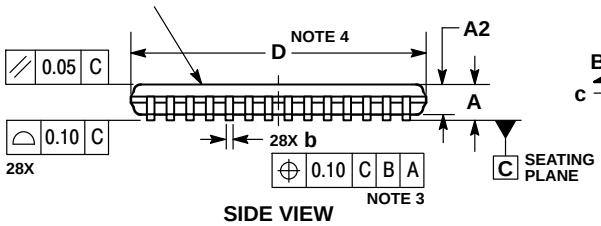
DATE 08 FEB 2012



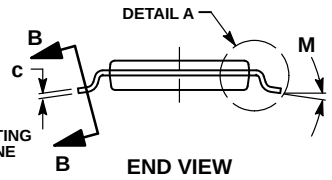

TOP VIEW



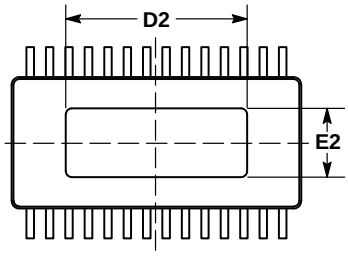

SECTION B−B
NOTE 8



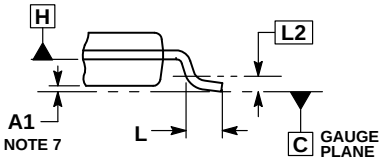

SIDE VIEW




END VIEW




BOTTOM VIEW

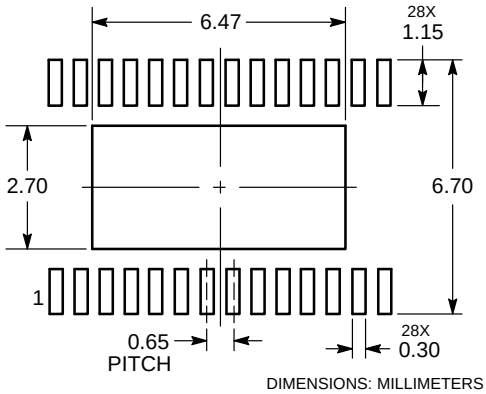



DETAIL A

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.07 MAX AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 FROM THE LEAD TIP.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | −−− | 1.20 |
| A1 | 0.00 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| b1 | 0.19 | 0.25 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 9.60 | 9.80 |
| D2 | 5.21 | 6.17 |
| E | 6.40 BSC | |
| E1 | 4.30 | 4.50 |
| E2 | 1.44 | 2.40 |
| e | 0.65 BSC | |
| L | 0.45 | 0.75 |
| L2 | 0.25 BSC | |
| M | 0 ° | 8 ° |

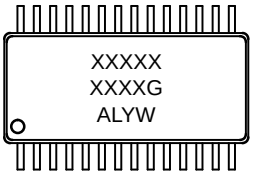
**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| DOCUMENT NUMBER: | 98AON67255E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | TSSOP28 EP, 9.7X4.4MM, 0.65P | PAGE 1 OF 1 |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



Downloaded from Arrow.com.

**onsemi**, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

Downloaded from Arrow.com.