3.3V ULTRA-PRECISION 1:4 LVDS FANOUT BUFFER/TRANSLATOR WITH INTERNAL TERMINATION

Precision Edge®
SY89833L

Precision Edge®

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **DC-to > 2GHz throughput**
  - **<600ps propagation delay (IN-to-Q)**
  - **<20ps within-device skew**
  - **<190ps rise/fall times**
- **Ultra-low jitter design**
  - **<1ps$_{RMS}$ cycle-to-cycle jitter**
  - **<10ps$_{PP}$ total jitter**
  - **<1ps$_{RMS}$ random jitter**
  - **<10ps$_{PP}$ deterministic jitter**
- **Unique input termination and VT pin accepts DC- and AC-coupled inputs**
- **High-speed LVDS outputs**
- **3.3V power supply operation**
- **Industrial temperature range: –40°C to +85°C**
- **Available in 16-pin (3mm x 3mm) MLF® package**

APPLICATIONS

- **Processor clock distribution**
- **SONET clock distribution**
- **Fibre Channel clock distribution**
- **Gigabit Ethernet clock distribution**

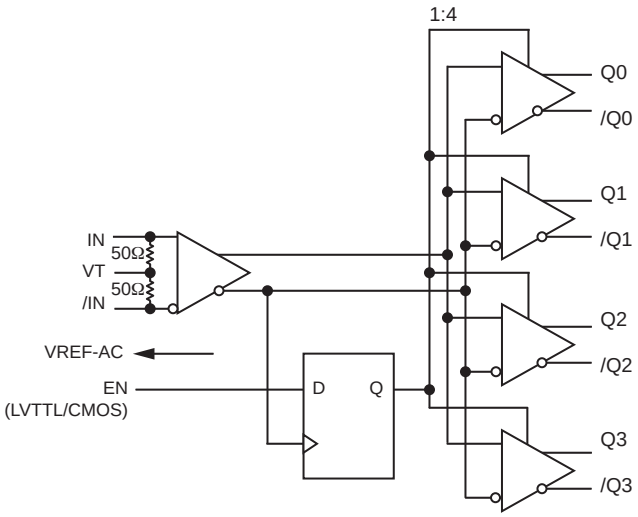
DESCRIPTION

The SY89833L is a 3.3V, high-speed 2GHz differential Low Voltage Differential Swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

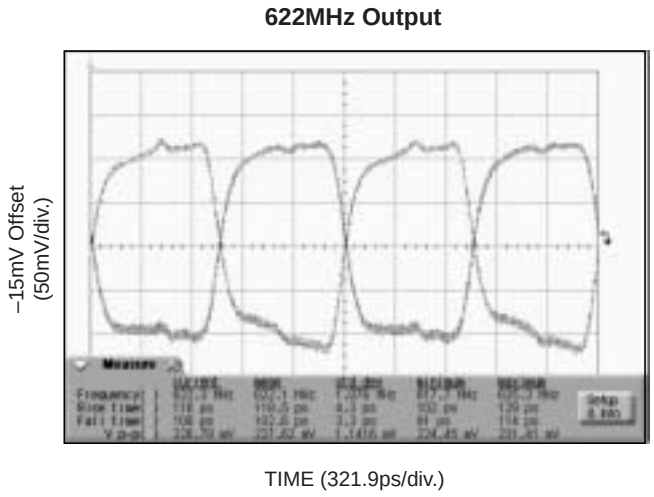
The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference is included for AC-coupled applications.

The SY89833L is part of Micrel's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V ±5% supply. For applications that require a different I/O combination, consult the Micrel website at: www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE



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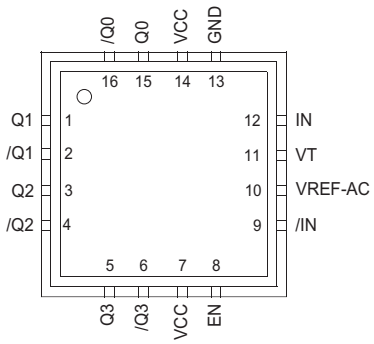
*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF® (MLF-16)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89833LMI	MLF-16	Industrial	833L	Sn-Pb
SY89833LMITR[2]	MLF-16	Industrial	833L	Sn-Pb
SY89833LMG[3]	MLF-16	Industrial	833L with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89833LMGTR[2, 3]	MLF-16	Industrial	833L with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential (Outputs): Normally terminated with 100Ω across the pair (Q, /Q). See "LVDS Outputs" section, Figure 2a. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signs as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Pleae refer to the "Input Interface Applications" section for more details.
10	VREF–AC	Reference Voltage: These outputs bias to V_{CC}–1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01μF low ESR capacitor to V_{CC}. See "Input Interface Applications" section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more detaiils.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each VCC pin as possible.

TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[1]	1[1]

Note 1. On next negative transition of the input signal (IN).

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
LVDS Output Current (I_{OUT}) ..... ±10mA
Input Current
  Source or Sink Current on (IN, /IN) ..... ±50mA
V_{REF-AC} Current
  Source or Sink Current on (I_{VT}) ..... ±2mA
Maximum Operating Junction Temperature ..... 125°C
Lead Temperature (Soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(2)

Supply Voltage Range ..... +3.0V to +3.60V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance(3)
  MLF® (θ_{JA})
    Still-Air ..... 60°C/W
  MLF® (ψ_{JB}) ..... 33°C/W

DC ELECTRICAL CHARACTERISTICS(4)

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		0.1		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage (IN, /IN)		–0.3		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	**Note 3,** see Figure 2c.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage	**Note 3,** see Figure 2d.	0.2			V
|IIN|	Input Current IN, /IN				45	mA
$V_{REF–AC}$	Reference Voltage	**Note 5**	V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Due to the internal termination (see "Input Buffer Structure" section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 2c.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[6]

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current				–300	µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[7]

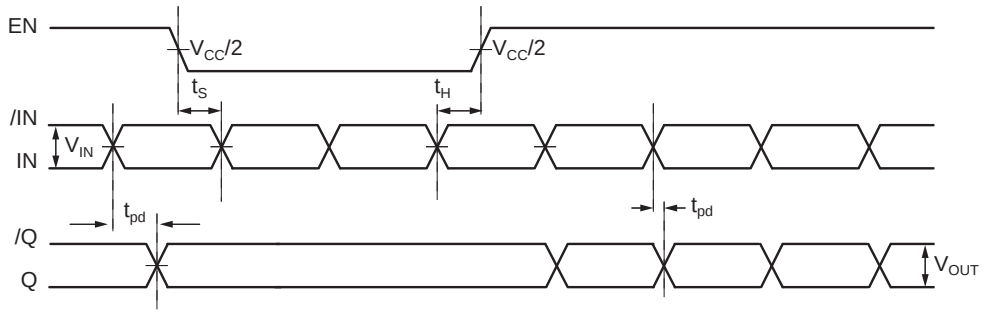
V_{CC} = +3.3V ±10%; R_L = 100Ω across the outputs; T_A = –40°C to +85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	V_{OUT} ≥ 200mV	2.0			GHz
t_{pd}	Propagation Delay IN-to-Q	V_{IN} < 400mV	400	500	600	ps
	IN-to-Q	V_{IN} ≥ 400mV	330	440	530	ps
t_{SKEW}	Within-Device Skew	**Note 8**		5	20	ps
	Part-to-Part Skew	**Note 9**			200	ps
t_S	Set-Up Time EN to IN, /IN	**Note 10**	300			ps
t_H	Hold Time EN to IN, /IN	**Note 10**	500			ps
t_{JITTER}	Data Random Jitter (RJ) Deterministic Jitter (DJ)	 **Note 11** **Note 12**			 1 10	 ps_{RMS} ps_{PP}
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	 **Note 13** **Note 14**			 1 10	 ps_{RMS} ps_{PP}
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	60	110	190	ps

Notes:

7. High-frequency AC parameters are guaranteed by design and characterization.
8. Within device skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.
11. Random jitter is measured with a K28.7 pattern, measured at ≤f_{MAX}.
12. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

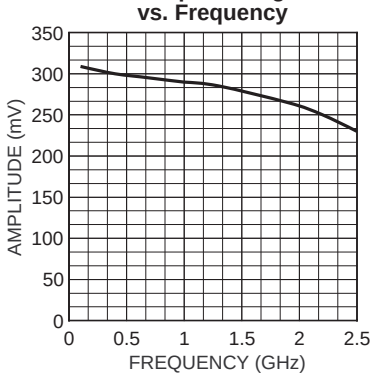
TIMING DIAGRAM



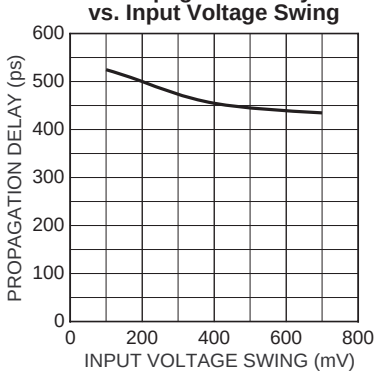
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.

Output Swing vs. Frequency



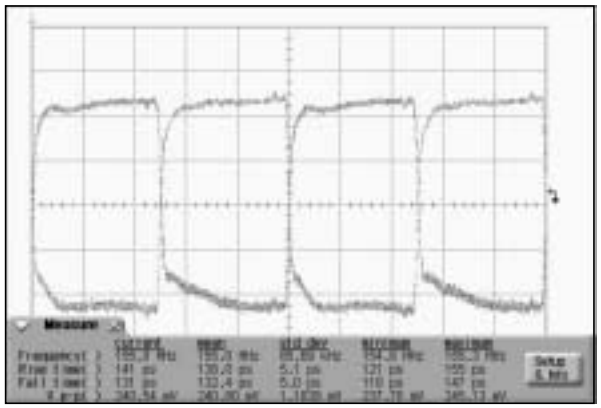
Propagation Delay vs. Input Voltage Swing



FUNCTIONAL CHARACTERISTICS

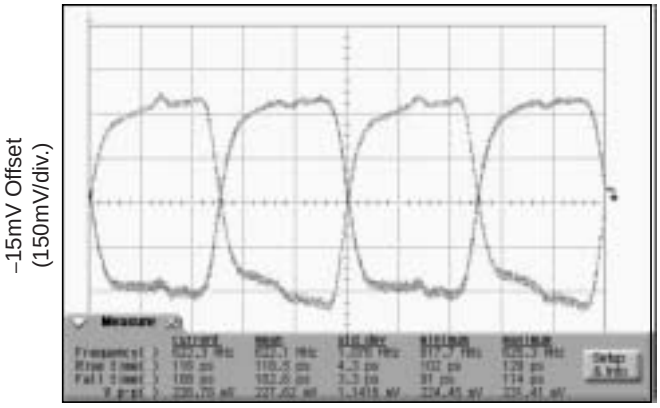
V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

155MHz Output



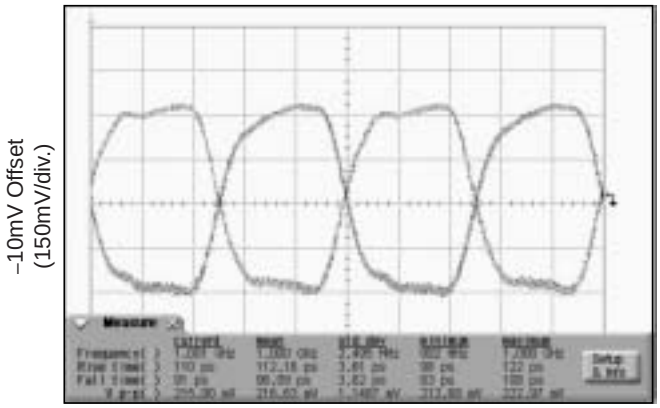
TIME (1.29ns/div.)

622MHz Output



TIME (321.9ps/div.)

1GHz Output



TIME (200ps/div.)

INPUT STAGE

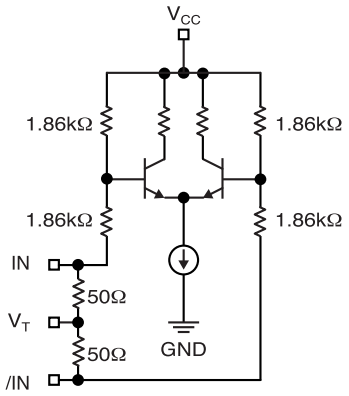


Figure 1. Simplified Differential Input Buffer

LVDS OUTPUTS

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver.

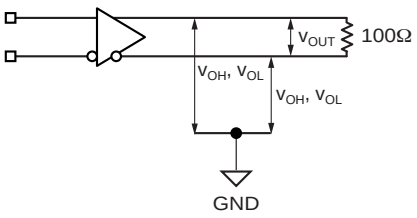


Figure 2a. LVDS Differential Measurement

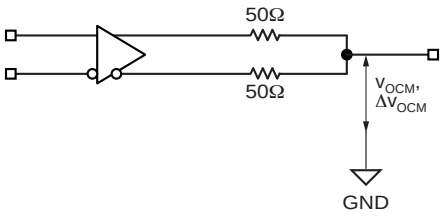


Figure 2b. LVDS Common Mode Measurement

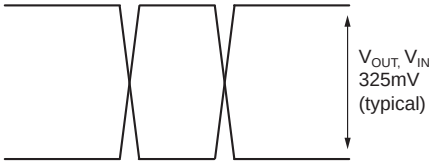


Figure 2c. Single-Ended Swing

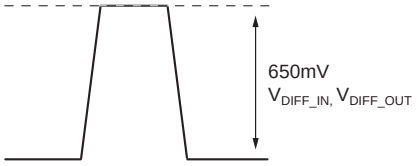


Figure 2d. Differential Swing

INPUT INTERFACE APPLICATIONS

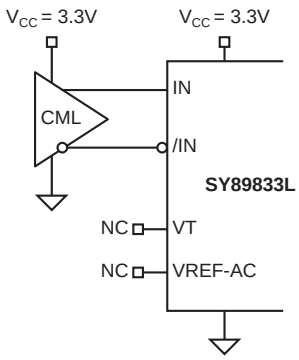


Figure 3a. DC-Coupled CML Input Interface

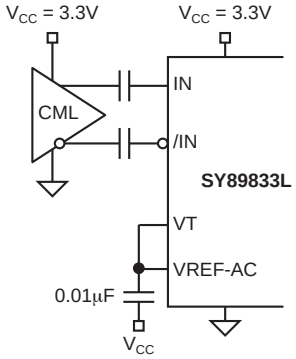


Figure 3b. AC-Coupled CML Input Interface

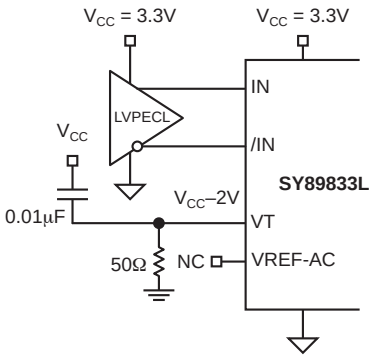


Figure 3c. DC-Coupled LVPECL Input Interface

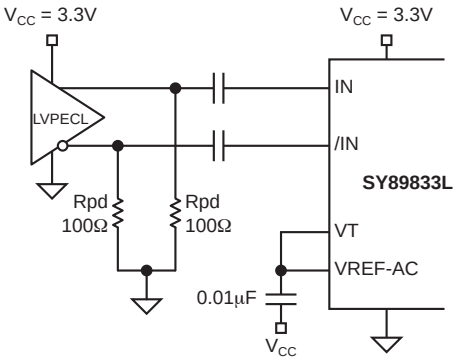


Figure 3d. AC-Coupled LVPECL Input Interface

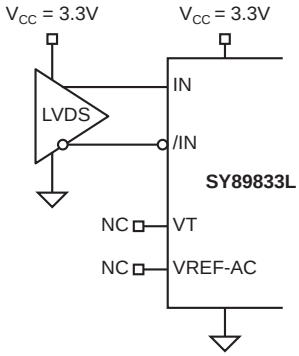
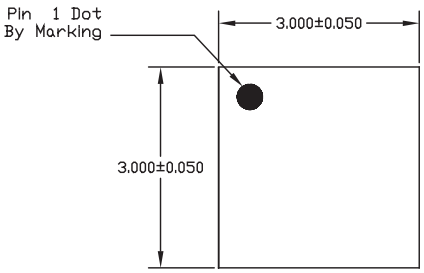


Figure 3e. LVDS Input Interface

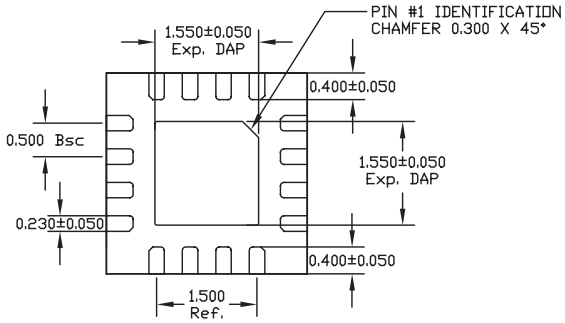
RELATED PRODUCT AND SUPPORT DOCUMENTS

Part Number	Function	Data Sheet Link
SY89830U	2.5V/3.3V/5V 2.5GHz 1:4 PECL/ECL Clock Driver with 2:1 Differential Input MUX	http://www.micrel.com/product-info/products/sy89830u.shtml
SY89831U	Ultra-Precision 1:4 LVPECL Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89831u.shtml
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/product-info/products/sy89832u.shtml
SY89834U	2.5/3.3V Two Input, 1GHz LVTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	http://www.micrel.com/product-info/products/sy89834u.shtml
	16-MLF® Manufacturing Guidelines Exposed Pad Application Note	http://www.amkor.com/products/notes_papers/MLF_appnote_0301.pdf
HBW Solutions	New Products and Termination App. Note	http://www.micrel.com/product-info/as/solutions.shtml

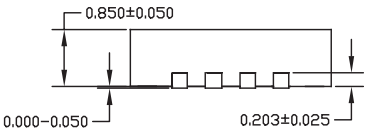
16-PIN EPAD *Micro*LeadFrame® (MLF-16)



TOP VIEW

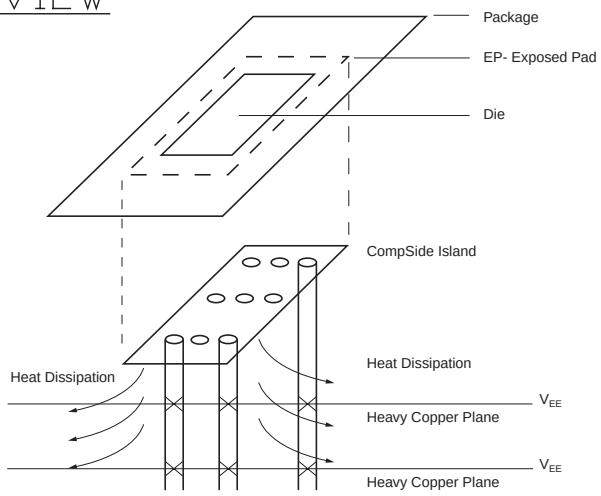


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and are shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com