PD70222

IdealBridge™ Dual MOSFET-based Bridge Rectifier

PRELIMINARY

Description

PD70222 is a dual pack of MOSFET-based full-bridge rectifiers. It contains low-R_{DS} 0.15Ω N-channel MOSFETs for much higher overall efficiency and higher output power, particularly when used in Powered Devices for Power over Ethernet (PoE) applications. The entire drive circuitry for driving the MOSFETs is on-chip, including a charge pump for driving the high-side N-channel MOSFETs. The total forward drop (bridge offset) introduced by the IdealBridge™ rectifier is only 180mV at 0.6A, compared to a standard bridge rectifier that typically presents 2000mV of forward drop.

PD70222 IdealBridge™ can support over 1A current, making it the ideal choice not only for modern energy-saving 2-pair applications compliant with IEEE802.3af and IEEE802.3at (Type 1 and Type 2), but also 4-pair Powered Devices such as for UPOE (51W) and POH (Power over HDBase-T, 73W).

In addition, PD70222 is capable of helping to identify at the physical layer itself whether a 2-pair PSE or a 4-pair PSE is providing power over the cable. It does that by sensing the voltage on the line (un-rectified) side of the pairs.

Features

- Active circuit with low forward-drop to replace dissipative passive diode bridges
- Self-contained drive circuitry for MOSFETs
- Designed to support IEEE802.3af/at, UPOE and Power over HDBase-T (PoH)
- Integrated 0.15Ω N-Channel MOSFETs for 0.3Ω total path resistance
- "Power present" indicator signals for identifying 4-pair bridge power
- Low leakage, < 12µA during detection
- Wide operating voltage range up to 57V
- -40°C to +85°C ambient
- Available in 40 pin package
- RoHS Compliant

Applications

- Power over Ethernet (all IEEE compliant 2-pair modes)
- Proprietary 4-pair standards, UPOE (Universal PoE) and POH

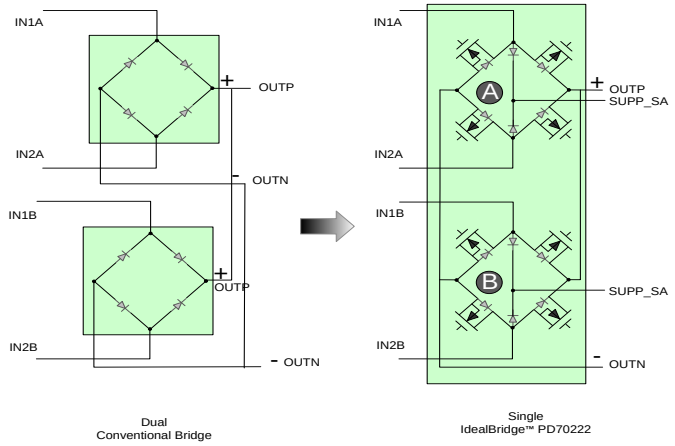
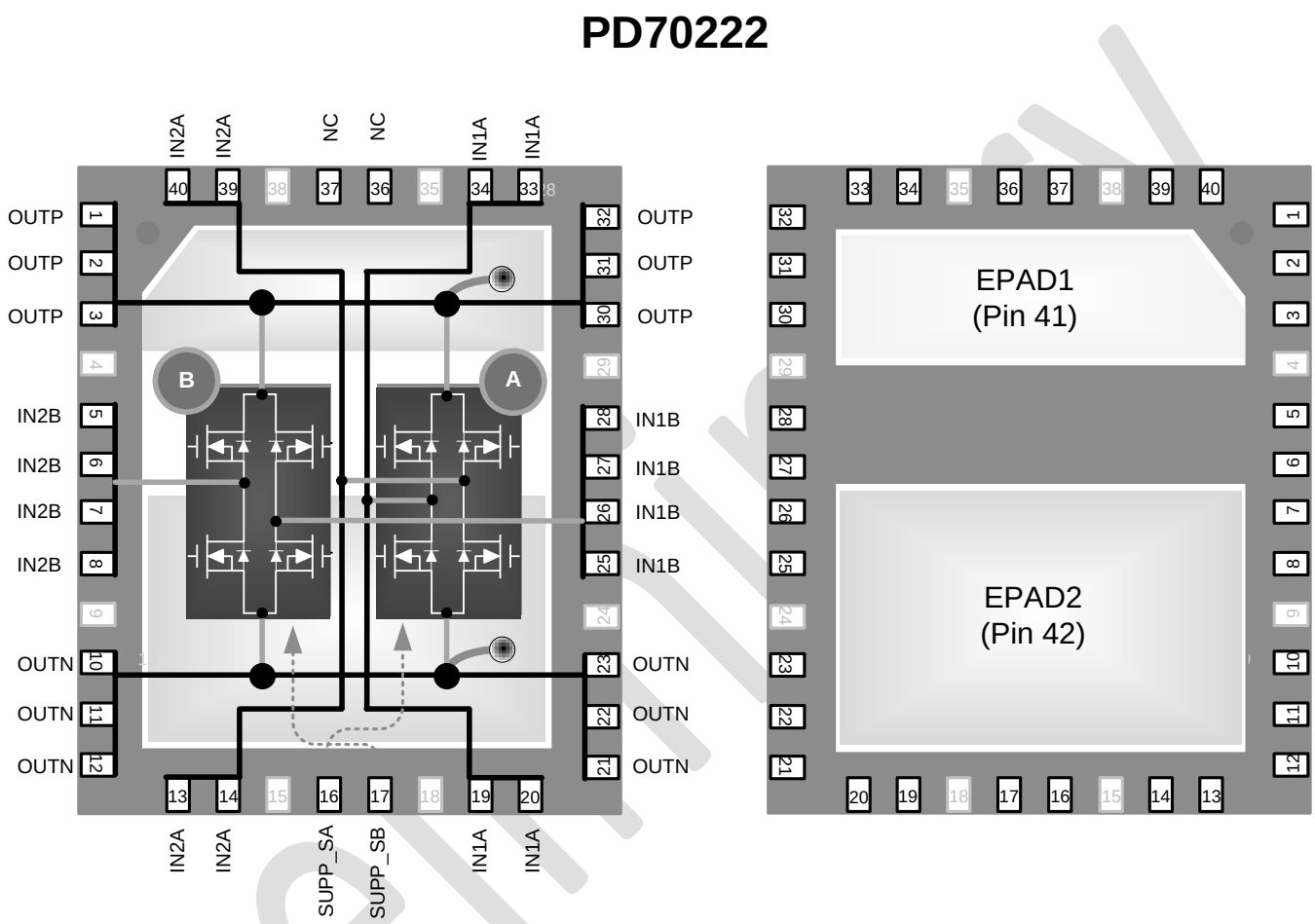


Figure 1

Pin Configuration and Pinout



TOP VIEW
6×8 MLPQ – 40L

BOTTOM VIEW
6×8 MLPQ – 40L

Figure 2: Internal Construction and Pinout

Ordering Information

Ambient Temperature	Type	Part Marking	Tape and Reel	Package
-40 to 85°C	RoHS compliant, Pb-free	PD70222	PD70222ILQ-TR	MLP-Quad (40 lead)

Pin Description

Pin Number	Pin Designator	Description
1, 2, 3	OUTP	Rectified positive (upper) rail shared by both bridges
4	N.A.	Not applicable (pin not present)
5, 6, 7, 8	IN2B	Input "2" of bridge rectifier number B
9	N.A.	Not applicable (pin not present)
10, 11, 12	OUTN	Rectified negative (lower) rail shared by both bridges
13, 14	IN2A	Input "2" of bridge rectifier number A
15	N.A.	Not applicable (pin not present)
16	SUPP_SA	Input power supply detect pin for bride rectifier number A. Goes high when pairs connected to this bridge are powered by the PSE
17	SUPP_SB	Input power supply detect pin for bride rectifier number B. Goes high when pairs connected to this bridge are powered by the PSE
18	N.A.	Not applicable (pin not present)
19, 20	IN1A	Input "1" of bridge rectifier number A
21, 22, 23	OUTN	Rectified negative (lower) rail shared by both bridges, same as Pins 10, 11 and 12
24	N.A.	Not applicable (pin not present)
25, 26, 27, 28	IN1B	Input "1" of bridge rectifier number B
29	N.A.	Not applicable (pin not present)
30, 31, 32	OUTP	Rectified positive (upper) rail shared by both bridges. Same as Pins 1, 2 and 3
33, 34	IN1A	Input "A" of bridge rectifier number 1. Same as Pins 19 and 20
35	N.A.	Not applicable (pin not present)
36, 37	N.C	Not connected; do not connect externally (leave floating)
38	N.A.	Not applicable (pin not present)
39, 40	IN2A	Input "2" of bridge rectifier number A. Same as Pins 13 and 14
41	EPAD1	Connect to OUTP on PCB
42	EPAD2	Connect to OUTN on PCB

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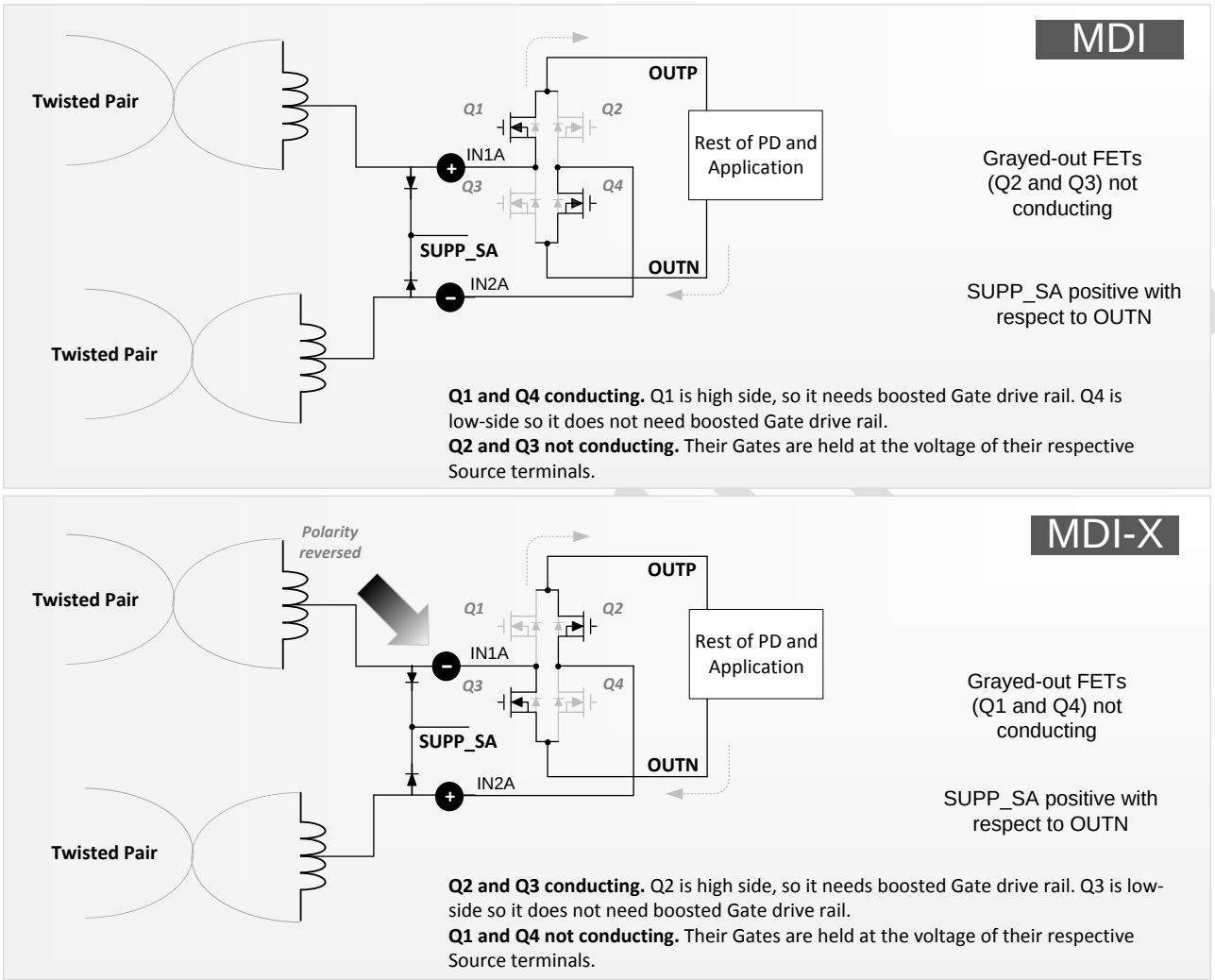
Bridge Rectifier "A" (powered with MDI or MDI-X

The MOSFETs and active bridge circuitry is guaranteed to turn ON at a threshold set between 23.1V and 32V. Below that threshold, rectifier operation is through their body diodes only



PURPOSE OF CHARGE PUMP:
Therefore, in both cases above, the FETs connected to OUTP (the "high-side" FETs) are the ones which require a boosted Gate drive rail so they can be turned ON. The on-chip charge pump provides the boosted Gate drive rail for the high-side FETs. The FETs connected to OUTN ("low-side" FETs) do not need a boosted drive rail to be turned ON.

PURPOSE AND USE OF SUPPLY PINS:
Since the above twisted pair set is delivering power, in both cases above, SUPP_SA is positive with respect to OUTN. But if these two twisted pairs were not connected to a PSE, SUPP_SA would be low. Therefore, in the case of a standard 2-pair or 4-pair PDs with two bridge rectifiers (4-pairs), one connected to the data pairs, the other to the spare pairs, the presence of high voltage on SUPP_SA and/or SUPP_SB will indicate whether the data pairs or spare pairs, or both, are connected to PSEs. So SUPP_SA and SUPP_SB can be used to indicate 2-pair or 4-pair PoE operation.

Figure 3: Principle of Operation

Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

		Min	Max	Units
IN1A, IN1B, IN2A, IN2B to OUTN		-0.3	72	V
IN1A to IN2A		-0.3	72	V
IN1B to IN2B		-0.3	72	V
IN1A, IN1B, IN2A, IN2B to OUTP		-72		V
IN1A, IN2A to IN1B		-0.3	72	V
IN1A, IN2A to IN2B		-0.3	72	V
OUTP to OUTN		-0.3	72	V
OUTP to IN1A, IN1B, IN2A, IN2B		-0.3	72	V
SUPP_SA, SUPP_SB to OUTN		-0.3	72	V
I_{INA}, I_{INB} (currents through bridge A and/or B)			TBD	A
Junction Temperature			150	°C
Lead Soldering Temperature (40s, reflow)			260	°C
Storage Temperature		-65	150	°C
ESD rating	HBM		±2	kV
	MM		±200	V
	CDM		±500	V

Note: EPAD1 is connected by copper plane on PCB to OUTP, and EPAD2 is similarly connected to OUTN. OUTN is ground for IC.

Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

	Min	Max	Units
IN1A, IN1B to OUTN	TBD	57	V
IN2A, IN2B to OUTN	TBD	57	V
Junction Temperature	-40	125	°C
Port Current (I_{INx})	0	1.5	A

Note: Corresponding Ambient Temperature is -40 to 85 °C

Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
θ_{JA}		31		°C/W
θ_{JL}		2.5		°C/W
θ_{JC}		TBD		°C/W

Note: The θ_{Jx} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

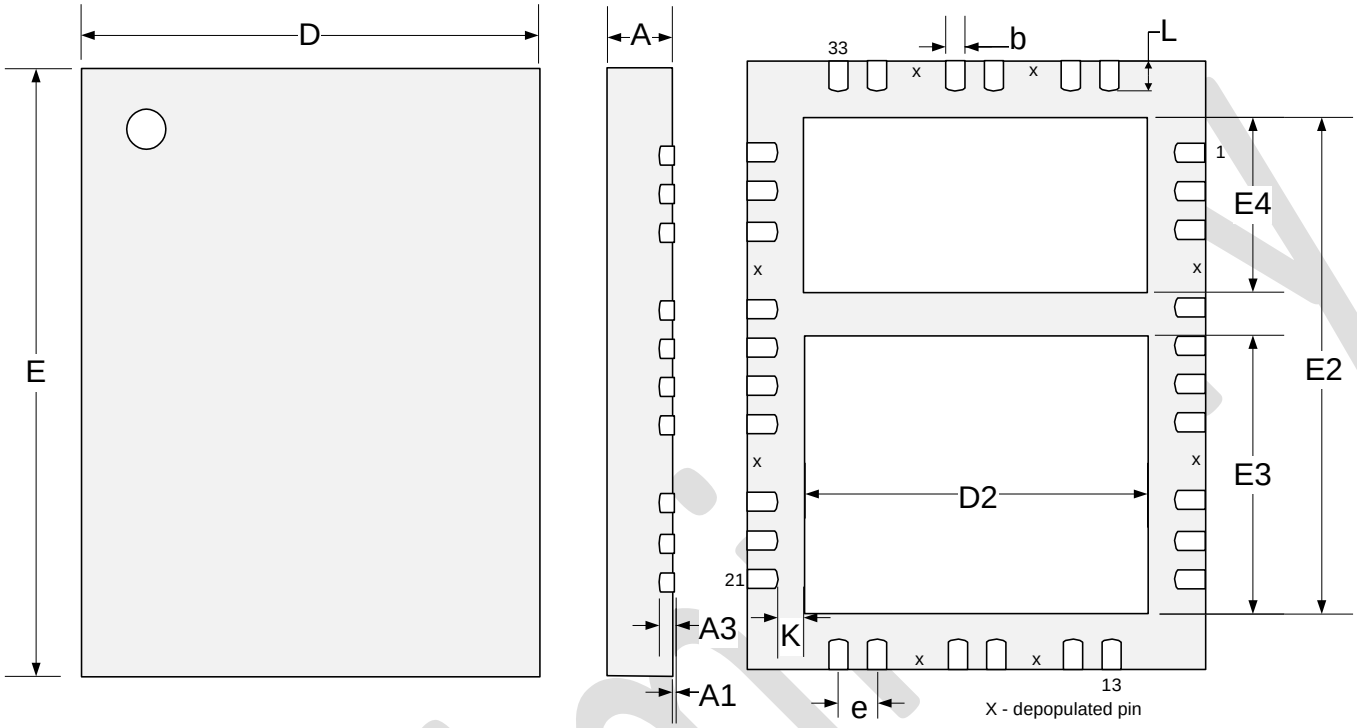
Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25°C ambient.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{INx}	Input Voltage for Bridge "x", where x is "A" or "B".				57	V
I_Q	Quiescent Current (both bridges combined)	2.5V < V_{INx} < 10.1V, 500µ load or 25k signature detection resistor connected. No load on SUPP_Sx pins.		6	12	µA
		10.2V < V_{INx} < 23V, 50mA load between OUTP and OUTN. No load on SUPP_Sx pins.			80	µA
		V_{INx} = 55V. 1.5A load between OUTP and OUTN. 900kΩ load resistor on each SUPP_Sx pin.			750	µA
V_{TURN_ON}	Active turn-on voltage of FETs		23.1	27.5	32	V
V_{HYS}	Turn-on voltage hysteresis			TBD		V

	Alternate input voltage polarity			200			ms
V_{OFFSET}	Bridge offset	V_{INx} > 32V, two FETs in series	I_{INx} = 0.6A		180	TBD	mV
			I_{INx} = 0.6A		300	TBD	
		V_{INx} < 32V, two body diodes in series	I_{INx} = 1mA	398		1190	
			I_{INx} = 5mA	508		1294	
			I_{INx} = 40mA	658		1116	
R_{DS}	FET Drain to Source Resistance	I_D = 0.6A			TBD	TBD	Ω
		I_D = 1A			TBD		
		I_D = 1.5A			0.15		
I_R	Leakage Current (Reverse)	$V_{OUTP} - V_{OUTN}$ = 57V				40	µA
V_{BFD}	Backfeed Voltage	Between input terminals with 100kΩ resistor across them and 57V between OUTP and OUTN				2.7	V
I_{MAX_LOW}	Maximum Forward Current (per bridge) below V_{TURN_ON}	Polarity changeover > 20ms				0.45	A
I_{MAX_HIGH}	Maximum Forward Current (per bridge) above V_{TURN_ON}			1.5		TBD	A
V_{SUPP_HIGH}	Max voltage on SUPP_SA and SUPP_SB pins	V_{INx} = 36V		34			V
V_{SUPP_LOW}	Min voltage on SUPP_SA and SUPP_SB pins	V_{INx} = TBDV				26	V

Package Outline Drawing 40 Pin QFN 6x8 mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.00 BSC		0.236 BSC	
E	8.00 BSC		0.315 BSC	
D2	4.35	4.6	0.171	0.181
E2	6.35	6.6	0.250	0.260
E3	3.5	3.75	0.138	0.148
E4	2.2	2.4	0.087	0.094
e	0.50 BSC		0.020 BSC	
K	0.20	-	0.008	-
L	0.37	0.57	0.014	0.022

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in millimeters, inches for reference only.

Recommended PCB layout

Recommended PCB layout pattern for PD70222 is described in the following three figures.

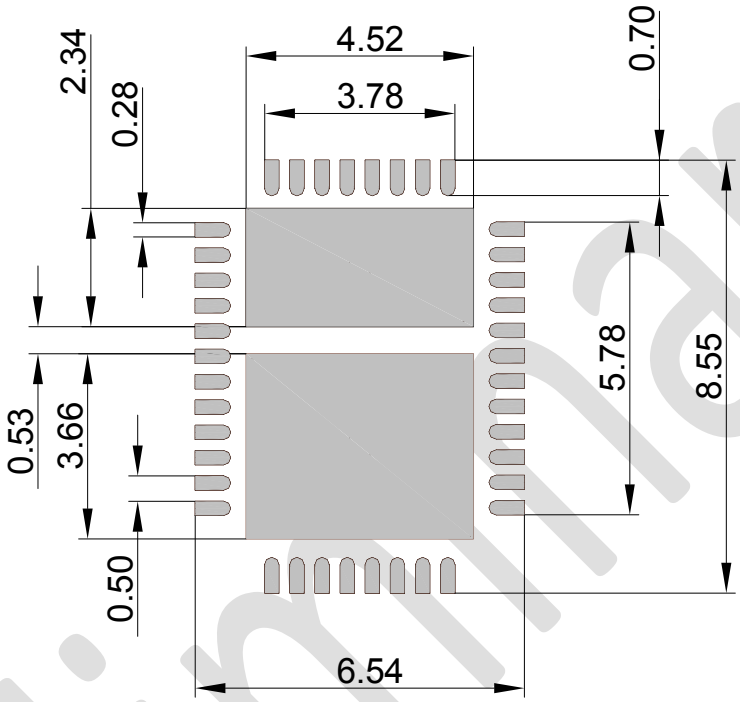


Figure 4: PD70222 Top layer Copper Recommended PCB Layout (mm)

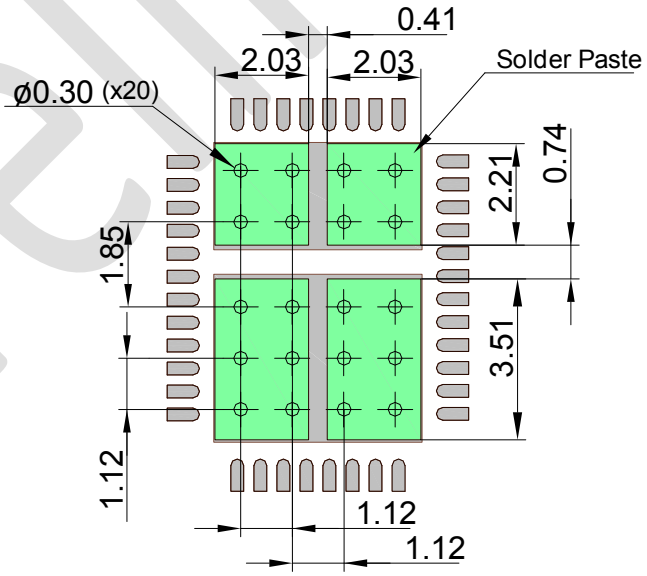


Figure 5: PD70222 Top layer Solder Paste and Vias Recommended PCB Layout for Thermal Pad Array (mm)

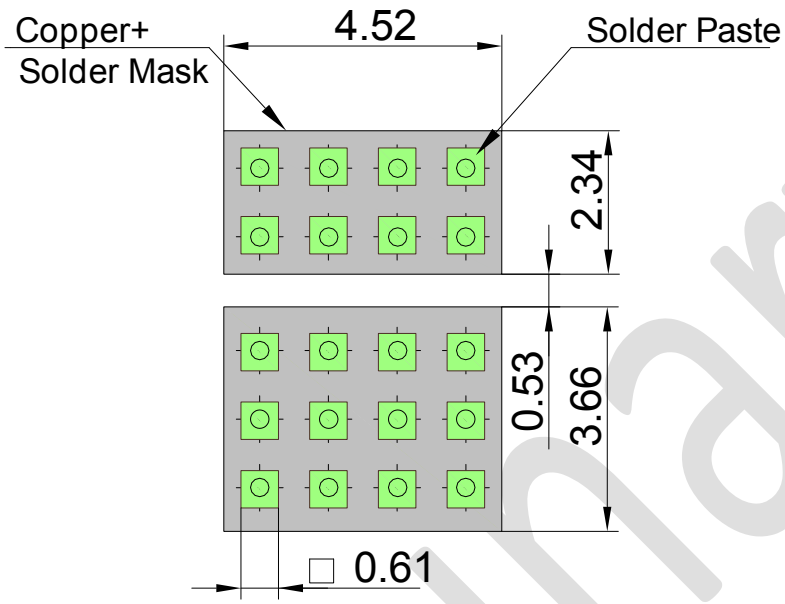


Figure 6: PD70222 Bottom layer Copper and Solder Paste Recommended PCB Layout for Thermal Pad Array (mm)

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Revision History

Revision Level / Date	Para. Affected	Description
0.2 / 4 Oct 2012	-	Initial Release – Preliminary version
0.3 / 30 April 2013		Adding package description and Recommended PCB layout
0.35 / 8 May 2013		Adding Package tollerances

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Visit our web site at: **www.microsemi.com** **Catalog Number**: DS_PD70222