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March 2015

# FDD306P
# P-Channel 1.8V Specified PowerTrench® MOSFET

## Features

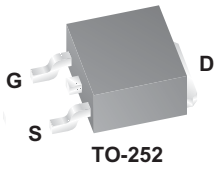
- –6.7 A, –12 V. $R_{DS(ON)}$ = 28 mΩ @ $V_{GS}$ = –4.5 V
  $R_{DS(ON)}$ = 41 mΩ @ $V_{GS}$ = –2.5 V
  $R_{DS(ON)}$ = 90 mΩ @ $V_{GS}$ = –1.8 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

## Applications

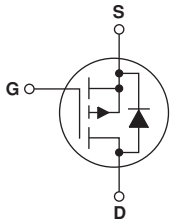
- DC/DC converter

## General Description

This P-Channel 1.8V Specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management.



TO-252




## Absolute Maximum Ratings $T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –12 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | V |
| $I_D$ | Drain Current – Continuous | (Note 3) | –6.7 | A |
| | – Pulsed | (Note 1a) | –54 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1) | 52 | W |
| | | (Note 1a) | 3.8 | |
| | | (Note 1b) | 1.6 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +175 | °C |
| **Thermal Characteristics** | | | | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 2.9 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 96 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDD306P | FDD306P | 13” | 16mm | 2500 units |

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## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –12 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | –0.6 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V | | | –1 | µA |
| $I_{GSSF}$ | Gate–Body Leakage | $V_{GS}$ = ±8V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –0.4 | –0.5 | –1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | 2.2 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –6.7 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –6.1 A<br>$V_{GS}$ = –1.8 V, $I_D$ = –4.8 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –6.7A, $T_J$ = 125°C | | 21<br>29<br>42<br>25 | 28<br>41<br>90 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –4.5 V, $V_{DS}$ = –5 V | –45 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –6.7 A | | 22 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –6 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1290 | | pF |
| $C_{oss}$ | Output Capacitance | | | 590 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 430 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 4.2 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –6 V, $I_D$ = –1 A, $V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω | | 16 | 29 | ns |
| $t_r$ | Turn–On Rise Time | | | 8 | 16 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 34 | 54 | ns |
| $t_f$ | Turn–Off Fall Time | | | 41 | 65 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –6V, $I_D$ = –6.7 A, $V_{GS}$ = –4.5 V | | 15 | 21 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.0 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 4.4 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –3.2 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –3.2 A (Note 2) | | –0.8 | –1.2 | V |
| Trr | Diode Reverse Recovery Time | IF = –6.7 A, diF/dt = 100 A/µs (Note 3) | | 37 | | ns |
| Irm | Diode Reverse Recovery Current | | | 0.9 | | A |
| Qrr | Diode Reverse Recovery Charge | | | 17 | | nC |

**Notes:**

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in$^2$ pad of 2 oz copper



b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$ where $P_D$ is maximum power dissipation at $T_C$ = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS}$ = 10V.

4. Starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = -4 A, $V_{GS}$ = -10 V, $V_{DD}$ = -12 V.



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## Typical Characteristics

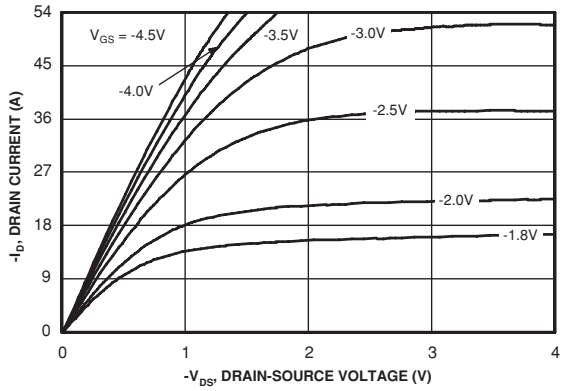



**Figure 1. On-Region Characteristics.**

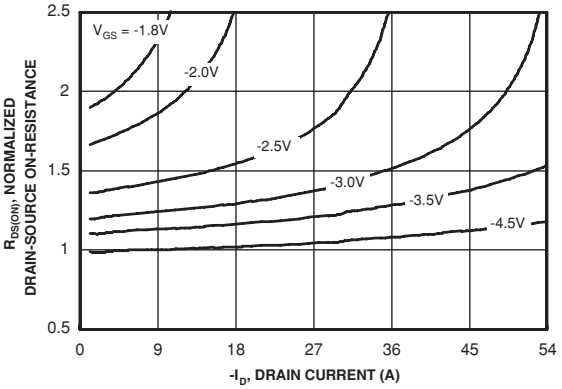



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

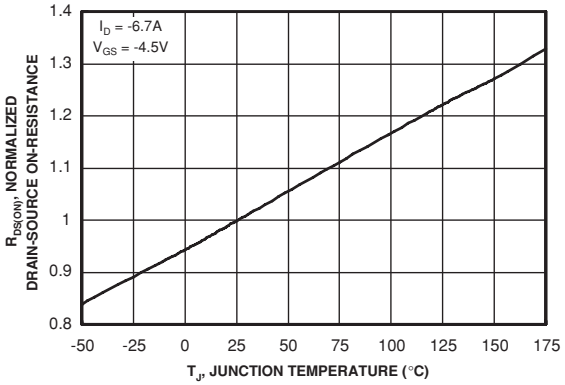



**Figure 3. On-Resistance Variation withTemperature.**

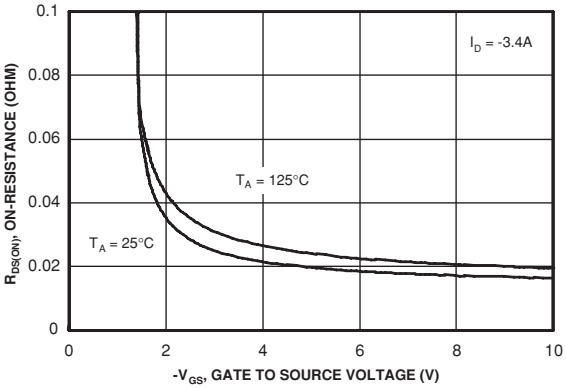



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

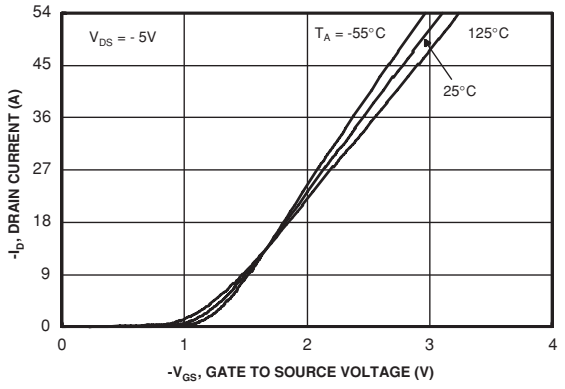



**Figure 5. Transfer Characteristics.**

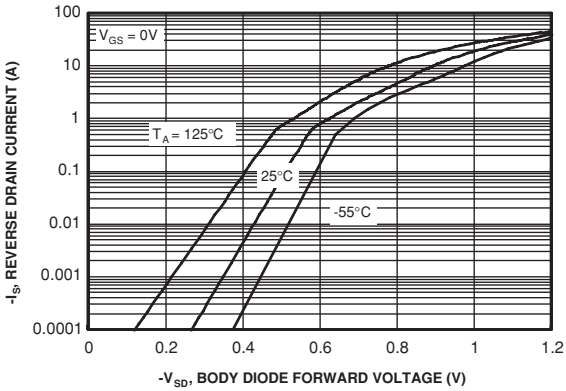



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**



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## Typical Characteristics

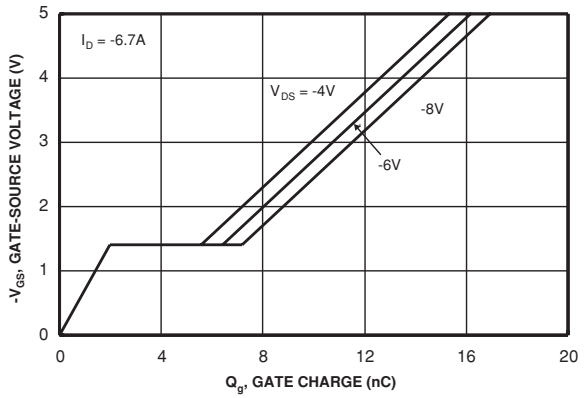



Figure 7. Gate Charge Characteristics.

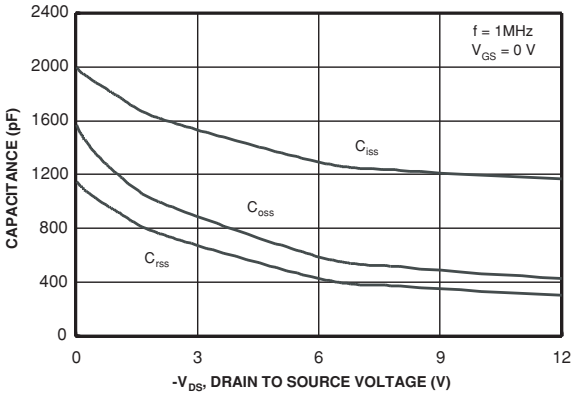



Figure 8. Capacitance Characteristics.

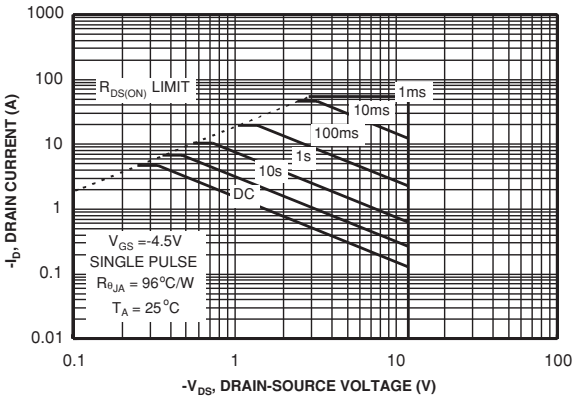



Figure 9. Maximum Safe Operating Area.

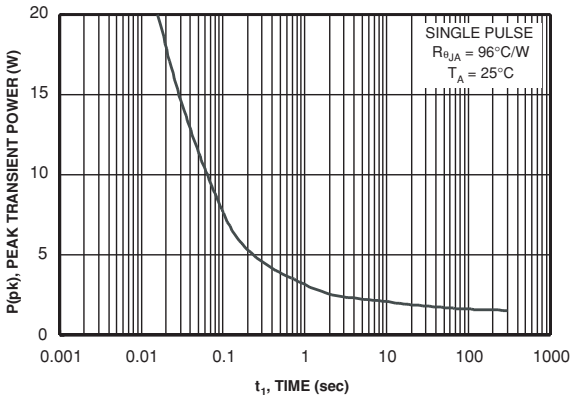



Figure 10. Single Pulse Maximum Power Dissipation.

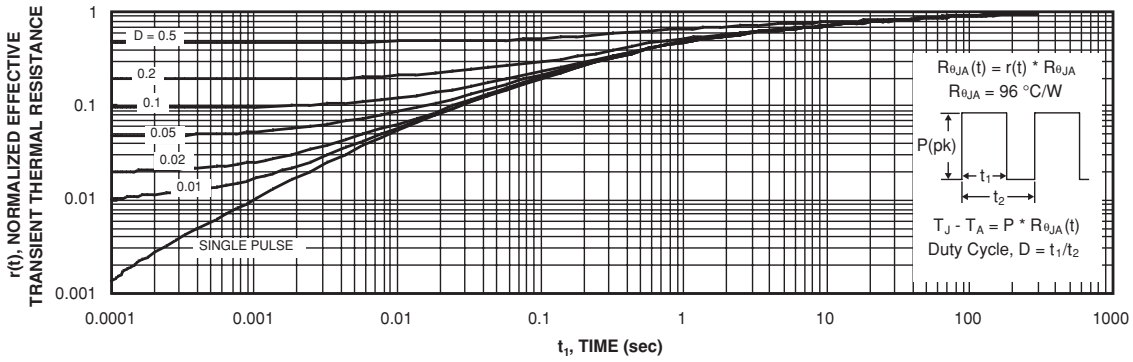
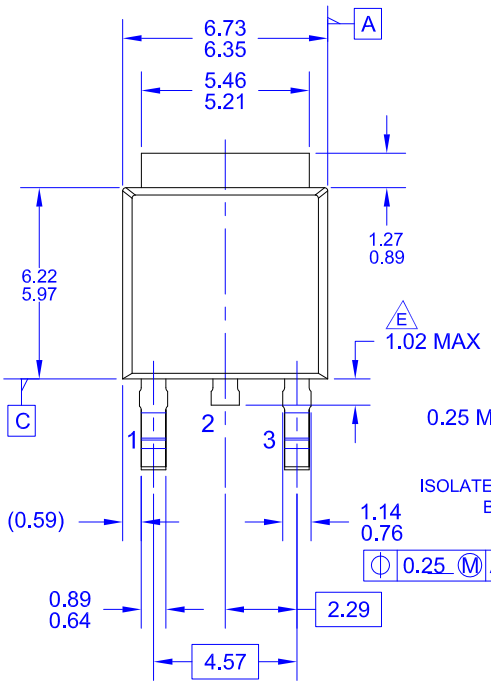



Figure 11. Transient Thermal Response Curve.

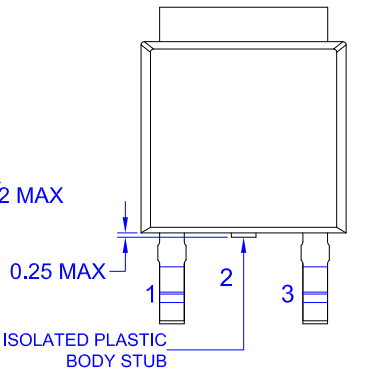
**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**



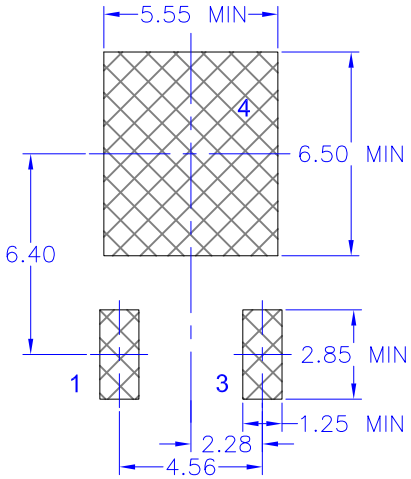
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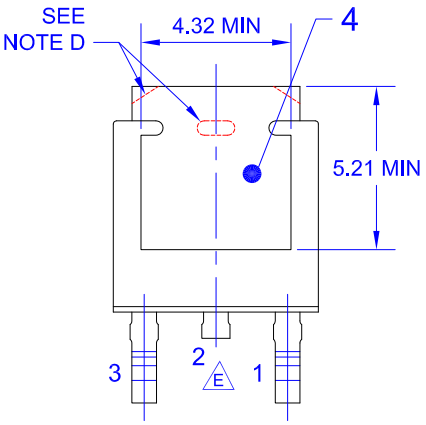

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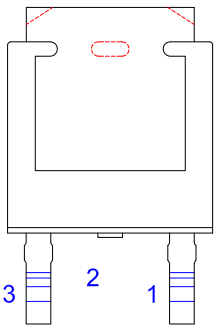

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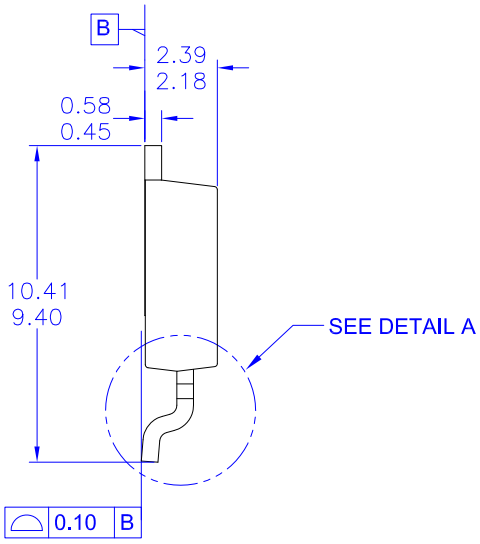

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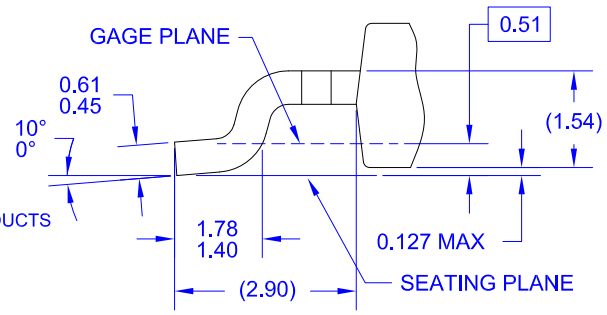



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