Si5340-EVB

Si5340 Evaluation Board User's Guide

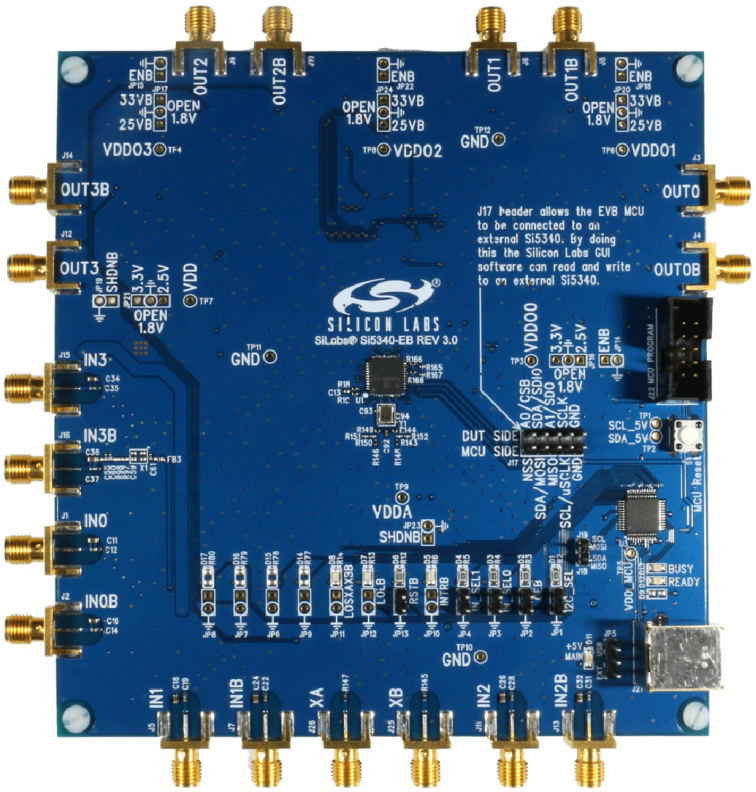
Description

The Si5340-EVB is used for evaluating the Si5340 Low Jitter Any-Frequency Clock Generator. The Si5340 uses the patented Multisynth™ technology to generate up to 10 independent clock frequencies each with 0 ppm synthesis error. The Si5340-EVB has 3 independent input clocks, an optional feedback input clock for zero delay mode, and 4 independent output clocks. The Si5340-EVB can be controlled and configured using the Clock Builder Pro™ (CB Pro™) software tool.

Features

- Powered from USB port or external power supply
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5340 or up to 3 input clocks for synchronous clocking
- Feedback clock input for optional zero delay mode
- CBPro™ GUI-programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI-programmable VDDO supplies allow each of the 4 outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5340
- SMA connectors for input and output clocks

Si5340 Evaluation Board



1. Functional Block Diagram

Below is a functional block diagram of the Si5340-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section “3. Quick Start” or Section “9. Installing ClockBuilderPro (CBPro) Desktop Software” for more information.

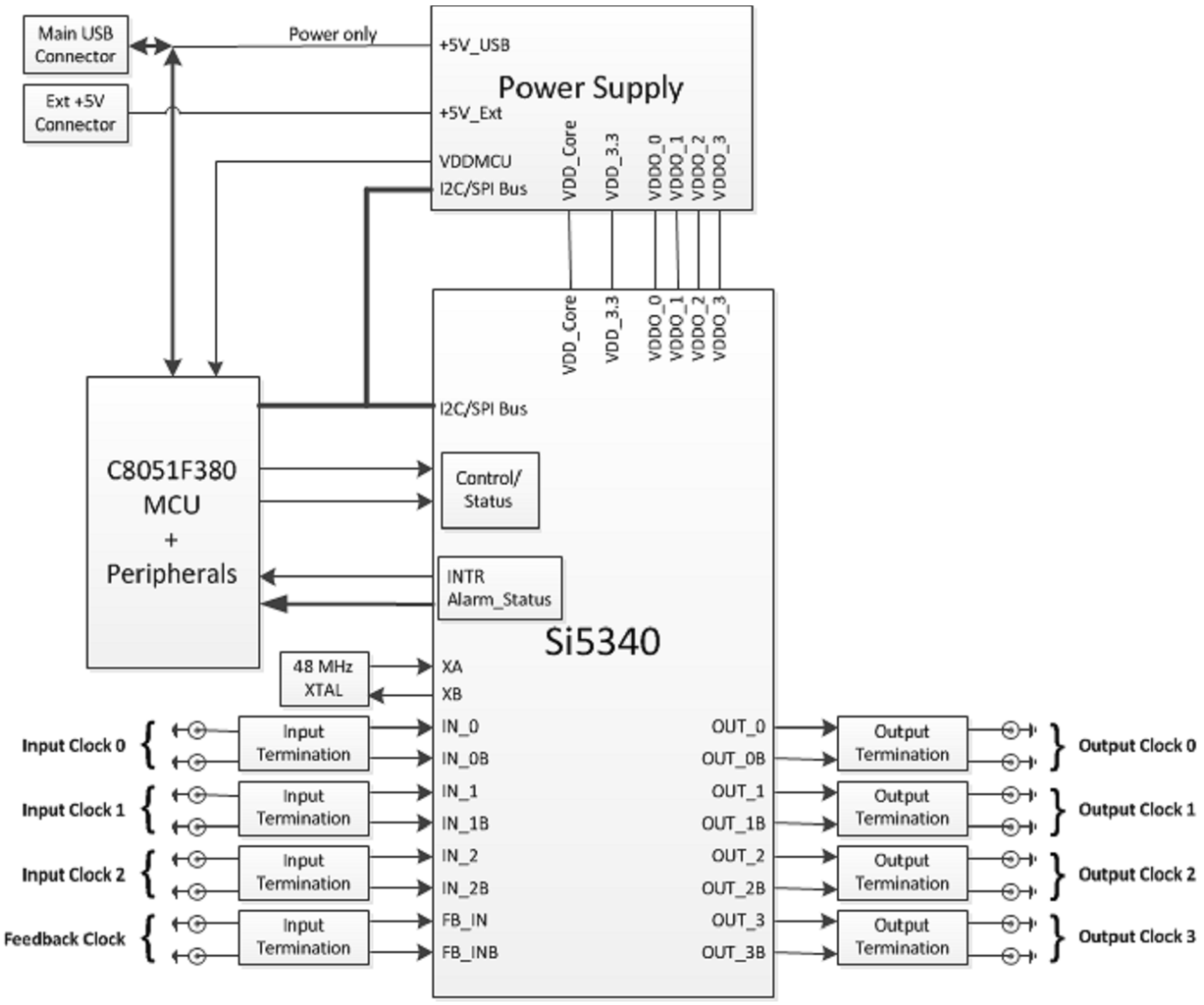


Figure 1. Si5340-EVB Block Diagram

2. Si5340 EVB Support Documentation and ClockBuilderPro™ Software

All Si5340 schematics, BOMs, User's Guides, and software can be found on-line at the following link:

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

3. Quick Start

1. Install ClockBuilderPro™ desktop software: http://www.silabs.com/CBPro
2. Connect a USB cable from the Si5340-EVB to the PC where the software is installed.
3. Leave the jumpers as installed from the factory and launch the ClockBuilderPro™ software.
4. You can use ClockBuilderPro™ to create, download, and run a frequency plan on the Si5340-EVB.
5. For Si5340 data sheet go to: http://www.silabs.com/timing

4. Jumper Defaults

Si5340 EVB Jumper Defaults						
Location	**Type**	**I = Installed 0 = Open**		**Location**	**Type**	**I = Installed 0 = Open**
JP1	2 pin	I		JP14	2 pin	O
JP2	2 pin	I		JP15	2 pin	O
JP3	2 pin	O		JP16	3 pin	all open
JP4	2 pin	O		JP17	3 pin	all open
JP5	3 pin	1 to 2		JP18	2 pin	O
JP6	2 pin	O		JP19	2 pin	O
JP7	2 pin	O		JP20	3 pin	all open
JP8	2 pin	O		JP21	3 pin	all open
JP9	2 pin	O		JP22	2 pin	O
JP10	2 pin	O		JP23	2 pin	O
JP11	2 pin	O		JP24	3 pin	all open
JP12	2 pin	O				
JP13	2 pin	O		JP17	5x2 Hdr	All 5 installed
Note: Refer to the Si5340 EVB schematics for the functionality associated with each jumper.						

5. Status LEDs

Si5340 EVB Status LEDs			
Location	**Silkscreen**	**Color**	**Status Function Indication**
D5	INTRB	Blue	DUT Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB	Blue	DUT Loss of Reference
D11	+5V MAIN	Green	Main USB +5V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

D11 is illuminated when USB +5V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.

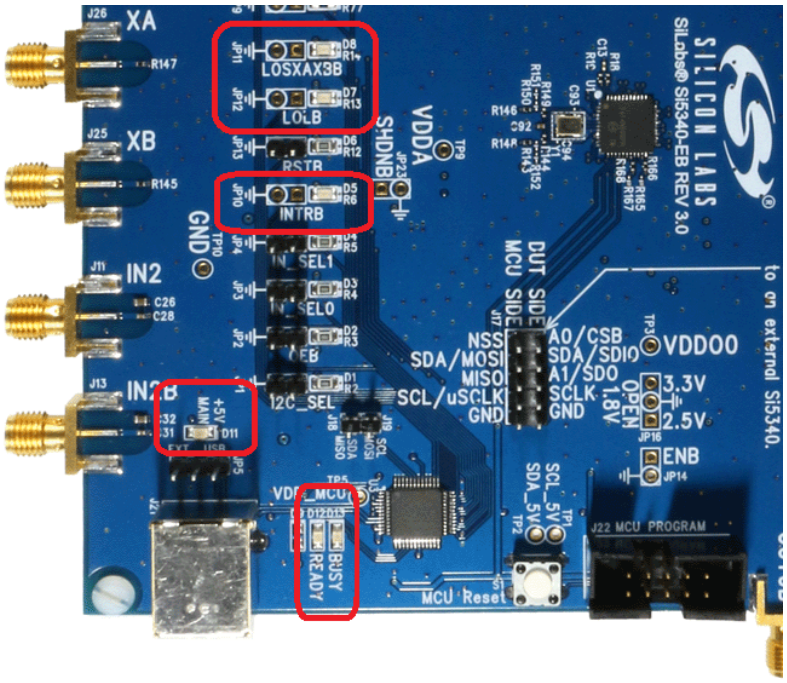


Figure 2. Status LEDs

6. External Reference Input (XA/XB)

An external reference (XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5340-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with a REFCLK, C93 and C94 must be populated and the XTAL removed (see Figure 3 below). The REFCLK can then be applied to J25 and J26.

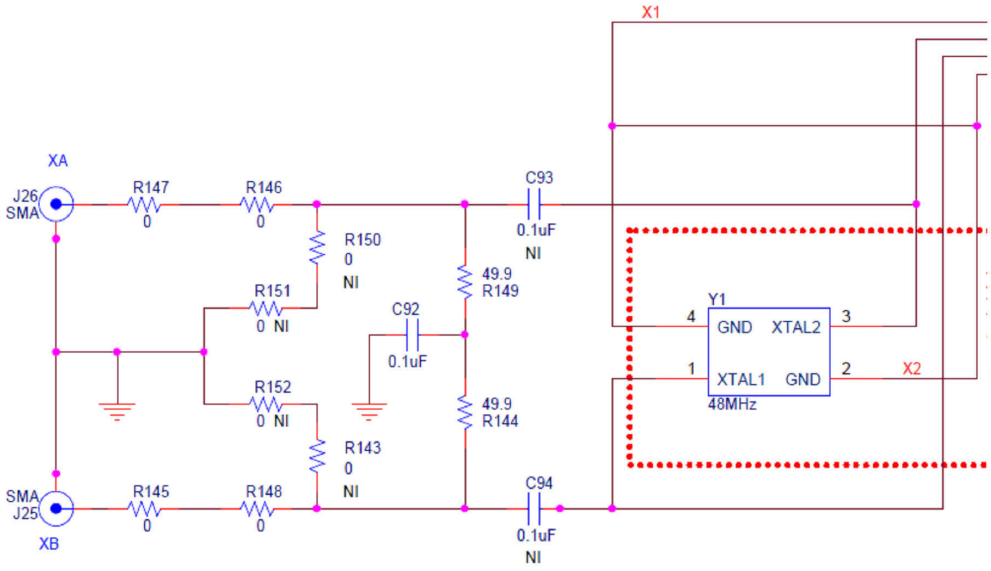


Figure 3. External Reference Input Circuit

7. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5340-EVB has eight SMA connectors (IN0/IN0B – IN2/IN2B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below.

Input clocks are AC coupled and 50-Ω terminated. This represents 4 differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5340 data sheet.

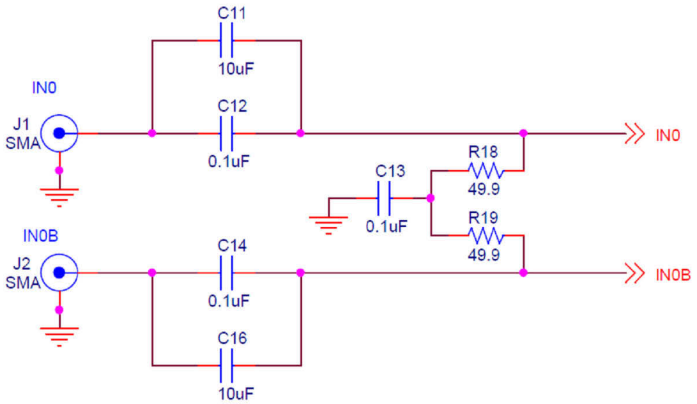


Figure 4. Input Clock Termination Circuit

8. Clock Output Circuits (OUTx/OUTxB)

Each of the 8 outputs (4 differential pairs) is AC coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal has no DC bias. If DC coupling is required, the AC coupling capacitors can be replaced with a resistor of appropriate value. The Si5340-EVB provides pads for optional output termination resistors and/or low frequency capacitors.

Note: Components with schematic "NI" designation are not normally populated on the Si5340-EVB and provide locations on the PCB for optional DC/AC terminations by the end user.

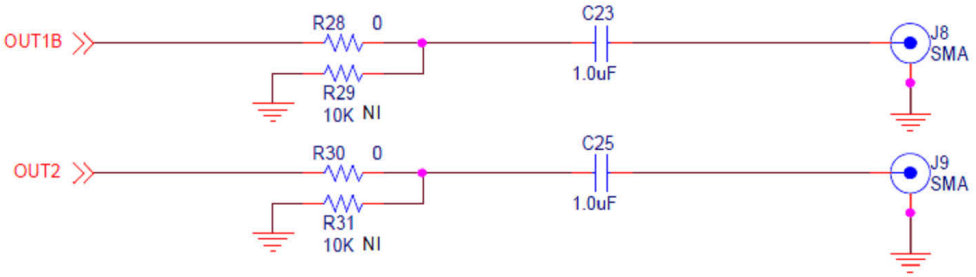


Figure 5. Output Clock Termination Circuit

9. Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBPro software on any Windows 7 (or later version) PC, do the following:

1. Go to http://www.silabs.com/CBPro/ and download ClockBuilderPro™ software.
2. Installation instructions and User's Guide for ClockBuilderPro™ can be found at the download link shown above. Please follow the instructions as indicated.

10. Using the Si5340 EVB

10.1. Connecting the EVB to Your Host PC

Once the ClockBuilderPro™ software in installed, connect the PC to the EVB with a USB cable as illustrated in Figure 6.

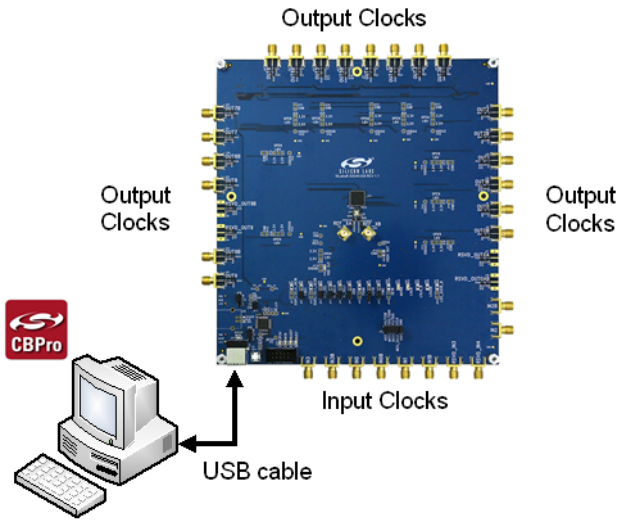


Figure 6. EVB Connection Diagram

10.2. Overview of ClockBuilderPro™ Applications

The ClockBuilderPro™ installer installs two main applications: the ClockBuilderPro Wizard and the EVB GUI.

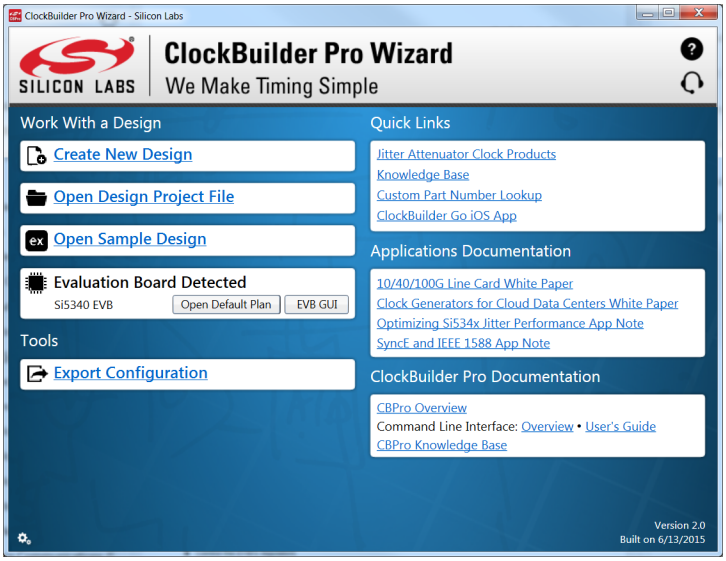


Figure 7. Application #1: ClockBuilderPro Wizard

Use the CBPro Wizard to do the following:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

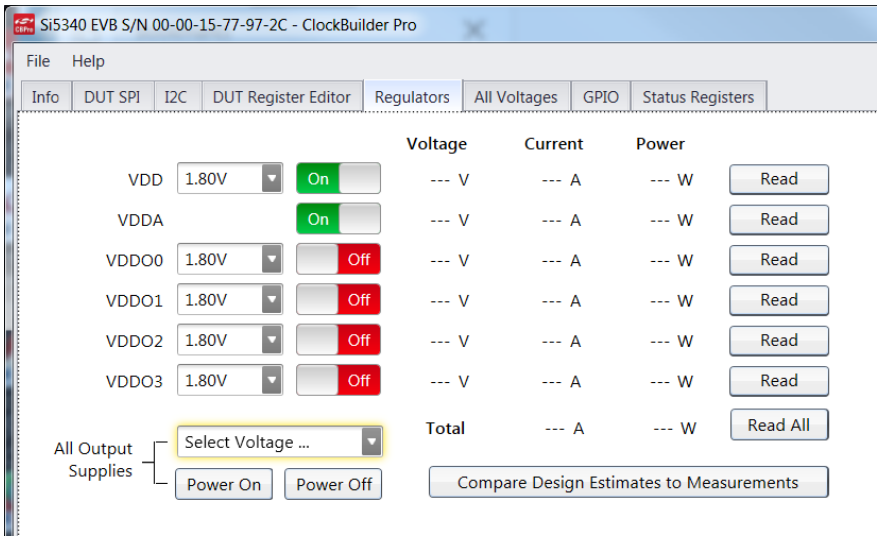


Figure 8. Application #2: EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5340)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

10.3. Common ClockBuilderPro™ Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5340 EVB. These workflow scenarios are as follows:

- Workflow Scenario #1: Testing a Silicon Labs-created default configuration
- Workflow Scenario #2: Modifying the default Silicon Labs-created device configuration
- Workflow Scenario #3: Testing a user-created device configuration

Each workflow scenario is described in more detail in the following sections.

10.3.1. Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

1. Once the PC and EVB are connected, launch ClockBuilder Pro by clicking this icon on your PC's desktop:

Figure 9. ClockBuilderPro Desktop Icon

2. If an EVB is detected, click on the **Open Default Plan** button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

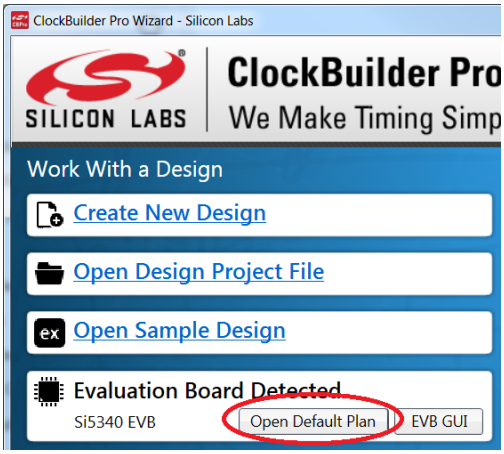


Figure 10. Open Default Plan

3. Once you open the default plan (based on your EVB model number), a popup window appears.

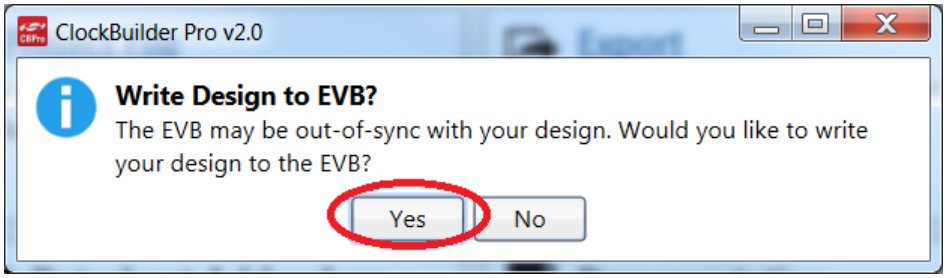


Figure 11. Write Design to EVB Dialog

4. Select **Yes** to write the default plan to the Si5340 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

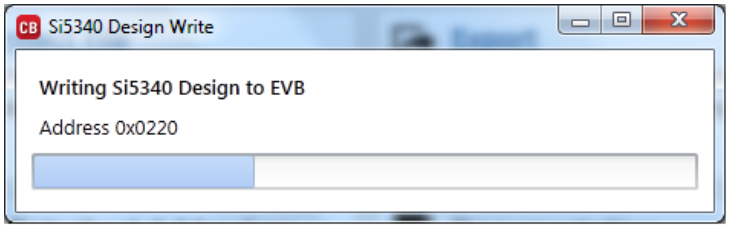


Figure 12. Writing Design Status

5. After CBPro writes the default plan to the EVB, click on **Open EVB GUI** as shown in Figure 13.

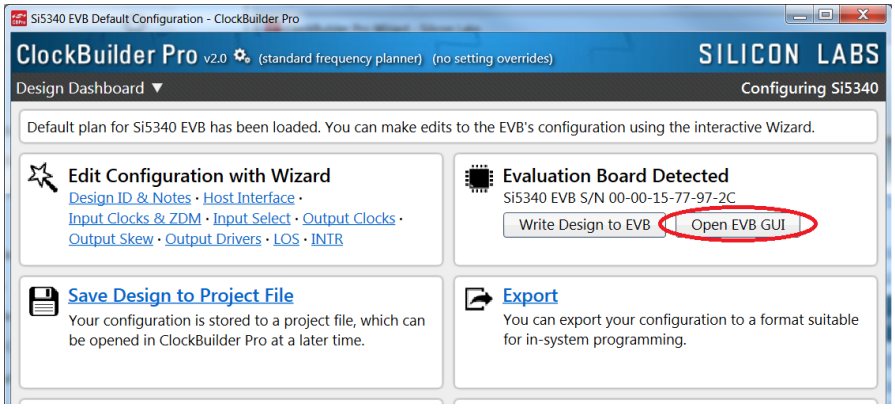


Figure 13. Open EVB GUI

6. The EVB GUI opens.
   Note: All power supplies are set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown in Figure 14.

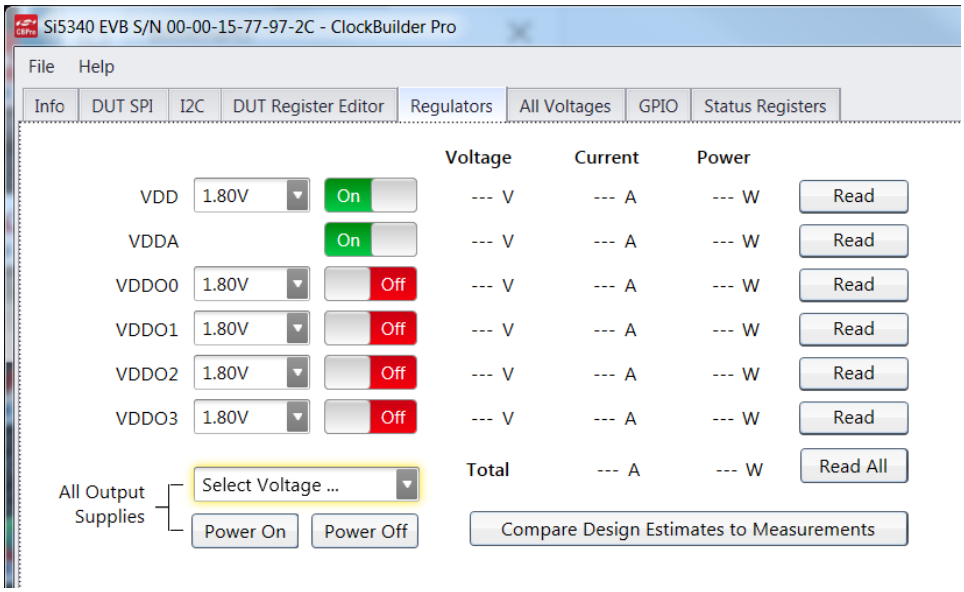


Figure 14. EVB GUI Window

Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the **Read All** button (the bottom-right of Figure 14) and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA power supplies "Off" and then "On" will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select **Write Design to EVB**:

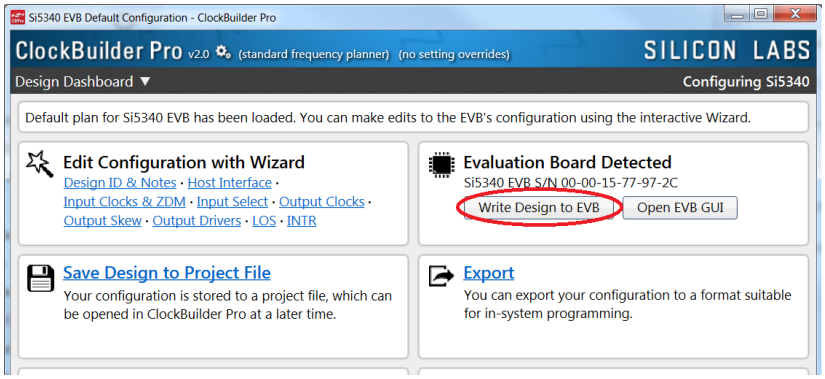


Figure 15. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running in free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on **View Design Report** as highlighted in Figure 16.

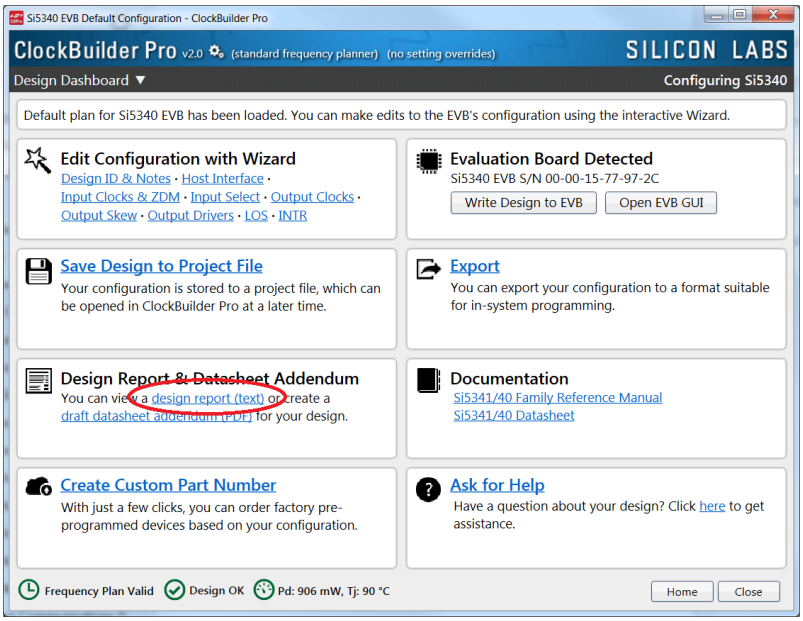


Figure 16. View Design Report

Your configuration's design report appears in a new window, shown in Figure 17. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

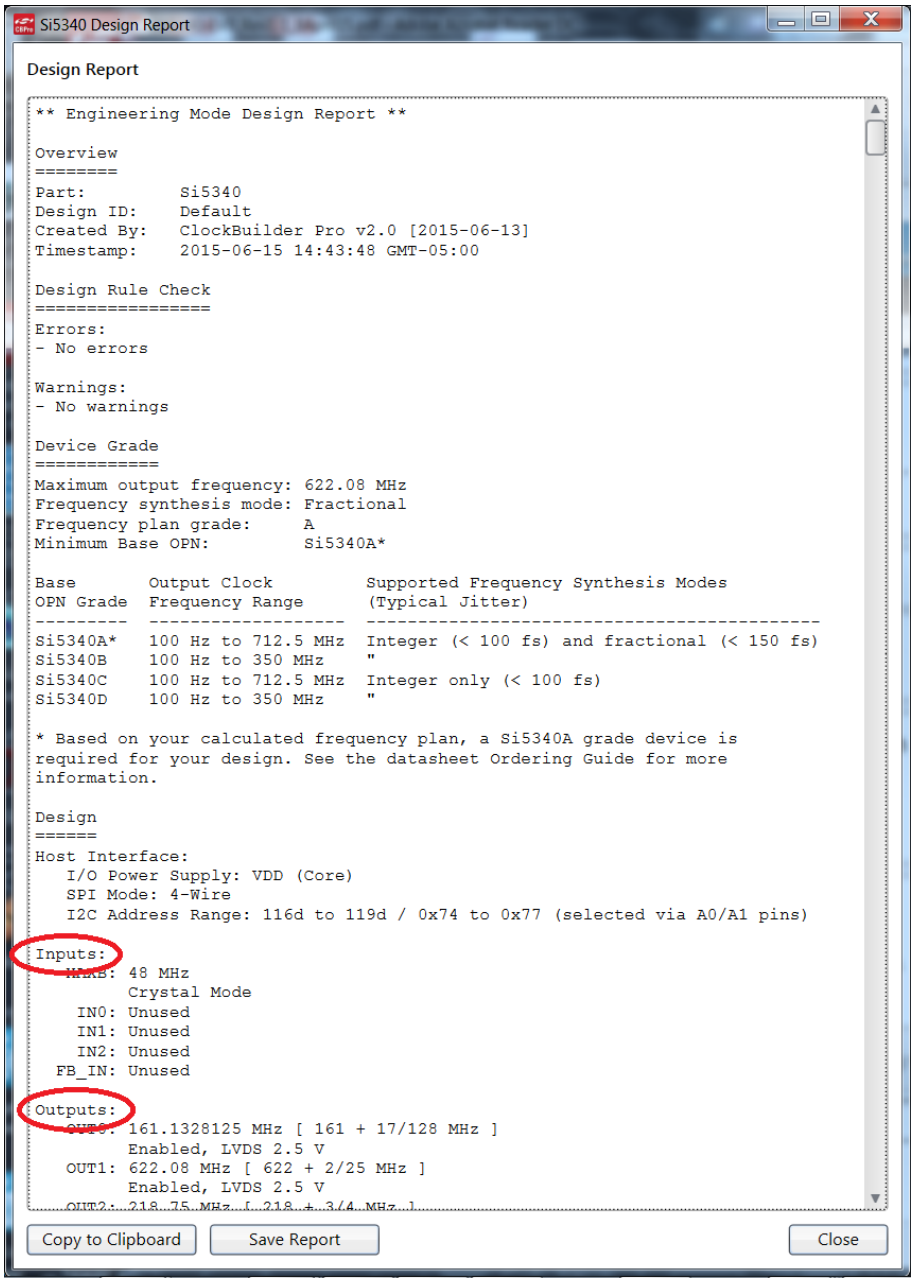


Figure 17. Design Report Window

Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

10.3.2. Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on **Edit Configuration with Wizard**.

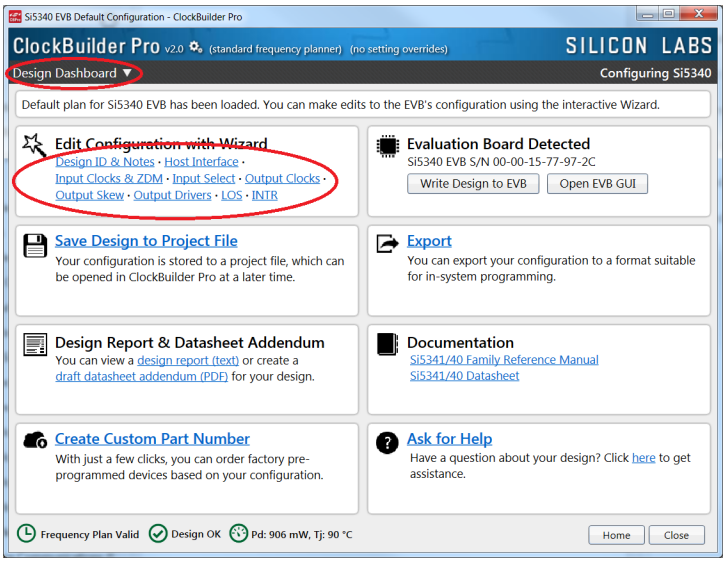


Figure 18. Edit Configuration with Wizard

You are then taken to the Wizard's step-by-step menus which allow you to change any of the default plan's operating configurations.

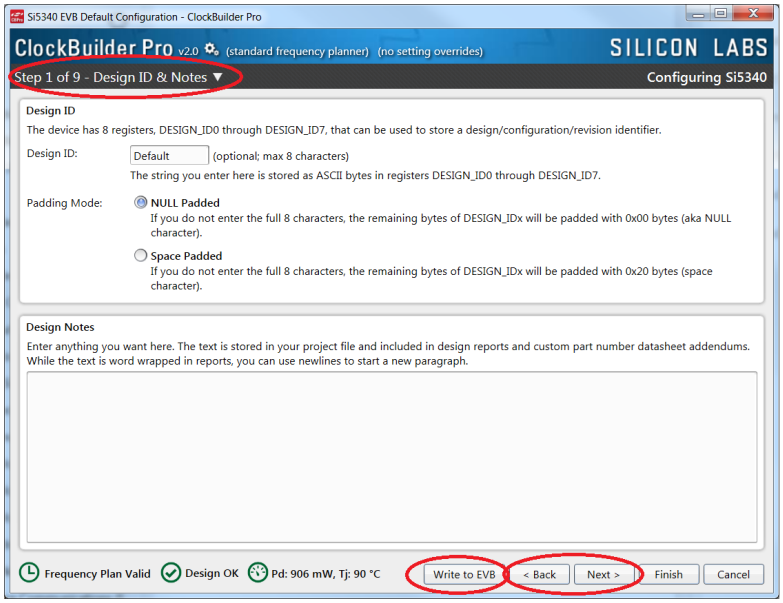


Figure 19. Design Wizard

Note: You can click on the icon on the lower left hand of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on **Write to EVB** to update the DUT to reconfigure your device in real-time. The Design Write status window opens each time you make a change.

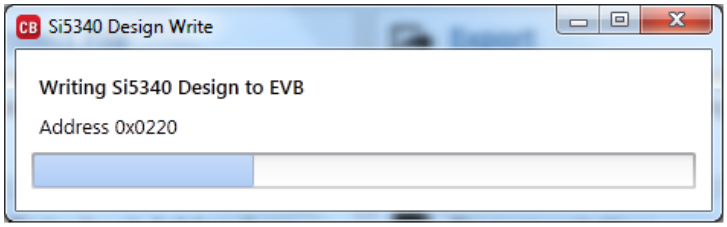


Figure 20. Writing Design Status

10.3.3. Workflow Scenario #3: Testing a User-Created Device Configuration

1. To test a previously-created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting **Open Design Project File**.

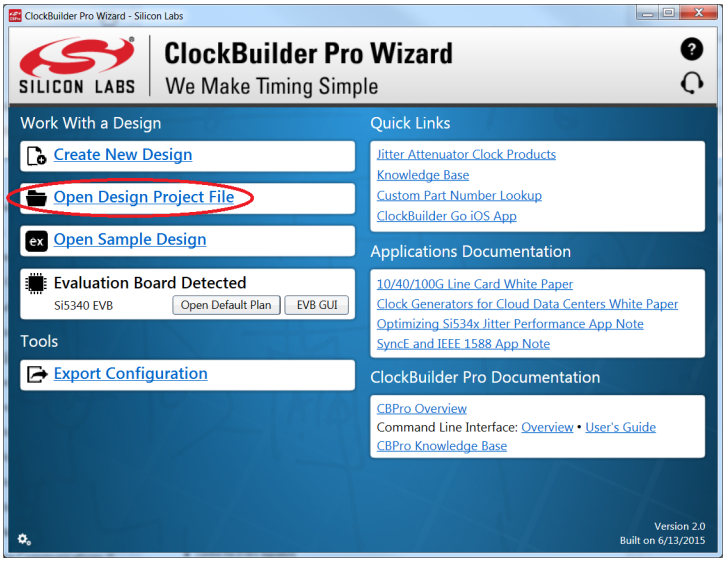


Figure 21. Open Design Project File

2. Locate your CBPro design file (*.slabtimeproj or *.sitproj file) in the Windows file browser.

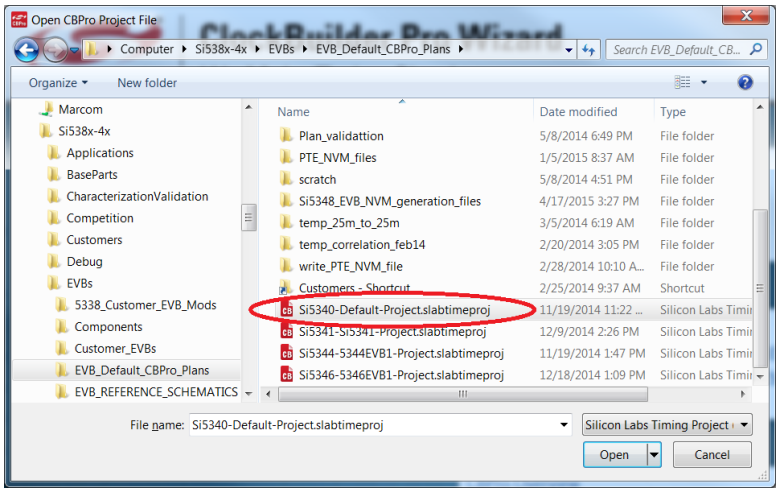


Figure 22. Browse for Project Files

3. Select **Yes** when the *Write Design to EVB* popup appears.

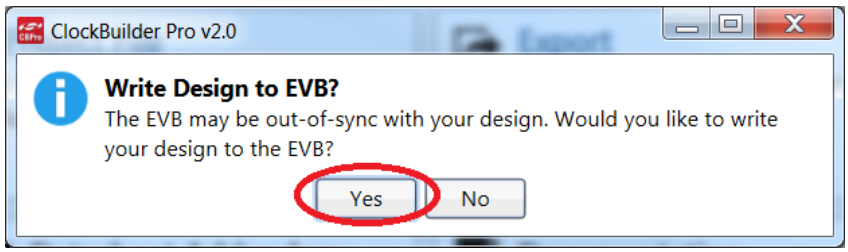


Figure 23. Write Design to EVB Dialog

4. The progress bar is launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.4. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting **Export** as shown in Figure 24.

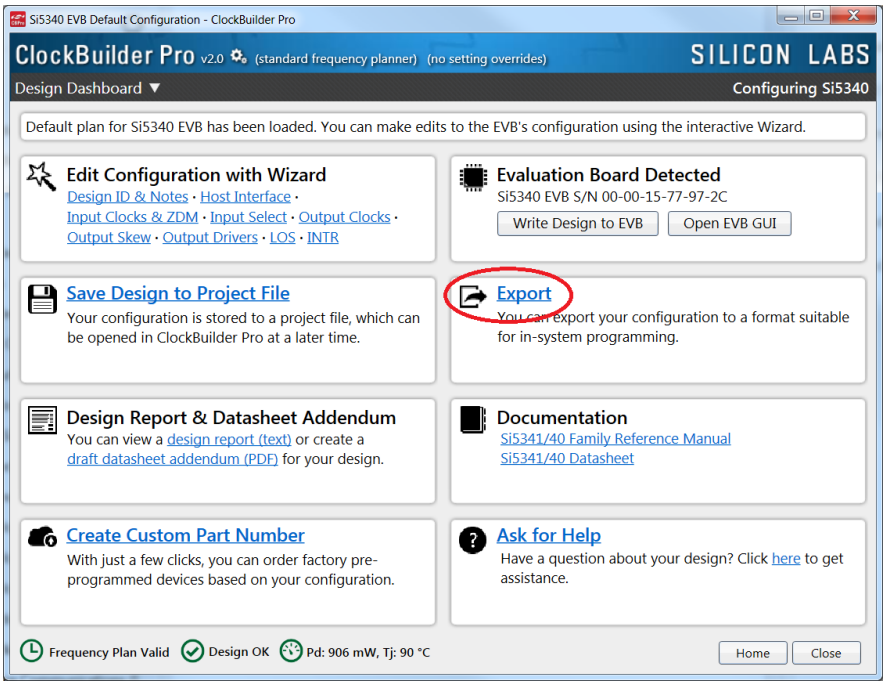


Figure 24. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

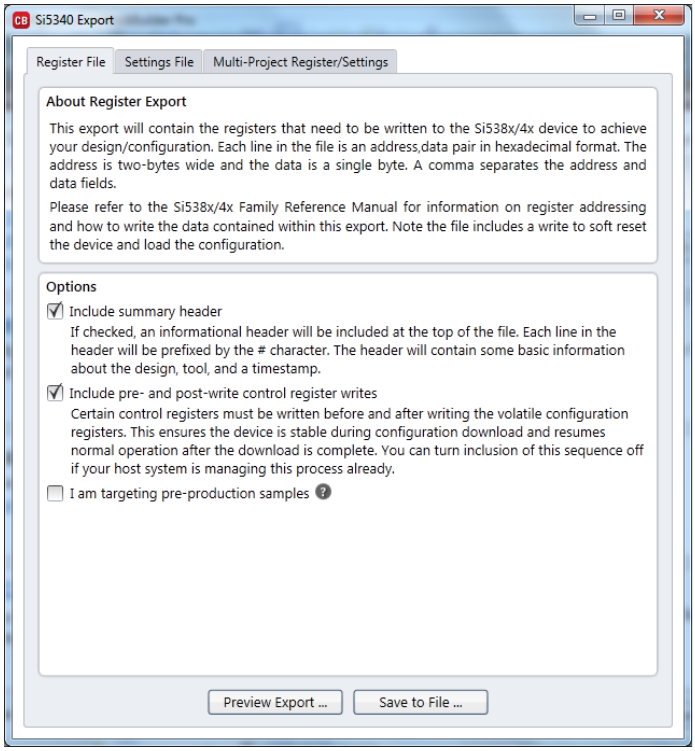


Figure 25. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device's non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5340 using ClockBuilderPro on the Si5340 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5340 RAM space and can be done virtually unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device datasheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

12. Serial Device Communications (Si5340 <—> MCU)

12.1. On-Board SPI Support

The MCU on-board the Si5340-EVB communicates with the Si5340 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5340 device is the SPI slave. The Si5340 device can also support a 2-wire I2C serial interface, although the Si5340-EVB does NOT support the I2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I2C.

12.2. External I2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5340 pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5340 device. The shunt at JP1 (I2C_SEL) must also be removed to select I^2C as Si5340 interface type. An external I2C controller connected to the Si5340 side of J17 can then communicate to the Si5340 device. (For more information on I^2C signal protocol, please refer to the Si5340 data sheet.)

Figure 26 below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5340 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I^2C operation should use J17 pin 4 (DUT_SDA_SDIO) as the I^2C SDA and J17 pin 8 (DUT_SCLK) as the I^2C SCLK. Please note the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

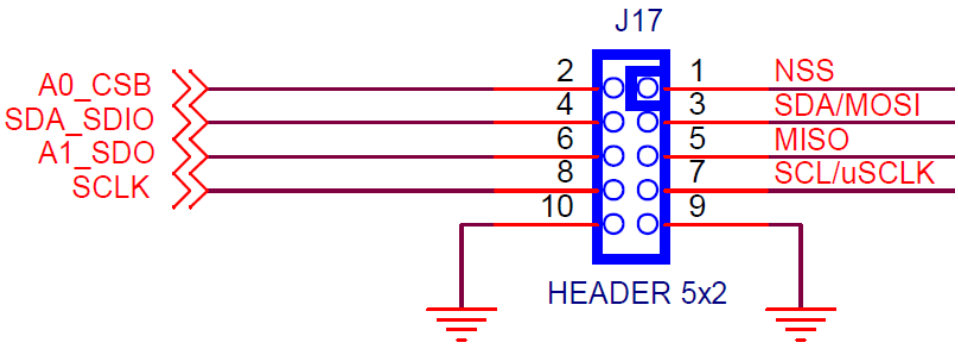


Figure 26. Serial Communications Header J17

13. Si5340-EVB Schematic and Bill of Materials (BOM)

The Si5340 EVB Schematic and Bill of Materials (BOM) can be found online at:

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

Please be aware the Si5340 EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

Document Change List

Revision 1.0

- Initial Release

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