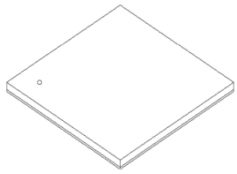
CMOS Digital Integrated Circuit Silicon Monolithic

TC358743XBG

Mobile Peripheral Devices

TC358743XBG



P-TFBGA64-0606-0.65-001

Weight: 76 mg (typ.)

Overview

The HDMI®-RX to MIPI® CSI-2-TX is a bridge device that converts HDMI stream to MIPI CSI-2 TX.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input

TC358743XBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.

Features

- HDMI-RX Interface
  - ✧ HDMI-RX
    - Video Formats Support (Up to 1080P @60fps)
      - ➢ RGB, YCbCr444: 24-bpp @60fps
      - ➢ YCbCr422 24-bpp @60fps
    - Audio Supports
      - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - Support HDCP (optional)
    - DDC Support
    - EDID Support
      - ➢ Release A, Revision 1 (Feb 9, 2000)
      - ➢ First 128 bytes (EDID 1.3 structure)
      - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
      - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
    - Maximum HDMI clock speed: 165 MHz
  - ✧ Does not support Audio Return Path and HDMI Ethernet Channels
- CSI-2 TX Interface
  - ✧ MIPI CSI-2 compliant
  - ✧ Supports up to 1 Gbps per data lane
    - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
  - ✧ Supports up to 4 data lanes
- I^2C Target Interface
  - ✧ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
  - ✧ Support Ultra Fast-mode (2 MHz)
  - ✧ Configure all TC358743XBG internal registers
- Audio Output Interface

  Either I^2S or TDM Audio interface available (pins are multiplexed)

  I^2S Audio Interface
  - ✧ Single data lane for stereo data
  - ✧ Support Controller Clock mode only
  - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
  - ✧ Support Left or Right-justify with MSB first
  - ✧ Support 32 bit-wide time-slot only
  - ✧ Output Audio Oversampling clock (256fs)

  TDM (Time Division Multiplexed) Audio Interface
  - ✧ Fixed to 8 channels (depend on HDMI input stream)
  - ✧ Support 32 bit-wide time slot only
  - ✧ Support Controller Clock mode only
  - ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
  - ✧ Output Audio Oversampling clock (256fs)
- InfraRed (IR)
  - ✧ Support NEC Infrared protocol.
- System
  - ✧ Internal core has two power domains (VDDC1 and VDDC2)
    - VDDC1 is always on power domain
    - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
  - ✧ Core and MIPI D-PHY: 1.2 V
  - ✧ I/O: 1.8V – 3.3 V
  - ✧ HDMI-RX: 3.3 V
  - ✧ APLL: 3.3 V/2.5 V
- Power Consumption during typical operations
  - ✧ 720P: 0.48 W
  - ✧ 1080P @30fps: 0.48 W
  - ✧ 1080P @60fps: 0.54 W

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Table of contents

REFERENCES 5
1. Overview 6
2. Features 7
3. External Pins 10
3.1. TC358743XBG BGA64 Pin Count Summary 12
3.2. Pin Layout 12
4. Package 13
5. Electrical Characteristics 15
5.1. Absolute Maximum Ratings 15
5.2. Operating Condition 15
5.3. DC Electrical Specification 16
6. Revision History 17
RESTRICTIONS ON PRODUCT USE 18

List of Figures

Figure 1.1 TC358743XBG System Overview 6
Figure 2.1 Package Marking with HDCP Key, HAL is appended to lot code 9
Figure 2.2 Package Marking without HDCP Key, HNL is appended to lot code 9
Figure 3.1 TC358743XBG 64-Pin Layout (Top View) 12
Figure 4.1 TC358743XBG package (64 pins) 13

List of Tables

Table 2.1 TC358743XBG Power Consumption during typical operations 8
Table 3.1 TC358743XBG Functional Signal List 10
Table 3.2 BGA64 Pin Count Summary 12
Table 4.1 Mechanical Dimension 14
Table 6.1 Revision History 17

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1. Overview

The HDMI-RX to MIPI CSI-2-TX is a bridge device that converts HDMI stream to MIPI CSI-2 TX.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input

TC358743XBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.

TC358743XBG System Overview block diagram is shown below.

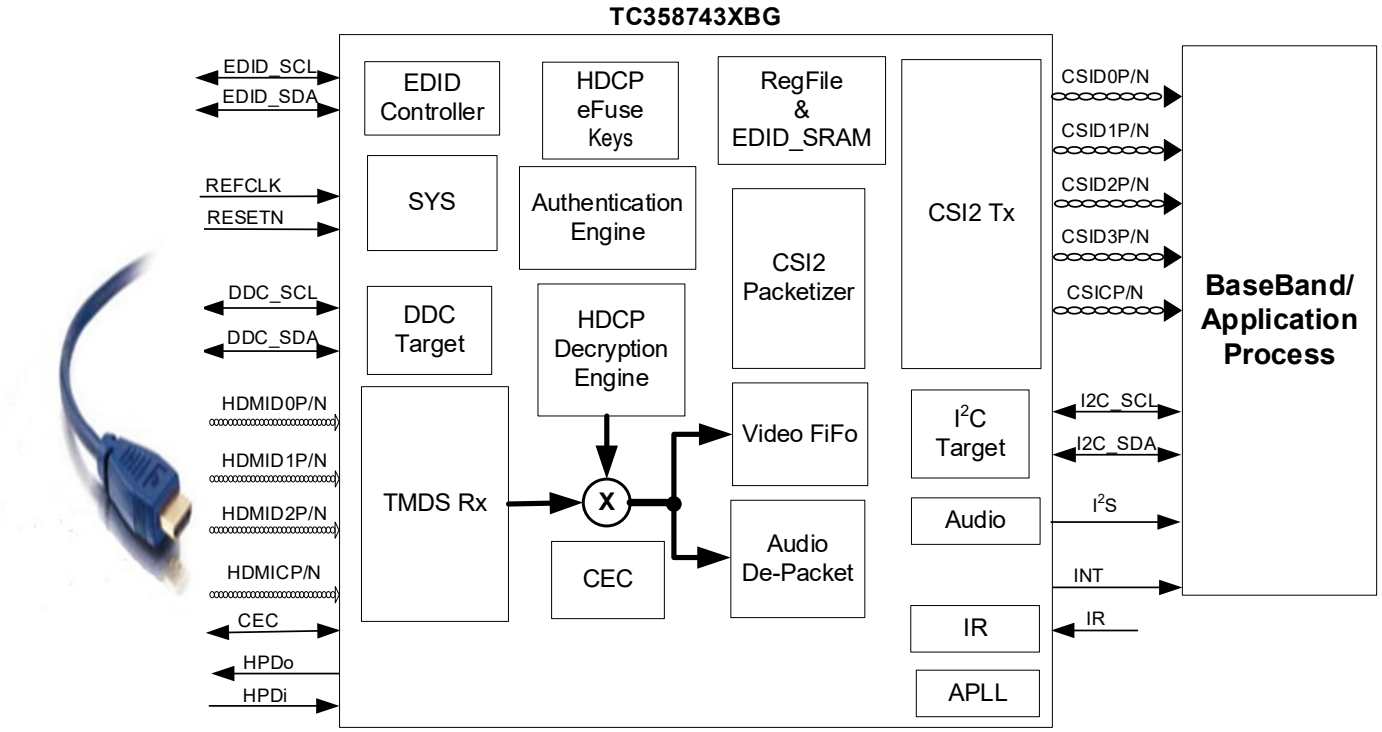


Figure 1.1 TC358743XBG System Overview

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2. Features

Below are the main features supported by TC358743XBG.

- HDMI-RX Interface
  - ✧ HDMI-RX 1.4
    - Video Formats Support (Up to 1080P @60fps)
      - ➢ RGB, YCbCr444: 24-bpp @60fps
      - ➢ YCbCr422 24-bpp @60fps
    - Audio Supports
      - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - Support HDCP (optional)
    - DDC Support
    - EDID Support
      - ➢ Release A, Revision 1 (Feb 9, 2000)
      - ➢ First 128 bytes (EDID 1.3 structure)
      - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
      - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
    - Maximum HDMI clock speed: 165 MHz
  - ✧ Does not support Audio Return Path and HDMI Ethernet Channels

- CSI-2 TX Interface
  - ✧ MIPI CSI-2 compliant
  - ✧ Supports up to 1 Gbps per data lane
    - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
  - ✧ Supports up to 4 data lanes

- I^2C Target Interface
  - ✧ Support for Normal-mode (100 kHz) and Fast-mode (400 kHz)
  - ✧ Support Ultra Fast-mode (2 MHz)
  - ✧ Configure all TC358743XBG internal registers

- Audio Output Interface

  Either I^2S or TDM Audio interface available (pins are multiplexed)

  I^2S Audio Interface
  - ✧ Single data lane for stereo data
  - ✧ Support Controller Clock mode only
  - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
  - ✧ Support Left or Right-justify with MSB first
  - ✧ Support 32 bit-wide time-slot only
  - ✧ Output Audio Oversampling clock (256fs)

  TDM (Time Division Multiplexed) Audio Interface
  - ✧ Fixed to 8 channels (depend on HDMI input stream)
  - ✧ Support 32 bit-wide time slot only
  - ✧ Support Controller Clock mode only

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- ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
- ✧ Output Audio Oversampling clock (256fs)

- InfraRed (IR)
  - ✧ Support NEC Infrared protocol.

- System
  - ✧ Internal core has two power domains (VDDC1 and VDDC2)
    - VDDC1 is always on power domain
    - VDDC2 can be shut-off during deep sleep mode

- Power supply inputs
  - ✧ Core and MIPI D-PHY: 1.2 V
  - ✧ I/O: 1.8 V – 3.3 V
  - ✧ HDMI-RX: 3.3 V
  - ✧ APLL: 3.3 V/2.5 V

- Power Consumption during typical operations
  - ✧ 720P : 0.48 W
  - ✧ 1080P @30fps: 0.48 W
  - ✧ 1080P @60fps: 0.54 W

Table 2.1 TC358743XBG Power Consumption during typical operations

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDD25	Total Power	Unit
		1.2	1.2	3.3	1.8	1.2	3.3	1.2	2.5		
720P @60Frames	Current (A)	0.0472		0	0.0009	0.0178	0.0879	0.0656	0.0128	480.47	mW
	Power (W)	0.05664		0	0.0017	0.0214	0.2901	0.0787	0.032		
1080P @60Frames	Current (A)	0.0766		0	0.0009	0.0228	0.0881	0.0829	0.0128	543.19	mW
	Power (W)	0.09192		0	0.0017	0.0274	0.2907	0.0995	0.032		
Sleep 0x0002 = 0x0001	Current (μA)	0.91		0.002	0.0430	0.0490	32.3700	0.3200	0.2	108.94	μW
	Power (μW)	1.092		0.0066	0.0774	0.0588	106.8210	0.3840	0.5		

Note:

- Attention about ESD. This product is weak against ESD. Please handle it carefully.
- TC358743XBG does not perform YCbCr ↔ YUV conversion. In this document they are used interchangeably.
- TC358743XBG is provided with and without HDCP keys. They are identified with package mark shown below.
  - Figure 2.1, indicates HDCP keys are burned into the device.
  - Figure 2.2, shows HDCP key is not included, please ignore all the registers field related to HDCP functionality.

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Figure 2.1 Package Marking with HDCP Key, HAL is appended to lot code

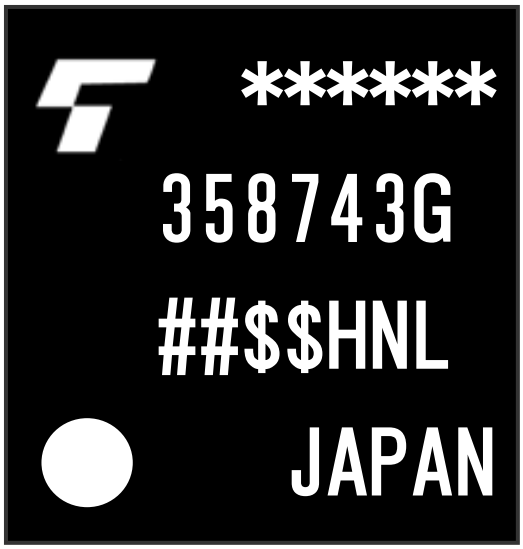


Figure 2.2 Package Marking without HDCP Key, HNL is appended to lot code

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3. External Pins

TC358743XBG resides in BGA64 pin packages. The following table gives the signals of TC358743XBG and their function.

Table 3.1 TC358743XBG Functional Signal List

Group	Pin Name	I/O	Init (O)	Type	Function	Voltage Supply	Note
System: Reset & Clock (4)	RESETN	I	-	Sch	System reset input, active low	VDDIO2	1.8 V - 3.3 V
	REFCLK	I	-	N	Reference clock input (27/26 MHz or 42 MHz)	VDDIO2	1.8 V - 3.3 V
	TEST	I	-	N	TEST mode select 0: Normal mode 1: Test mode	VDDIO2	1.8 V - 3.3 V
	INT	O	L	N	Interrupt Output signal – active high (Level)	VDDIO2	1.8 V - 3.3 V
CSI-2 TX (10)	CSICP	-	H	MIPI-PHY	MIPI-CSI-2 clock positive	VDD_MIPI	1.2 V
	CSICN	-	H	MIPI-PHY	MIPI-CSI-2 clock negative	VDD_MIPI	1.2 V
	CSID0P	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 positive	VDD_MIPI	1.2 V
	CSID0N	-	H	MIPI-PHY	MIPI-CSI-2 Data 0 negative	VDD_MIPI	1.2 V
	CSID1P	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 positive	VDD_MIPI	1.2 V
	CSID1N	-	H	MIPI-PHY	MIPI-CSI-2 Data 1 negative	VDD_MIPI	1.2 V
	CSID2P	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 positive	VDD_MIPI	1.2 V
	CSID2N	-	H	MIPI-PHY	MIPI-CSI-2 Data 2 negative	VDD_MIPI	1.2 V
	CSID3P	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 positive	VDD_MIPI	1.2 V
	CSID3N	-	H	MIPI-PHY	MIPI-CSI-2 Data 3 negative	VDD_MIPI	1.2 V
HDMI-RX (8)	HDMICP	-	-	HDMI-PHY	HDMI Clock channel positive	AVDD33	3.3 V
	HDMICN	-	-	HDMI-PHY	HDMI Clock channel negative	AVDD33	3.3 V
	HDMID0P	-	-	HDMI-PHY	HDMI Data 0 channel positive	AVDD33	3.3 V
	HDMID0N	-	-	HDMI-PHY	HDMI Data 0 channel negative	AVDD33	3.3 V
	HDMID1P	-	-	HDMI-PHY	HDMI Data 1 channel positive	AVDD33	3.3 V
	HDMID1N	-	-	HDMI-PHY	HDMI Data 1 channel negative	AVDD33	3.3 V
	HDMID2P	-	-	HDMI-PHY	HDMI Data 2 channel positive	AVDD33	3.3 V
	HDMID2N	-	-	HDMI-PHY	HDMI Data 2 channel negative	AVDD33	3.3 V
DDC (2)	DDC_SCL	IO	-	N (Note 2)	DDC Target Clock	VDDIO1	3.3 V (Note 1)
	DDC_SDA	IO	-	N (Note 2)	DDC Target data	VDDIO1	3.3 V (Note 1)
EDID (2)	EDID_SCL	IO	-	N (Note 2)	EDID Controller Clock	VDDIO2	1.8 V - 3.3 V
	EDID_SDA	IO	-	N (Note 2)	EDID Controller Data	VDDIO2	1.8 V - 3.3 V
CEC	CEC	IO	-	N (Note 2)	CEC signal	VDDIO1	3.3 V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	VDDIO1	3.3 V (Note 1)
	HPDO	O	L	N	Hot Plug Detect Output	VDDIO1	3.3 V
Audio (4)	A_SCK	O	L	N	I^2S/TDM Bit Clock signal	VDDIO2	1.8 V - 3.3 V
	A_WFS	O	L	N	I^2S Word Clock or TDM Frame Sync signal	VDDIO2	1.8 V - 3.3 V
	A_SD	O	L	N	I^2S/TDM data signal	VDDIO2	1.8 V - 3.3 V
	A_OSCK	O	L	N	Audio Oversampling Clock	VDDIO2	1.8 V - 3.3 V
IR	IR	I	-	Sch	Infrared signal	VDDIO2	1.8 V - 3.3 V
I^2C (2)	I2C_SCL	IO	-	N (Note 2)	I^2C serial clock	VDDIO2	1.8 V - 3.3 V
	I2C_SDA	IO	-	N (Note 2)	I^2C serial data	VDDIO2	1.8 V - 3.3 V
APLL (4)	BIASDA	O	L	-	BIAS signal Connect to AVSS through 0.1 µF when not used	-	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock Please leave open when not used	-	-
	PCKIN	I	-	-	Audio PLL Reference Input clock Connect to AVSS through 0.1 µF when not used	-	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1 µF when not used	-	-

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Group	Pin Name	I/O	Init (O)	Type	Function	Voltage Supply	Note
POWER (12)	VDDC1, VDDC2	-	-	-	VDD for Internal Core (3)	-	1.2 V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	-	3.3 V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	-	1.8 V - 3.3 V
	VDD_MIPI	-	-	-	VDD for the MIPI CSI-2 (2)	-	1.2 V
	AVDD12	-	-	-	HDMI PHY 1.2 V power supply (2)	-	1.2 V
	AVDD33	-	-	-	HDMI PHY 3.3 V power supply (2)	-	3.3 V
	AVDD25	-	-	-	APLL 2.5 V power supply (1)	-	2.5 V
Ground (10)	VSS	-	-	-	Ground	-	-
Misc (2)	REXT	-	-	-	External Reference Resistor, please connect to AVDD33 with a 2 kΩ resistor (± 1%)	-	-
	VPGM	-	-	-	eFuse program power supply, please tie to ground	-	-

Total 64 pins

Note 1: These IO are 5 V tolerant.
Note 2: Bi-directional IO with Schmitt triggered input.

Buffer Type Abbreviation:

N: Normal IO
NPD: Normal IO with weak Internal Pull-Down
NPU: Normal IO with weak Internal Pull-Up
FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input
FS: Failed Safe IO
Sch: Schmitt input buffer
MIPI-PHY: front-end analog IO for CSI-2
HDMI-PHY: front-end analog IO for HDMI-RX

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3.1. TC358743XBG BGA64 Pin Count Summary

Table 3.2 BGA64 Pin Count Summary

Group Name	Pin Count
System	4
CSI-2 TX	10
HDMI-RX	8
DDC	2
EDID	2
CEC	1
HPD	2
Audio	4
IR	1
I^2C	2
APLL	4
POWER	12
Ground	10
Misc	2
TOTAL	**64**

3.2. Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8
REXT	VSS	VPGM	BIASDA	DAOUT	PFIL	CSID3N	CSID3P
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**
AVDD33	AVDD12	INT	IR	AVDD25	PCKIN	CSID2N	CSID2P
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**
HDMICP	HDMICN	VDDC2	VSS	VSS	VDD_MIPI	CSICN	CSICP
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**
HDMID0P	HDMID0N	AVDD12	VSS	VSS	VSS	CSID1N	CSID1P
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**
HDMID1P	HDMID1N	VSS	VSS	TEST	VSS	CSID0N	CSID0P
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
HDMID2P	HDMID2N	AVDD33	VDDIO1	VDDC2	VDD_MIPI	A_SCK	A_SD
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**
CEC	VDDC1	DDC_SDA	I2C_SDA	RESETN	EDID_SDA	A_WFS	A_OSCK
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**
HPDO	HPDI	DDC_SCL	I2C_SCL	REFCLK	EDID_SCL	VDDIO2	VSS

Figure 3.1 TC358743XBG 64-Pin Layout (Top View)

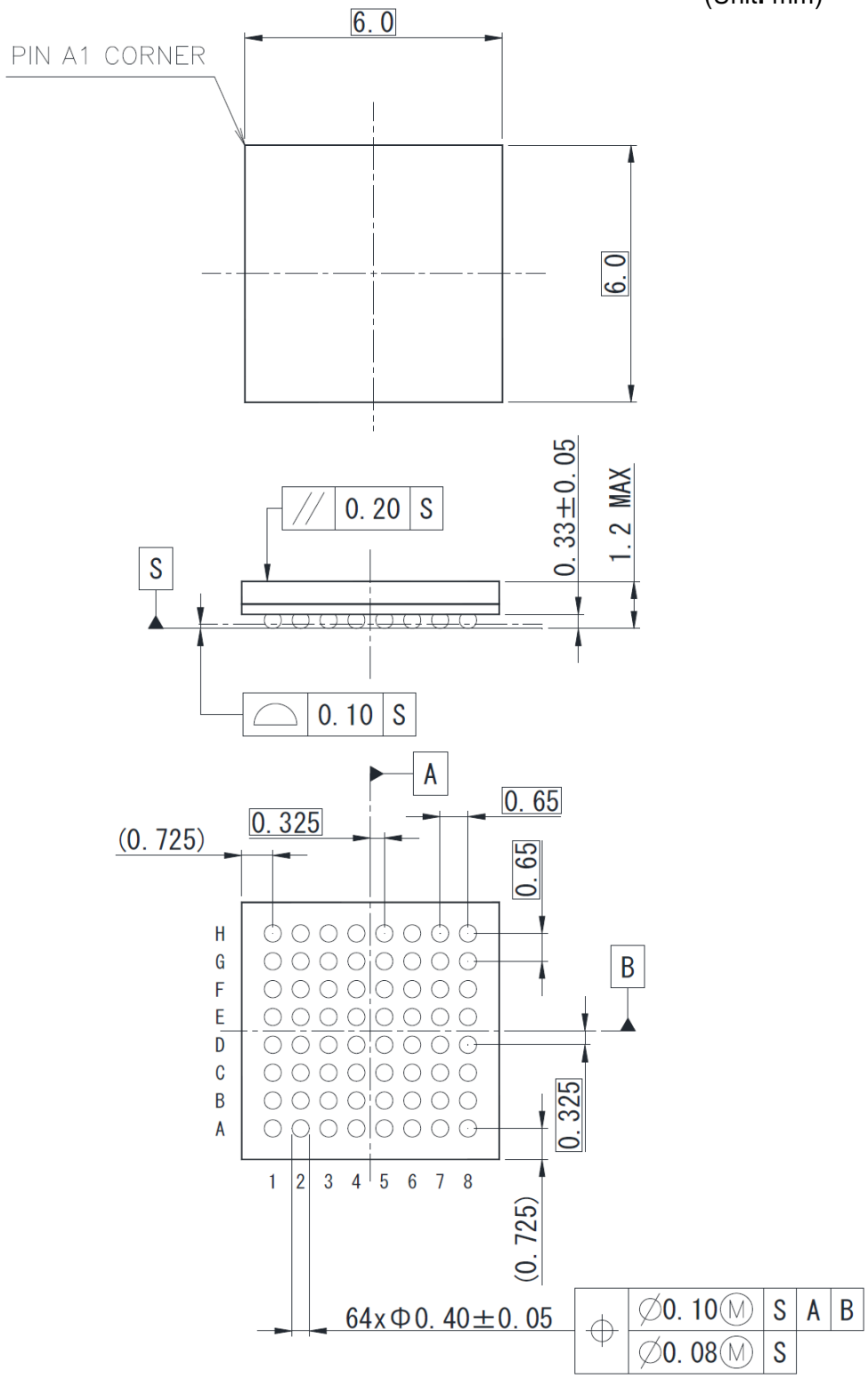
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4. Package

The packages for TC358743XBG are described in the figures below.

P-TFBGA64-0606-0.65-001 (Unit: mm)



Weight: 76 mg (typ.)

Figure 4.1 TC358743XBG package (64 pins)

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Table 4.1 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Package dimension	-	6.0 × 6.0 mm^2	-
Package height	-	-	1.2 mm

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5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2 V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3 V – HDMIRX PHY)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2 V – HDMIRX PHY)	AVDD12	-0.3 to +1.8	V
Supply voltage (2.5 V – APLL)	AVDD25	-0.3 to +2.75	V
Input voltage (CSI IO)	V_{IN_CSI}	-0.3 to VDD_MIPI + 0.3	V
Output voltage (CSI IO)	V_{OUT_CSI}	-0.3 to VDD_MIPI + 0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO + 0.3	V
Output voltage (APLL)	V_{OUT_APLL}	-0.3 to AVDD25 + 0.3	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-40 to +125	°C

5.2. Operating Condition

VSS = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3 V – Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3 V – HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2 V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2 V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Supply voltage (2.5 V – APLL)	AVDD25	2.25	2.5	2.75	V
Operating temperature (ambient temperature with voltage applied)	T_a	-30	25	70	°C
Supply Noise Voltage	VSN	-	-	0.1	Vpp
Supply voltage (3.3 V – HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply Noise Voltage for AVDD33	VSN33	-	-	0.08	Vpp
Supply voltage (1.2 V – HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply Noise Voltage for AVDD12	VSN12	-	-	0.04	Vpp

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5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input (Note 1)	V_{IH}	0.7 x VDDIO	-	VDDIO	V
Input voltage, Low level input (Note 1)	V_{IL}	0	-	0.3 x VDDIO	V
Input voltage High level CMOS Schmitt Trigger (Note 1), (Note 2)	V_{IHS}	0.7 x VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger (Note 1), (Note 2)	V_{ILS}	0	-	0.3 x VDDIO	V
Output voltage High level (Note 1), (Note 2)	V_{OH}	0.8 x VDDIO	-	VDDIO	V
Output voltage Low level (Note 1), (Note 2)	V_{OL}	0	-	0.2 x VDDIO	V
Input leak current, High level (Condition: V_{IN} = +VDDIO, VDDIO = 3.6 V)	I_{ILH1} (Note 3)	-10	-	10	µA
Input leak current, Low level (Condition: V_{IN} = 0 V, VDDIO = 3.6 V)	I_{ILL1} (Note 4)	-10	-	10	µA

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note 4: Normal pin applied VSS (0 V) to Vin (input voltage)

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6. Revision History

Table 6.1 Revision History

Revision	Date	Description
0.582	2014-05-16	Newly released
0.621	2015-12-18	Typo Init(O) DAOUT pin in External Pins
0.622	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.0	2017-10-26	Added comment to HDCP in Features. Changed header, footer and the last page. Changed corporate name.
1.10	2026-03-05	Updated the terms "Master/Slave" to "Controller/Target". Corrected typos.

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