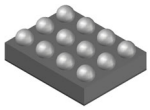
Buck Regulator 3 A, Constant On Time (COT)

FAN53730



WLCSP12 1.07 x 1.36 x 0.432, 0.35P
CASE 567GK

Description

The FAN53730 is a constant on time (COT) buck converter that supports a minimum of 3 A load current. The device's COT topology provides the fastest transient recovery and optimal efficiency vs load due to its variable frequency operation.

Two device options are available (see Ordering Information):

- I^2C Controlled
- Logic Controlled (pin selectable V_{OUT})

Both options have automatic DCM/CCM mode operation with Forced CCM control.

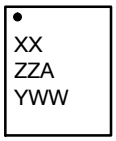
Features

- Input Voltage Range: 2.3 V to 5.5 V
- Output Voltage:
  - Programmable from 0.3 V to 2 V
  - Pin Selectable Defaults
- Low Quiescent Current: 12 µA
- Internal Soft−Start Limits Input Current During Turn−On
- 2.5 MHz Switching Frequency in Continuous Conduction Operation
- 1.2 V and 1.8 V Logic Compatible
- Fault Protection (Input Under Voltage, Short Circuit, Over Current, and Thermal)
- Power Good Output (PG)
- Forced Continuous Conduction Mode (FCCM)
- Audio Reduction Mode Eliminates Audible Tones Due to Switching
- −40°C to +85°C Ambient Temperature Range
- This is a Pb−Free Device

Applications

- LPDDR Memory
- Mobile and Smart Devices
- RF Modules

MARKING DIAGRAM



XX = Specific Device Code
ZZ = Assembly Lot
A = Site Code
Y = Year
WW = 2 Digit Work Week

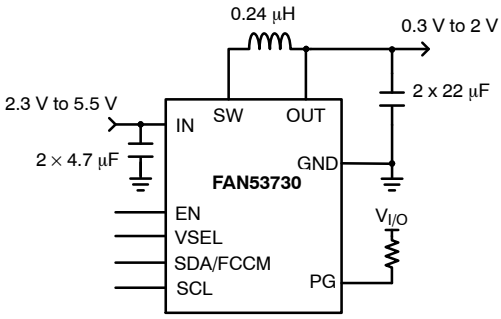


Figure 1. Typical Application Circuit

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Device Option	Default VSEL	I²C Address	Ambient Temperature Range	Package	Shipping†	Specific Device Code
FAN53730UCX	I²C Controlled	VSET1 = 1.00 V VSET2 = 1.05 V	7 h'20	−40°C to 85°C	1.07 mm × 1.36 mm, 0.35 mm pitch, 12−bump WLCSP	3000 / Tape & Reel	MH
FAN53730UC01X	I²C Controlled	VSET1 = 1.00 V VSET2 = 1.05 V	7 h'22			3000 / Tape & Reel	WE
FAN53730UC02X	I²C Controlled	VSET1 = 1.00 V VSET2 = 1.05 V	7 h'30			3000 / Tape & Reel	WF
TBD	Logic Controlled	VSET1 = TBD VSET2 = TBD	Not Applicable			TBD / Tape & Reel	TBD

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Additional options available upon request.

PIN CONFIGURATION

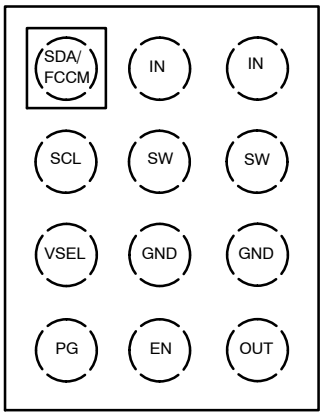

Figure 2. Bumps Facing Down

PIN DEFINITIONS

Pin #	Name	Description
A1	SDA/FCCM	SDA I/O in I²C controlled device. In the logic controlled device this pin is the FCCM control. Connect to V_{IN} to force continuous conduction at all loads. Connect to GND for variable frequency operation.
A2, A3	IN	Input voltage connection. Connect to a 2.3 V to 5.5 V input supply.
B1	SCL	SCL input in I²C controlled device. In the logic controlled device this pin is unused and should connect to GND.
B2, B3	SW	Device switching node. Connect to inductor.
C1	VSEL	Voltage select input. Drive VSEL low to select VSET1. Drive VSEL high to select VSET2.
C2, C3	GND	Ground connection
D1	PG	Power good output. PG goes open drain when V_{OUT} is in regulation (I²C device can change polarity of PG).
D2	EN	Device logic high enable input. Drive EN high to enable the device. I²C bus remains active when EN is low.
D3	OUT	Output voltage sense input. Connect to positive terminal of output capacitor.

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BLOCK DIAGRAM

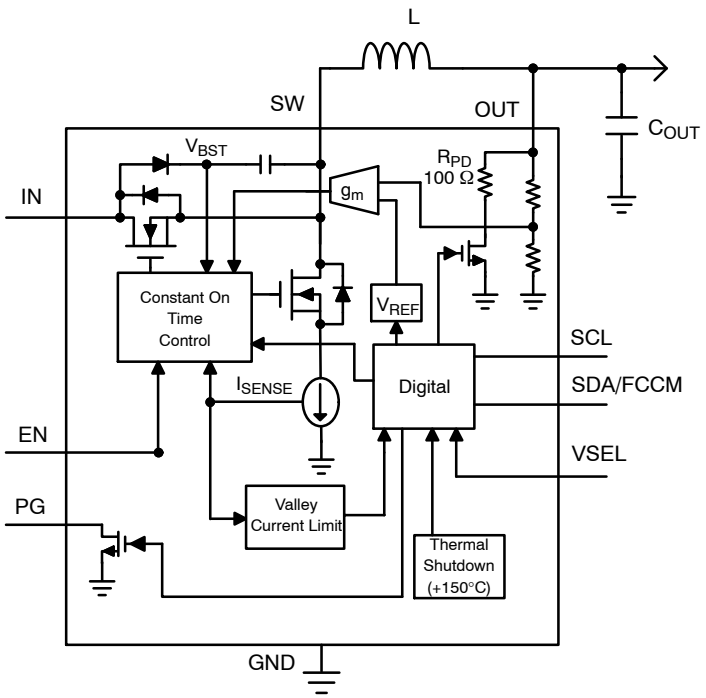

Figure 3. Simplified Block Diagram

MAXIMUM RATINGS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage		−0.3	–	6.0	V
V_{SW}	Voltage on SW Pin		−0.3	–	V_{IN} + 0.3	V
V_{OUT}	Output Voltage		−0.3	–	V_{IN} + 0.3	V
V_{EN}	Enable Input Voltage		−0.3	–	V_{IN} + 0.3	V
V_{SCL}, $V_{SDA/FCCM}$	SCL, SDA/FCCM Voltage		−0.3	–	V_{IN} + 0.3	V
V_{SEL}	Voltage Select Input voltage		−0.3	–	V_{IN} + 0.3	V
V_{PG}	Power Good Output Voltage		−0.3	–	V_{IN} + 0.3	V
ESD	Electrostatic Discharge Protection Level	Human Body Model	–	2.0	–	kV
		Charged Device Model	–	1000	–	V
T_J	Junction Temperature		−40	–	+150	°C
T_{STG}	Storage Temperature		−65	–	+150	°C
T_L	Soldering Temperature (10 Seconds)		–	–	+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL PROPERTIES

Thermal resistance is a function of application and board layout. Theta JA is based on a 2s2p with and without via−in−pad center bump vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature TJ(max) at a given ambient temperature T_A.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	2S2P w/o via−in−pad PCB @ 0.5 W Dissipation	–	130	–	°C/W
θ_{JA}	Junction−to−Board Thermal Resistance	2S2P with via−in−pad PCB @ 0.5 W Dissipation	–	50	–	°C/W

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.3	–	5.5	V
V_{OUT}	Output Voltage Range		0.3	–	2	V
L	Inductor (Nominal Value)		–20%	0.24	+20%	μH
C_{IN}	Input Capacitor		–	4.7	–	μF
C_{OUT}	Output Capacitor (Typical Derated Value)	C_{OUT} = 2 × 22 μF (0402), V_{OUT} = 1 V, DC bias derated	–20%	36	–	μF
T_A	Ambient Temperature Range		–40	–	+85	°C
T_J	Junction Temperature		–40	–	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at 2.3 V ≤ V_{IN} ≤ 5.5 V, 0.3 V ≤ V_{OUT} ≤ 2 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.8 V, V_{OUT} = 1.0 V (Note 1, Note 2)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
GENERAL						
R_{PD}	Output Discharge Resistance	EN = Low	72	93	131	Ω
I_{OUT_SENSE}	OUT Sense Input Leakage Current	V_{OUT} = 1 V	–	–	1	μA
T_{SD}	Thermal Shutdown	Die Temperature Rising	–	150	–	°C
T_{SD_HYST}	Thermal Shutdown Hysteresis		–	30	–	°C
f_{CLK}	Fault Clock Frequency		450	500	550	kHz
R_{PG}	PG Output Pull–down		–	–	133	Ω
V_{PG_TH}	V_{OUT} Rising Threshold for PG Going Open Drain, PG_POL = 1	V_{OUT} = 0.3 V	–	93	–	%
I_{PG_POL}	PG Leakage Current	EN = Low, V_{PG} = 5.5 V	–	0.01	–	μA
I_{EN_L}	EN Input Leakage Current	EN = 5.5 V	–	0.01	–	μA
V_{IH}	Logic High Voltage (VSEL, EN, FCCM)		0.825	–	–	V
V_{IL}	Logic Low Voltage (VSEL, EN, FCCM)		–	–	0.4	V
V_{OUT} ACCURACY						
V_{OUT_ACC}	Output Voltage Accuracy	V_{OUT} < 1 V, No Load, V_{IN} ≥ V_{OUT} + 1.5 V	–20	–	9	mV
		V_{OUT} ≥ 1 V, No Load, V_{IN} ≥ V_{OUT} + 1.5 V	–16	–	12	mV
		V_{OUT} < 1 V, FCCM, No Load, V_{IN} ≥ V_{OUT} + 1.5 V	–14	–	13	mV
		V_{OUT} ≥ 1 V, FCCM, No Load, V_{IN} ≥ V_{OUT} + 1.5 V	–1	–	1.1	%
OPERATING CURRENT						
I_{SHDN}	Shutdown Supply Current	I^2C Controlled device, EN = Low, SDA = SCL = 1.2 V	–	1.5	3.5	μA
I_{SHDN}	Shutdown Supply Current	Logic Controlled device, EN = Low	–	1.5	3.5	μA
I_{Q_ACTIVE}	Active Supply Current	V_{OUT} = 1 V, EN = High, No Load, No Switching	–	12.8	19.3	μA
CURRENT LIMIT						
I_{VALLEY}	Valley Current Limit	V_{OUT} = 1 V, [VAL_ILIM] = 1	3.5	4.2	4.8	A
I_{VALLEY}	Valley Current Limit	V_{OUT} = 1 V, [VAL_ILIM] = 0	1.9	2.3	2.6	A
I_{LIM_NEG}	Negative Current limit		–	1.5	–	A
t_{SHORT}	Short–Circuit Timeout	V_{OUT} < 0.1 V (Note 3)	–	40	–	μs

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ELECTRICAL CHARACTERISTICS (continued)
Minimum and maximum values are at 2.3 V ≤ V_{IN} ≤ 5.5 V, 0.3 V ≤ V_{OUT} ≤ 2 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.8 V, V_{OUT} = 1.0 V (Note 1, Note 2)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
CURRENT LIMIT						
V_{SHORT}	Output Short Circuit Threshold	t < t_{SHORT}	68	140	212	mV
SWITCH ON TIME						
t_{ON}	High side switch on−time	V_{IN} = 2.3 V, V_{OUT} = 1 V	181	196	202	ns
t_{ON}	High side switch on−time	V_{IN} = 3.8 V, V_{OUT} = 1 V	104	113	116	ns
t_{ON}	High side switch on−time	V_{IN} = 5.5 V, V_{OUT} = 1 V	70	78	80	ns
UVLO DETECTION						
V_{UVLO_R}	Under−Voltage Lockout Threshold	Rising V_{IN}	–	–	2.3	V
V_{UVLO_F}	Under−Voltage Lockout Threshold	Falling V_{IN}	2.1	–	–	V
V_{UVLO_H}	UVLO Hysteresis		–	100	–	mV
POWER MOSFETs RDSON						
RDS_{ON_LOW}	Low Side NMOS Resistance (Ball−to−Ball)	V_{IN} = V_{GS} = 3.8 V	–	23	–	mΩ
RDS_{ON_HIGH}	High Side NMOS Resistance (Ball−to−Ball)	V_{IN} = V_{GS} = 3.8 V	–	33	–	mΩ
AUDIO MODE						
R_{AUDIO}	Pull−down FET for Output Discharge	V_{IN} = 3.8 V	–	5	–	Ω
t_{AUDIO}	Maximum Dead Time in Audio Mode	[ARM_TO] = 0	–	25	–	μs
t_{AUDIO}	Maximum Dead Time in Audio Mode	[ARM_TO] = 1	–	40	–	μs
I^2C TIMING AND PERFORMANCE – FOR I^2C VERSION (Note 4)						
V_{IL}	SDA and SCL Logic Low threshold		–	–	0.4	V
V_{IH}	SDA and SCL Logic High threshold		0.825	–	5.5	V
V_{OL}	SDA Logic Low Output	3 mA sink	–	–	0.4	V
f_{SCL}	SCL Clock Frequency	Fast Mode Plus	–	–	1000	kHz
t_{BUF}	Bus−Free Time Between STOP and START Conditions	Fast Mode Plus	0.5	–	–	μs
$t_{HD;\,STA}$	START or Repeated START Hold Time	Fast Mode Plus	260	–	–	ns
t_{LOW}	SCL LOW Period	Fast Mode Plus	0.5	–	–	μs
t_{HIGH}	SCL HIGH Period	Fast Mode Plus	260	–	–	ns
t_R	SDA and SCL Rise Time	Fast Mode Plus	–	–	120	ns
t_F	SDA and SCL Fall Time	Fast Mode Plus, V_{DD} = 1.8 V	6.55	–	120	ns
$t_{SU;\,STO}$	Stop Condition Setup Time	Fast Mode Plus	260	–	–	ns
C_I	SDA and SCL Input Capacitance		–	–	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Refer to Typical Characteristics waveforms/graphs for closed loop data and variation with input supply and temperature.
2. Electrical Characteristics reflects open loop steady state data. System Characteristics reflects both steady state and dynamic close loop data associated with the recommended external components.
3. Short−Circuit timeout is the time after V_{OUT} falls below V_{SHORT} to when the FAN53730 is placed into the Fault state.
4. Guaranteed by Design. Characterized on the ATE or Bench.

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SYSTEM CHARACTERISTICS

System Characteristics reflects both steady state and dynamic closed loop data associated with the recommended external components. They are verified during Application Validation and are not performed in production testing. Recommended operating conditions, unless otherwise noted are 2.3 V ≤ V_{IN} ≤ 5.5 V, 0.3 V ≤ V_{OUT} ≤ 2 V, V_{IN} = V_{OUT} + 1.5 V, −40°C ≤ T_A ≤ 85°C. Typical values are based on V_{IN} = 3.8 V, V_{OUT} = 1.0 V and T_A = 25°C. System Specifications are based on the Typical Application Circuit, L = 0.24 μH, C_{IN} = 10 μF, C_{OUT} = 2 x 22 μF (nominal)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
GENERAL						
IQ_{IN_DCM}	DCM Quiescent Current	EN = High, 2.3 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} = 1 V, [BIAS_MODE] = 00, No Load	–	12.8	19.3	μA
		EN = High, [BIAS_MODE] = 1X, No Load	–	262	–	μA
IQ_{CCM}	CCM Quiescent Current	EN = High, FCCM, No Load	–	13.9	–	mA
tss	Soft−Start	From EN High to 95% of V_{OUT} Target, No Load, [RR_DVS] = 001	–	800	–	μs
EFFICIENCY						
eff	Efficiency	I_{OUT} = 1 mA, V_{OUT} = 1.0 V, V_{IN} = 3.8 V	–	82.1	–	%
eff	Efficiency	I_{OUT} = 10 mA, V_{OUT} = 1.0 V, V_{IN} = 3.8 V	–	86.8	–	%
eff	Efficiency	I_{OUT} = 100 mA, V_{OUT} =1.0 V, V_{IN} = 3.8 V	–	87.5	–	%
eff	Efficiency	I_{OUT} = 500 mA, V_{OUT} = 1.0 V, V_{IN} = 3.8 V	–	88.2	–	%
eff	Efficiency	I_{OUT} = 1000 mA, V_{OUT} = 1.0 V, V_{IN} = 3.8 V	–	89.3	–	%
eff	Efficiency	I_{OUT} = 3000 mA, V_{OUT} = 1.0 V, V_{IN} = 3.8 V	–	83	–	%
I_{OUT} MAX						
I_{OUT_MAX}	Maximum Output Current (Note 6)	V_{IN} from 2.5 V to 5.5 V, V_{OUT} from 0.3 V to 1 V	3	–	–	A
V_{OUT} LOAD REGULATION						
V_{LO_REG}	Load Regulation	I_{OUT} = 10 μA to 3 A, V_{IN} = 2.5 V to 5.5 V, V_{OUT} = 1 V, [BIAS_MODE] = 00	–	–	0.6	%/A
V_{LO_REG}	Load Regulation	I_{OUT} = 10 μA to 3 A, V_{IN} = 2.5 V to 5.5 V, V_{OUT} = 1 V, [BIAS_MODE] = 1X	–	–	0.4	%/A
V_{LO_REG}	Load Regulation (CCM)	I_{OUT} = 10 μA to 3 A, V_{IN} = 2.5 V to 5.5 V, V_{OUT} = 1 V, FCCM	–	–	0.4	%/A
VOUT LINE REGULATION						
V_{LREG_CCM}	Line Regulation 10 μA	I_{OUT} = 10 μA, V_{OUT} = 1 V, V_{IN} = 2.5 V to 5.5 V	–	–	0.12	%/V
V_{LREG_DCM}	Line Regulation 10 mA	I_{OUT} = 10 mA, V_{OUT} = 1 V, V_{IN} = 2.5 V to 5.5 V	–	–	0.08	%/V
V_{LREG_DCM}	Line Regulation 3 A	I_{OUT} = 3 A, V_{OUT} = 1 V, V_{IN} = 2.5 V to 5.5 V	–	–	0.08	%/V
SWITCHING						
V_{RIPPLE_DCM}	Output Ripple	V_{IN} = 2.3 V to 5.5 V, I_{OUT} = 10 mA, FCCM, V_{OUT} = 1 V	–	12	–	mVpp
V_{RIPPLE_CCM}	Output Ripple	V_{IN} = 2.3 V to 5.5 V, I_{OUT} = 3 A, V_{OUT} = 1 V	–	6	–	mVpp

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SYSTEM CHARACTERISTICS (continued)

System Characteristics reflects both steady state and dynamic closed loop data associated with the recommended external components. They are verified during Application Validation and are not performed in production testing. Recommended operating conditions, unless otherwise noted are 2.3 V ≤ V_{IN} ≤ 5.5 V, 0.3 V ≤ V_{OUT} ≤ 2 V, V_{IN} = V_{OUT} + 1.5 V, −40°C ≤ T_A ≤ 85°C. Typical values are based on V_{IN} = 3.8 V, V_{OUT} = 1.0 V and T_A = 25°C. System Specifications are based on the Typical Application Circuit, L = 0.24 μH, C_{IN} = 10 μF, C_{OUT} = 2 x 22 μF (nominal)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
f_{CCM}	Switching Frequency in CCM Mode	I_{OUT} = 1 A, FCCM	–	2.5	–	MHz
CURRENT LIMIT						
I_{VALLEY_CL}	Closed Loop Valley Current Limit (Note 5)	V_{IN} ≥ 2.5 V, [VAL_ILIM] = 1	–	4.6	–	A
		V_{IN} ≥ 2.5 V, [VAL_ILIM] = 0	–	2.3	–	A
		V_{IN} = 2.3 V, [VAL_ILIM] = 1	–	2.8	–	A
		V_{IN} = 2.3 V, [VAL_ILIM] = 0	–	1.8	–	A

5. Closed loop current limit reflects the maximum control loop error amplifier voltage output, which can mean that the inductor valley current limit has reached its maximum value, or that the control loop has reached a maximum duty cycle.
6. Refer to Fig. 33 Typical Derating Curve for additional $I_{OUT(MAX)}$ guidance.

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TYPICAL CHARACTERISTICS

Unless otherwise specified V_{IN} = 3.8 V, V_{OUT} = 1 V, T_A = 25°C, Circuit of Figure 36 and components from Applications Circuit Components Table.

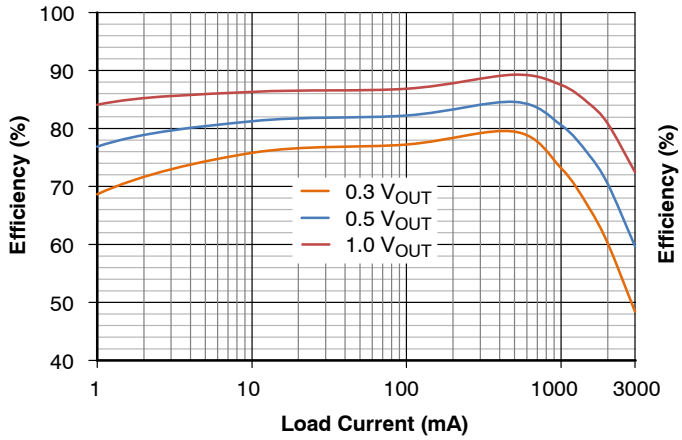

Figure 4. Efficiency vs. I_{OUT}, V_{IN} = 2.5 V

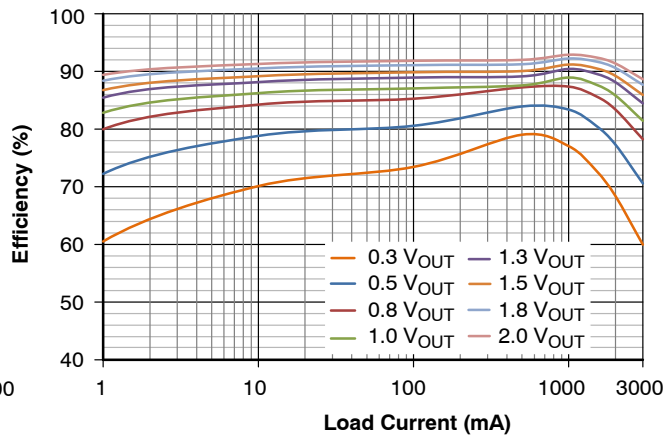

Figure 5. Efficiency vs. I_{OUT}, V_{IN} = 3.8 V

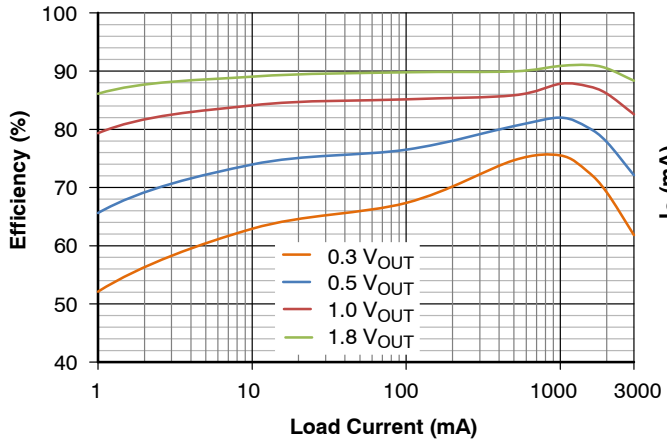

Figure 6. Efficiency vs. I_{OUT}, V_{IN} = 5.0 V

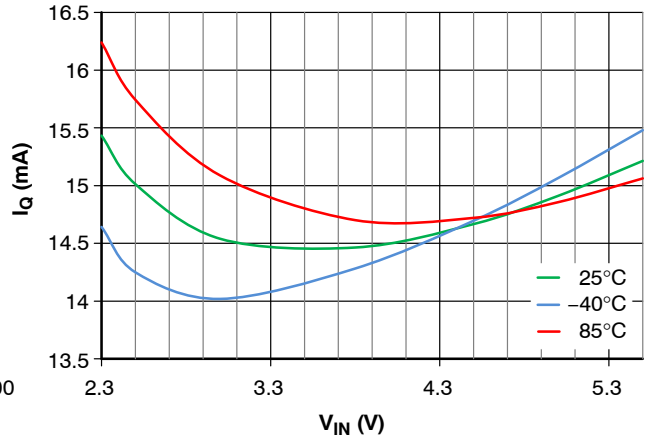

Figure 7. Quiescent Current (FCCM) vs. V_{IN}

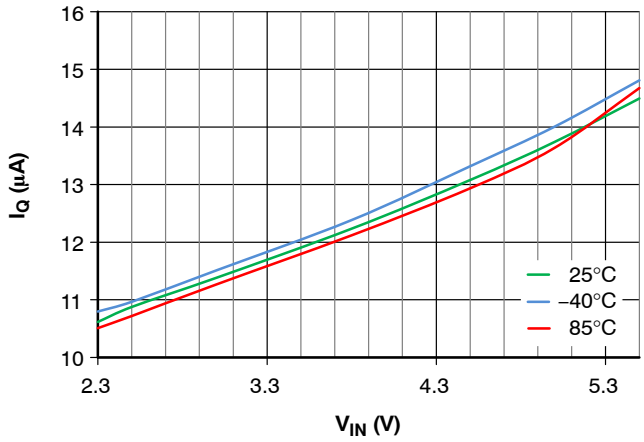

Figure 8. Quiescent Current (DCM) vs. V_{IN}, [BIAS_MODE] = 00

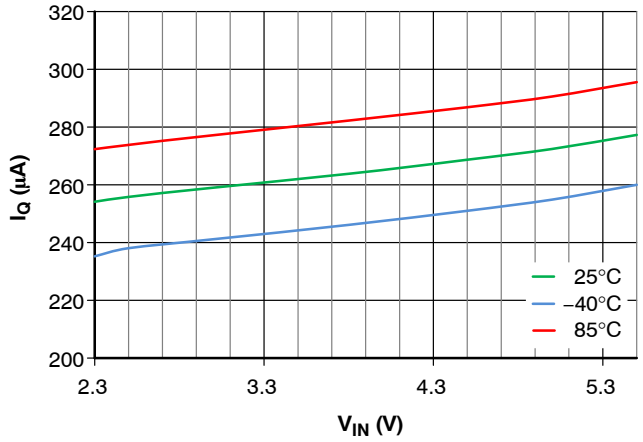

Figure 9. Quiescent Current (DCM) vs. V_{IN}, [BIAS_MODE] = 1X

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TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified V_{IN} = 3.8 V, V_{OUT} = 1 V, T_A = 25°C, Circuit of Figure 36 and components from Applications Circuit Components Table.

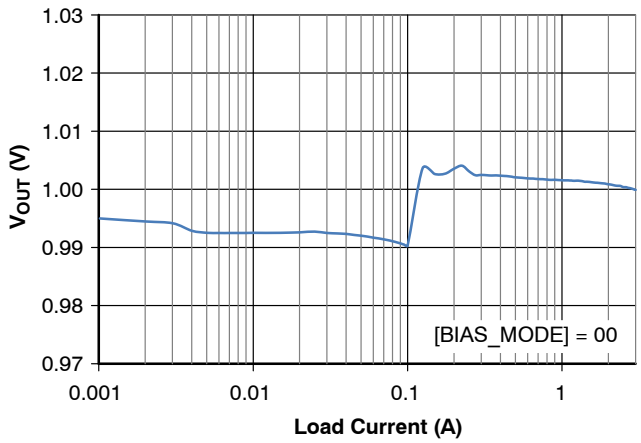

Figure 10. Load Regulation (DCM), [BIAS_MODE] = 00

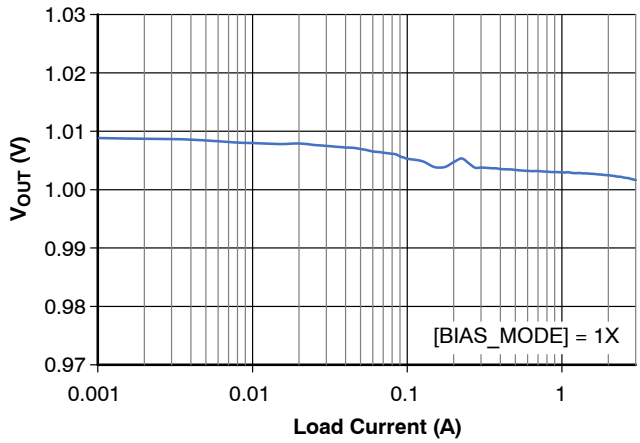

Figure 11. Load Regulation (DCM), [BIAS_MODE] = 1X

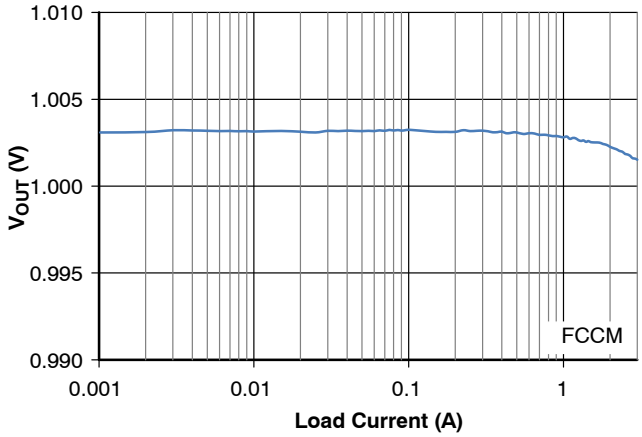

Figure 12. Load Regulation (FCCM)

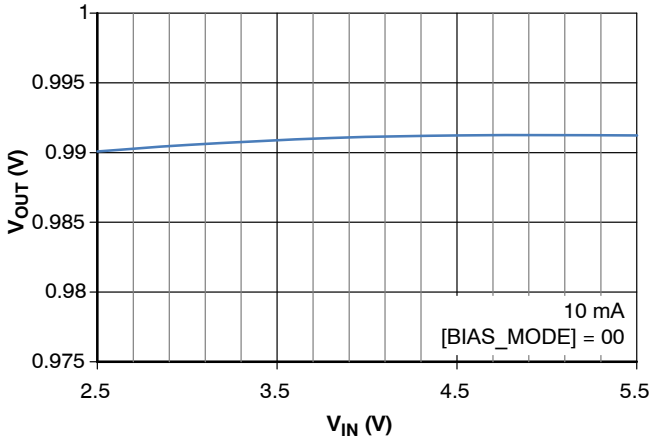

Figure 13. Line Regulation (DCM), I_{OUT} = 10 mA, [BIAS_MODE] = 00

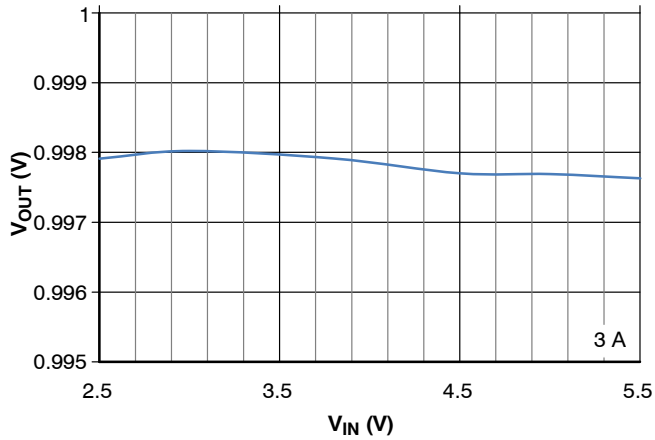

Figure 14. Line Regulation, I_{OUT} = 3 A

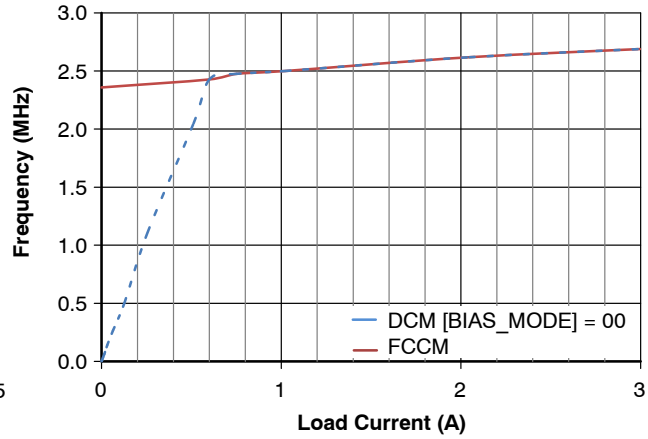

Figure 15. Switching Frequency vs. I_{OUT}, FCCM (Solid), DCM [BIAS_MODE] = 00 (Dotted)

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TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified V_{IN} = 3.8 V, V_{OUT} = 1 V, T_A = 25°C, Circuit of Figure 36 and components from Applications Circuit Components Table.

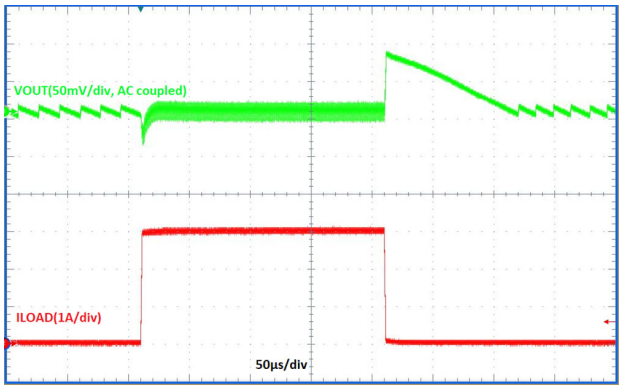

Figure 16. Load Transient (DCM), I_{OUT} = 10 mA ↔ 3 A, Trise = Tfall = 1 µs

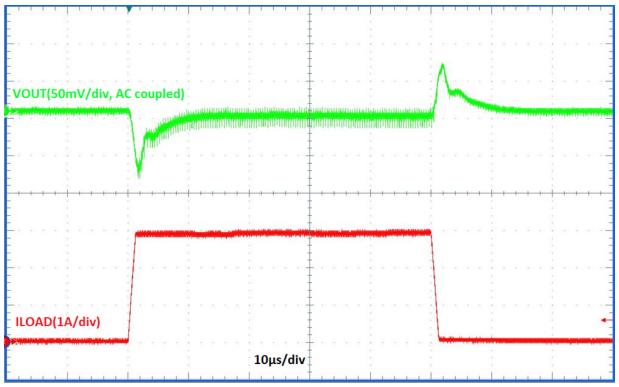

Figure 17. Load Transient (FCCM), I_{OUT} = 10 mA ↔ 3 A, Trise = Tfall = 1 µs

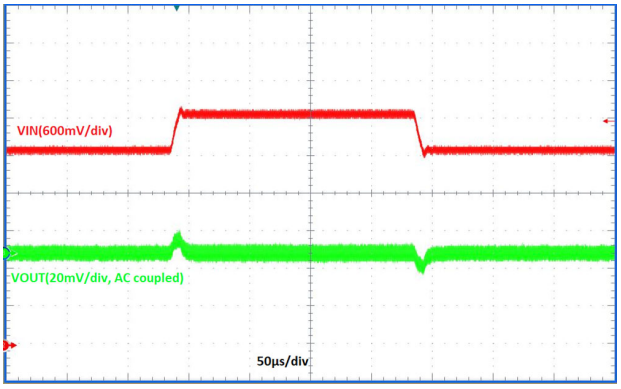

Figure 18. Line Transient, V_{IN} = 3.3 V ↔ 3.8 V, Slew Rate = 100 mV/µs, I_{OUT} = 3 A

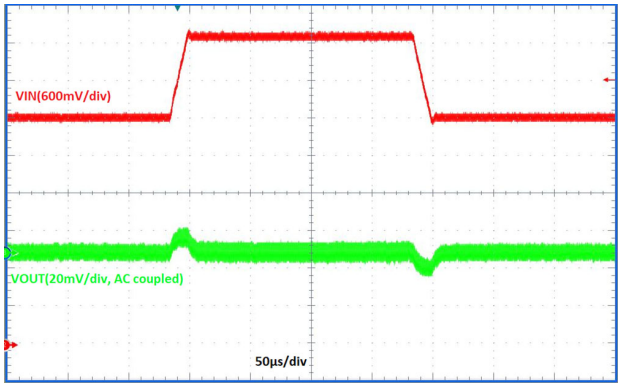

Figure 19. Line Transient, V_{IN} = 3.8 V ↔ 5 V, Slew Rate = 100 mV/µs, I_{OUT} = 3 A

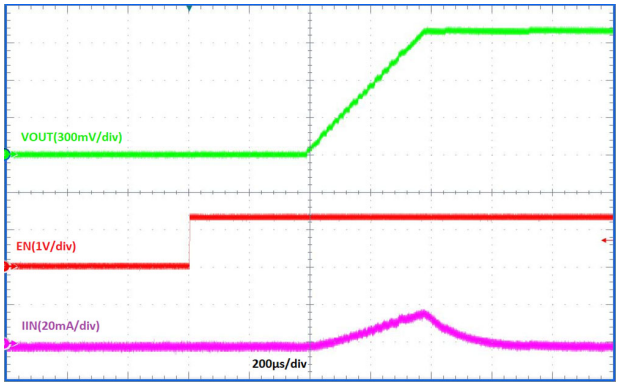

Figure 20. Start−up, No Load

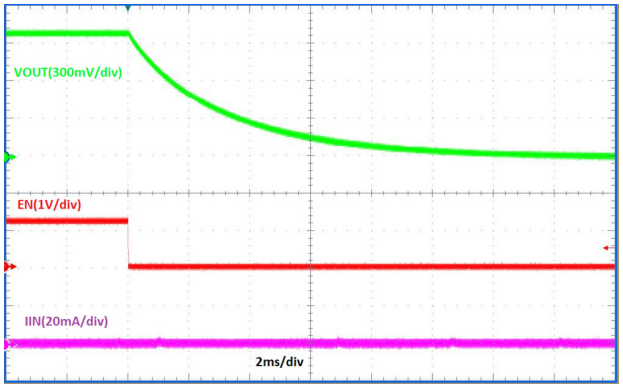

Figure 21. Shut−down, No Load

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TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified V_{IN} = 3.8 V, V_{OUT} = 1 V, T_A = 25°C, Circuit of Figure 36 and components from Applications Circuit Components Table.

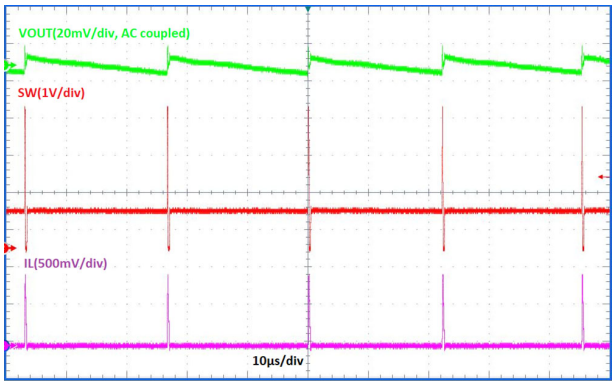

Figure 22. Device Switching (DCM), I_{OUT} = 10 mA

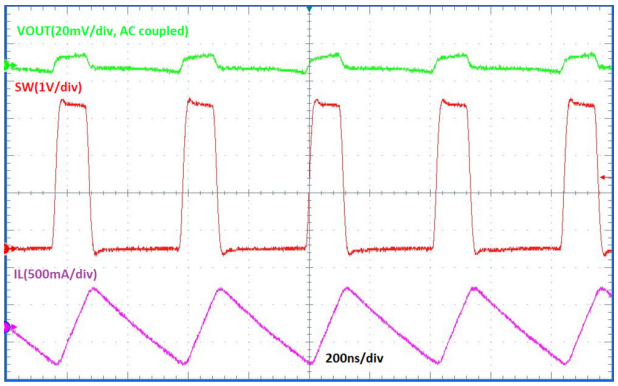

Figure 23. Device Switching (FCCM), I_{OUT} = 10 mA

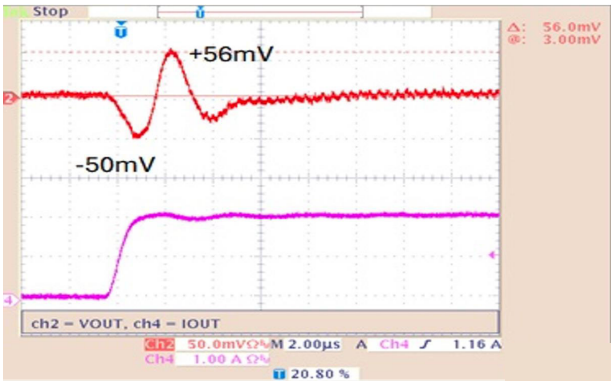

Figure 24. TRANSIENT_ENHANCEMENT bit enabled, 10 mA ↔ 2 A, Slew Rate = 2 A/µs

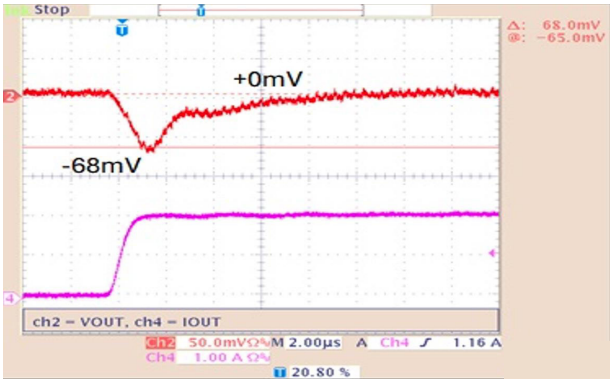

Figure 25. TRANSIENT_ENHANCEMENT bit disabled, 10 mA ↔ 2 A, Slew Rate = 2 A/µs

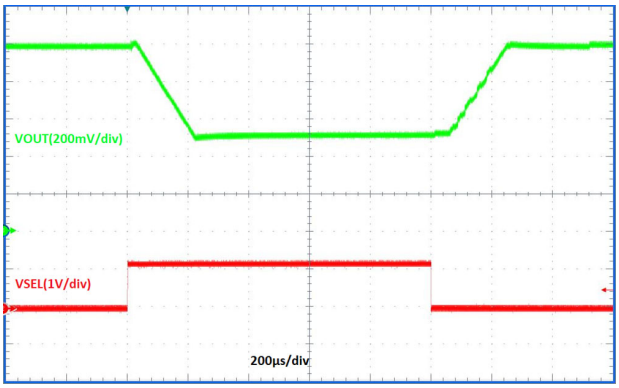

Figure 26. Vsel Toggle, V_{OUT} = 1 V to 0.5 V to 1 V, No Load, [DVS_FCCM] = 1

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FUNCTIONAL SPECIFICATIONS

Device Options

Options and Features

The FAN53730 has two options:

1. A fully programmable I^2C version.
2. A logic controlled fixed output voltage version.

The following table lists the differences between the two:

FAN53730 FEATURE BREAKDOWN

Feature	Logic Controlled Device	I^2C Controlled Device
Enable (EN)	Logic Enable Input Only	Logic Enable Input and Enable Bit
Thermal Shutdown	Yes, 150°C	Yes, 150°C
Under Voltage Lockout (UVLO)	Yes	Yes
Power Good Output (PG)	Yes (goes open drain when V_{OUT} > 93% of target)	Yes (programmable active high or active low)
Output Pull−Down	Yes, In shutdown (100 Ω)	Yes, In shutdown (100 Ω). Can be disabled via I^2C
Forced Continuous Conduction (FCCM)	Yes, via FCCM input	Yes, via I^2C or when VSEL = High and [VSEL_FCCM] = 1
Voltage Select Input (VSEL)	Yes, VSET1 and VSET2 are fixed by device voltage options	Yes, VSET1 and VSET2 targets are programmable
Audio Reduction Mode (ARM)	No (disabled)	Yes, can be enabled via I^2C
Valley Current Limit	Fixed at 4.6 A (typ)	Programmable to 4.6 A or 2.3 A to accommodate different sized inductors
Dynamic Voltage Scaling	Yes	Yes, 8 programmable slew rates. Can be disabled via I^2C
Low Power Mode (PFM) During Light Load	Yes	Yes, can be disabled via I^2C
Output Short Fault	Yes	Yes
Fault Auto−Restart / Shutdown	Auto−Restart	Can be programmed to auto−restart after a fault, or go into shutdown

Overview

Constant On−Time Operation (COT)

The FAN53730 is a constant on−time (COT) synchronous buck which regulates a 0.3 V to 2 V output voltage from a 2.3 V to 5.5 V input voltage. The COT controller operates as follows:

When the output voltage falls out of regulation the input power switch turns on for the fixed on time (t_{ON}) and ramps the inductor current. At the end of t_{ON} the input switch turns off and the low side synchronous FET turns on and discharges the inductor into the output. If the inductor current reaches 0 before the load pulls the output voltage out of regulation, both the input FET and the synchronous FET will turn off and the device enters an idle state where it will remain until the output falls below the regulation target. Once the output falls below the regulation target the switching action starts again. This results in a variable frequency operation (load dependent) for light currents. At higher load currents (dependent on V_{IN}, and V_{OUT}) the inductor current will no longer hit 0 before the output voltage falls out of regulation. This results in an approximate constant switching frequency at heavy loads.

On−Time and Maximum Switching Frequency

The Buck switch on−time (t_{ON}) varies with V_{IN} and V_{OUT} in order to approximately target a 2.5 MHz switching frequency at V_{IN} = 3.8 V and V_{OUT} = 1 V, when the device is operating in continuous conduction mode. Although this switching frequency will have some variation due to delays and non−linearities in the timing circuit, as well as load dependence effects due to resistive drops that make the effective V_{IN} lower. Typical CCM frequency variation is shown in the typical operating characteristic graphs.

Efficiency

The load dependent switching frequency allows the buck converter to only switch as necessary to keep the load in regulation. This provides for an optimum efficiency response vs load, as the light load switching losses are

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minimized. When forced CCM (FCCM) is enabled the light load efficiency will be drastically reduced due to increased switching losses.

Low Power Mode

During low output current conditions the idle state can be very long compared to the on and off times. During these conditions (typically for I_{OUT} < 2 mA), the FAN53730 will enter a low power state where the device is shutdown during the idle period. This results in low quiescent current.

Enable Input

The Enable input (EN) is an active high device enable. When EN is driven low the FAN53730 is in a low power shutdown mode. When driven high the device is in the active state and the output is regulating at its target voltage. For the I^2C controlled device, the EN input must be high and the ENABLE (REG 06h[0]) bit set to 1 to enable the device.

In the shutdown state, the output pull−down (typically 100 Ω) is active and V_{OUT} will discharge to GND. The I^2C version has the ability to disable the active pull−down. The EN input is a high impedance input and should not be left floating.

Soft−Start

The FAN53730 incorporates a soft−start which ramps the output from 0 to the target voltage during turn−on. This will limit the high input in−rush current during start−up. The soft−start ramp uses the same ramp as the DVS, but soft−start cannot be disabled using the DVS_EN (Reg 06h [4]) bit. The default start−up ramp time is set to 4 µs per step which results in a soft−start ramp time of typically 400 µs with V_{OUT} = 1 V and no load. This is in addition to approximately 400 µs of initialization time for the bias and reference to wake−up.

Additionally, the device will always start−up in DCM mode until the V_{OUT} ramp is done, even if the part is set for FCCM.

Power Good

Power Good Output

Power Good (PG) is an open drain output which is active when V_{OUT} rises above 93% of the regulation target and when the V_{OUT} ramp has completed. PG will remain active as long as: the output is enabled, V_{OUT} is above 93% of the V_{OUT} target, and no faults are detected (PG is inactive in the FAULT state). The following figure details the operation of PG when set for active high operation.

1. EN goes high and the bias and reference are enabled.
2. After the 400 µs start−up delay, V_{OUT} begins ramping to the target voltage. During this time PG is low.
3. When the V_{OUT} ramp stops and V_{OUT} is higher than 93% of the target, a 128 µs de−glitch timer starts If V_{OUT} remains above 93% of the target voltage during the de−glitch timer, PG is pulled high.
4. When a voltage change occurs which forces V_{OUT} to a higher level, PG goes low.
5. After the V_{OUT} ramp completes and the 128 µs de−glitch timer expires, PG goes high.
6. When V_{OUT} is set to a new lower voltage, PG remains high because V_{OUT} is above 93% of the new target voltage.
7. If V_{OUT} is forced below 93% of the target voltage for t > 128 µs (or if any fault occurs PG will pull−low).
8. PG will go high again if the condition which forced V_{OUT} to drop is removed and V_{OUT} again rises above 93% of the target output voltage (after 128 µs de−glitch timer expires).
9. When enable is brought low, the PG output will pull low immediately.

During a fault condition, PG will pull low after the fault passes the de−glitch time. This can make PG inactive sooner than the 128 µs de−glitch time (see below).

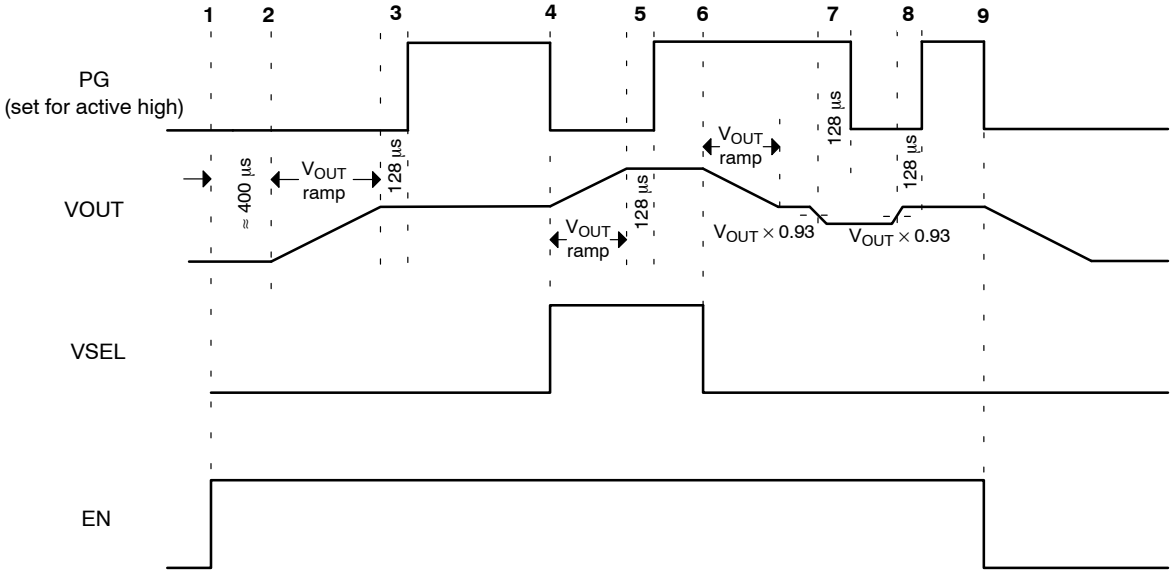

Figure 27. PG Operation

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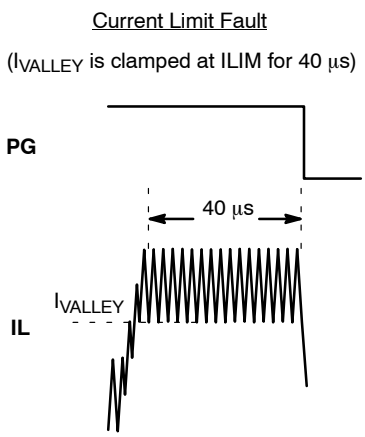

Figure 28. Current Limit Fault

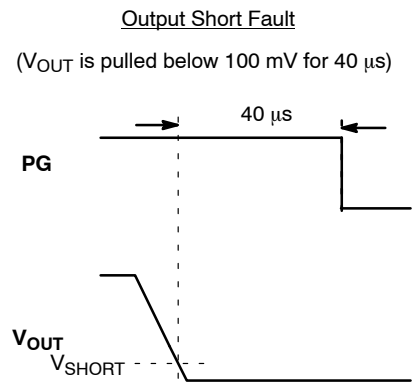

Figure 29. Output Short Fault

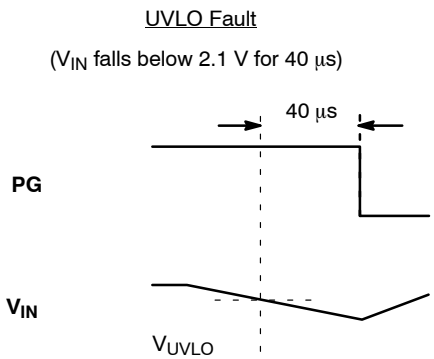

Figure 30. UVLO Fault

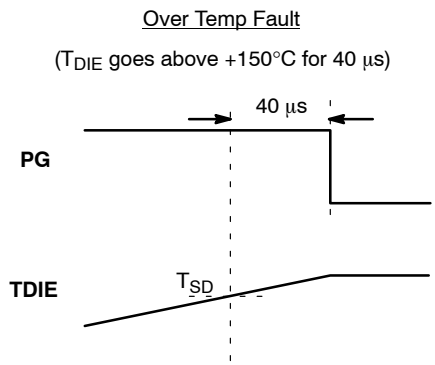

Figure 31. Over Temperature Fault

Power Good Polarity

The PG polarity bit, PG_POL (Reg 03h [0]), sets the active state of the power good output. By default, the PG output will go open drain (externally pulled high) in the active state. When PG_POL is set to 0, the PG output will pull low in the active state.

Power Good Bit

The POWER_GOOD (Reg 01h [5] bit sets to 1 when the PG output is in it's active state.

Output Pull−Down

Output Pull−Down

During shutdown and fault timeout, the output has a 100 Ω pull−down. The pull−down resistor can be disabled via OUT_DISCHARGE (Reg06h[3]).

UVLO

UVLO Rising

The Under Voltage Lockout (UVLO) holds the device in shutdown until V_{IN} rises above the UVLO rising threshold.

UVLO Falling

If V_{IN} falls below the UVLO falling threshold, the FAN53730 will trigger a UVLO event and shutdown.

Valley Current Limit

Valley Current Limit

In CCM operation the FAN53730 will regulate the valley of the inductor current in order to keep V_{OUT} at its target voltage. However, there is a maximum valley inductor current capability (I_{VALLEY}) allowed in the FAN53730's power path. When I_{OUT} increases to the point where the inductor valley current reaches I_{VALLEY}, the FAN53730's control loop will be clamped at this valley current limit threshold and will no longer be able to regulate V_{OUT} at the target voltage. When this happens V_{OUT} will tend to drop out. The maximum output current from the FAN53730 is approximately:

$$I_{OUT_MAX} = I_{VALLEY} + (V_{IN} - V_{OUT})/(2L) \times t_{ON} \quad \text{(eq. 1)}$$

where I_{VALLEY} is the valley current limit threshold. For the logic controlled device I_{VALLEY} is fixed at VAL_ILIM (Reg 03h [0]) = 1. For the I^2C controlled device VAL_ILIM is programmable.

For inductor selection, typically the peak inductor current is required. Keep in mind that the peak inductor current will typically be 20% to 30% higher than the valley current.

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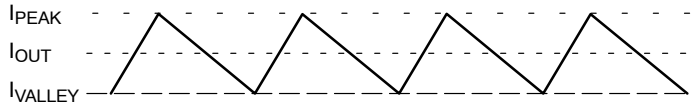

$I_{OUT_MAX} = I_{VALLEY} + (V_{IN} - V_{OUT}) \times t_{ON}/(2 \times L)$
$I_{PEAK} = I_{OUT} + (V_{IN} - V_{OUT}) \times t_{ON}/(2 \times L)$

For example:
V_{OUT} = 1 V, V_{IN} = 3.8 V, I_{VALLEY} = 4.6 A
I_{PEAK} = 4.6 A + (3.8 V − 1 V) × 79 ns / 0.24 μH = 4.6 A + 0.922 A = 5.52 A

Figure 32. Current Limit Description

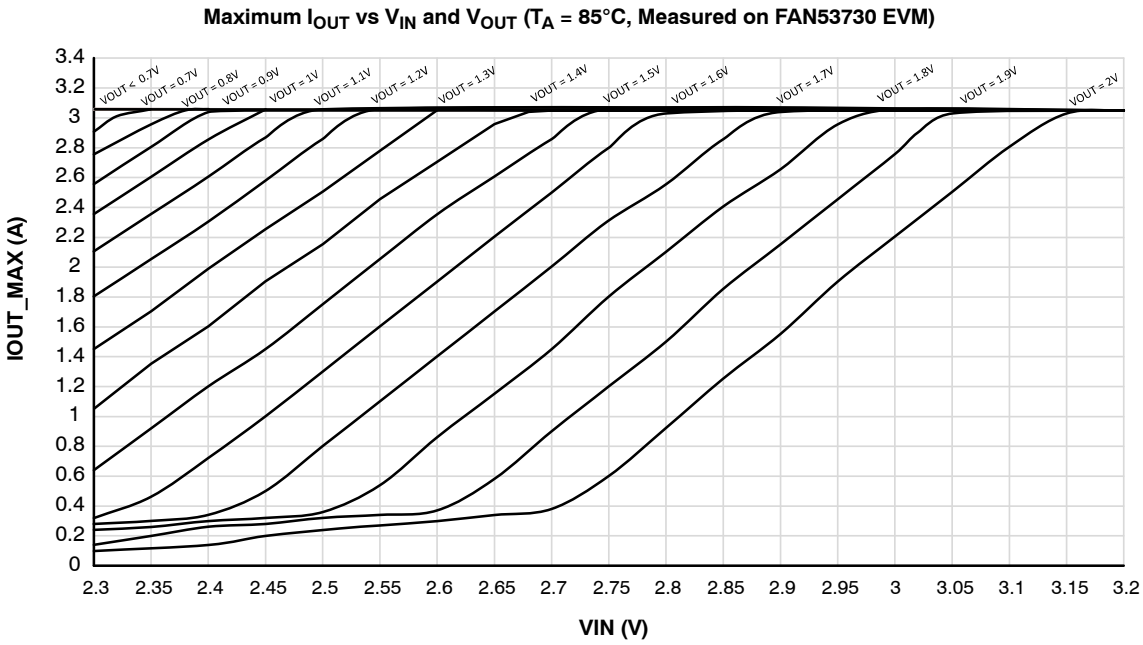

Figure 33. Typical Derating Curve vs. V_{IN}, V_{OUT}, I_{LOAD}

Maximum Duty Cycle

For some V_{IN} to V_{OUT} conditions, the maximum output current can be limited by the device minimum off time (t_{OFF_MIN}),which can be up to 100 ns. This places a limitation on the maximum duty cycle the device can attain in CCM. Parameters which effect the required duty cycle are V_{IN}, V_{OUT}, and I_{LOAD}. Typically the FAN53730 can reach a duty cycle of $t_{ON}/(t_{ON} + t_{OFF_MIN})$ at no load. However, as load increases, the effective voltage across the inductor is less, and the required duty cycle increases. This will limit the maximum current below 3 A for some V_{IN}/V_{OUT} configurations. Figure 16 shows a typical derating curve for V_{IN}, V_{OUT}, and Load for T_A = 85°C. This can be used for targeting the maximum load for different V_{IN}/V_{OUT} configurations.

V_{OUT} < 0.8 V Operation

If V_{OUT} < 0.8V (VSET1 or VSET2 ≤ code 0x4F), set HIGH_BANDWIDTH (Reg 02h [1]) = 0 to avoid low phase margin conditions and possible output voltage oscillations.

Audio Reduction Mode

Audio Reduction Mode

The I^2C controlled device features an Audio Reduction Mode (ARM). In this mode the switching frequency is kept above a programmed target frequency to eliminate audible noise typically generated in ceramic capacitors with changing electric fields. The ARM is is enabled by setting ARM_EN (Reg 06h [5]) = 1. When enabled, the Buck's DCM idle time (dead time between switching events) is monitored. If t_{IDLE} reaches the programmed maximum period before the start of a new t_{ON}, then the synchronous MOSFET will be forced on long enough to pull V_{OUT} out of regulation and force a new switching cycle. This forced switching period is approximately equal to the ARM time−out period. Programmable timeout periods are 25 μs and 40 μs (see ARM_TO (Reg 02h [6])) which result in minimum allowed frequency targets of 1/40 μs = 25 kHz and 1/25 μs = 40 kHz.

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Dynamic Voltage Scaling

Dynamic Voltage Scaling (DVS)

The I²C controlled device features a Dynamic Voltage Scaling mode (DVS), which is the controlled slewing of the output voltage (up or down) depending on the direction of the new target output voltage. The slewing of V_{OUT} (or ramp rate) is done by incrementing through each voltage set−point (10 mV/step) between the current target and the new target, until the new target voltage is reached. The time per step is programmable using RR_DVS (Reg 02h [4:2]). Programmable times per step are shown below:

DVS PROGRAMMABLE TIME PER STEP

DVS_EN	RR_DVS	Time per Step
0	XXX	Immediate
1	000	2 μs/step
1	001	4 μs/step
1	010	6 μs/step
1	011	8 μs/step
1	100	10 μs/step
1	101	12 μs/step
1	110	14 μs/step
1	111	16 μs/step

For example: DVS is enabled with RR_DVS set to 10 μs/step. V_{OUT} is initially set to 0.5 V and has reached steady state. V_{OUT} is then programmed to 1 V. The output will increment from 0.5 V to 1 V through each voltage set−point (10 mV/step) with a pause at each step of 10 μs. The total ramp time is given as:

$$[(1000\text{ mV} - 500\text{ mV}) / (10\text{ mV/step}) - 1] \times 10\ \mu\text{s/step} = 490\ \mu\text{s}$$

During negative transitions (high voltage to lower voltage), if there is a no load condition the output can take a long time to decay to its new target. There is an option to have FCCM turn on during high to low voltage transitions in order to rapidly bring V_{OUT} down to its new target (see DVS_FCCM (Reg 02h [5])).

DVS control also applies when the output voltage transitions between VSET1 and VSET2 settings following a VSEL change.

The DVS control can be disabled with the DVS_EN (Reg 06h [4] bit, in which case any V_{OUT} transition will immediately change to the new value without a ramp. However, disabling the DVS ramp will not effect the ramp during soft−start. Soft−start will continue to use the programmed DVS setting regardless of the setting of DVS_EN. Additionally, disabling the DVS ramp with FORCE_FCCM = 1 will still utilize slew rate control during high to low voltage transitions.

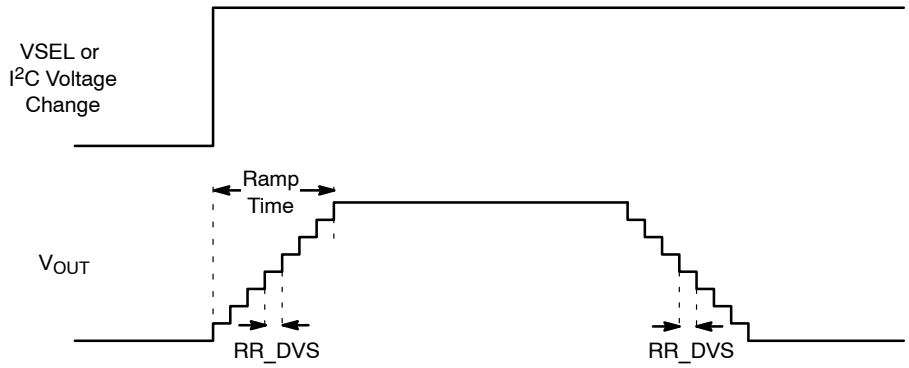

Figure 34. DVS Voltage Ramp

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Forced Continuous Conduction Mode

Forced Continuous Conduction Mode (FCCM)

Forced continuous conduction mode will disable the zero cross detection and allow the inductor current to conduct negative during light load conditions. This allows the FAN53730 to switch continuously at all loads. FCCM is beneficial when the DCM switching frequency would cause unwanted noise and interference. During constant frequency operation, the light load efficiency will be much lower compared to variable frequency operation due to higher switching losses in the converter.

The I^2C controlled device has a dedicated bit for FCCM, FORCE_CCM (Reg 06h [1]). The logic controlled device has a dedicated pin, called FCCM, for this feature.

The figure below shows the basic differences between DCM and CCM operation. DCM operation occurs for light load conditions while CCM operation occurs at heavy load or if the FCCM control is set. In DCM, the device will switch once and then enter the idle state. During the idle state, I_{OUT} will continue to discharge the output capacitor. When V_{OUT} falls below the regulation target, a new switching cycle is initiated. This causes V_{OUT} to regulate to the bottom of the output voltage ripple, and the average value to be slightly higher at $V_{OUT} + \Delta V_{OUT_DCM}/2$. In CCM operation (either with FCCM high or at heavy loads when V_{OUT} falls out of regulation before I_L reaches zero), the output voltage is regulated via a high gain feedback loop. This causes the average value of V_{OUT} to become the regulation target. The parameters listed in the following figure are approximations because they ignore circuit losses and circuit delays, but can give a good idea of the various buck converter operating conditions.

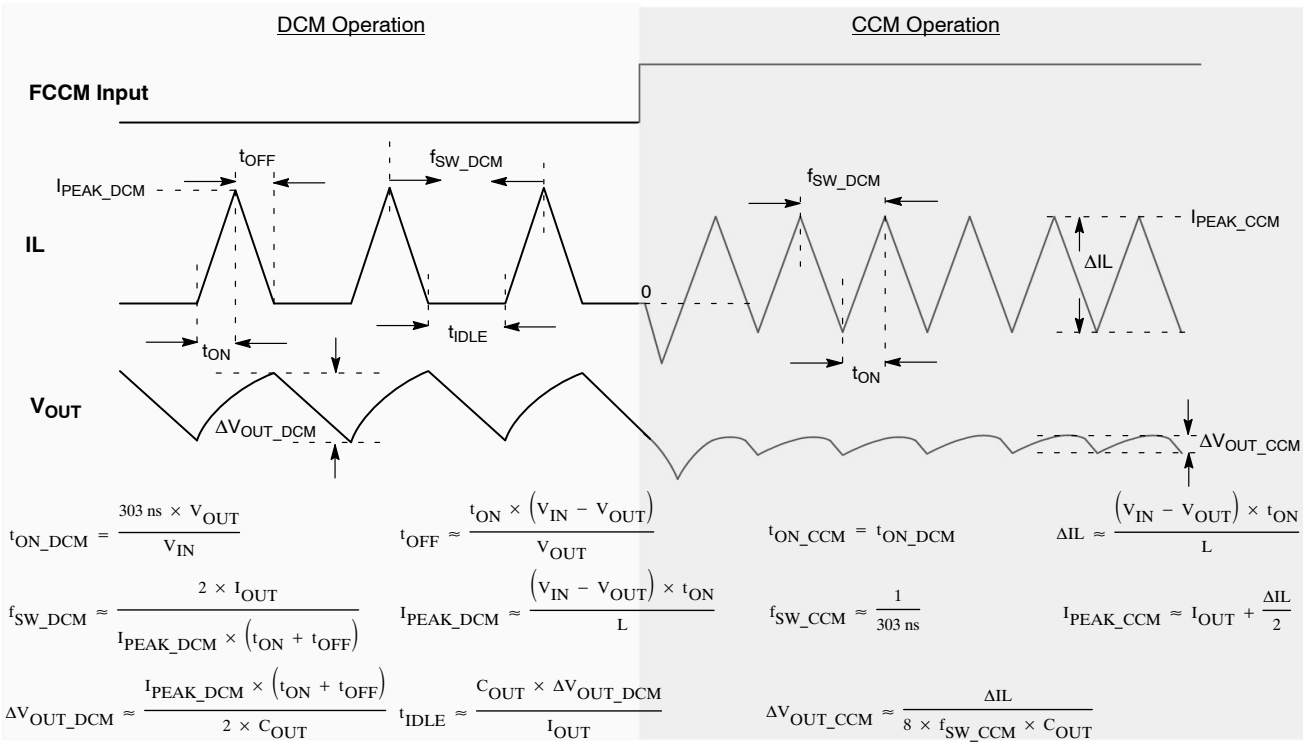

Figure 35. DCM vs. CCM Operation

Voltage Select Input

Voltage Select (VSEL Input)

VSEL is a logic input which shifts V_{OUT} between two target voltages. In the logic controlled device, VSEL will shift the target output voltage to the fixed VSET2 level when driven to a logic high. When VSEL is driven to a logic low, the output voltage will shift to the fixed VSET1 target.

In the I^2C controlled device the VSEL input operates the same except the VSET1 and VSET2 targets are programmable.

FCCM Tied to VSEL

Forced continuous conduction mode (FCCM) can be made to follow the VSEL input by enabling the VSEL_FCCM (Reg 06h [2]) bit. When this bit is set, a logic high at VSEL will change the V_{OUT} target and will place the buck in FCCM. If this bit is not set, the device remains in auto mode when VSEL is high or low. The FORCE_CCM bit will always override the VSEL_FCCM setting. See following table.

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VSEL AND FCCM

FORCE_CCM Bit	VSEL_FCCM Bit	VSEL Input	Result
0	X	0	VOUT = VSET1 target and buck is in Auto DCM/CCM
0	0	1	VOUT = VSET2 target and buck is in Auto DCM/CCM
0	1	1	VOUT = VSET2 target and buck is in FCCM
1	X	0	VOUT = VSET1 target and buck is in FCCM
1	X	1	VOUT = VSET2 target and buck is in FCCM

Bias Modes

The I^2C controlled device has three programmable bias mode options for reducing the device's quiescent current. These BIAS_MODE (Reg 03h [2:1]) bits disable infrequently used internal logic blocks during long SW idle periods, as described below:

High Bias Mode

All circuitry active when the part is enabled. Under certain conditions this mode can provide for a faster response to transient disturbances, but at the expense of higher quiescent current.

Low Bias Mode

Forces some of the FAN53730's circuitry into shutdown during the DCM idle state. This will greatly reduce no load quiescent current, but under certain conditions can lead to a slower response to a transient event.

Ultra Low Bias Mode

This mode is the default selection and will provide the lowest no load quiescent current. The logic version of the device also has the Low Bias Mode option enabled.

Transient Enhancement Bit

Setting TRANSIENT_ENHANCEMENT (Reg 03h [4]) bit will force the FAN53730's on−time to double when VOUT drops 30 mV below its regulation target. This allows for a faster recovery of V_{OUT} during load step events (low to high load). The drawback to using this mode is that during V_{OUT} recovery, because the on−time and inductor current ripple have doubled, the output can see significant overshoot. Refer to Figures 24 and 25 in Typical Characteristics section.

Protection Features

Fault Protection

The FAN53730 contains four fault modes consisting of:

- V_{IN} UVLO Fault
- Current Limit Fault
- Output Short Fault
- Thermal Fault

When any of these faults occur, the FAN53730 is placed in the fault state and is shutdown. By default, the OUT_DISCHARGE (Reg 06h [3]) bit enables the output discharge resistor during shutdown.

During Current Limit and Output Short faults the converter will auto−restart every 20 ms. This feature can be disabled by setting FAULT_SHDN (Reg 03h [3]) = 1, and instead the ENABLE bit will be reset to 0 (device remains in shutdown).

Under Voltage Fault

A V_{IN} UVLO is detected if V_{IN} falls below the UVLO_F threshold for 40 µs. Once this happens, the device stops switching and is placed in the Fault State. In the I^2C version the UVLO_FAULT Flag is set. If V_{IN} continues to fall past the UVLO threshold and crosses the power on reset threshold, the FAN53730 will immediately shutdown.

Current Limit Timeout

During valley current limit events, when I_L is clamped at I_{VALLEY}, the fault clock begins counting. If the fault clock reaches 40 µs of a continuous valley current limit condition, the device is placed into the fault state. During the fault count, if a period occurs without a valley current limit clamp event then the count is reset to 0.

In the I^2C version, when the part is placed into the fault state, the ILIM_FAULT flag is set.

Output Short Fault

If the output voltage falls below 100 mV for 40 µs, after the device has reached the active state (power good), the device will detect an output short fault and be forced into the fault state.

In the I^2C version, when the part is placed into the fault state, the SHORT_FAULT flag is set.

Thermal Shutdown

When the die temperature increases due to a high load condition and/or a high ambient temperature, the FAN53730 can reach a thermal fault condition and be placed in the Fault State. In the I^2C version the OVER_TEMP_FAULT flag is set. The device will restart after it cools below the hysteresis level.

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Operation

I²C Interface

The I²C interface is compatible with Standard, Fast, and Fast Plus I²C bus specifications. The SCL line is an input and the SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

The equivalent 7 bit slave identification for the FAN53730UCX device version is 7h'20. This is followed by the read/write bit (0 = Write) and (1 = Read).

7−Bit	Binary	Hex
7h'20	0100000	8h'40

REGISTER MAP

REGISTER MAPPING TABLE

					Read Only	Write Only	Read / Write	Read / Clear	Write/Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x01	FAULT FLAGS	0		POWER_GOOD	0	UVLO_FAULT	OVER_TEMP_FAULT	SHORT_FAULT	ILIM_FAULT
0x02	CONFIG1	0	ARM_TO	DVS_FCCM	RR_DVS			HIGH_BANDWIDTH	VAL_ILIM
0x03	CONFIG2	0			Transient_ Enhancement	FAULT_SHDN	BIAS_MODE		PG_POL
0x04	VOUT_SET_1	VSET1							
0x05	VOUT_SET_2	VSET2							
0x06	ENABLE	0		ARM_EN	DVS_EN	OUT_DISCHARGE	VSEL_FCCM	FORCE_CCM	ENABLE
0x09	RESET	SOFT_RESET							

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REGISTER DETAILS

Table 1. REGISTER DETAILS – 0 × 01 FAULT FLAGS

0 × 01 FAULT FLAGS				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	UNUSED			
5	POWER_GOOD	0	Read	Reset condition: 0 PG Bit (Tracks the state of PG Output Active state) *Code* — *Power Good Status* 0 — Power good output is not active 1 — Power good output is active
4	UNUSED			
3	UVLO_FAULT	0	R/CLR	Reset condition: 0 Displays UVLO fault status. This flag is set when a UVLO fault occurs. The flag is cleared upon read. *Code* — *Input Under Voltage Fault Occurrence* 0 — No UVLO fault occurred 1 — A UVLO fault occured
2	OVER_TEMP_FAULT	0	R/CLR	Reset condition: 0 Displays over temp fault status. This flag is set when a die over temp fault occurs. The flag is cleared upon read. *Code* — *Die Over Temperature Fault* 0 — No over temp fault 1 — An over temp fault occurred
1	SHORT_FAULT	0	R/CLR	Reset condition: 0 Displays V_{OUT} short fault status. This flag is latched when a V_{OUT} short fault occurs. The flag is cleared upon read. *Code* — *Vout Short Fault* 0 — The output has not shorted 1 — V_{OUT} has dropped below 100 mV for > 40 μs
0	ILIM_FAULT	0	R/CLR	Reset condition: 0 The ILIM flag is set if the valley current limit is triggered continuously for 40 μs. The flag is cleared upon read. *Code* — *VALLEY Current Limit Fault* 0 — No ILIM fault 1 — ILIM triggered event for 40 μs

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Table 2. REGISTER DETAILS – 0 × 02 CONFIG1

0 × 02 CONFIG1				Default = 00000111
Bit	**Name**	**Default**	**Type**	**Description**
7	UNUSED			
6	ARM_TO	0	R/W	Reset condition: 0 Sets the timeout period for Audio Reduction Mode forced switching event *Code* — *Audio Reduction Mode Timeout* 0 — 25 µs 1 — 40 µs
5	DVS_FCCM	0	R/W	Reset condition: 0 Controls whether the Force CCM functionality is active when DVS is enabled and the voltage is programmed from high to low. *Code* — *CCM During high to low DVS Transition* 0 — Force CCM is not active during negative V_{OUT} transitions 1 — Force CCM is active during negative V_{OUT} transitions
4:2	RR_DVS	001	R/W	Reset condition: 001 DVS (and also Soft−Start) ramp rate *Code* — *DVS Time per step* 000 — 2 µs/step 001 — 4 µs/step 010 — 6 µs/step 011 — 8 µs/step 100 — 10 µs/step 101 — 12 µs/step 110 — 14 µs/step 111 — 16 µs/step
1	HIGH_BANDWIDTH	1	R/W	Reset condition: 1 Control loop high bandwidth adjust. Set to “0” when V_{OUT} < 0.8 V. *Code* — *Bandwidth Adjust* 0 — Low Bandwidth setting 1 — High Bandwidth setting
0	VAL_ILIM	1	R/W	Reset condition: 1 Valley Current Limit threshold. The FAN53730 will limit the valley of the inductor current to the I_{VALLEY} target. *Code* — *I_{VALLEY} (Typ)* 0 — 2.3 A 1 — 4.2 A

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Table 3. REGISTER DETAILS – 0 × 03 CONFIG2

0 × 03 CONFIG2				Default = 00010001
Bit	**Name**	**Default**	**Type**	**Description**
7:5	UNUSED			
4	TRANSIENT_ENHANCEMENT	1	R/W	Reset condition: 1
				Transient Enhancement Mode *Code* — *Transient Enhancement Mode* 0 — Disables the extended on–time during V_{OUT} dips 1 — Enables the extended on–time during V_{OUT} dips
3	FAULT_SHDN	0	R/W	Reset condition: 0
				This register enables/disables the shutdown option for faults. Note: For proper operation, this bit should only be written to when the device is in the shutdown state. *Code* — *Fault Shutdown Control* 0 — The converter will auto–restart after 20 ms if a fault occurs 1 — The converter will be placed into shutdown if a fault occurs
2:1	BIAS_MODE	00	R/W	Reset condition: 00
				Sets the converters ability to shutdown various blocks to achieve low quiescent current vs. output accuracy and response time. *Code* — *Low Bias Mode Control* 00 — Ultra Low Bias Mode 01 — Low Bias Mode 1X — High Bias Mode
0	PG_POL	1	R/W	Reset condition: 1
				Changes the polarity of the Power–Good Output *Code* — *Power–Good Polarity* 0 — PG output is active low 1 — PG output is active high

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Table 4. REGISTER DETAILS – 0 × 04 VOUT_SET_1

0 × 04 VOUT SET1				Default = 01100011 (1.00 V)							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VSET1	01100011	R/W	Reset conditions: 0 × 63							
				Sets the buck regulation target voltage when VSEL = low.							
				Hex	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*
				0 × 00	0.0100	0 × 40	0.6500	0 × 80	1.2900	0 × C0	1.9300
				0 × 01	0.0200	0 × 41	0.6600	0 × 81	1.3000	0 × C1	1.9400
				0 × 02	0.0300	0 × 42	0.6700	0 × 82	1.3100	0 × C2	1.9500
				0 × 03	0.0400	0 × 43	0.6800	0 × 83	1.3200	0 × C3	1.9600
				0 × 04	0.0500	0 × 44	0.6900	0 × 84	1.3300	0 × C4	1.9700
				0 × 05	0.0600	0 × 45	0.7000	0 × 85	1.3400	0 × C5	1.9800
				0 × 06	0.0700	0 × 46	0.7100	0 × 86	1.3500	0 × C6	1.9900
				0 × 07	0.0800	0 × 47	0.7200	0 × 87	1.3600	0 × C7	2.0000
				0 × 08	0.0900	0 × 48	0.7300	0 × 88	1.3700	0 × C8	2.0100
				0 × 09	0.1000	0 × 49	0.7400	0 × 89	1.3800	0 × C9	2.0200
				0 × 0A	0.1100	0 × 4A	0.7500	0 × 8A	1.3900	0 × CA	2.0300
				0 × 0B	0.1200	0 × 4B	0.7600	0 × 8B	1.4000	0 × CB	2.0400
				0 × 0C	0.1300	0 × 4C	0.7700	0 × 8C	1.4100	0 × CC	2.0500
				0 × 0D	0.1400	0 × 4D	0.7800	0 × 8D	1.4200	0 × CD	2.0600
				0 × 0E	0.1500	0 × 4E	0.7900	0 × 8E	1.4300	0 × CE	2.0700
				0 × 0F	0.1600	0 × 4F	0.8000	0 × 8F	1.4400	0 × CF	2.0800
				0 × 10	0.1700	0 × 50	0.8100	0 × 90	1.4500	0 × D0	2.0900
				0 × 11	0.1800	0 × 51	0.8200	0 × 91	1.4600	0 × D1	2.1000
				0 × 12	0.1900	0 × 52	0.8300	0 × 92	1.4700	0 × D2	2.1100
				0 × 13	0.2000	0 × 53	0.8400	0 × 93	1.4800	0 × D3	2.1200
				0 × 14	0.2100	0 × 54	0.8500	0 × 94	1.4900	0 × D4	2.1300
				0 × 15	0.2200	0 × 55	0.8600	0 × 95	1.5000	0 × D5	2.1400
				0 × 16	0.2300	0 × 56	0.8700	0 × 96	1.5100	0 × D6	2.1500
				0 × 17	0.2400	0 × 57	0.8800	0 × 97	1.5200	0 × D7	2.1600
				0 × 18	0.2500	0 × 58	0.8900	0 × 98	1.5300	0 × D8	2.1700
				0 × 19	0.2600	0 × 59	0.9000	0 × 99	1.5400	0 × D9	2.1800
				0 × 1A	0.2700	0 × 5A	0.9100	0 × 9A	1.5500	0 × DA	2.1900
				0 × 1B	0.2800	0 × 5B	0.9200	0 × 9B	1.5600	0 × DB	2.2000
				0 × 1C	0.2900	0 × 5C	0.9300	0 × 9C	1.5700	0 × DC	2.2100
				0 × 1D	0.3000	0 × 5D	0.9400	0 × 9D	1.5800	0 × DD	2.2200
				0 × 1E	0.3100	0 × 5E	0.9500	0 × 9E	1.5900	0 × DE	2.2300
				0 × 1F	0.3200	0 × 5F	0.9600	0 × 9F	1.6000	0 × DF	2.2400
				0 × 20	0.3300	0 × 60	0.9700	0 × A0	1.6100	0 × E0	2.2500
				0 × 21	0.3400	0 × 61	0.9800	0 × A1	1.6200	0 × E1	2.2600
				0 × 22	0.3500	0 × 62	0.9900	0 × A2	1.6300	0 × E2	2.2700
				0 × 23	0.3600	0 × 63	1.0000	0 × A3	1.6400	0 × E3	2.2800
				0 × 24	0.3700	0 × 64	1.0100	0 × A4	1.6500	0 × E4	2.2900
				0 × 25	0.3800	0 × 65	1.0200	0 × A5	1.6600	0 × E5	2.3000

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Table 4. REGISTER DETAILS – 0 × 04 VOUT_SET_1 (continued)

0 × 04 VOUT SET1				Default = 01100011 (1.00 V)							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VSET1	01100011	R/W	Reset conditions: 0 × 63							
				Sets the buck regulation target voltage when VSEL = low.							
				Hex	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*
				0 × 26	0.3900	0 × 66	1.0300	0 × A6	1.6700	0 × E6	2.3100
				0 × 27	0.4000	0 × 67	1.0400	0 × A7	1.6800	0 × E7	2.3200
				0 × 28	0.4100	0 × 68	1.0500	0 × A8	1.6900	0 × E8	2.3300
				0 × 29	0.4200	0 × 69	1.0600	0 × A9	1.7000	0 × E9	2.3400
				0 × 2A	0.4300	0 × 6A	1.0700	0 × AA	1.7100	0 × EA	2.3500
				0 × 2B	0.4400	0 × 6B	1.0800	0 × AB	1.7200	0 × EB	2.3600
				0 × 2C	0.4500	0 × 6C	1.0900	0 × AC	1.7300	0 × EC	2.3600
				0 × 2D	0.4600	0 × 6D	1.1000	0 × AD	1.7400	0 × ED	2.3600
				0 × 2E	0.4700	0 × 6E	1.1100	0 × AE	1.7500	0 × EE	2.3600
				0 × 2F	0.4800	0 × 6F	1.1200	0 × AF	1.7600	0 × EF	2.3600
				0 × 30	0.4900	0 × 70	1.1300	0 × B0	1.7700	0 × F0	2.3600
				0 × 31	0.5000	0 × 71	1.1400	0 × B1	1.7800	0 × F1	2.3600
				0 × 32	0.5100	0 × 72	1.1500	0 × B2	1.7900	0 × F2	2.3600
				0 × 33	0.5200	0 × 73	1.1600	0 × B3	1.8000	0 × F3	2.3600
				0 × 34	0.5300	0 × 74	1.1700	0 × B4	1.8100	0 × F4	2.3600
				0 × 35	0.5400	0 × 75	1.1800	0 × B5	1.8200	0 × F5	2.3600
				0 × 36	0.5500	0 × 76	1.1900	0 × B6	1.8300	0 × F6	2.3600
				0 × 37	0.5600	0 × 77	1.2000	0 × B7	1.8400	0 × F7	2.3600
				0 × 38	0.5700	0 × 78	1.2100	0 × B8	1.8500	0 × F8	2.3600
				0 × 39	0.5800	0 × 79	1.2200	0 × B9	1.8600	0 × F9	2.3600
				0 × 3A	0.5900	0 × 7A	1.2300	0 × BA	1.8700	0 × FA	2.3600
				0 × 3B	0.6000	0 × 7B	1.2400	0 × BB	1.8800	0 × FB	2.3600
				0 × 3C	0.6100	0 × 7C	1.2500	0 × BC	1.8900	0 × FC	2.3600
				0 × 3D	0.6200	0 × 7D	1.2600	0 × BD	1.9000	0 × FD	2.3600
				0 × 3E	0.6300	0 × 7E	1.2700	0 × BE	1.9100	0 × FE	2.3600
				0 × 3F	0.6400	0 × 7F	1.2800	0 × BF	1.9200	0 × FF	2.3600

Table 5. REGISTER DETAILS – 0 × 05 VOUT_SET_2

0 × 05 VOUT SET2				Default = 01101000 (1.05 V)							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VSET2	01101000	R/W	Reset conditions: 0 × 68							
				Sets the buck regulation target voltage when VSEL = high.							
				Hex	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*
				0 × 00	0.0100	0 × 40	0.6500	0 × 80	1.2900	0 × C0	1.9300
				0 × 01	0.0200	0 × 41	0.6600	0 × 81	1.3000	0 × C1	1.9400
				0 × 02	0.0300	0 × 42	0.6700	0 × 82	1.3100	0 × C2	1.9500
				0 × 03	0.0400	0 × 43	0.6800	0 × 83	1.3200	0 × C3	1.9600
				0 × 04	0.0500	0 × 44	0.6900	0 × 84	1.3300	0 × C4	1.9700

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Table 5. REGISTER DETAILS – 0 × 05 VOUT_SET_2 (continued)

0 × 05 VOUT SET2				Default = 01101000 (1.05 V)							
Bit	**Name**	**Default**	**Type**	**Description**							
				0 × 05	0.0600	0 × 45	0.7000	0 × 85	1.3400	0 × C5	1.9800
				0 × 06	0.0700	0 × 46	0.7100	0 × 86	1.3500	0 × C6	1.9900
				0 × 07	0.0800	0 × 47	0.7200	0 × 87	1.3600	0 × C7	2.0000
				0 × 08	0.0900	0 × 48	0.7300	0 × 88	1.3700	0 × C8	2.0100
				0 × 09	0.1000	0 × 49	0.7400	0 × 89	1.3800	0 × C9	2.0200
				0 × 0A	0.1100	0 × 4A	0.7500	0 × 8A	1.3900	0 × CA	2.0300
				0 × 0B	0.1200	0 × 4B	0.7600	0 × 8B	1.4000	0 × CB	2.0400
				0 × 0C	0.1300	0 × 4C	0.7700	0 × 8C	1.4100	0 × CC	2.0500
				0 × 0D	0.1400	0 × 4D	0.7800	0 × 8D	1.4200	0 × CD	2.0600
				0 × 0E	0.1500	0 × 4E	0.7900	0 × 8E	1.4300	0 × CE	2.0700
				0 × 0F	0.1600	0 × 4F	0.8000	0 × 8F	1.4400	0 × CF	2.0800
				0 × 10	0.1700	0 × 50	0.8100	0 × 90	1.4500	0 × D0	2.0900
				0 × 11	0.1800	0 × 51	0.8200	0 × 91	1.4600	0 × D1	2.1000
				0 × 12	0.1900	0 × 52	0.8300	0 × 92	1.4700	0 × D2	2.1100
				0 × 13	0.2000	0 × 53	0.8400	0 × 93	1.4800	0 × D3	2.1200
				0 × 14	0.2100	0 × 54	0.8500	0 × 94	1.4900	0 × D4	2.1300
				0 × 15	0.2200	0 × 55	0.8600	0 × 95	1.5000	0 × D5	2.1400
				0 × 16	0.2300	0 × 56	0.8700	0 × 96	1.5100	0 × D6	2.1500
				0 × 17	0.2400	0 × 57	0.8800	0 × 97	1.5200	0 × D7	2.1600
				0 × 18	0.2500	0 × 58	0.8900	0 × 98	1.5300	0 × D8	2.1700
				0 × 19	0.2600	0 × 59	0.9000	0 × 99	1.5400	0 × D9	2.1800
				0 × 1A	0.2700	0 × 5A	0.9100	0 × 9A	1.5500	0 × DA	2.1900
				0 × 1B	0.2800	0 × 5B	0.9200	0 × 9B	1.5600	0 × DB	2.2000
				0 × 1C	0.2900	0 × 5C	0.9300	0 × 9C	1.5700	0 × DC	2.2100
				0 × 1D	0.3000	0 × 5D	0.9400	0 × 9D	1.5800	0 × DD	2.2200
				0 × 1E	0.3100	0 × 5E	0.9500	0 × 9E	1.5900	0 × DE	2.2300
				0 × 1F	0.3200	0 × 5F	0.9600	0 × 9F	1.6000	0 × DF	2.2400
				0 × 20	0.3300	0 × 60	0.9700	0 × A0	1.6100	0 × E0	2.2500
				0 × 21	0.3400	0 × 61	0.9800	0 × A1	1.6200	0 × E1	2.2600
				0 × 22	0.3500	0 × 62	0.9900	0 × A2	1.6300	0 × E2	2.2700
				0 × 23	0.3600	0 × 63	1.0000	0 × A3	1.6400	0 × E3	2.2800
				0 × 24	0.3700	0 × 64	1.0100	0 × A4	1.6500	0 × E4	2.2900
				0 × 25	0.3800	0 × 65	1.0200	0 × A5	1.6600	0 × E5	2.3000

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Table 5. REGISTER DETAILS – 0 × 05 VOUT_SET_2 (continued)

0 × 05 VOUT SET2				Default = 01101000 (1.05 V)							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VSET2	01101000	R/W	Reset conditions: 0 × 68							
				Sets the buck regulation target voltage when VSEL = high.							
				Hex	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*	*Hex*	*VOUT(V)*
				0 × 26	0.3900	0 × 66	1.0300	0 × A6	1.6700	0 × E6	2.3100
				0 × 27	0.4000	0 × 67	1.0400	0 × A7	1.6800	0 × E7	2.3200
				0 × 28	0.4100	0 × 68	1.0500	0 × A8	1.6900	0 × E8	2.3300
				0 × 29	0.4200	0 × 69	1.0600	0 × A9	1.7000	0 × E9	2.3400
				0 × 2A	0.4300	0 × 6A	1.0700	0 × AA	1.7100	0 × EA	2.3500
				0 × 2B	0.4400	0 × 6B	1.0800	0 × AB	1.7200	0 × EB	2.3600
				0 × 2C	0.4500	0 × 6C	1.0900	0 × AC	1.7300	0 × EC	2.3600
				0 × 2D	0.4600	0 × 6D	1.1000	0 × AD	1.7400	0 × ED	2.3600
				0 × 2E	0.4700	0 × 6E	1.1100	0 × AE	1.7500	0 × EE	2.3600
				0 × 2F	0.4800	0 × 6F	1.1200	0 × AF	1.7600	0 × EF	2.3600
				0 × 30	0.4900	0 × 70	1.1300	0 × B0	1.7700	0 × F0	2.3600
				0 × 31	0.5000	0 × 71	1.1400	0 × B1	1.7800	0 × F1	2.3600
				0 × 32	0.5100	0 × 72	1.1500	0 × B2	1.7900	0 × F2	2.3600
				0 × 33	0.5200	0 × 73	1.1600	0 × B3	1.8000	0 × F3	2.3600
				0 × 34	0.5300	0 × 74	1.1700	0 × B4	1.8100	0 × F4	2.3600
				0 × 35	0.5400	0 × 75	1.1800	0 × B5	1.8200	0 × F5	2.3600
				0 × 36	0.5500	0 × 76	1.1900	0 × B6	1.8300	0 × F6	2.3600
				0 × 37	0.5600	0 × 77	1.2000	0 × B7	1.8400	0 × F7	2.3600
				0 × 38	0.5700	0 × 78	1.2100	0 × B8	1.8500	0 × F8	2.3600
				0 × 39	0.5800	0 × 79	1.2200	0 × B9	1.8600	0 × F9	2.3600
				0 × 3A	0.5900	0 × 7A	1.2300	0 × BA	1.8700	0 × FA	2.3600
				0 × 3B	0.6000	0 × 7B	1.2400	0 × BB	1.8800	0 × FB	2.3600
				0 × 3C	0.6100	0 × 7C	1.2500	0 × BC	1.8900	0 × FC	2.3600
				0 × 3D	0.6200	0 × 7D	1.2600	0 × BD	1.9000	0 × FD	2.3600
				0 × 3E	0.6300	0 × 7E	1.2700	0 × BE	1.9100	0 × FE	2.3600
				0 × 3F	0.6400	0 × 7F	1.2800	0 × BF	1.9200	0 × FF	2.3600

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Table 6. REGISTER DETAILS – 0 × 06 ENABLE

0 × 06 ENABLE				Default = 00011000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	UNUSED			
5	ARM_EN	0	R/W	Reset condition: 0
				Audible Reduction Mode Control *Code* — *Audio Reduction Mode Control* 0 — Audio Reduction Mode Disabled 1 — Audio Reduction Mode Enabled
4	DVS_EN	1	R/W	Reset condition: 0
				This bit enables/disables the DVS functionality Note: The dvs_en bit only controls whether the part ramps up/down the vout_code in steady state. The part will always ramp up at the programmed DVS ramp during start−up. Additionally, when FCCM is selected the DVS cannot be disabled. *Code* — *DVS Enable* 0 — DVS disabled 1 — DVS enabled
3	OUT_DISCHARGE	1	R/W	Reset condition: 1
				Enabled/Disables the 100 Ω output discharge resistance in shutdown *Code* — *Output Discharge Control* 0 — Output discharge is disabled 1 — Output discharge is enabled when device is placed in shutdown
2	VSEL_FCCM	0	R/W	Reset condition: 0
				VSEL activates Force CCM *Code* — *VSEL Control FCCM* 0 — FCCM and VSEL are separate functions 1 — FCCM will be enabled when VSEL is at a logic high
1	FORCE_CCM	0	R/W	Reset condition: 0
				Forces the part to operate in CCM regardless of the load current *Code* — *Force CCM Control* 0 — Auto (DCM/CCM depending on load current) 1 — Force CCM at all loads
0	ENABLE	0	R/W	Reset condition: 0
				This register enables/disables the FAN53730. The EN bit must be set and the EN input must be driven high to enable the device. *Code* — *FAN53730 Enable* 0 — Device disabled 1 — Device enabled

Table 7. REGISTER DETAILS – 0 × 09 RESET

0 × 09 RESET				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	SOFT_RESET	0	Write	Reset condition: 0 × 00
				The software reset register allows all I^2C settings to be reverted to POR defaults when 0 × 45h code is written to it.

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APPLICATION CIRCUIT

Application Circuit Diagram

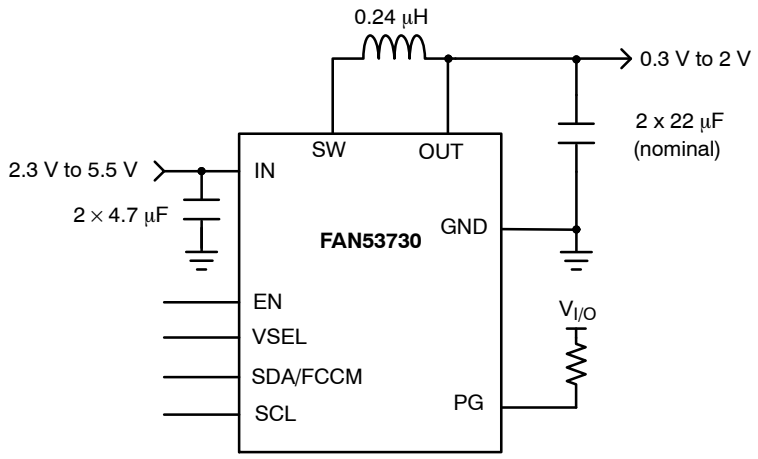

Figure 36. Typical Application Circuit

APPLICATION GUIDELINES

Applications Circuit Components

The following table shows the components used in the typical application curves and the System Specifications Table (unless otherwise noted). This table should be used as a guide in selecting equivalent components from different manufacturers.

Components Table

APPLICATIONS CIRCUIT COMPONENTS EXAMPLES

Component	Manufacturer	Part Number	Value	Case Size (nominal)	Rating	Notes
CIN	Murata	GRM155R61A475MEAA#	4.7 μF	1 mm × 0.5 mm × 0.5 mm	6.3 V	Local capacitor
COUT	Murata	GRM158R60J226ME01D	22 μF	1 mm × 0.5 mm × 0.5 mm	6.3 V	Requires 2
L	Taiyo Yuden	LSCNE2012HKTR24MD	0.24 μH	2 mm × 1.25 mm × 0.8 mm	4.8 A	

Input Capacitor Consideration

The input current into a buck is discontinuous and can see very fast di/dt (> 3 A/ns). As a result, the input capacitor selection and placement is critical in ensuring the input voltage is clean and the voltage ripple is kept low. A 10 μF effective input capacitance can be sufficient to filter the FAN53730's input current, provided that CIN is placed very close to the IN bump and GND bump (see Recommended Layout). If this is not the case then parasitic inductance between (CIN+ and IN), and (CIN – and GND) will create high frequency voltage spikes on the V_{IN} and GND paths which can feed into V_{OUT} and other nodes.

Typically two 4.7 μF (0402) local capacitors are enough for bypassing IN. However, if CIN is located far away from a low impedance power source (VBATT), any appreciable series inductance between VBATT and CIN can cause a resonance frequency on the IN terminal during load or line transients which can disturb V_{OUT}. Depending on the amount of series inductance from VBATT to IN, the CIN capacitance may have to be increased.

Inductor Consideration

The inductor selection should be based on the required inductor saturation and maximum current rating to support the load current. The Application Circuit Components Table lists the inductor used to generate the typical operating curves, and should be used as a reference for selecting similar inductors for the specific application.

Output Capacitor Considerations

The FAN53730 is designed to use a minimum (2 x 22 μF) nominal output capacitor (or equivalent). COUT should be placed as close as possible to the inductor and the GND bumps. This will minimize any PCB inductance which can cause high frequency conducted noise at the output. The minimum capacitance for stability was based on the typical derating curve below (single device). The part number is shown in the Application Circuit Components Table. This nominal curve should be used as a target for selecting suitable capacitors not shown in the Typical Applications Components Table, which are equivalent or better than this.

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For capacitors which derate more vs DC bias, it may be necessary to add more in parallel to attain the suitable minimum capacitance.

For I_{OUT} < 500 mA, a single 22 µF(0402) capacitor can be used as long as HIGH_BANDWIDTH (Reg 02h [1]) = 0 and $V_{OUT} \geq 0.8$ V.

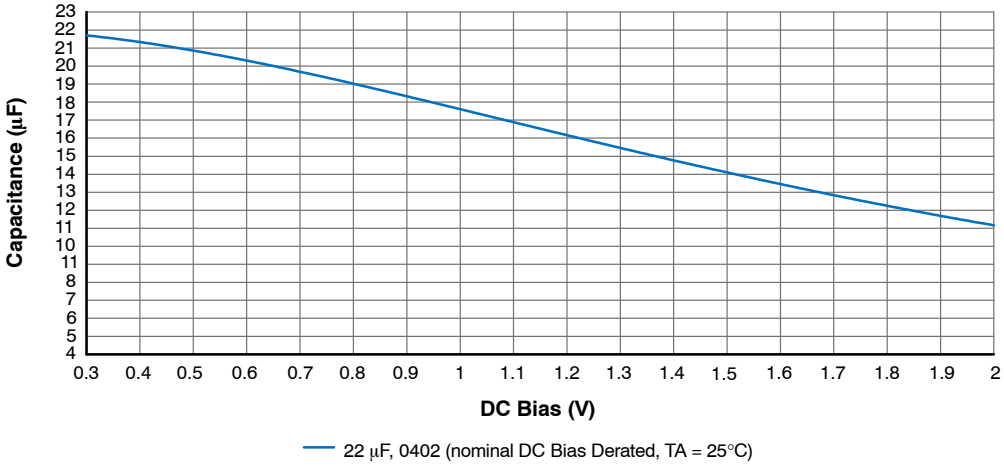

Figure 37. Typical 22 µF Ceramic Capacitor Value vs. DC Bias Voltage

Layout Examples

The buck converter layout is centered around the placement of CIN, COUT, and the inductor L. Because of the discontinuous input current, the placement of CIN is the most critical and should be placed as close to the IN and GND terminals as possible. Secondly, the inductor (L) should be placed close to the COUT+ terminal and have a direct connection to SW with minimal PCB trace area. Minimizing the PCB trace area will limit the parasitic capacitance at SW which can cause a degradation in efficiency. Third, COUT(s) should return as close as possible to the inductor and GND connection as possible. The following figure details a layout which can be used as a guideline.

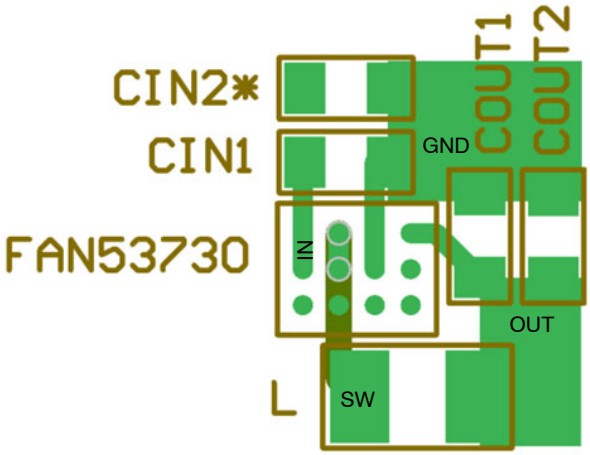

Figure 38. Layout Example

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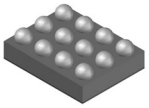
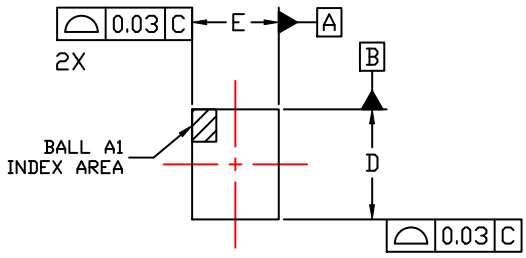
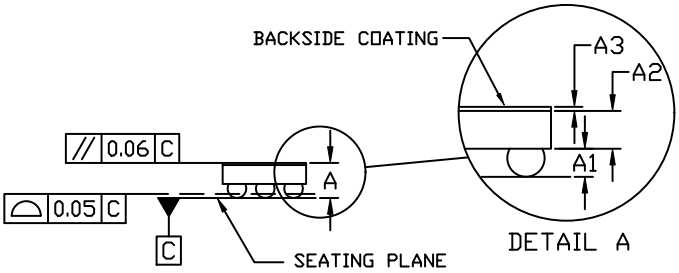


WLCSP12 1.07x1.36x0.432, 0.35P
CASE 567GK
ISSUE O

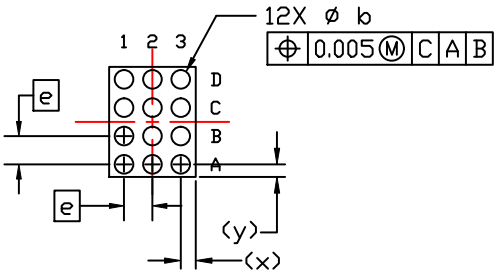
DATE 09 NOV 2021



TOP VIEW



SIDE VIEW

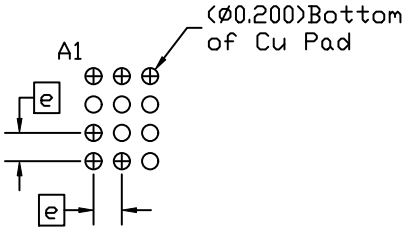


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.391	0.432	0.473
A1	0.154	0.174	0.194
A2	0.215	0.233	0.251
A3	0.022	0.025	0.028
b	0.211	0.231	0.251
D	1.330	1.360	1.390
E	1.040	1.070	1.100
e	0.35 BSC		
x	0.170	0.185	0.200
y	0.140	0.155	0.170



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(NSMD PAD TYPE)

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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