RTKA210040DR0000BU

The RTKA210040DR0000BU demonstration board (shown in Figure 2 and Figure 3) features the RAA210040. Capable of delivering up to 4A of continuous current, the RAA210040 is a compact, synchronous step-down, non-isolated complete power supply that is optimized for space-constrained applications. The RAA210040 is based on a peak current mode PWM control scheme that provides a fast transient response and excellent loop stability. The switching frequency is programmable from 500kHz to 4MHz with either the external resistor or synchronization to an external clock through the SYNC pin.

The RTKA210040DR0000BU demonstration board is a 1×1 inch 4-layer FR4 board with 2oz. copper on all layers. It is optimized to minimize the complete power module solution size. Operating from a single 2.7V to 5.5V input power rail, the RTKA210040DR0000BU demonstration board offers adjustable output voltages down to 0.6V, up to 95% efficiency, and better than 1.5% accuracy over line, load, and temperature. A dedicated enable pin and power-good flag allow for easy system power rails sequencing.

By default, the board is set to a 1.2V output voltage with a 1.2MHz switching frequency.

Features

- Wide input voltage range from 2.7V to 5.5V
- Adjustable output voltage down to 0.6V with ±1.5% accuracy over line, load, and temperature
- Up to 95% conversion efficiency
- 100% duty cycle
- Internal 1ms soft-start time
- Prebias output start-up
- External frequency synchronization up to 4MHz
- Dedicated enable pin and PGOOD flag
- UVLO, overcurrent, negative overcurrent, overvoltage, and over-temperature protections

Specifications

The demonstration board is configured and optimized for the following operating conditions:

- V_{IN} = 2.7V to 5.5V
- V_{OUT} = 1.2V
- $I_{OUT-MAX}$ = 4A
- f_{SW} = 1.2MHz

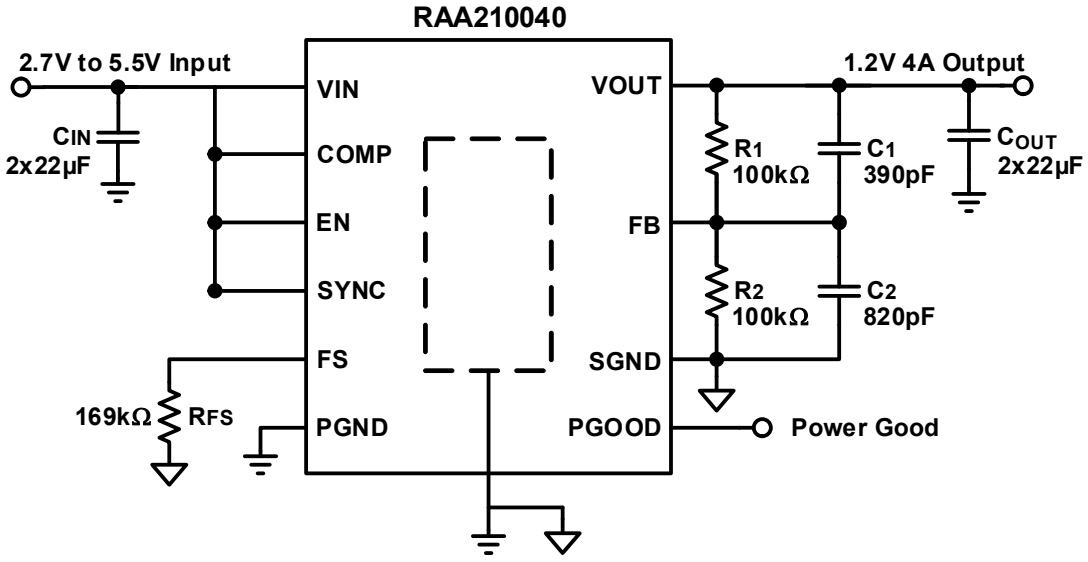


Figure 1. RTKA210040DR0000BU Block Diagram

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1. Functional Description

The RTKA210040DR0000BU provides the peripheral circuitry to demonstrate the feature set of the RAA210040. The demonstration board includes several connectors, test points, and jumpers that simplify the validation of the module. The module is enabled and disabled by moving the jumper across the EN pin as shown in Figure 2. Selecting features like external frequency synchronization is performed by removing the pull-up resistor R_3 of the SYNC pin and connecting the signal generator (square pulse waveform clock signal) to TP4 of the SYNC pin. The output voltage (0.6V - 5V) and the switching frequency (500kHz to 4MHz) are programmed by changing the resistors as shown in Figure 3.

1.1 Recommended Testing Equipment

- 0V to 5.5V power supply with at least 4A source current capability
- Electronic loads capable of sinking current up to 4A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

1.2 Quick Test Guide

1. Disable the module by connecting the jumper across 2 and 1 on J3 for the EN pin as shown in Figure 2 and Figure 7.
2. Use the appropriate cables to connect the DC input power supply to banana sockets J1 and J2 and the electronic load to sockets J4 and J5. Ensure that the polarity for the power leads is correct and the input voltage is within the operating range (2.7V - 5.5V) of the module. Use test points TP1 (VIN) and TP2 (PGND) for accurately measuring the input voltage.
3. Turn on the input power supply.
4. To enable the module, you can connect the jumper across 2 and 3 on J3 for the EN pin to enable the module.
5. To enable external frequency synchronization, remove the pull-up resistor R_3 of the SYNC pin and connect the external clock to TP4 (SYNC). To ensure proper operation, Renesas recommends that the external SYNC frequency is within ±25% of the switching frequency set by R_2 and the FS pin.
6. Probe test points TP6 (VOUT) and TP7 (PGND) to observe the output voltage. The output voltage should read 1.2V.
7. Adjust the input voltage, V_{IN}, within the specified range and observe the output voltage. The output voltage variation should be within ±1.5%.
8. Adjust the load current to within the specified range (0 - 4A) and observe the output voltage. The output voltage variation should be within ±1.5%.
9. To change V_{OUT}, disconnect the demonstration board from the setup and populate standard 0402 resistors at the R_{10} and R_{11} locations on the bottom layer. The Output Voltage Resistor Settings table in the RAA210040 datasheet can be used as a reference for programming different output voltages. See the RAA210040 Design Guide Matrix table in Table 1 for correct input and output capacitors, switching frequency, and output voltage combinations.
10. The switching frequency is modified by populating a standard 0402 resistor at the R_2 location on the bottom layer. See Equation 1 in the RAA210040 datasheet for selecting the correct value of R_2 within the admissible operating range (500kHz - 4MHz).

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Table 1. RAA210040 Design Guide Matrix (See Figure 1)

Case	V_{IN} (V)	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	C_{IN} (Ceramic) (µF)	C_{OUT} (Ceramic) (µF)	Freq (MHz)	R_{FS} (kΩ)	C_1 (pF)	C_2 (pF)
1	3.3	0.6	100	open	2x22	1x47	0.8	261	390	820
2	3.3	0.8	100	301	2x22	2x22	0.9	232	390	820
3	3.3	0.9	100	200	2x22	2x22	1	205	390	820
4	3.3	1	100	150	2x22	2x22	1	205	390	820
5	3.3	1.2	100	100	2x22	2x22	1.2	169	390	820
6	3.3	1.5	100	66.5	2x22	2x22	1.3	154	390	680
7	3.3	1.8	100	49.9	2x22	2x22	1.5	133	390	560
8	3.3	2.5	100	31.6	2x22	2x22	1.8	107	390	470
9	5	1	100	150	2x22	2x22	1	205	390	820
10	5	1.2	100	100	2x22	2x22	1.2	169	390	820
11	5	1.5	100	66.5	2x22	2x22	1.3	154	390	680
12	5	1.8	100	49.9	2x22	2x22	1.5	133	390	560
13	5	2.5	100	31.6	2x22	2x22	1.8	107	390	470
14	5	3.3	100	22.1	2x22	2x22	2.4	76.8	390	470

1.3 Thermal Considerations and Current Derating

To ensure the module can operate safely and deliver the maximum allowable power, the board layout is critical. For the board to operate properly at high ambient temperature environments and carry full load current, carefully design the board layout to maximize thermal performance. To achieve this, use enough trace width, copper weight, and proper connectors.

The RTKA210040DR0000BU demonstration board is capable of operating at 4A full-load current at room temperature without the need for additional cooling systems. However, if the board needs to operate at elevated ambient temperatures, the available output current may need to be derated. See the derated current curves in the RAA210040 datasheet to determine the maximum output current that the module can supply.

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2. Board Design

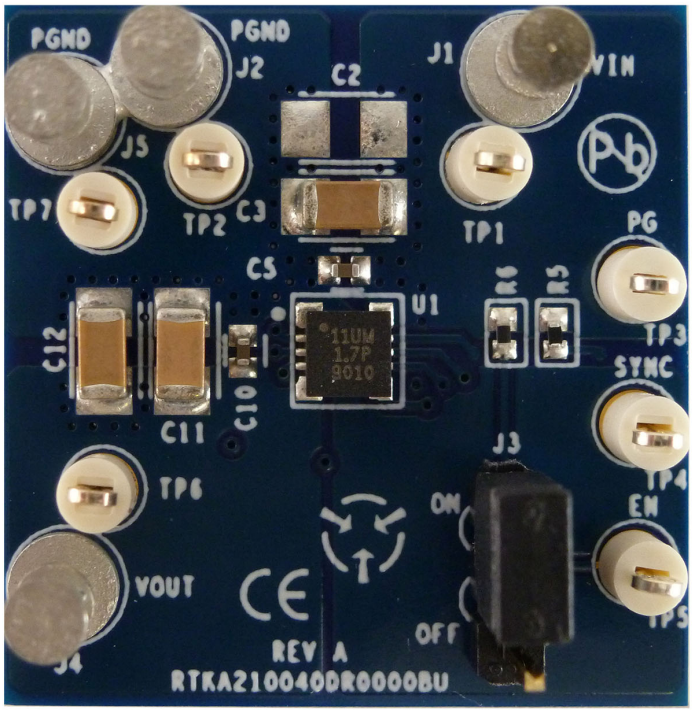


Figure 2. Top of Board

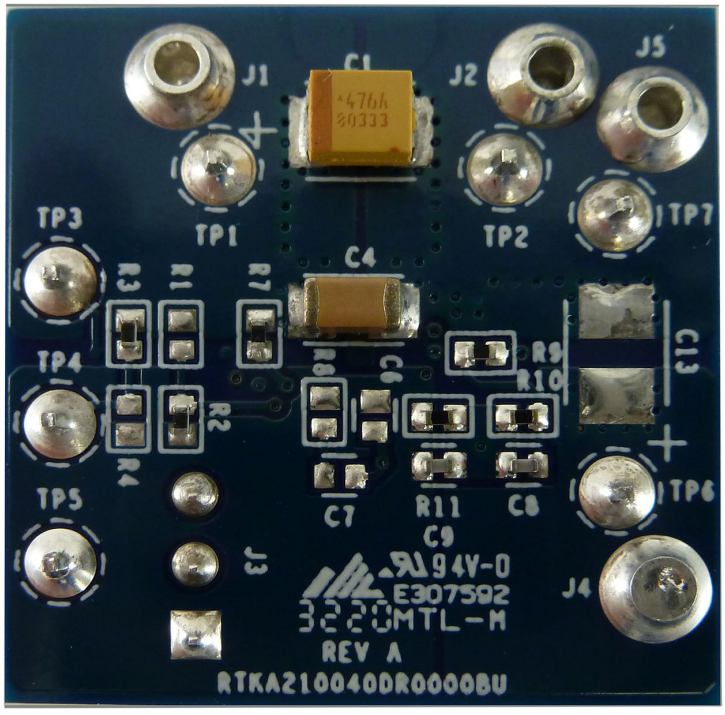


Figure 3. Bottom of Board

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2.1 Layout Guidelines

The RTKA210040DR0000BU demonstration board is a 1x1 inch four-layer FR-4 board with 2oz. copper on all the layers. The board can be used as a single 4A reference design. See Figure 8 through Figure 13 for board layout information.

The RTKA210040DR0000BU board layout is optimized for compact complete power module solution size, good electrical and thermal performance. For similar performance in designs involving RAA210040, follow these layout design tips.

2.1.1 Layout Considerations

- Place the input ceramic capacitors as close as possible to the module input. These ceramic capacitors minimize the high frequency noise by reducing the parasitic inductance of the power loop. Proper placement of these capacitors not only leads to less PHASE node spikes and ringing, but also minimizes the switching noise coupled to the module. Renesas recommends using dielectric X7R or equivalent with a minimum total capacitance of 44µF at the module input. A layout example is shown in Figure 4 and Figure 5.
- Use large copper planes to minimize conduction loss and thermal stress for VIN, VOUT, and PGND. Use multiple vias to connect the power planes in different layers.
- Use a separate SGND plane for components that are connected to SGND. Connect SGND and PGND at a single point on the top layer as shown in Figure 6.
- Use a remote-sensing trace to connect to the point-of-load and achieve tight output voltage regulation. Route the remote-sensing trace underneath the PGND layer and avoid routing it near noisy planes. Place an optional 2Ω resistor close to the output voltage resistor divider and FB pin to damp the noise on the trace.

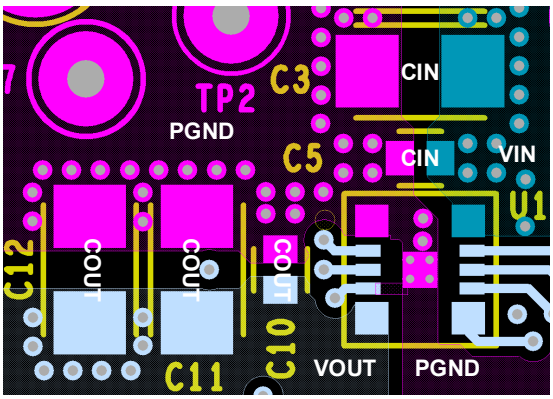


Figure 4. Layout Example - Top Layer

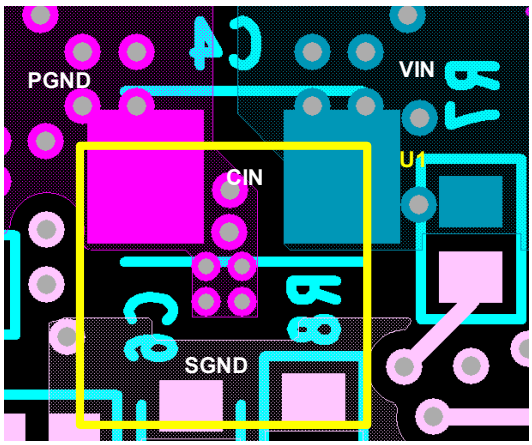


Figure 5. Layout Example - Bottom Layer

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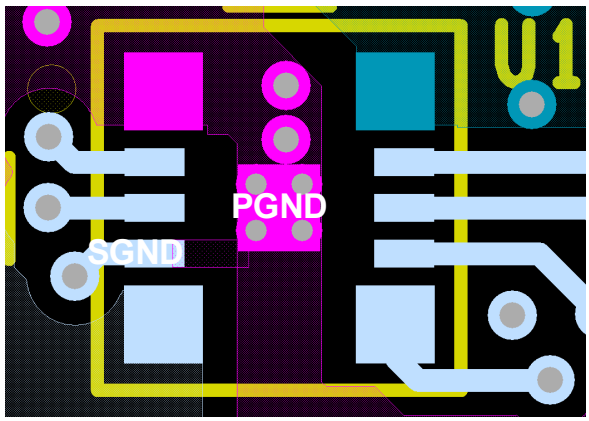


Figure 6. Layout Example - SGND is Connected to PGND at Single Point

2.2 Schematic Drawing

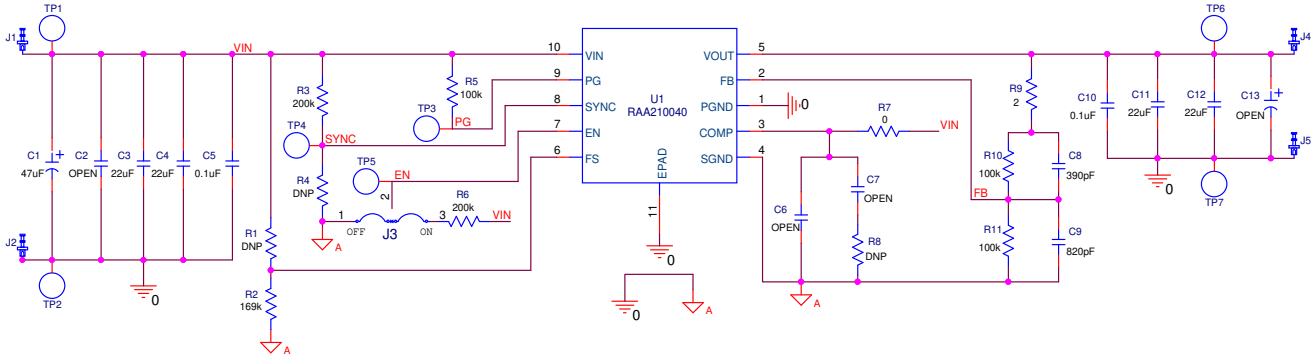


Figure 7. Schematic

2.3 Bill of Materials

Qty	Reference Designators	Value	Tol.	Volt	PWR	Package Type	Manufacturer	Part Number	Description
1	C1	47µF	±10%	10V		1411	AVX Corporation	TPSB476K010R0250	POSCAP
1	C2	OPEN	±10%	10V		1206	Murata	GRM31CR71A226KE15L	Ceramic Capacitor
2	C3, C4	22uF	±10%	10V		1206	Murata	GRM31CR71A226KE15L	Ceramic Capacitor
2	C5, C10	0.1µF	±10%	50V		0402	Murata	GRM155R71H104KE14D	Ceramic Capacitor
2	C6, C7	OPEN	±10%	50V		0402	Murata		Ceramic Capacitor
1	C8	390pF	±5%	50V		0402	Murata	GRM1555C1H391JA01D	Ceramic Capacitor
1	C9	820pF	±5%	50V		0402	Murata	GRM1555C1H821JA01D	Ceramic Capacitor

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Qty	Reference Designators	Value	Tol.	Volt	PWR	Package Type	Manufacturer	Part Number	Description
2	C11, C12	22µF	±10%	6.3V		1206	Murata	GRM31CR70J226KE19L	Ceramic Capacitor
1	C13	OPEN	±10%	6.3V		1206	Murata	GRM31CR70J226KE19L	Ceramic Capacitor
1	R1	DNP				0402			Thick Film Chip Resistor
1	R2	169kΩ	±1%		1/16W	0402	Stackpole	RMCF0402FT169K	Thick Film Chip Resistor
2	R3, R6	200kΩ	±1%		1/16W	0402	Stackpole	RMCF0402FT200K	Thick Film Chip Resistor
2	R4, R8	DNP			1/16W	0402			Thick Film Chip Resistor
1	R5	100kΩ	±1%		1/10W	0402	Panasonic	ERJ-2RKF1003X	Miniature PC Test Point
1	R7	0Ω			1/16W	0402	Stackpole	RMCF0402ZT0R00	Thick Film Chip Resistor
1	R9	2Ω	±1%		1/16W	0402	Vishay Dale	CRCW04022R00FNED	Thick Film Chip Resistor
2	R10, R11	100kΩ	±0.5%		1/16W	0402	Vishay Dale	CRCW0402100KDHEDP	Thick Film Chip Resistor
4	J1, J2, J3, J4					Through Hole	Keystone	1514-2	Terminal Turret Connector Single End
1	J3					Through Hole	Metz Connect	PR20203VBNN	Connector Header
5	TP1, TP2, TP3, TP4, TP5					CONN-MINI TEST POINT	Keystone	5002	Miniature PC Test Point
1	U1					10Ld 3x3 Dual Flat Embedded Laminate	Renesas	RAA210040	Power Module

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2.4 PCB Layout

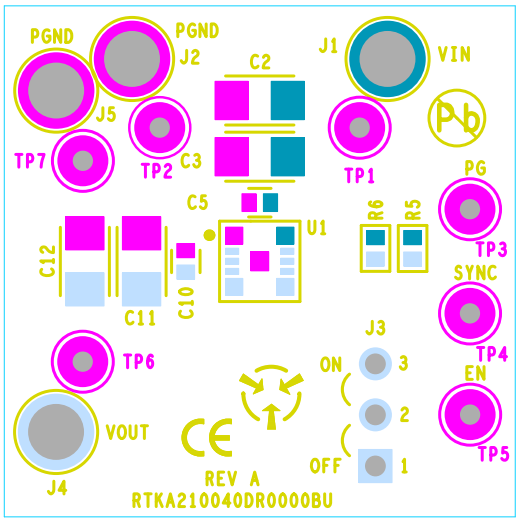


Figure 8. Silkscreen Top

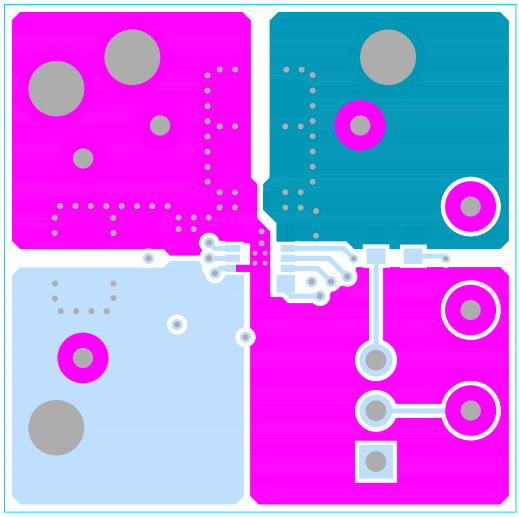


Figure 9. Top Layer

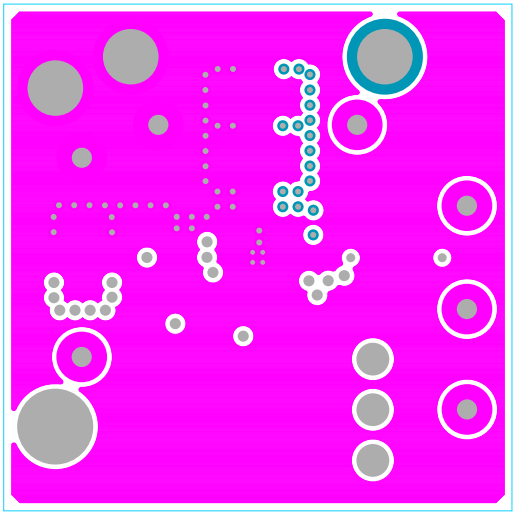


Figure 10. Layer 2

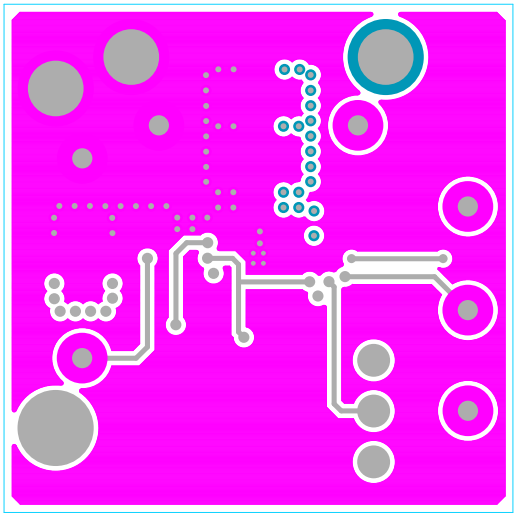


Figure 11. Layer 3

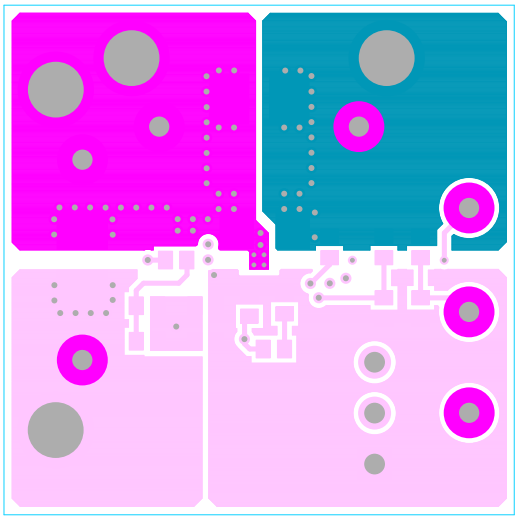


Figure 12. Layer 4

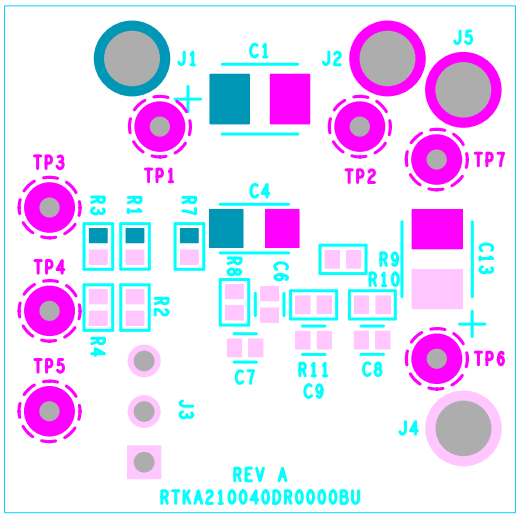


Figure 13. Silkscreen Bottom

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3. Typical Performance Graphs

The following data was acquired using the RTKA210040DR0000BU demonstration board at +25C ambient and free air 0LFM. Operating condition: V_{OUT} = 1.2V, f_{SW} = 1.2MHz, unless otherwise noted. See the Table 1 for recommended configurations for different output voltages.

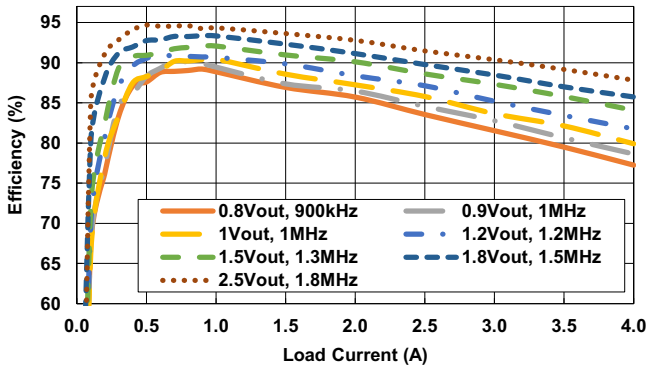


Figure 14. Efficiency vs Load Current at V_{IN} = 3.3V

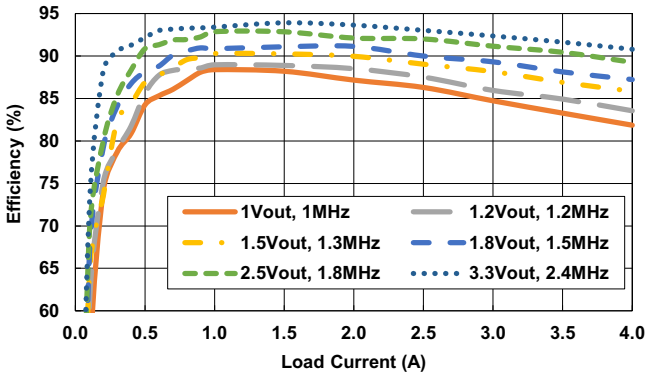


Figure 15. Efficiency vs Load Current at V_{IN} = 5V

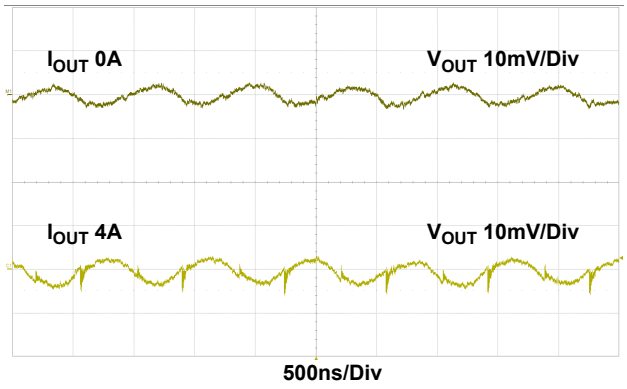


Figure 16. Output Ripple, V_{IN} = 3.3V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, C_{OUT} = 2x22µF Ceramic

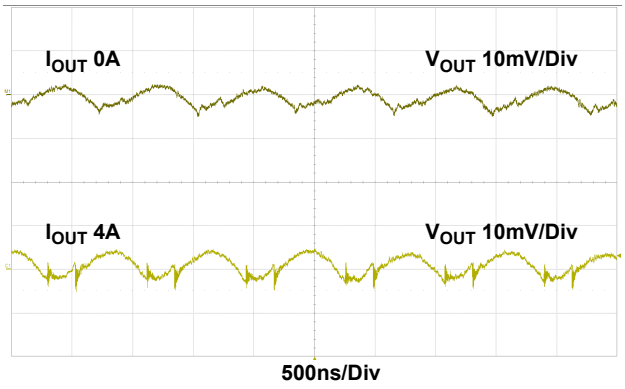


Figure 17. Output Ripple, V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, C_{OUT} = 2x22µF Ceramic

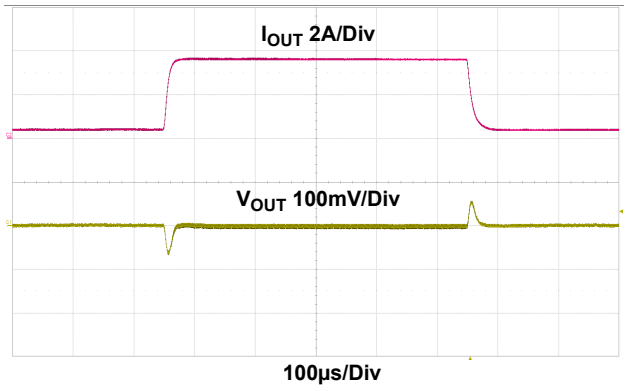


Figure 18. Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, 0.4A to 3.6A, C_{OUT} = 2x22µF Ceramic

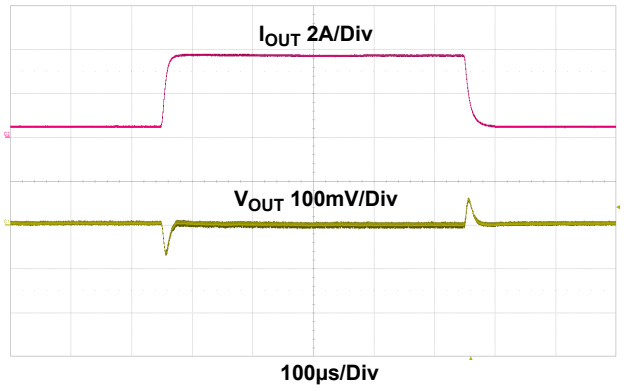


Figure 19. Transient Response, V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, 0.4A to 3.6A, C_{OUT} = 2x22µF Ceramic

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Operating condition: V_{OUT} = 1.2V, f_{SW} = 1.2MHz, unless otherwise noted.

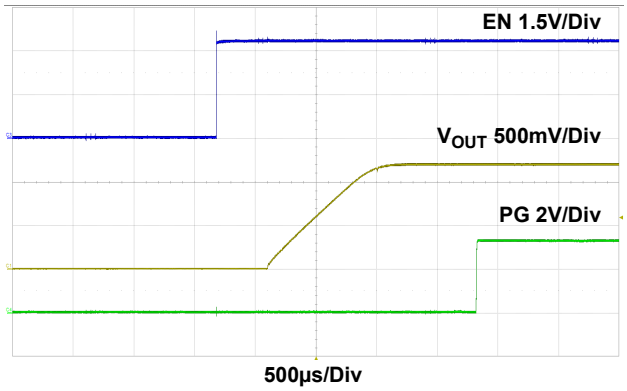


Figure 20. Start-Up Waveform, V_{IN} = 3.3V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = 0A, C_{OUT} = 2x22µF Ceramic

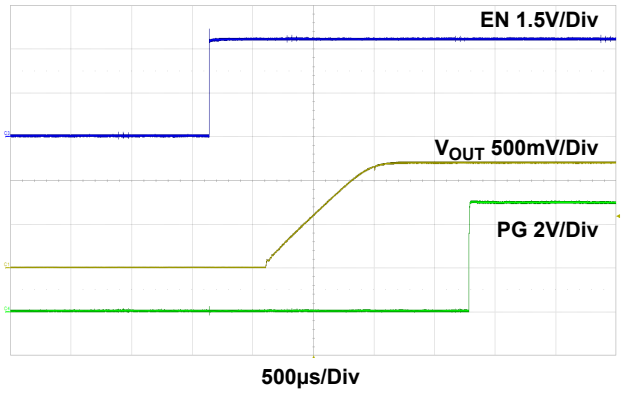


Figure 21. Start-Up Waveform, V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = 0A, C_{OUT} = 2x22µF Ceramic

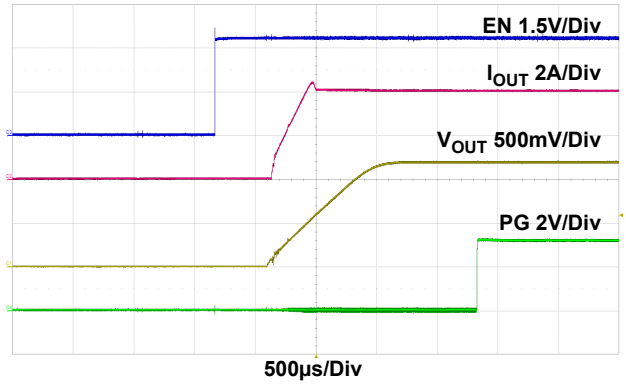


Figure 22. Start-Up Waveform, V_{IN} = 3.3V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = 2A, C_{OUT} = 2x22µF Ceramic

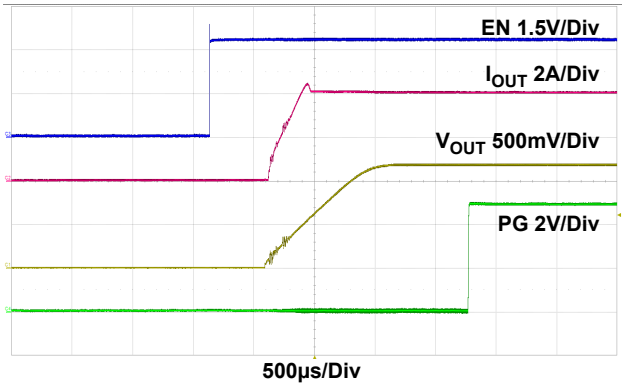


Figure 23. Start-Up Waveform, V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = 2A, C_{OUT} = 2x22µF Ceramic

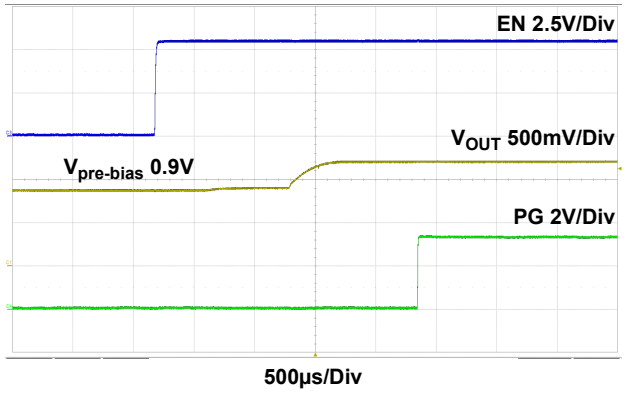


Figure 24. Pre-biased Power-Up Waveform, Pre-biased Voltage = 0.9V, V_{IN} = 3.3V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = No Load, C_{OUT} = 2x22µF Ceramic

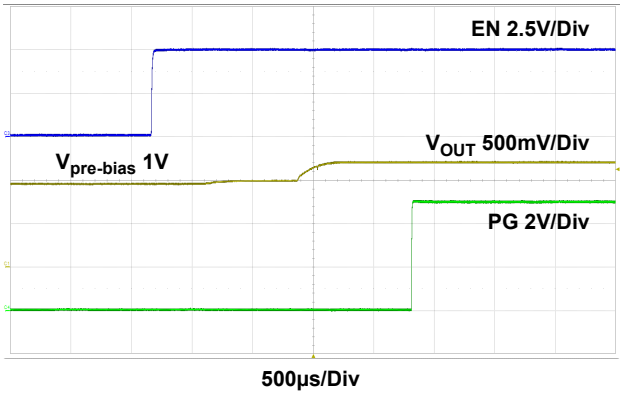


Figure 25. Pre-biased Power-Up Waveform, Pre-biased Voltage = 1V, V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1.2MHz, I_{OUT} = No Load, C_{OUT} = 2x22µF Ceramic

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Operating condition: V_{OUT} = 1.2V, f_{SW} = 1.2MHz, unless otherwise noted.

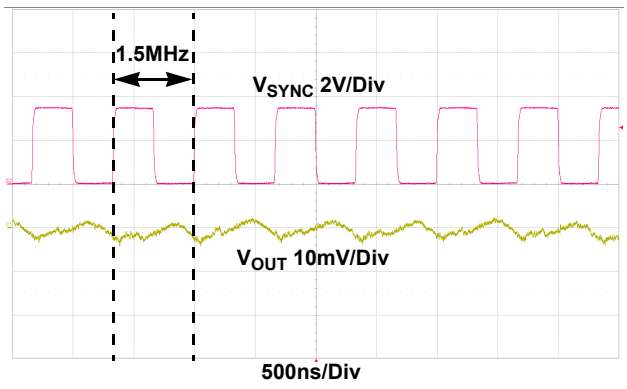


Figure 26. External Frequency Synchronization Waveform, V_{IN}= 3.3V, V_{OUT} = 1.2V, f_{SYNC} = 1.5MHz, I_{OUT} = 0A, C_{OUT} = 2x22uF Ceramic

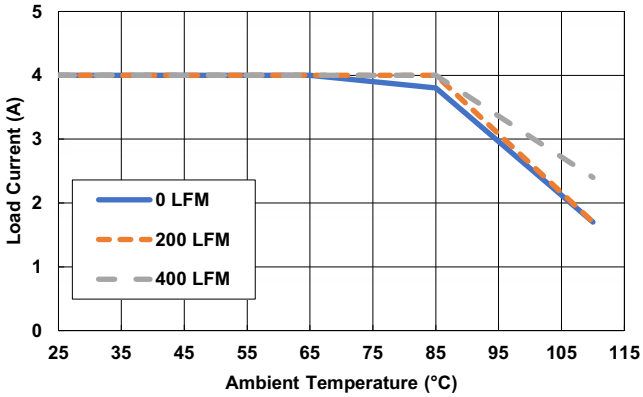


Figure 27. Derating Curve, V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 2x22µF Ceramic

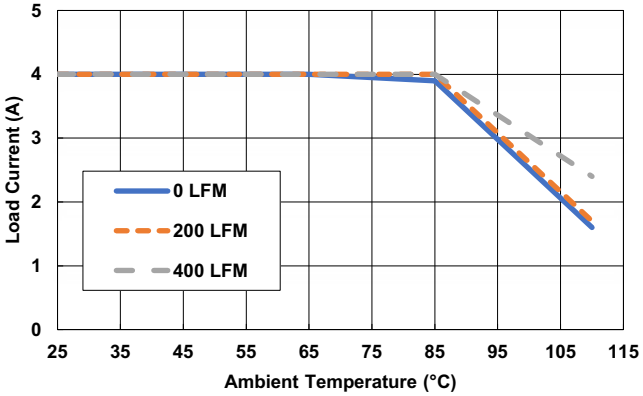


Figure 28. Derating Curve, V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 2x22µF Ceramic

4. Ordering Information

Part Number	Description
RTKA210040DR0000BU	RAA210040 5V, 4A power module demonstration board

5. Revision History

Rev.	Date	Description
1.1	Apr 14, 2021	Updated file number to correct numbering: R16UH0009EU0101. Updated Quick Test Guide section Steps 5 and 6.
1.0	Apr 4, 2021	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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