STRUCTURE : Silicon Monolithic Integrated Circuit

PRODUCT SERIES : Power Driver for Compact Disc Player

TYPE : BA5984FP

PACKAGE OUTLINES : fig.1 (Plastic Mold)

POWER DISSIPATION : fig.2

BLOCK DIAGRAM : fig.3

APPLICATION : fig.4

TEST CIRCUIT : fig.5-1,2

機 能 :
- 4channel BTL driver、1channel reversible driver.
- Small surface mounting power package (HSOP-28).
- Thermal-shut-down circuit built in.
- Wide dynamic range (6.0V(Typ.)at VCC=8V, RL=8Ω)

<BTL driver>
- Input pins consist of (+) and (-), therefore various input types are available such as differential input.

<Loading driver>
- Brake circuit built in.
- Circuit protection diode built in

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	13.5	V
Power dissipation	Pd	1.7 *1	W
Operating temperature	Topr	−40 ～ 85	℃
Storage temperature	Tstg	−55 ～ 150	℃

*1 On less than 3% (percentage occupied by copper foil), 70×70mm², t=1.6mm, glass epoxy mounting. Reduce power by 13.6mW for each degree above 25℃.

GUARANTEED OPERATING RANGES

VCC	4.3 ～ 13.2 V

●ELECTRICAL CHARACTERISTICS (Unless otherwise note, Ta=25℃, Vcc=8V, BIAS=2.5V, RL=8Ω)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions	test circuit
Quiescent current	ICC	—	24	34	mA	$R_L=\infty$	fig.5-1
<BTL driver>							
Output offset voltage	VOO	-50	0	50	mV		fig.5-2
Max. output voltage	VOM	5.4	6.0	—	V		fig.5-2
Closed loop voltage gain	GVC	14.0	16.1	18.0	dB		fig.5-2
Mute on voltage	VMTON	—	—	0.5	V		fig.5-1, 2
Mute off voltage	VMTOFF	1.5	—	—	V		fig.5-1, 2
Input current for Mute pin	IMUTE	—	180	270	uA	VMUTE=5V	fig.5-1
Input current for Bias pin	IBIAS	—	75	120	uA	VBIAS=2.5V	fig.5-1
<OP-AMP>							
Common mode input voltage rang	VICM	0.5	—	6.8	V		
Input offset voltage	VOFOP	-6	0	6	mV		fig.5-2
Input bias current	IBOP	—	—	300	nA		fig.5-2
High level output voltage	VOHOP	7.5	—	—	V		fig.5-2
Low level output voltage	VOLOP	—	—	0.5	V		fig.5-2
Output sink current	ISIN	1	—	—	mA	Output to PreVCC by 50Ω	fig.5-2
Output source current	ISOU	1	—	—	mA	Output to GND by 50Ω	fig.5-2
slew rate	SROP	—	1	—	V/us	Input pulse 100KHz, 2Vp-p	fig.5-2
<Loading driver>							
Output saturation voltage 1	VSAT1	0.7	1.1	1.6	V	Upper + Lower saturation, IL=200mA	fig.5-2
Output saturation voltage between F&R	ΔVSAT1	—	—	0.1	V	Output saturation voltage 1 between FWD and REV	fig.5-2
Output saturation voltage 2	VSAT2	1.0	1.55	2.3	V	Upper + Lower saturation, IL=500mA	fig.5-2
<Loading driver input logic>							
Input high level voltage	VIHLD	1.5	—	VCC	V		fig.5-2
Input low level voltage	VILLD	-0.3	—	0.5	V		fig.5-2
Input high level current	IIHLD	—	180	270	uA	VFWD=VREV=5V	fig.5-1

● This product is not designed for protection against radioactive rays.

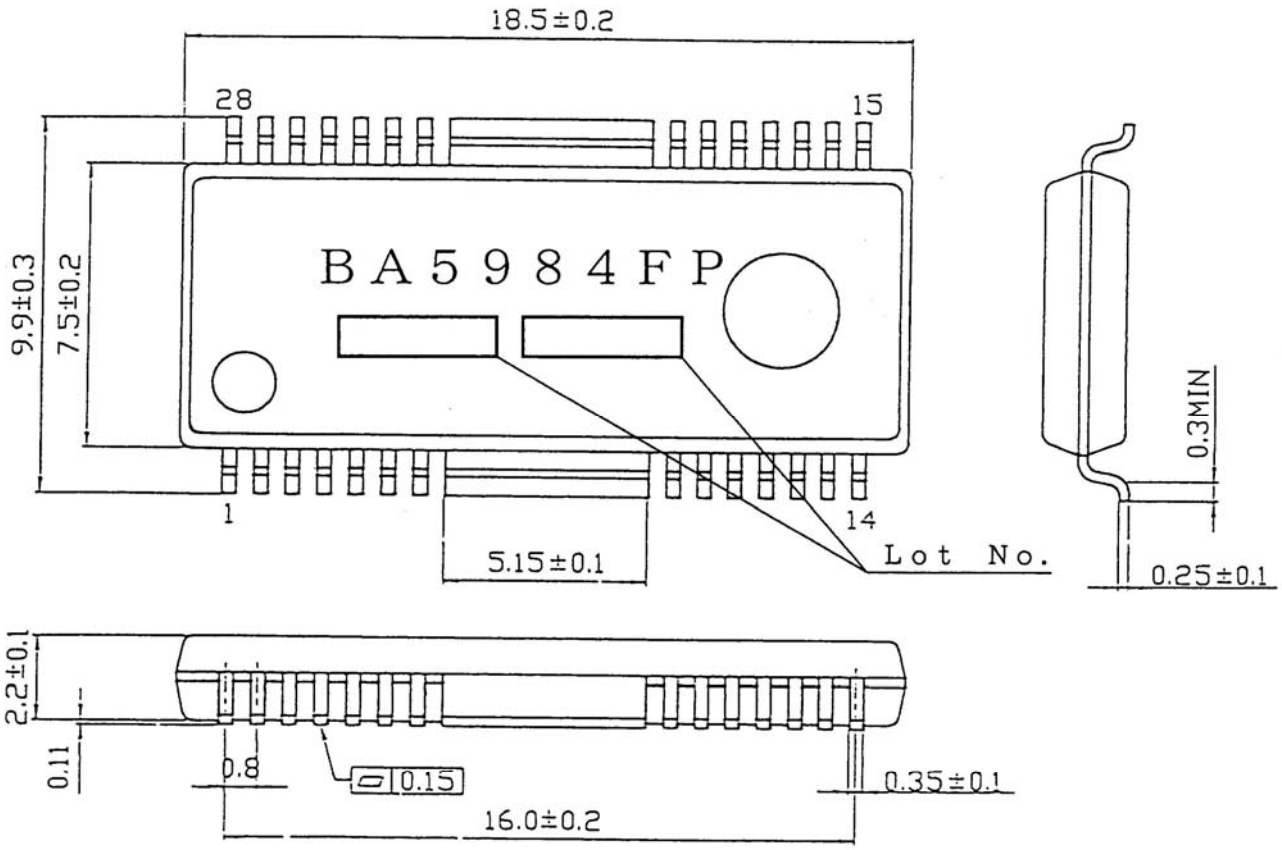
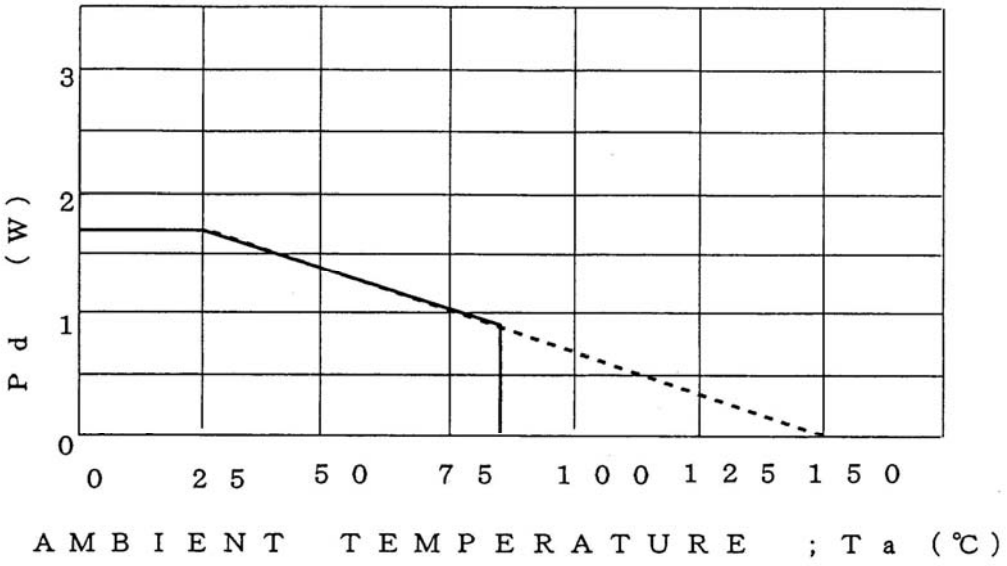


fig.1 PACKAGE OUTLINES

(UNIT : mm)

Figure number ; B0835

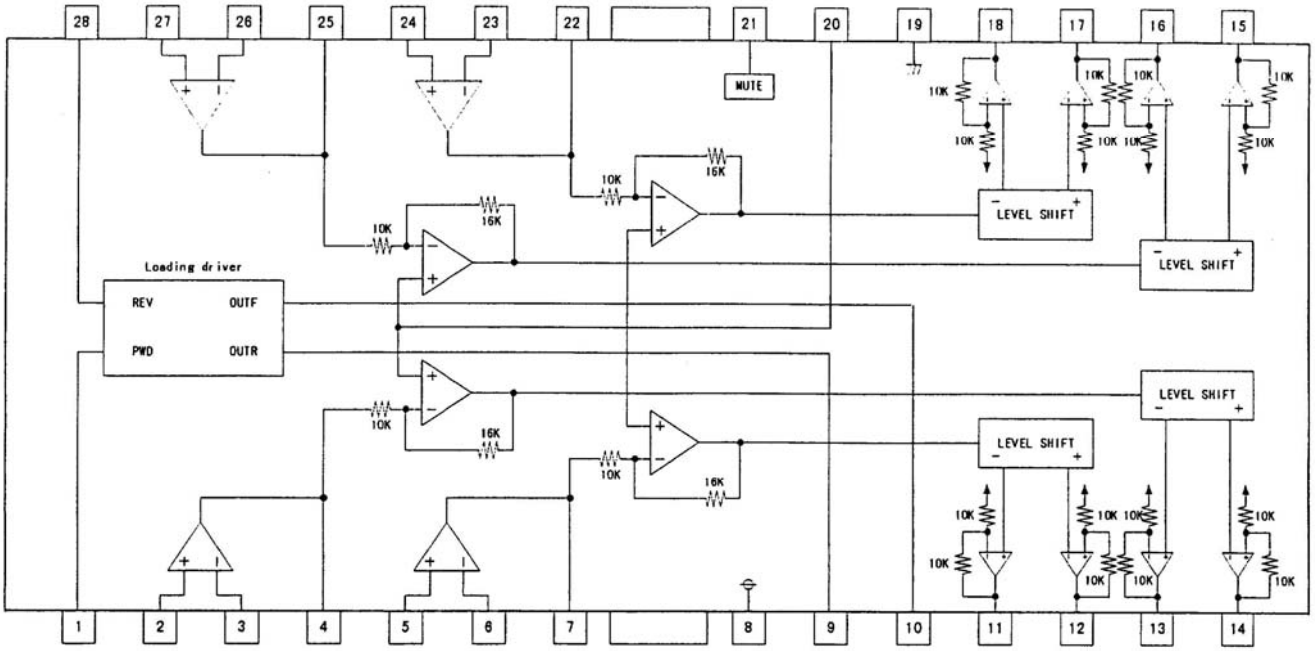
●Electrical characteristic curves



Pd ; power dissipation

* On less than 3% (percentage occupied by copper foil), 70X70mm², t=1.6mm, glass epoxy mounting.

fig2. POWER DISSIPATION



resister unit (Ω)

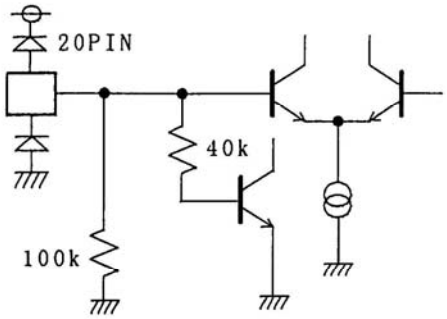
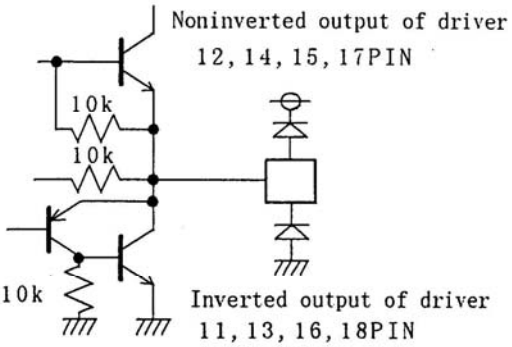
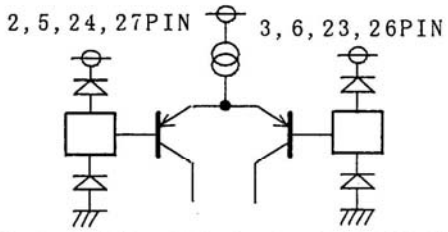
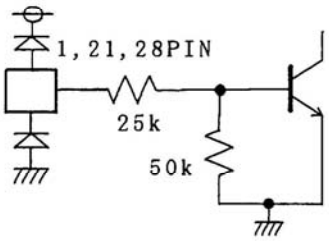
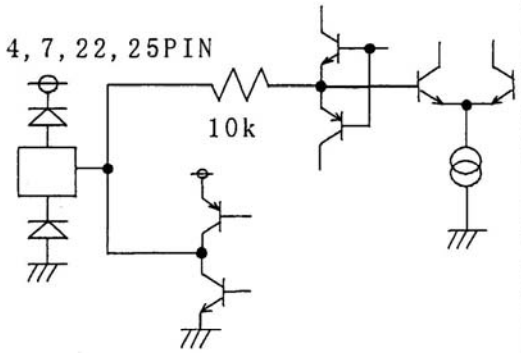
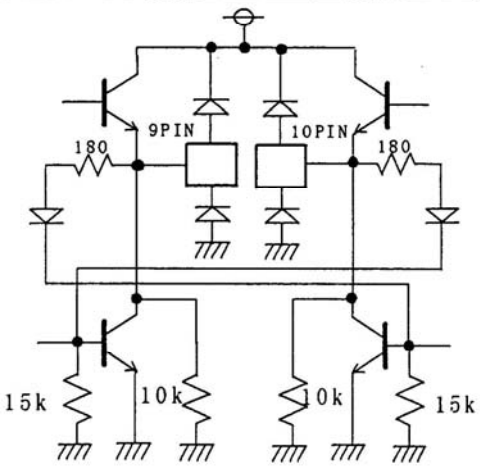
fig.3 BLOCK DIAGRAM

●Pin description

No	Symbol	Function	No	Symbol	Function
1	FWD	Input for loading forward	15	VO4(+)	Non inverted output of CH4
2	OPIN1(+)	Non inverted input of CH1 OP-AMP	16	VO4(-)	Inverted output of CH4
3	OPIN1(-)	inverted input of CH1 OP-AMP	17	VO3(+)	Non inverted output of CH3
4	OPOUT1	Output of CH1 OP-AMP	18	VO3(-)	Inverted output of CH3
5	OPIN2(+)	Non inverted input of CH2 OP-AMP	19	GND	Substrate ground
6	OPIN2(-)	inverted input of CH2 OP-AMP	20	BIAS	Input for Bias-amplifier
7	OPOUT2	Output of CH2 OP-AMP	21	MUTE	Input for mute control
8	VCC	VCC	22	OPOUT3	Output for CH3 OP-AMP
9	VOL(-)	Inverted output of loading	23	OPIN3(-)	Inverting input for CH3 OP-AMP
10	VOL(+)	Non inverted output of loading	24	OPIN3(+)	Non inverting input for CH3 OP-AMP
11	VO2(-)	Inverted output of CH2	25	OPOUT4	Output for CH4 OP-AMP
12	VO2(+)	Non inverted output of CH2	26	OPIN4(-)	Inverting input for CH4 OP-AMP
13	VO1(-)	Inverted output of CH1	27	OPIN4(+)	Non inverting input for CH4 OP-AMP
14	VO1(+)	Non inverted output of CH1	28	REV	Input for loading reverse

notes) Symbol of + and - (output of drivers) means polarity to input pin.
(For example if voltage of pin4 high, pin14 is high.)

● EQUIVALENT CIRCUIT OF TERMINALS

Input for Bias amplifier	Output of BTL Driver
	
Input for OP-amp	**Input for Mute · loading driver**
	
Output for op-amp & Input for BTL driver	**Output for loading driver**
	

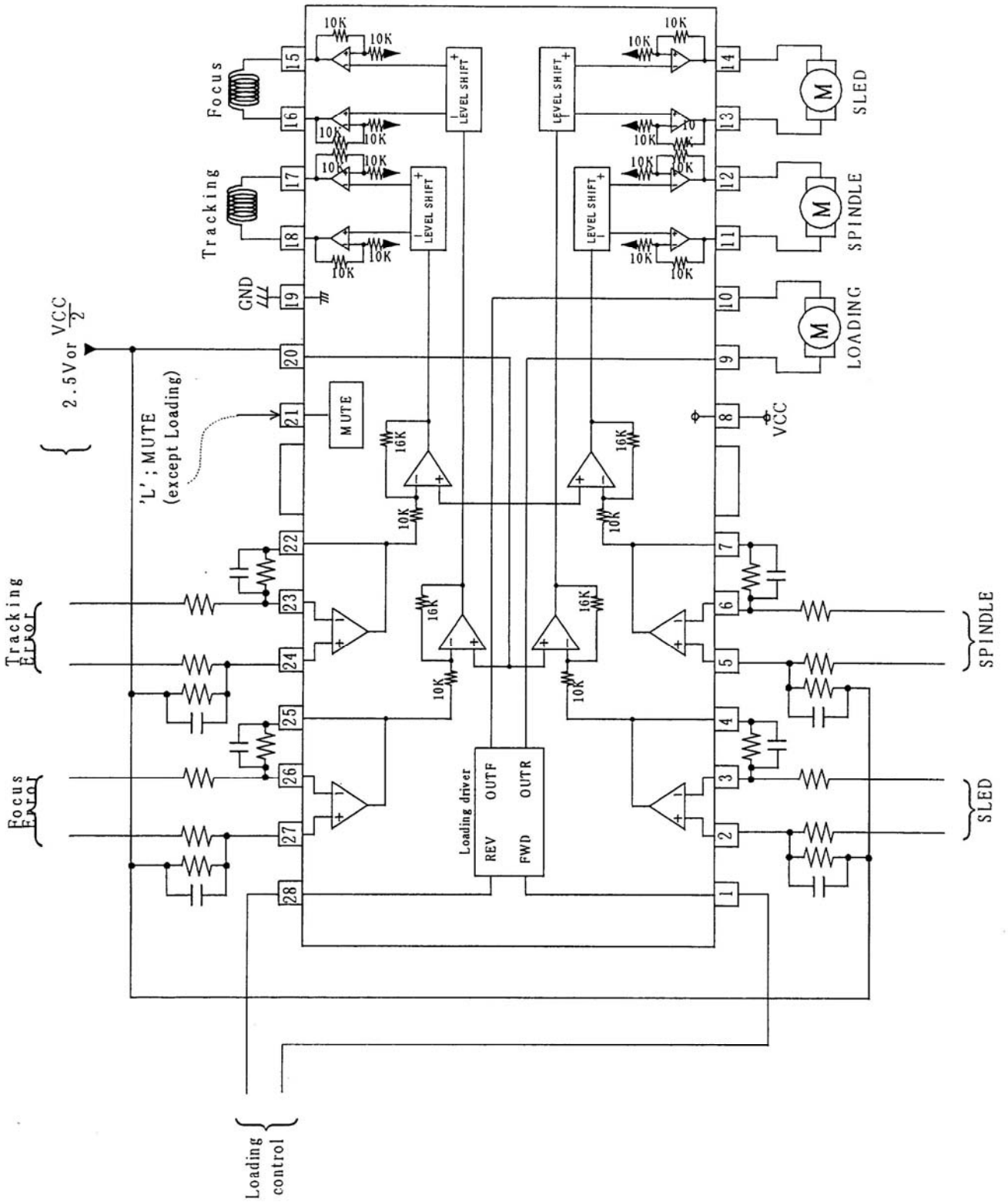


fig.4 APPLICATION

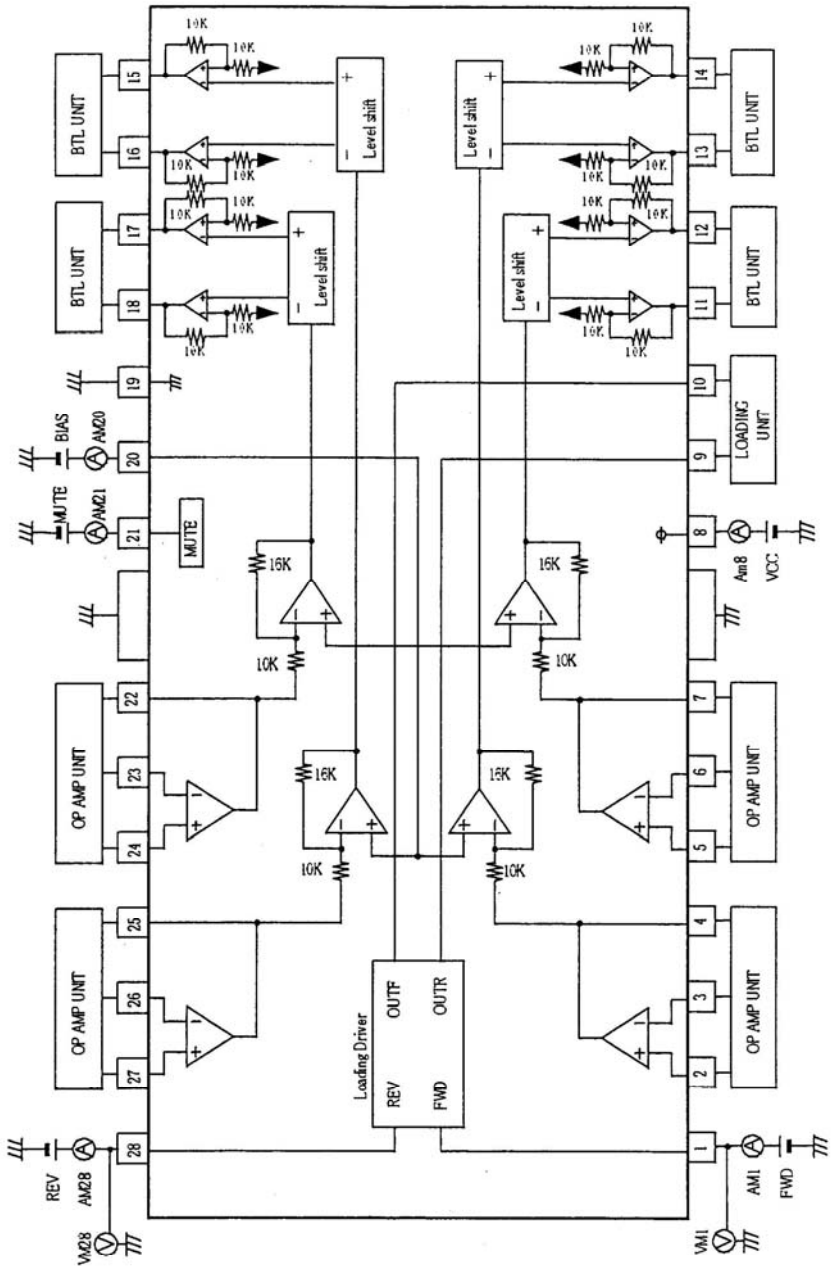


fig5-1 Test Circuit ①

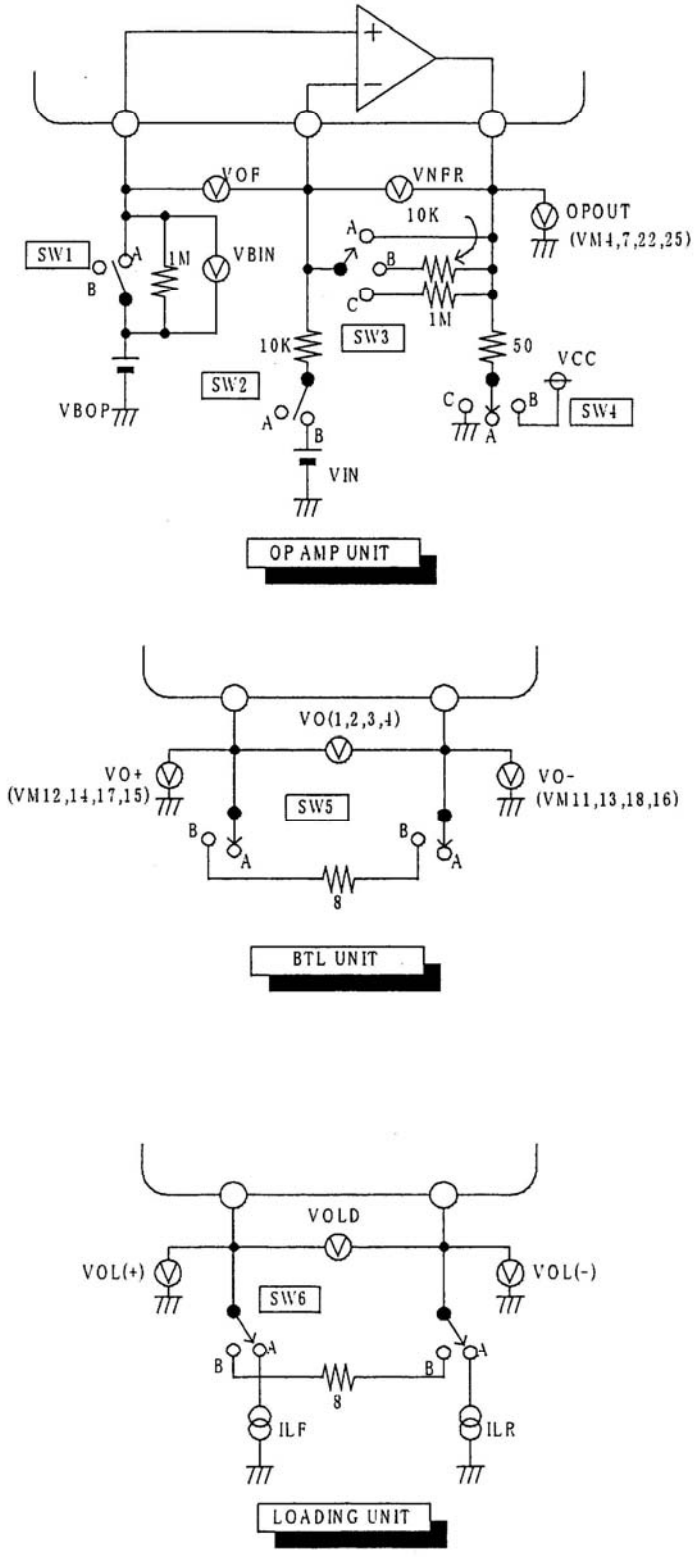


fig5-2 Test Circuit ②

◎ SWITCH TABLE

※ Unless otherwise noted, VCC=8V、BIAS=2.5V、SW ; Aposition

(MUTE3=V、VBOP=2.5

	Switch						Input voltage (V)				Conditions	Measure point
	1	2	3	4	5	6						
Quiescent current												AM8

OBTL DRIVER

	Switch						Input voltage (V)				Conditions	Measure point
	1	2	3	4	5	6	MUTE	BIAS	VBOP	VIN		
Output offset voltage					B		3	2.5	2.5	–		VO
Max. output voltage		B	C		↓		↓	↓	↓	0		VO
		↓	↓		↓		↓	↓	↓	8		VO
Closed loop voltage gain					↓		↓	↓	3	–		VO
					↓		↓	↓	2	–		VO
Mute on voltage							0.5	↓	3	–	input parameter	VO
Mute off voltage							1.5	↓	3	–	input parameter	VO
Input current for Mute pin							5	↓	2.5	–		AM21
Input current for Bias pin							↓	↓	↓	–		AM20

OOP-AMP (MUTE=3V)

	Switch						Input voltage(V), current(mA)				Conditions	Measure point
	1	2	3	4	5	6			VBOP	VIN		
Common mode input voltage rang H									7	–		VOF
Common mode input voltage rang L									0.45	–		VOF
Input offset voltage									2.5	–		VOF
Input bias current	B		C						2.5	–		VBIN,VNFR
High level output voltage		B	C						↓	0		OPOUT
Low level output voltage		B	C						↓	8		OPOUT
Output sink current				B					↓	–		(VCC-OPOUT)/50
Output source current				C					↓	–		OPOUT/50
slew rate									※	–	※Input pulse 100kHz、$2V_{P-P}$	OPOUT

O loading driver (MUTE=3V、BIAS=2.5V、VBOP=2.5V)

	Switch						Input voltage(V), current(mA)				Conditions	Measure point
	1	2	3	4	5	6	FWD	REV	ILF	ILR		
Output saturation voltage 1 +					B		1.4	0.6	-200	200		VCC-VOLD
Output saturation voltage 1 –					↓		0.6	1.4	200	-200		VCC-VOLD
Output saturation voltage 1 F/R					↓						The Vsat1 difference between FWD & REV	
Output saturation voltage 2					↓		1.4	0.6	-500	500		VCC-VOLD
					↓		0.6	1.4	500	-500		VCC-VOLD

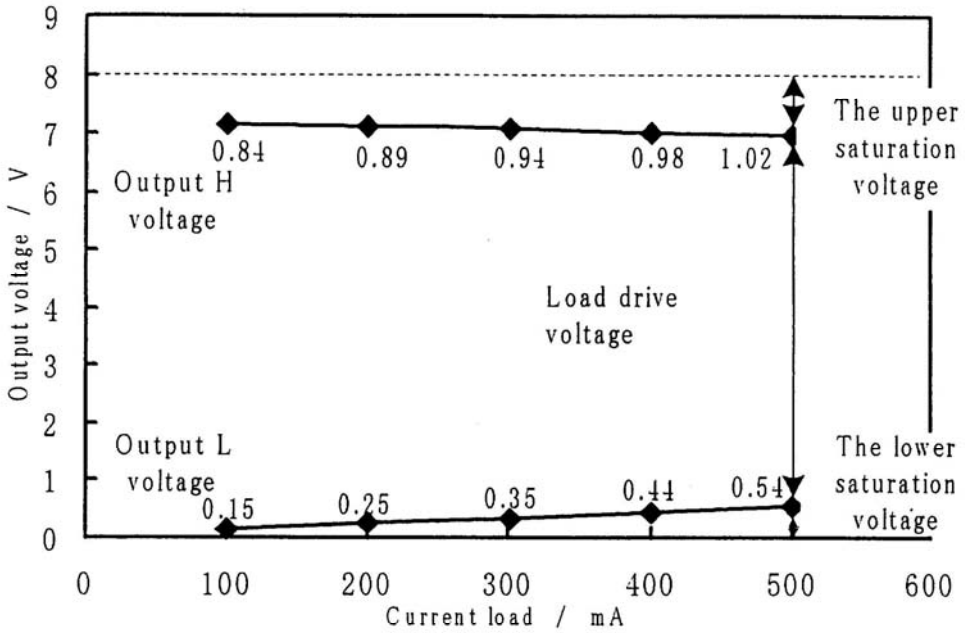
O Loading logic input (MUTE=3V、VBOP=2.5V)

	Switch						Input voltage(V), current(mA)				Conditions	Measure point
	1	2	3	4	5	6	FWD	REV				
Input high level voltage(1pin)							1.5	-			input parameter	
Input high level voltage(28pin)							-	1.5			input parameter	
Input low level voltage(1pin)							0.5	-			input parameter	
Input low level voltage(28pin)							-	0.5			input parameter	
Input high level current							5	-				AM1
							-	5				AM28

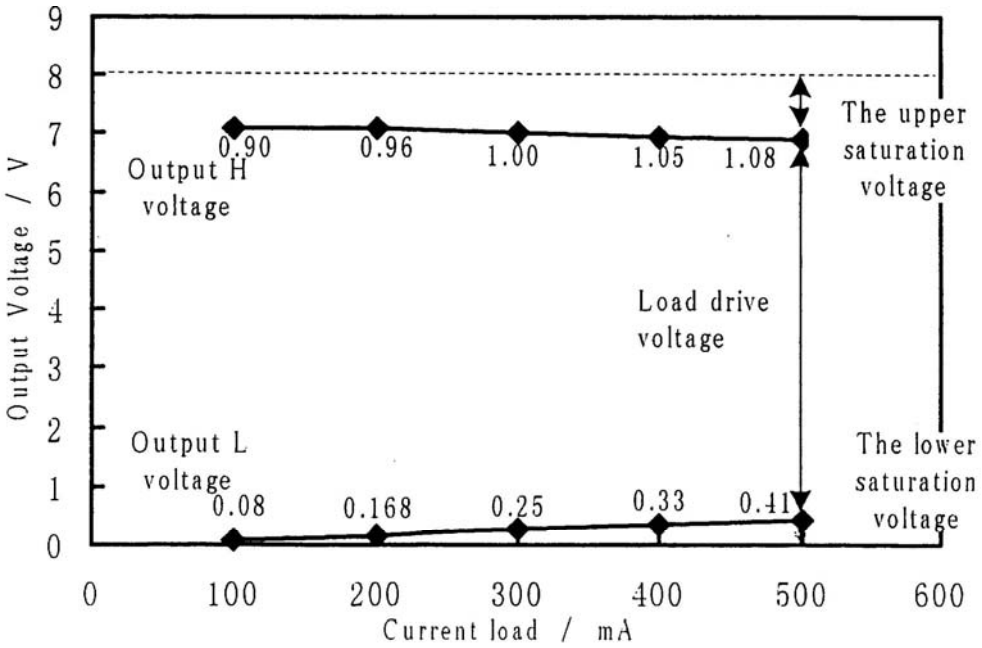
●reference

☆Characteristic of Output saturation voltage－Current load (VCC=8V)

a) BTL DRIVER



b) LOADING DRIVER



○NOTES

1. Thermal-shut-down circuit built in.
When IC chip temperature rise to 175℃(typ.), output current is muted, and when IC chip temperature reaches 150℃(typ.), the driver circuit starts up.

2. When mute-terminal(pin.21) voltage is open or lowered below 0.5V, output current is muted.
Under normal use condition, pull up the mute terminal above 1.5V.

3. When supply voltage falls below 3.8V(typ.), output current is muted. Next time supply voltage rises to 4.0V(typ.), the driver circuit start.

4. When bias-terminal(pin.20) voltage is below 0.7V(typ.), driver is muted. Under normal use condition, set above 1.1V .

5. All drivers are muted by thermal-shutdown . When bias terminal voltage falls and mute is ON, BTL driver except loading driver is muted .
Previous stage operational amplifier is in no case muted.
Output terminal of muted BTL driver applies internal bias voltage (VCC-0.7)/2 (V).

6. loading driver logic input

FWD (1pin)	REV (28pin)	VOL(+) (10pin)	VOL(-) (9pin)	FUNCTION
L	L	OPEN	OPEN	OPEN MODE
L	H	L	H	REVERSE MODE
H	L	H	L	FORWARD MODE
H	H	L	L	BRAKE MODE

Input circuit of pin1 and pin28 is designed to avoid simultaneous activation of upper and lower output Tr. ; however, in order to improve reliability, apply motor forward/backward input once through open mode.
We recommend time period for open mode longer than 10msec.
When motor is locked, do not allow current to exceed 700mA at its peak.

7. Insert the by-pass capacitor between Vcc-terminal and GND-terminal of IC as near as possible (approximately 0.1μF).

8. Heat dissipation fins are attached to the GND on the inside of the package.
Make sure to be connected to the external GND.

9. In principle, do not apply voltage below sub-potential of IC to terminal.
Examine in consideration of operation margin, when each driver output falls below sub-voltage of IC(GND) due to counter-electromotive-force of load .

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