Wide Input Range Synchronous Regulator Controller with Accurate Current Limit

FEATURES

- **Wide Input Range: 2.5V to 60V**
- **Integrated Buck-Boost Supply for 7.5V MOSFET Gate Drive**
- **Programmable Constant-Current Operation with Current Monitor Output**
- **Low I_Q: 75µA, $12V_{IN}$ to $3.3V_{OUT}$**
- **Selectable Low Output Ripple Burst Mode® Operation**
- V_{OUT} Up to 60V
- Adjustable and Synchronizable: 50kHz to 1MHz
- Internal OVLO Protects for Input Transients Up to 80V
- Accurate Input Overvoltage and Undervoltage Threshold
- Programmable Soft-Start with Voltage Tracking
- Power Good and Output OVP
- 28-Lead TSSOP and 38-Lead 4mm × 6mm QFN Packages

APPLICATIONS

- Automotive Supplies
- Industrial Systems
- Distributed DC Power Systems

DESCRIPTION

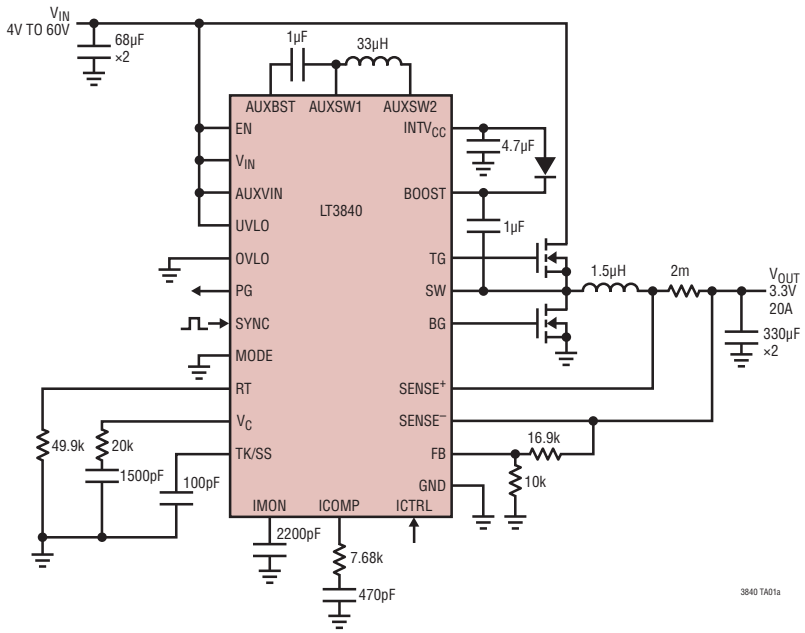
The LT®3840 is a high voltage synchronous step-down switching regulator controller capable of operating from a 2.5V to 60V supply.

The LT3840's low quiescent current, when configured for user selectable Burst Mode operation, helps extend run time in battery-powered systems by increasing efficiency at light loads. The LT3840 uses a constant frequency, current mode architecture. High current applications are possible with large N-channel gate drivers capable of driving multiple low $R_{DS(ON)}$ MOSFETs.

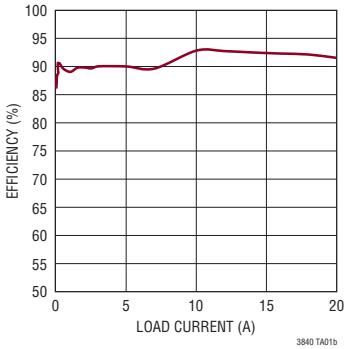
An integrated buck-boost switching regulator generates a 7.5V bias supply voltage for MOSFET gate drive and IC power allowing higher efficiency operation over the entire input voltage range and eliminating the need for an external bias voltage. An accurate current limit set point regulates the maximum output current. A current monitor reports the average output current.

TYPICAL APPLICATION

High Efficiency Synchronous Step-Down Converter



$12V_{IN}$ to $3.3V_{OUT}$ Efficiency



Rev B

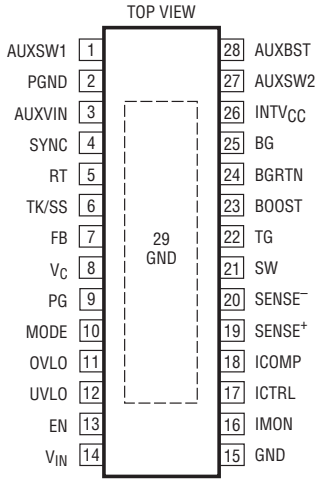
ABSOLUTE MAXIMUM RATINGS

(Note 1)

AUXVIN, V_{IN}, EN and UVLO ..... –0.3V to 80V
PG ..... –0.3V to 25V
MODE ..... –0.3V to 9V
$SENSE^+$ and $SENSE^-$ ..... –0.3V to 60V
$SENSE^+$ to $SENSE^-$ ..... –1V to 1V
OVLO, V_C, FB, SYNC, TK/SS and ICTRL ..... –0.3V to 6V

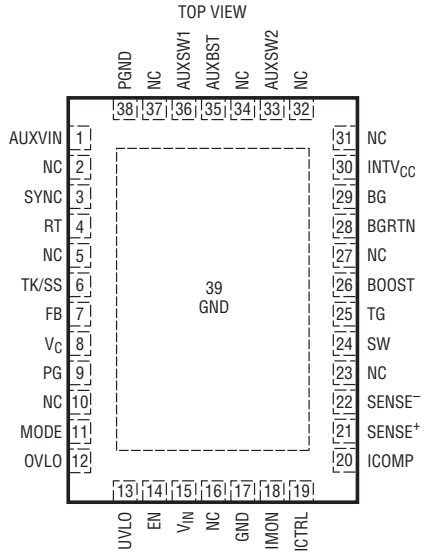
Junction Temperature Range
LT3840E (Note 2) ..... –40°C to 125°C
LT3840I ..... –40°C to 125°C
LT3840H ..... –40°C to 150°C
LT3840MP ..... –55°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP Only ..... 300°C
Storage Temperature ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP

θ_{JA} = 30°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFE PACKAGE
38-LEAD (4mm × 6mm) PLASTIC QFN

θ_{JA} = 38°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3840EFE#PBF	LT3840EFE#TRPBF	LT3840FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3840IFE#PBF	LT3840IFE#TRPBF	LT3840FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3840HFE#PBF	LT3840HFE#TRPBF	LT3840FE	28-Lead Plastic TSSOP	–40°C to 150°C
LT3840MPFE#PBF	LT3840MPFE#TRPBF	LT3840FE	28-Lead Plastic TSSOP	–55°C to 150°C
LT3840EUFE#PBF	LT3840EUFE#TRPBF	3840	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 125°C
LT3840IUFE#PBF	LT3840IUFE#TRPBF	3840	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.analog.com/leadfree/
For more information on tape and reel specifications, go to: http://www.analog.com/tapeandreel/

Rev B

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
V_{IN} Minimum Operating Voltage		●			2.5	V
V_{IN} Supply Current				20		µA
V_{IN} Burst Mode Current	V_{MODE} = 0V			20	30	µA
V_{IN} Shutdown Current	V_{EN} = 0.3V	●		0.1	1	µA
$AUXV_{IN}$ Minimum Operating Voltage		●			2.5	V
$AUXV_{IN}$ Overvoltage Lockout		●	60			V
$AUXV_{IN}$ Supply Current	(Note 3)			300		µA
$AUXV_{IN}$ Burst Mode Current	V_{MODE} = 0V			0.1		µA
$AUXV_{IN}$ Shutdown Current	V_{EN} = 0.3V			0.1	1	µA
EN Enable Threshold (Rising)		●	1.20	1.25	1.30	V
EN Hysteresis				30		mV
EN Pin Bias Current	V_{EN} = 1.25V			2		nA
UVLO Enable Threshold (Rising)		●	1.20	1.25	1.30	V
UVLO Hysteresis				45		mV
UVLO Pin Bias Current	V_{UVLO} = 1.25V			1		nA
OVLO Threshold (Rising)		●	1.20	1.25	1.30	V
OVLO Hysteresis				125		mV
OVLO Pin Bias Current	V_{OVLO} = 1.25V			1		nA
Voltage Regulation						
Regulated FB Voltage	E- and I-Grade	●	1.237	1.250	1.263	V
Regulated FB Voltage	MP- and H-Grade	●	1.232	1.250	1.263	V
FB Overvoltage Protection	% Above FB Voltage	●	8	12	16	%
FB Overvoltage Protection Hysteresis				2.5		%
FB Input Bias Current				5	20	nA
FB Voltage Line Regulation	2.5V ≤ V_{IN} ≤ 60V			0.002	0.02	%/V
FB Error Amp Transconductance				300		µS
FB Error Amp Sink/Source Current				±25		µA
Peak Current Limit Sense Voltage	0% Duty Cycle		80	95	110	mV
Peak Current Limit Sense Voltage	100% Duty Cycle			60		mV
TK/SS Charge Current				9		µA
Current Regulation						
Sense Common Mode Range		●	0		60	V
Average Current Limit Sense Voltage	V_{ICTRL} = Open	●	47.5	50	52.5	mV
	V_{ICTRL} = 800mV			40		mV
IMON Voltage	V_{SENSE} = 50mV	●	0.95	1.00	1.05	V
	V_{SENSE} = 20mV			0.4		V
ICTRL Current	V_{ICTRL} = 1V			7		µA
Reverse Protect Sense Voltage	V_{MODE} = 7.5V			–50		mV
Reverse Current Sense Voltage Offset	V_{MODE} = V_{FB} or V_{MODE} = 0V			5		mV
Sense Input Current	$SENSE^+$ = $SENSE^-$ = 12V			300		µA
Oscillator						
Switching Frequency	R_T = 49.9k	●	280	300	320	kHz
	R_T = 348k			50		kHz
	R_T = 13.7k			1000		kHz
SYNC Threshold				1.2		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Good						
PG Threshold as a Percentage of V_{FB}	V_{FB} Rising	●	87	90	93	%
PG Hysteresis as a Percentage of V_{FB}				2.5		%
PG Leakage	V_{PG} = 5V			0.1	1	µA
PG Sink Current	V_{PG} = 0.3V	●	35	65		µA
MOSFET Gate Drivers						
Non-Overlap Time TG to BG				75		ns
Non-Overlap Time BG to TG				75		ns
TG Minimum On Time				150		ns
TG Minimum Off Time				240		ns
TG Maximum Duty Cycle	R_T = 49.9k			99		%
TG, BG Drive On Voltage				7.5		V
TG, BG Drive Off Voltage				5		mV
TG, BG Drive Rise Time	C_{TG} = C_{BG} = 3300pF			20		ns
TG, BG Drive Fall Time	C_{TG} = C_{BG} = 3300pF			20		ns
BOOST UVLO (Rising)	V_{BOOST} - V_{SW}		4.5	5.3		V
BOOST UVLO Hysteresis				350		mV
Internal Auxiliary Supply						
$INTV_{CC}$ Regulation Voltage		●	7.25	7.5	7.75	V
$INTV_{CC}$ UVLO Threshold (Rising)			6.25	6.5	6.75	V
$INTV_{CC}$ UVLO Hysteresis				300		mV
$INTV_{CC}$ Current in Shutdown	V_{EN} = 0.3V			6		µA
$INTV_{CC}$ Output Current	2.5V ≤ V_{IN} ≤ 60V (Note 4)	●	100			mA
$INTV_{CC}$ Burst Mode Current	V_{MODE} = 0V			60		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3840E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3840I is guaranteed over the –40°C to 125°C operating junction temperature range. The LT3840H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT3840MP is 100% tested and guaranteed over the –55°C to 150°C temperature range. High junction temperatures degrade operating lifetimes; Operating lifetime is derated for junction temperatures greater than 125°C.

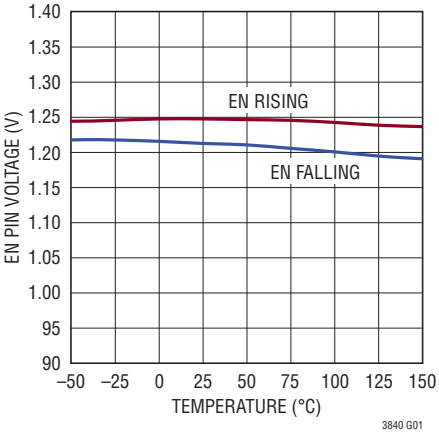
Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 4: Specification is not tested but is guaranteed by design, characterization and correlation with statistical process controls.

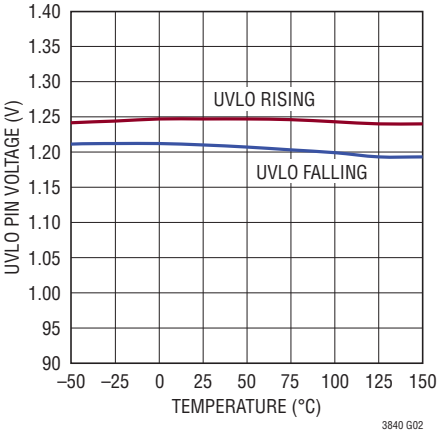
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

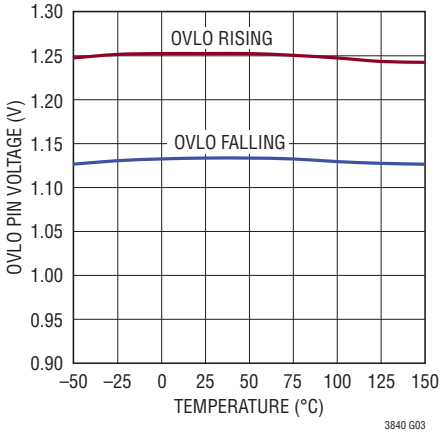
EN Threshold Voltage vs Temperature



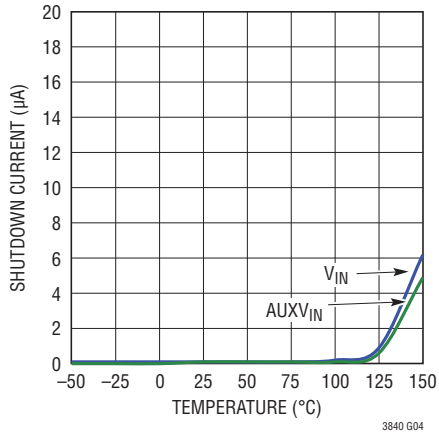
UVLO Threshold Voltage vs Temperature



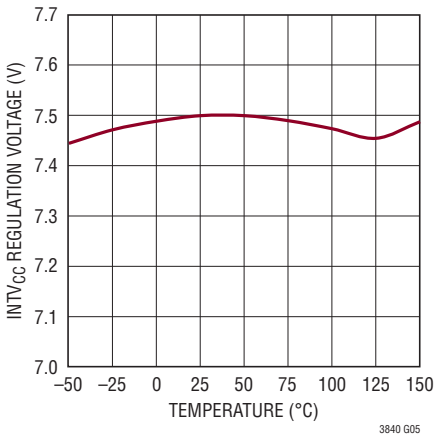
OVLO Threshold vs Temperature



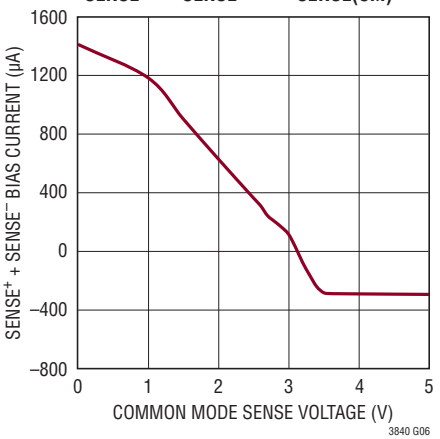
Shutdown Current vs Temperature



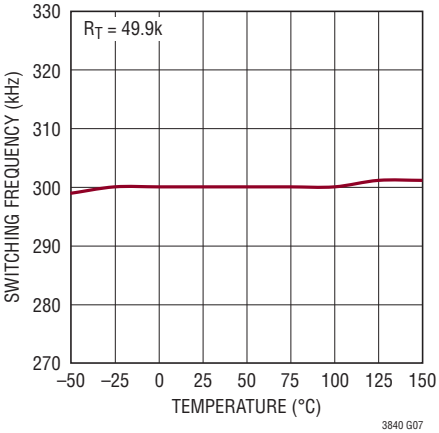
$INTV_{CC}$ Regulation Voltage vs Temperature



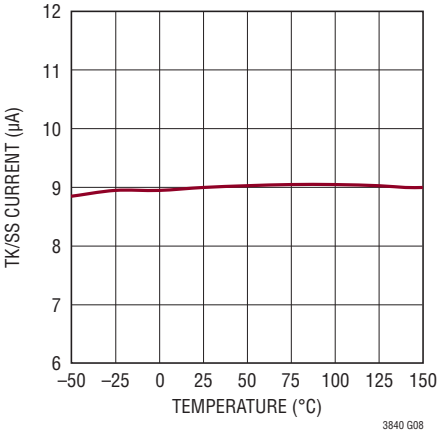
$I_{SENSE^+} + I_{SENSE^-}$ vs $V_{SENSE(CM)}$



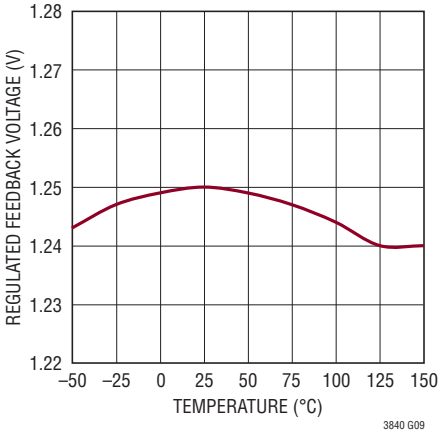
Switching Frequency vs Temperature



Soft-Start (TK/SS) Current vs Temperature



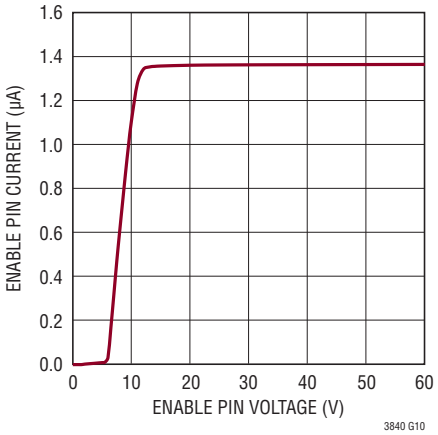
Regulated FB Voltage vs Temperature



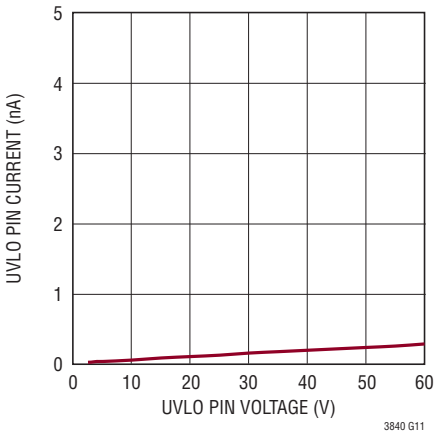
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

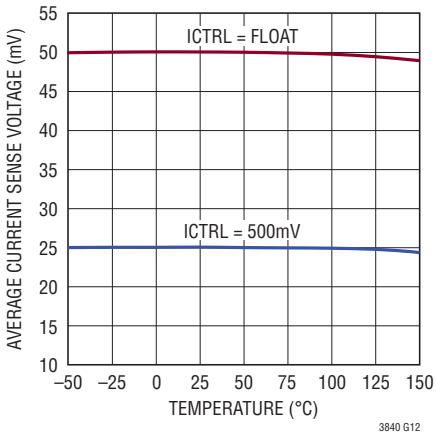
Enable Pin Current vs Enable Voltage



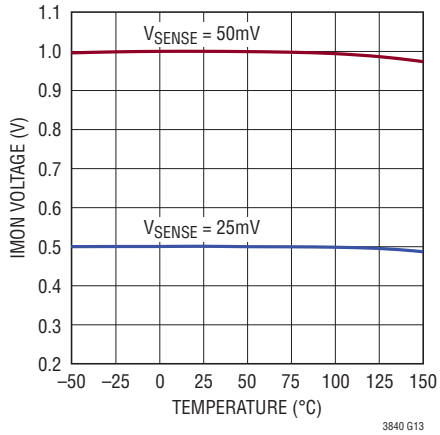
UVLO Pin Current vs UVLO Voltage



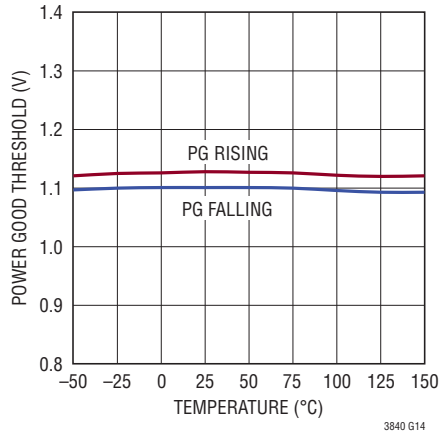
Average Current Sense Voltage vs Temperature



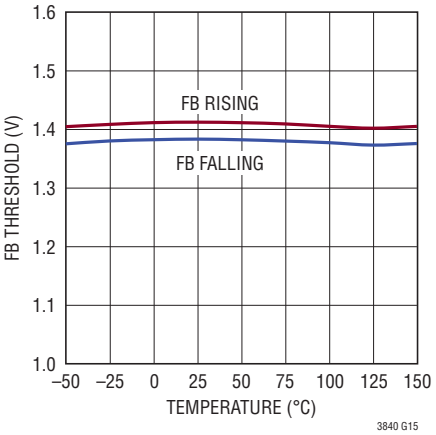
Current Monitor (IMON) Voltage vs Temperature



Power Good Threshold vs Temperature



FB Overvoltage Threshold vs Temperature



PIN FUNCTIONS (TSSOP/QFN)

AUXSW1 (Pin 1/Pin 36): AUXSW1 is a switching node of the auxiliary bias supply. Connect the pin to the auxiliary bias supply inductor.

PGND (Pin 2/Pin 38): PGND is the high current ground return for the auxiliary bias supply. Connect PGND to the negative terminal of the $INTV_{CC}$ decoupling capacitor and to system ground.

AUXVIN (Pin 3/Pin 1): AUXVIN is the supply pin to the auxiliary bias supply. Bypass the pin with a low ESR capacitor placed close to the pin and referenced to PGND.

SYNC (Pin 4/Pin 3): SYNC allows the LT3840 switching frequency to be synchronized to an external clock. Set the R_T resistor such that the internal oscillator frequency is 15% below the minimum external clock frequency. If unused connect the SYNC pin to GND.

RT (Pin 5/Pin 4): An external resistor on RT sets the switching frequency of the synchronous controller and auxiliary bias supply.

TK/SS (Pin 6/Pin 6): TK/SS is the LT3840 external tracking and soft-start input. The LT3840 regulates the V_{FB} voltage to the smaller of the internal reference or the voltage on the TK/SS pin. An internal pull-up current source is connected to this pin. A capacitor (C_{SS}) to ground sets the ramp rate. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LT3840 output to track another supply during start-up. Leave the pin open if the tracking and soft-start functions are unused.

FB (Pin 7/Pin 7): The regulator output voltage is set with a resistor divider connected to FB. FB is also the input for the output overvoltage and power good comparators.

V_C (Pin 8/Pin 8): V_C is the compensation node for the output voltage regulation control loop.

PG (Pin 9/Pin 9): PG is a power good pin and is the open-drain output of an internal comparator.

MODE (Pin 10/Pin 11): MODE is used to enable or disable Burst Mode operation. Connect MODE to ground for Burst Mode operation. Connect the pin to FB for pulse-skipping mode. Connect MODE to $INTV_{CC}$ for continuous mode.

OVLO (Pin 11/Pin 12): OVLO has a precision threshold with hysteresis to implement an accurate overvoltage lockout (OVLO). Controller switching is disabled during an overvoltage lockout (OVLO) event. $INTV_{CC}$ regulation is maintained during an OVLO event. Connect the pin to GND to disable the function.

UVLO (Pin 12/Pin 13): UVLO has a precision threshold with hysteresis to implement an accurate undervoltage lockout (UVLO). UVLO enables the controller switching. Connect the pin to V_{IN} to disable the function.

EN (Pin 13/Pin 14): EN has a precision IC enable threshold with hysteresis. EN enables the auxiliary bias supply and controller switching. Connect the pin to V_{IN} to disable the function. EN also has a lower threshold to put the LT3840 into a low current shutdown mode where all internal circuitry is disabled.

V_{IN} (Pin 14/Pin 15): V_{IN} provides an internal DC bias rail and should be decoupled to GND with a low value (0.1µF), low ESR capacitor located close to the pin.

GND (Pin 15, Exposed Pad Pin 29/Pin 17, Exposed Pad Pin 39): Ground. Solder GND and the exposed pad directly to the PCB ground plane.

IMON (Pin 16/Pin 18): The voltage on IMON represents the average output current of the converter. A small value capacitor filters the ripple voltage associated with the inductor ripple current.

ICTRL (Pin 17/Pin 19): The maximum average output current is programmed with a voltage applied to ICTRL. If unused, leave floating.

ICOMP (Pin 18/Pin 20): A capacitor and resistor connected to ICOMP compensates the average current limit circuit.

$SENSE^+$ (Pin 19/Pin 21): $SENSE^+$ is the positive input for the differential current sense comparator.

$SENSE^-$ (Pin 20/Pin 22): $SENSE^-$ is the negative input for the differential current sense comparator.

SW (Pin 21/Pin 24): SW is the high current return path of the TG MOSFET driver and is externally connected to the negative terminal of the BOOST capacitor.

PIN FUNCTIONS (TSSOP/QFN)

TG (Pin 22/Pin 25): TG is the high current gate drive for the top N-channel MOSFET.

BOOST (Pin 23/Pin 26): BOOST is the supply for the bootstrapped TG gate drive and is externally connected to a low ESR ceramic capacitor referenced to SW.

BGRTN (Pin 24/Pin 28): BGRTN is the high current return path of the BG MOSFET driver and is externally connected to the negative terminal of the $INTV_{CC}$ capacitor.

BG (Pin 25/Pin 29): BG is the high current gate drive for the bottom N-channel MOSFET.

$INTV_{CC}$ (Pin 26/Pin 30): $INTV_{CC}$ is the auxiliary bias supply output. Bypass the pin with a low ESR capacitor placed close to the pin. $INTV_{CC}$ provides supply for LT3840 internal bias and MOSFET gate drivers. The $INTV_{CC}$ pin cannot be back driven with a separate supply.

AUXSW2 (Pin 27/Pin 33): AUXSW2 is a switching node of the auxiliary supply and is connected to the auxiliary bias supply inductor.

AUXBST (Pin 28/Pin 35): AUXBST provides drive voltage for the auxiliary supply and is connected to a low ESR capacitor referenced to AUXSW1.

OPERATION

OVERVIEW

The LT3840 provides a solution for a high efficiency, general purpose DC/DC converter. It is a wide input voltage range switching regulator controller IC that uses a programmable fixed frequency, peak current mode architecture. An internal switching regulator efficiently provides an auxiliary bias supply to drive multiple, large N-channel MOSFET switches.

The LT3840 includes functions such as average output current control and monitoring, micro-power operation with low output ripple, soft-start, output voltage tracking, power good and a handful of protection features.

Voltage Control Loop

The LT3840 uses peak current mode control to regulate the supply output voltage. The error amplifier (EA) generates an error voltage (V_C) based on the difference between the feedback (FB) voltage and an internal reference. The externally compensated V_C voltage generates a threshold for the differential current sense comparator. During normal operation, the LT3840 internal oscillator runs at the programmed frequency. At the beginning of each oscillator cycle, the TG switch drive is turned on. The TG switch drive stays enabled until the sensed inductor current exceeds the V_C derived threshold of the current sense comparator.

If the current comparator threshold is not reached for the entire oscillator cycle, the switch driver stays on for up to eight cycles. If after eight cycles the TG switch driver is still on, it is turned off to regenerate the BOOST bootstrapped supply.

When the load current increases, the FB voltage decreases relative to the reference causing the EA to increase the V_C voltage until the average inductor current matches the new load current. Refer to Figure 1 for a block diagram of the LT3840 voltage control loop.

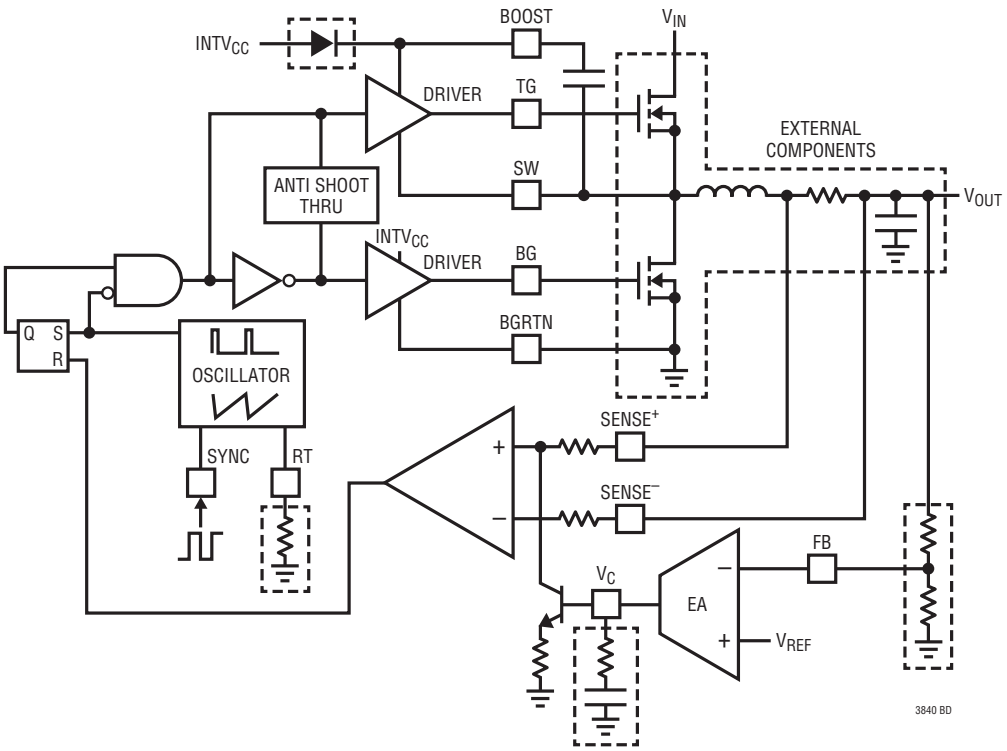


Figure 1. Peak Current Mode Voltage Control Functional Block Diagram

OPERATION

Light Load Operation (Burst Mode Operation, Pulse-Skipping Mode or Continuous Mode)

The LT3840 is capable of operating in Burst Mode, pulse-skipping mode, or continuous mode. Connect the MODE pin to GND for Burst Mode operation, to the FB pin for pulse-skipping mode, or to $INTV_{CC}$ for continuous mode.

In Burst Mode operation the LT3840 forces a minimum peak inductor current via an internal clamp on the V_C pin. If the average inductor current is greater than the load current the output voltage will begin to increase and the error amplifier, EA, will attempt to decrease the V_C voltage. When the internal voltage clamp on V_C is engaged and the FB voltage increases slightly, the LT3840 goes into sleep mode.

In sleep mode, both external MOSFETs are turned off and much of the internal circuitry is turned off, reducing the quiescent current. The load current is supplied by the output capacitor. As the output voltage decreases, the LT3840 comes out of sleep mode and the controller resumes normal operation by turning on the TG MOSFET on the next cycle of the internal oscillator. The output voltage increases and the controller goes back to sleep. This cycle repeats until the average load current is greater than the minimum forced peak inductor current.

When Burst Mode operation is selected, the inductor current is not allowed to go negative. A reverse current comparator turns off the BG MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In pulse-skipping mode, during light loads, the supply operates in discontinuous mode where the inductor current is not allowed to reverse direction. Output voltage regulation is maintained by skipping TG on pulses. At light loads pulse-skipping mode is more efficient than forced continuous mode, but not as efficient as Burst Mode operation.

In continuous operation the inductor current is allowed to reverse direction at light loads or under large transient conditions. The reverse current comparator protects the BG MOSFET by turning it off if the reverse current exceeds the maximum reverse current sense threshold voltage.

Constant Current Operation

For applications requiring a regulated current source the LT3840 has a control loop to accurately regulate the average output current. A current monitor function provides output current information for telemetry and diagnostics.

The current through the sense resistor, R_{SENSE}, produces a voltage applied to the SENSE pins. The differential sense voltage is amplified by 20x, buffered and output to the IMON pin. The capacitor on the IMON pin filters the ripple component to average the signal.

The 20x amplified differential sense voltage is also applied to an internal GM amplifier and compared against either 1V or ICTRL voltage, whichever is smaller. A voltage applied to ICTRL reduces the maximum average current sense threshold. When the 20× amplified differential sense voltage exceeds the 1V internal reference or the ICTRL voltage the ICOMP node is driven high and V_C is pulled

OPERATION

low. The V_C voltage is the DC control node that sets the peak inductor current. A resistor and capacitor on ICOMP compensate the current control loop. Figure 2 includes the block diagram of the average current control loop and transfer functions showing the relationship between V_{SENSE}, ICTRL and IMON.

Auxiliary Bias Supply

The LT3840 wide input voltage range is made possible with the auxiliary bias supply switching regulator. Other switching regulator controllers typically use a linear voltage regulator to provide the gate drive voltage from V_{IN}. This approach is limited by power dissipation at high input voltage and dropout at low voltage. The LT3840 bias regulator efficiently generates a 7.5V bias voltage, capable of adequately driving large multiple MOSFETs, at input voltages as low as 2.5V and as high as 60V.

The auxiliary bias supply is a monolithic buck-boost, peak current mode topology. The switching frequency is fixed and synchronized with the LT3840 synchronous buck controller. The switching regulator is internally compensated

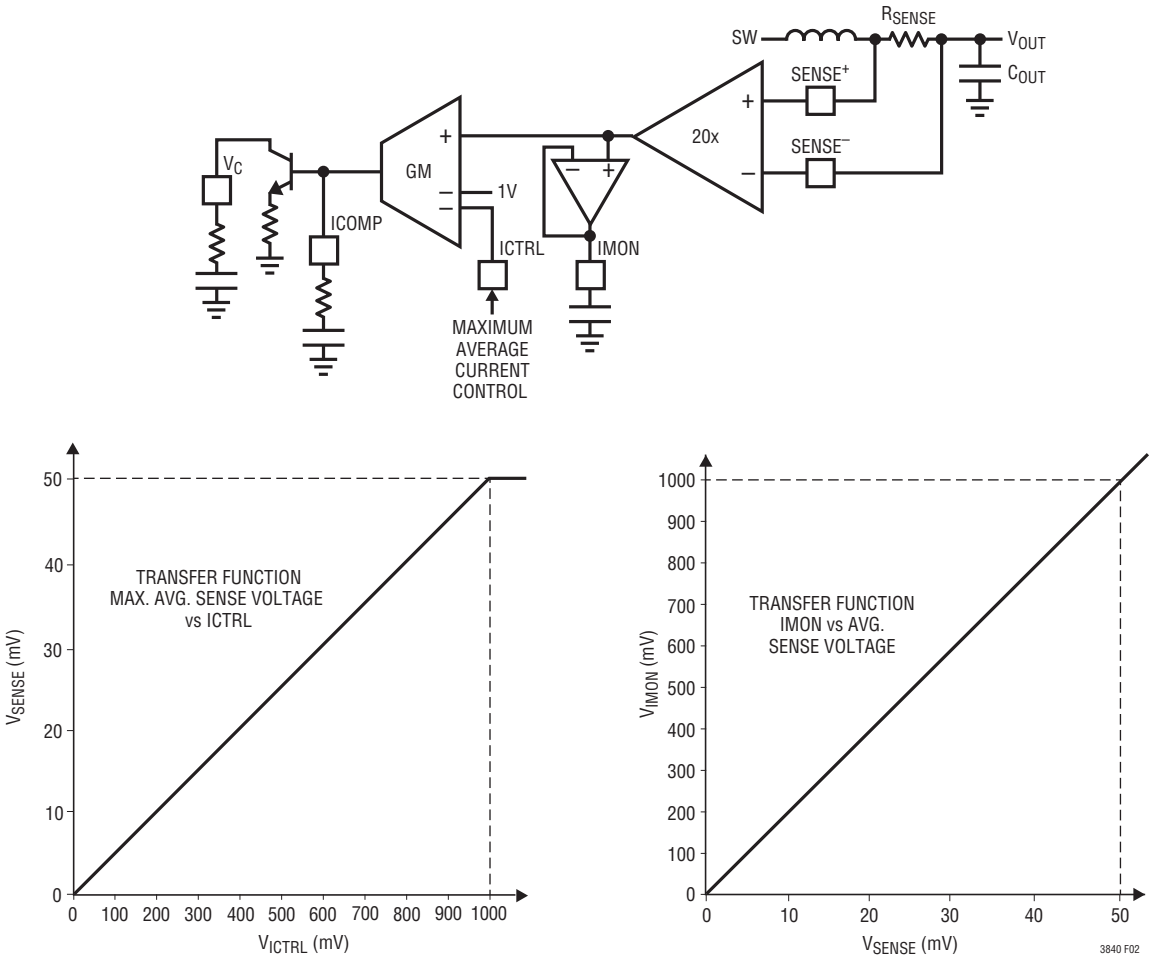


Figure 2. Average Output Current Limit Functional Block Diagram and Transfer Curves

OPERATION

and current limited. Figure 3 is a functional block diagram of the auxiliary bias supply.

Auxiliary Bias Supply Start-Up and Shutdown

The LT3840 auxiliary bias supply is enabled with the enable (EN) pin. When the EN pin voltage exceeds a diode threshold the LT3840 comes out of the low quiescent current shutdown mode and turns on the internal reference (V_{REF}) and internal bias (V_{REG}). When the EN pin voltage exceeds its precision voltage threshold the auxiliary bias switching regulator is activated and the $INTV_{CC}$ voltage is regulated. Figure 4 is a functional block diagram of the auxiliary bias supply start-up.

The auxiliary bias supply has its own enable pin to allow the $INTV_{CC}$ to be activated independent of the controller. $INTV_{CC}$ may be used to drive other circuitry in the application such as an LDO.

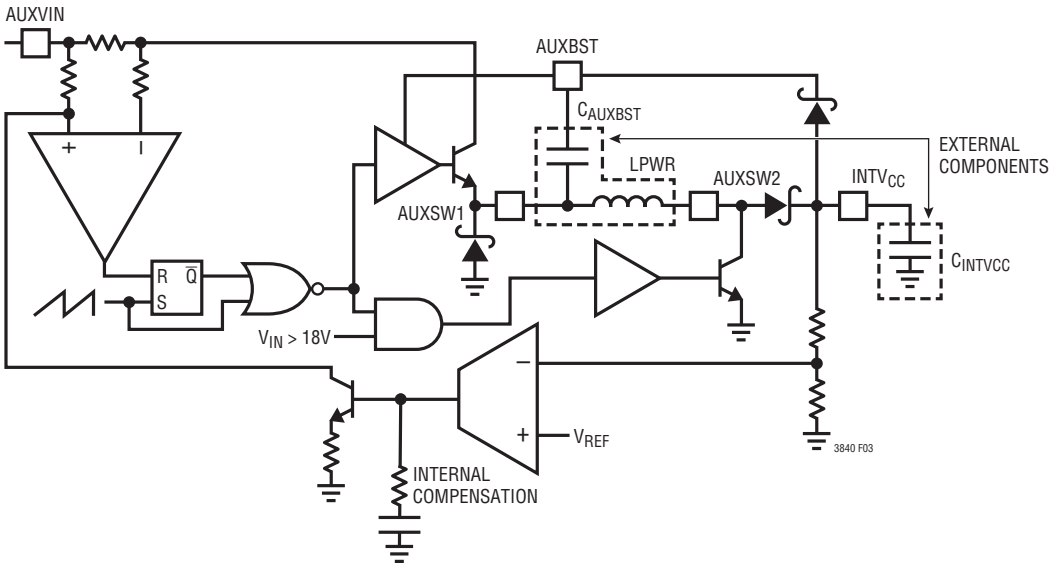


Figure 3. Auxiliary Bias Supply Functional Block Diagram

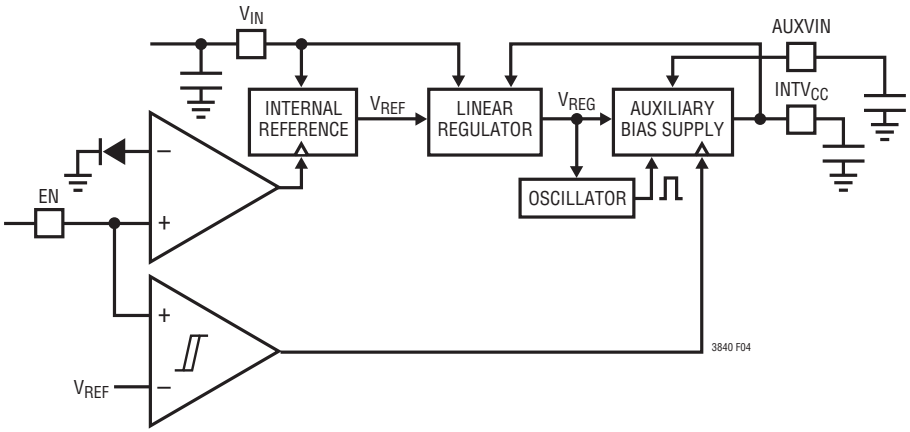


Figure 4. Auxiliary Bias Supply Start-Up Functional Block Diagram

OPERATION

Soft-Start/Output Voltage Tracking

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing.

TK/SS is an additional input to the error amplifier (EA). The voltage control loop regulates the output via the FB pin to whichever pin is lower, V_{REF} or TK/SS. An internal current source and a capacitor on the pin program the output voltage ramp time. Drive the pin with a voltage to use the output voltage tracking function for supply sequencing.

The TK/SS voltage is clamped to a diode above the FB voltage, therefore, during a short-circuit the TK/SS voltage is pulled low because the FB voltage is low. Once the short has been removed the FB voltage starts to recover. The soft-start circuit takes control of the output voltage slew rate once the FB voltage has exceeded the slowly ramping TK/SS voltage, reducing the output voltage overshoot through a short-circuit recovery. During a fault condition such as UVLO, OVLO or overtemperature, the soft-start capacitor is discharged. If unused, the pin can be left open and the internal current source will pull the pin voltage above the soft-start operating range. Figure 5 is a functional block diagram of the LT3840 soft-start/tracking function.

Power Good and Output Overvoltage Protection

When FB is within range of its regulated value an internal N-channel MOSFET, on the PG pin, is turned off allowing an external resistor to pull PG high. Power Good is valid when the LT3840 is enabled with the EN pin and the V_{IN} voltage is above 2.5V.

The LT3840 output overvoltage protection feature disables the synchronous buck controller switching when the FB pin exceeds its regulated value by a given amount (see Electrical Specification table). When this event occurs the PG pin voltage is pulled low.

Input Overvoltage Lockout

The LT3840 is capable of withstanding input voltage transients up to 80V. When the voltage on the AUXVIN pin exceeds 60V the auxiliary bias switching regulator is disabled.

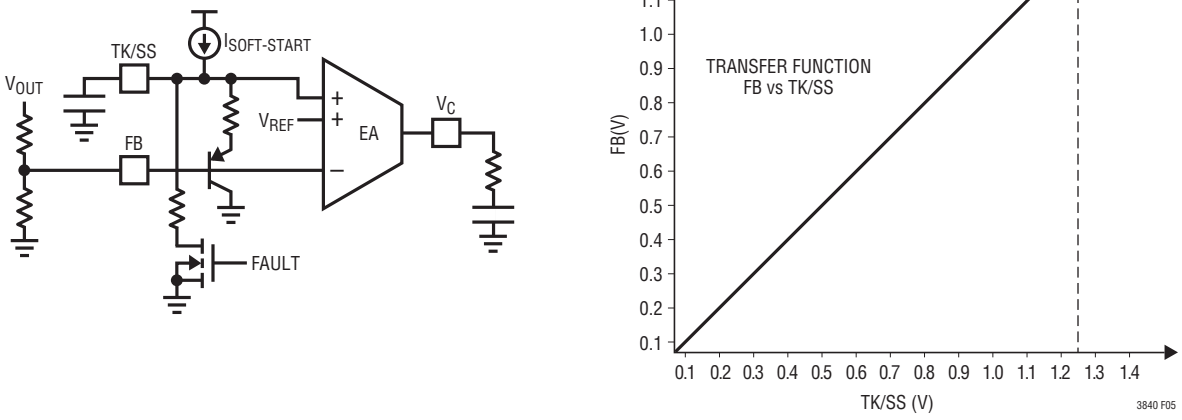


Figure 5. Soft-Start and Output Voltage Tracking Functional Block Diagram and Transfer Curve

APPLICATIONS INFORMATION

Switching Frequency

The choice of switching frequency is a trade-off between converter efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires more inductance for a given amount of ripple current, resulting in larger inductor size. Increasing the ripple current requires additional output capacitance to maintain the same output ripple voltage.

For converters with extremely high or low step-down V_{IN} to V_{OUT} ratios, another consideration is the minimum on and off times of the LT3840. A final consideration for operating frequency is in noise-sensitive systems where it is often desirable to keep the switching noise out of a sensitive frequency band.

The LT3840 uses a constant frequency architecture programmable with a single resistor (R_T) over a 50kHz to 1MHz range. The value of R_T for a given operating frequency can be chosen from Table 1 or from the following equation:

$$R_T(k\Omega) = 2.32 \bullet 10^4 \bullet f_{SW}^{(-1.08)}$$

Table 1. Recommended 1% Standard Values

R_T (kΩ)	f_{SW} (kHz)
348	50
158	100
76.8	200
49.9	300
36.5	400
28.0	500
23.2	600
19.1	700
16.5	800
14.3	900
13.7	1000

Inductor Selection

The critical parameters for the selection of an inductor are minimum inductance value, saturation current and RMS current. For a given ΔI_L, the inductance value is calculated as follows:

$$L \geq V_{OUT} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet V_{IN(MAX)} \bullet \Delta I_L}$$

The typical range of values for ΔI_L is $(0.2 \bullet I_{OUT(MAX)})$ to $(0.5 \bullet I_{OUT(MAX)})$, where $I_{OUT(MAX)}$ is the maximum load current of the supply. Using $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ yields a good design compromise between inductor performance versus inductor size and cost. A value of $\Delta I_L = 0.3 \bullet I_{OUT(MAX)}$ produces a ±15% of $I_{OUT(MAX)}$ ripple current around the DC output current of the supply. Lower values of ΔI_L require larger and more costly magnetics. Higher values of ΔI_L will increase the peak currents, requiring more filtering on the input and output of the supply. If ΔI_L is too high, the slope compensation circuit is ineffective and current mode instability may occur at duty cycles greater than 50%. To satisfy slope compensation requirements the minimum inductance is calculated as follows:

$$L_{MIN} > V_{OUT} \bullet \frac{2DC_{MAX} - 1}{DC_{MAX}} \bullet \frac{R_{SENSE} \bullet 30}{f_{SW}}$$

Magnetics vendors specify the saturation current, the RMS current or both. When selecting an inductor based on inductor saturation current, use the peak current through the inductor, $I_{OUT(MAX)} + \Delta I_L/2$. The inductor saturation current specification is the current at which the inductance, measured at zero current, decreases by a specified amount, typically 30%. When selecting an inductor based on RMS current rating, use the average current through the inductor, $I_{OUT(MAX)}$. The RMS current specification is the RMS current at which the part has a specific temperature rise, typically 40°C, above 25°C ambient. After calculating the minimum inductance value, the saturation current and the RMS current for your design, select an off-the-shelf inductor.

Contact the Applications Group at Analog Devices for further support. For more detailed information on selecting an inductor, please see the Inductor Selection section of Analog Devices Application Note 44.

APPLICATIONS INFORMATION

MOSFET Selection

Two external N-channel MOSFETs are used with the LT3840 controller, one top (main) switch, and one bottom (synchronous) switch. The gate drive levels are set by the $INTV_{CC}$ voltage. Therefore, standard or logic level threshold MOSFETs can be used.

Selection criteria for the power MOSFETs include breakdown voltage (BV_{DSS}), maximum current (I_{OUTMAX}), on-resistance (RDS_{ON}) and gate charge.

First select a MOSFET with a BV_{DSS} greater than V_{IN}. Next consider the package and current rating of the device. The maximum current rating of the device typically corresponds to a particular package. The RMS current of each device is calculated below:

$$\text{Top Switch Duty Cycle } (DC_{TOP}) = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Top Switch RMS Current} = DC_{TOP} \bullet I_{OUTMAX}$$

$$\text{Bottom Switch Duty Cycle } (DC_{BOT}) = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

$$\text{Bottom Switch RMS Current} = DC_{BOT} \bullet I_{OUTMAX}$$

Select a device that has a continuous current rating greater than the calculated RMS current.

Lastly, consider the RDS_{ON} and gate charge of the MOSFET. These two parameters are considered together because they are typically inversely proportional to one another. The RDS_{ON} determines the conduction losses of the MOSFET and the gate charge determines the switching losses.

The switching and conduction losses of each MOSFET can be calculated as follows:

$$P_{COND(TOP)} = I_{OUT(MAX)}^2 \bullet \frac{V_{OUT}}{V_{IN}} \bullet R_{DS(ON)}$$

$$P_{COND(BOT)} = I_{OUT(MAX)}^2 \bullet \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet R_{DS(ON)}$$

Note that RDS_{ON} has a large positive temperature dependence. The MOSFET manufacturer's data sheet contains a curve, RDS_{ON} vs Temperature. In the main MOSFET, transition losses are proportional to V_{IN}^2 and can be considerably large in high voltage applications (V_{IN} > 20V). Calculate the maximum transition losses:

$$P_{TRAN(TOP)} = V_{IN} \bullet I_{OUT} \bullet f_{SW} \bullet \frac{Q_{GSW}}{I_{DRIVE}}$$

where Q_{GSW} can be found in the MOSFET specification or calculated by:

$$Q_{GSW} = Q_{GD} + \frac{Q_{GS}}{2}$$

and I_{DRIVE} = 1A

The total maximum power dissipations of the MOSFET are:

$$P_{TOP(TOTAL)} = P_{COND(TOP)} + P_{TRAN(TOP)}$$

$$P_{BOT(TOTAL)} = P_{COND(BOT)}$$

Complete a thermal analysis to ensure that the MOSFET's junction temperatures are not exceeded.

$$T_J = T_A + P_{(TOTAL)} \bullet \theta_{JA}$$

where θ_{JA} is the package thermal resistance and T_A is the ambient temperature. Keep the calculated T_J below the maximum specified junction temperature, typically 150°C. Note that when V_{IN} is high and f_{SW} is high, the transition losses may dominate. A MOSFET with higher RDS_{ON} and lower gate charge may provide higher efficiency. MOSFETs with a higher voltage BV_{DSS} specification usually have higher RDS_{ON} and lower gate charge.

A Schottky diode can be inserted in parallel with the synchronous MOSFET to conduct during the dead time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period.

Input Capacitor Selection

A local input bypass capacitor is required for buck converters because the input current is pulsed with fast rise and fall times. The input capacitor selection criteria are based on

APPLICATIONS INFORMATION

the bulk capacitance and RMS current capability. The bulk capacitance will determine the supply input ripple voltage. The RMS current capability is used to prevent overheating the capacitor. The bulk capacitance is calculated based on maximum input ripple, ΔV_{IN}:

$$C_{IN(BULK)} = \frac{I_{OUT(MAX)} \bullet V_{OUT}}{\Delta V_{IN} \bullet f_{SW} \bullet V_{IN(MIN)}}$$

ΔV_{IN} is typically chosen at a level acceptable to the user. A good starting point is 100mV to 200mV. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor's RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})^2}}$$

If applicable, calculate it at the worst-case condition, V_{IN} = $2V_{OUT}$. The RMS current rating of the capacitor is specified by the manufacturer and should exceed the calculated $I_{CIN(RMS)}$. Due to their low ESR (equivalent series resistance), ceramic capacitors are a good choice for high voltage, high RMS current handling. Note that the ripple current ratings from aluminum electrolytic capacitor manufacturers are based on 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

The combination of aluminum electrolytic capacitors and ceramic capacitors is an economical approach to meeting the input capacitor requirements. The capacitor voltage rating must be rated greater than maximum V_{IN} voltage. Multiple capacitors may also be paralleled to meet size or height requirements in the design. Locate the capacitor very close to the MOSFET switch and use short, wide PCB traces to minimize parasitic inductance. Use a small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and GND, placed close to the LT3840.

Output Capacitor Selection

The output capacitance, C_{OUT}, selection is based on the design's output voltage ripple, ΔV_{OUT} and transient load requirements. ΔV_{OUT} is a function of ΔI_L and the C_{OUT} ESR. It is calculated by:

$$\Delta V_{OUT} = \Delta I_L \bullet \left(ESR + \frac{1}{(8 \bullet f_{SW} \bullet C_{OUT})} \right)$$

The maximum ESR required to meet a ΔV_{OUT} design requirement can be calculated by:

$$ESR(MAX) = \frac{(\Delta V_{OUT})(L)(f_{SW})}{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}$$

Worst-case ΔV_{OUT} occurs at the highest input voltage. Use paralleled multiple capacitors to meet the ESR requirements. Increasing the inductance is an option to lower the ESR requirements. For extremely low ΔV_{OUT}, an additional LC filter stage can be added to the output of the supply. Analog Devices Application Note 44 has some good tips on sizing an additional output filter.

Output Voltage Programming

A resistive divider sets the DC output voltage according to the following formula:

$$R2 = R1\left(\frac{V_{OUT}}{1.250V} - 1\right)$$

The external resistor divider is connected to the output of the converter as shown in Figure 6.

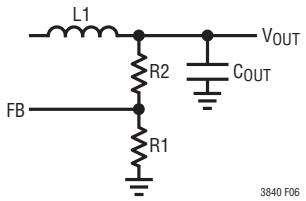


Figure 6. Output Voltage Feedback Divider

Tolerance of the feedback resistors will add additional error to the output voltage. The V_{FB} pin input bias current is typically 5nA, so use of extremely high value feedback resistors results in a converter output that is slightly

APPLICATIONS INFORMATION

higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 5nA \bullet R2$$

Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW node.

Output Current Programming and Monitoring

The average current control loop of the LT3840 accurately regulates the maximum output current of the switching regulator. The default maximum differential sense voltage, $V_{SENSE(MAX)}$, is 50mV, but a voltage applied to the ICTRL pin will program it lower. A 0V to 1V range on the ICTRL pin corresponds to 0mV to 50mV differential sense voltage. A way to provide the ICTRL programming voltage is to connect a linear regulator or voltage divider to the $INTV_{CC}$ pin.

Once the maximum differential sense voltage is determined the R_{SENSE} current sense resistor is calculated as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

Select a current sense resistor where the maximum power dissipation rating is greater than the calculated power dissipation:

$$P_{D(RSENSE)} = R_{SENSE} \bullet I_{OUT(MAX)}^2$$

The average current control loop is compensated at the ICOMP pin with a resistor and capacitor connected to GND.

The IMON pin is an accurate output current monitor pin. The LT3840 outputs a voltage that is 20 times the differential sense voltage. A 0mV to 50mV differential sense voltage corresponds to a 0V to 1V IMON voltage. A capacitor on the pin filters the voltage ripple due to the inductor ripple current. Typical capacitor values on the pin range from 1000pF to 0.1µF. The larger the capacitor value, the lower the ripple. The capacitor does not affect the average current control loop.

Output Short-Circuit Current Foldback

The LT3840 defaults to a straight line current limit where the short-circuit current is the same as the drop out current. For applications that require current foldback in a short-circuit load condition, a diode and resistor connected from V_{OUT} to the ICTRL pin is recommended (see Figure 7).

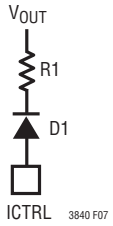


Figure 7. Output Short-Circuit Foldback Current Circuit

The foldback current in short-circuit, $I_{OUT(SC)}$, is calculated as follows:

$$I_{OUT(SC)} = \frac{(V_{F(D1)} + 7\mu A \bullet R1)}{20 \bullet R_{SENSE}}$$

where V_F is the forward voltage on the diode D1 at ~7uA current.

Internal Power Supply

The internal auxiliary supply requires three external components (C_{INTVCC}, C_{AUXBST} and L_{PWR}) for operation, as shown in Figure 3. C_{INTVCC}, a 4.7µF/10V ceramic capacitor, bypasses $INTV_{CC}$. C_{AUXBST}, a 1µF/10V ceramic capacitor, connected between the AUXBST pin and the AUXSW1 pin, provides bootstrapped drive to the internal switch.

A 33µH inductor with a saturation current greater than 0.6A is recommended for most applications. The Coilcraft ME3220-333 is a good fit.

C_{BOOST} Capacitor Selection

The recommended value of the BOOST capacitor, C_{BOOST}, is at least 100 times greater than the total gate capacitance of the topside MOSFET. Typical values for most applications range from 0.1µF to 1µF.

Soft-Start and Voltage Tracking

The desired soft-start time (t_{SS}) is programmed via the C_{SS} capacitor as follows:

$$C_{SS} = \frac{t_{SS} \bullet 9\mu A}{1.75}$$

APPLICATIONS INFORMATION

The soft-start capacitor is reset under fault conditions including UVLO, EN, OVLO, overtemperature shutdown and $INTV_{CC}$ UVLO. The soft-start pin is clamped through a diode to the V_{FB} pin. Therefore, the soft-start pin is reset during a short-circuit minimizing overshoot upon recovery.

EN, UVLO and OVLO

EN has a precision voltage threshold with hysteresis to enable the LT3840 auxiliary bias supply and synchronous controller. The pin is typically connected to V_{IN} through a resistor divider, however, it can be directly connected to V_{IN}. A lower voltage threshold on the EN pin is used to put the LT3840 into a low quiescent current shutdown mode.

UVLO has a precision voltage threshold with hysteresis to enable the LT3840 synchronous controller. The pin is typically connected to V_{IN} through a resistor divider, however, it can be directly connected to V_{IN}.

OVLO has a precision voltage threshold with hysteresis to disable the LT3840 synchronous controller. The pin is typically connected to V_{IN} through a resistor divider. OVLO can be directly connected to GND to disable the function.

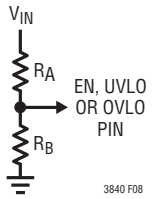


Figure 8. Precision EN, UVLO and OVLO Resistor Divider

Resistors are chosen by first selecting R_B. Then calculate R_A with the following formula:

$$R_A = R_B \bullet \left(\frac{V_{THRESHOLD}}{1.25V} - 1 \right)$$

$V_{THRESHOLD}$ is the V_{IN} referred voltage at which the supply is enabled (UVLO and EN) or disabled (OVLO).

Switching Frequency Synchronization

The oscillator can be synchronized to an external clock. Set the R_T resistor 15% below the lowest synchronized frequency. The rising edge of the SYNC pin waveform triggers the discharge of the internal oscillator capacitor. If unused, connect the SYNC pin to GND.

Layout Considerations Checklist

The following is a list of recommended layout considerations:

- Locate the V_{IN}, AUXVIN, $INTV_{CC}$, AUXBST and BOOST pin bypass capacitors in close proximity to the LT3840.
- Create a solid GND plane, preferably on layer two of the PCB.
- Minimize the hot loop. (See Figure 9)
- Use short wide traces for the MOSFET gate drivers (TG and BG), as well as, gate drive supply and return ($INTV_{CC}$ and BOOST, BGRTN and SW).
- Connect the FB pin directly to the feedback resistors, independent of any other nodes (i.e. $SENSE^+$).
- Locate the feedback resistors in close proximity to the LT3840 FB pin.
- Route the $SENSE^-$ and $SENSE^+$ traces close together and keep as short as possible.
- Solder the LT3840 exposed pad to the PCB. Add multiple vias to connect the exposed pad to the GND plane.
- Per the manufacturer's specification, add a sufficient PCB pad around MOSFETs and inductor to dissipate heat.

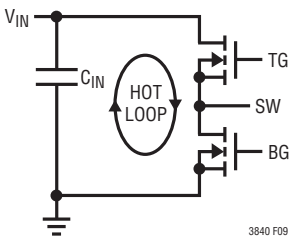
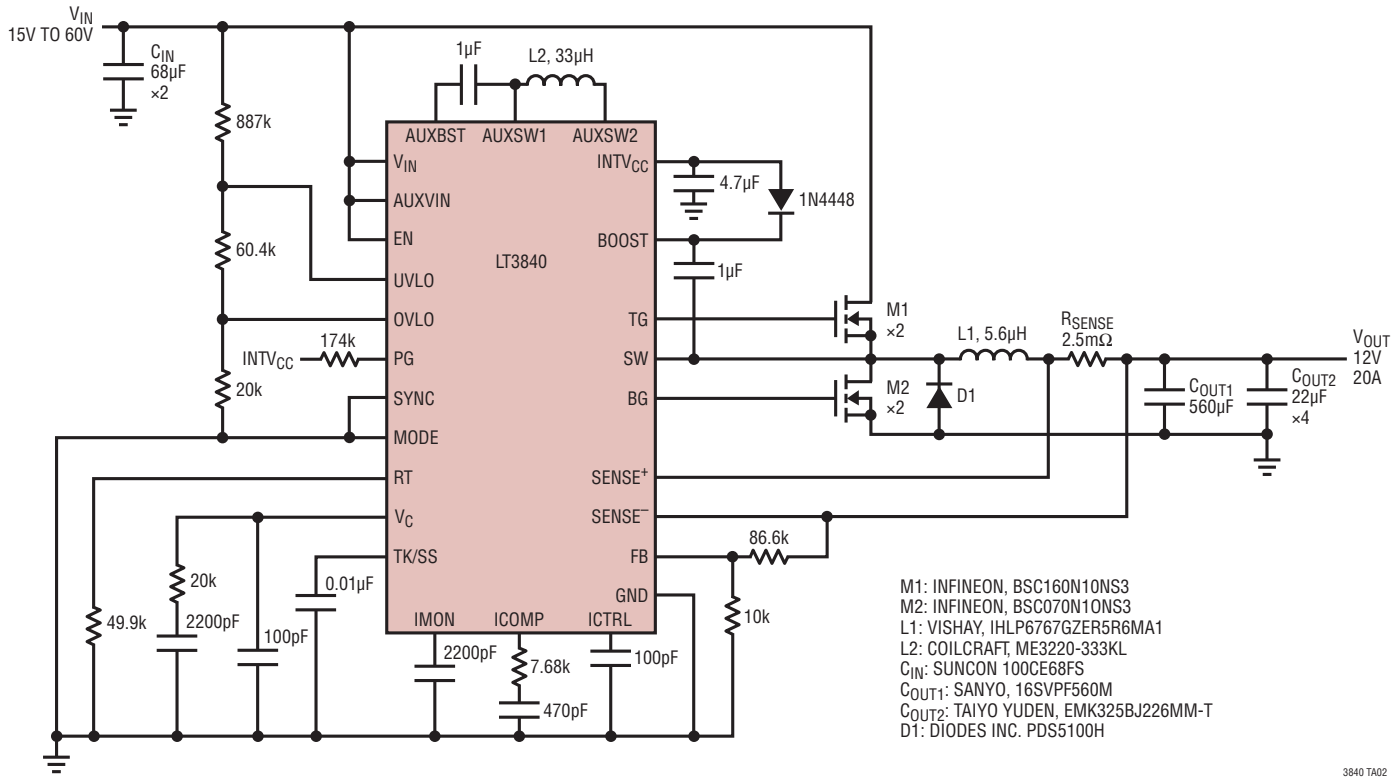


Figure 9. Hot Loop Layout for Synchronous Buck Regulator

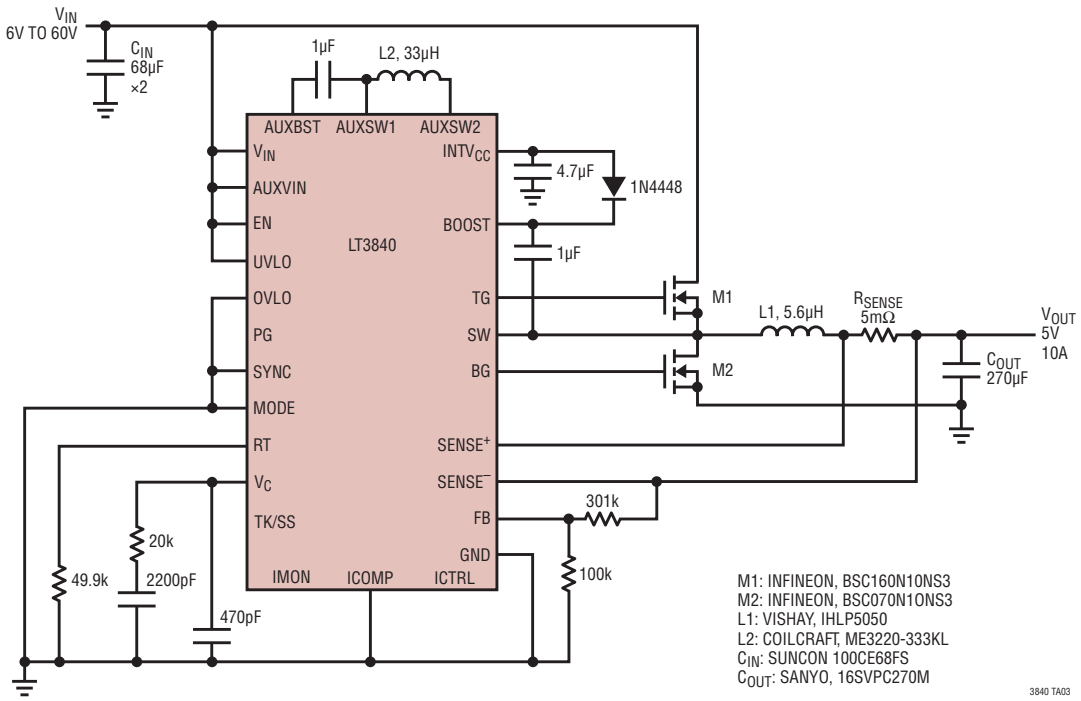
TYPICAL APPLICATIONS

Wide Input Range, High Power Output, 15V to 60V Input to 12V, 20A Output

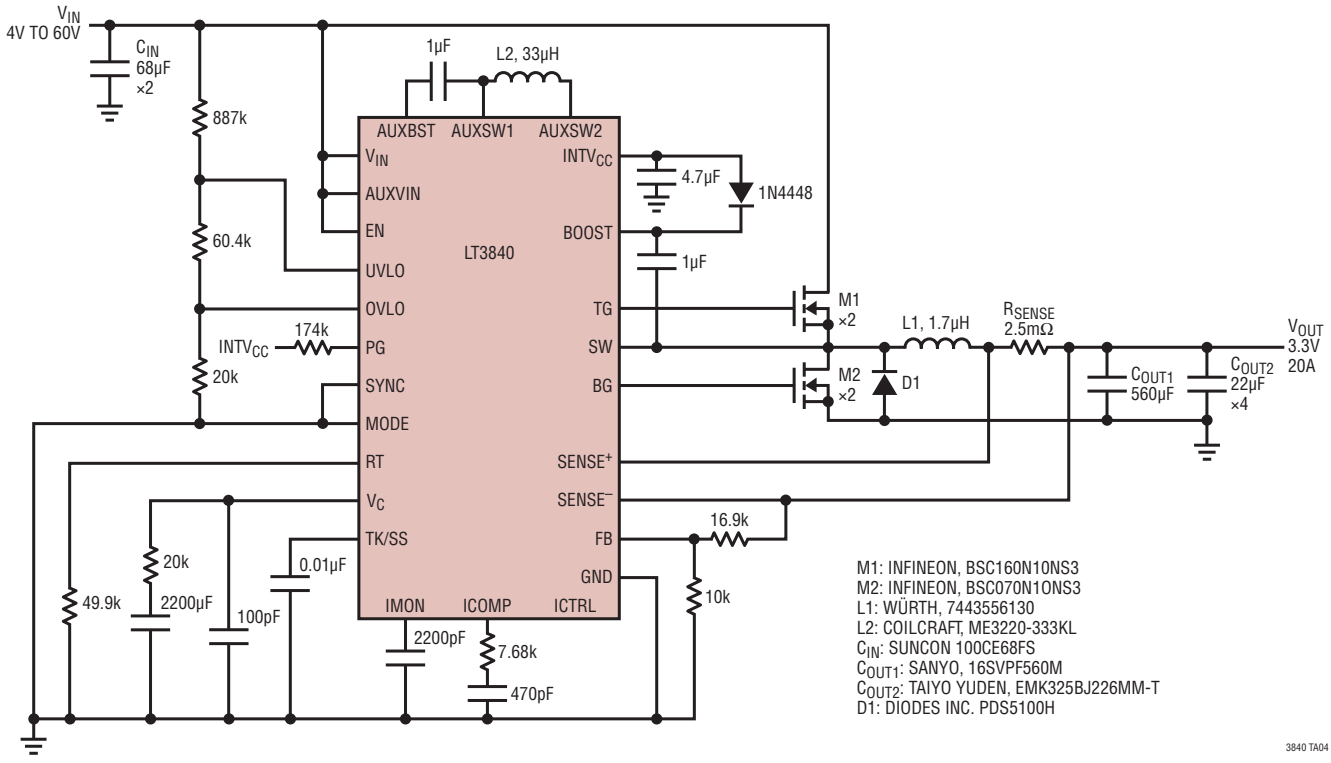


TYPICAL APPLICATIONS

Low Part Count Application, 6V to 60V Input to 5V, 10A Output



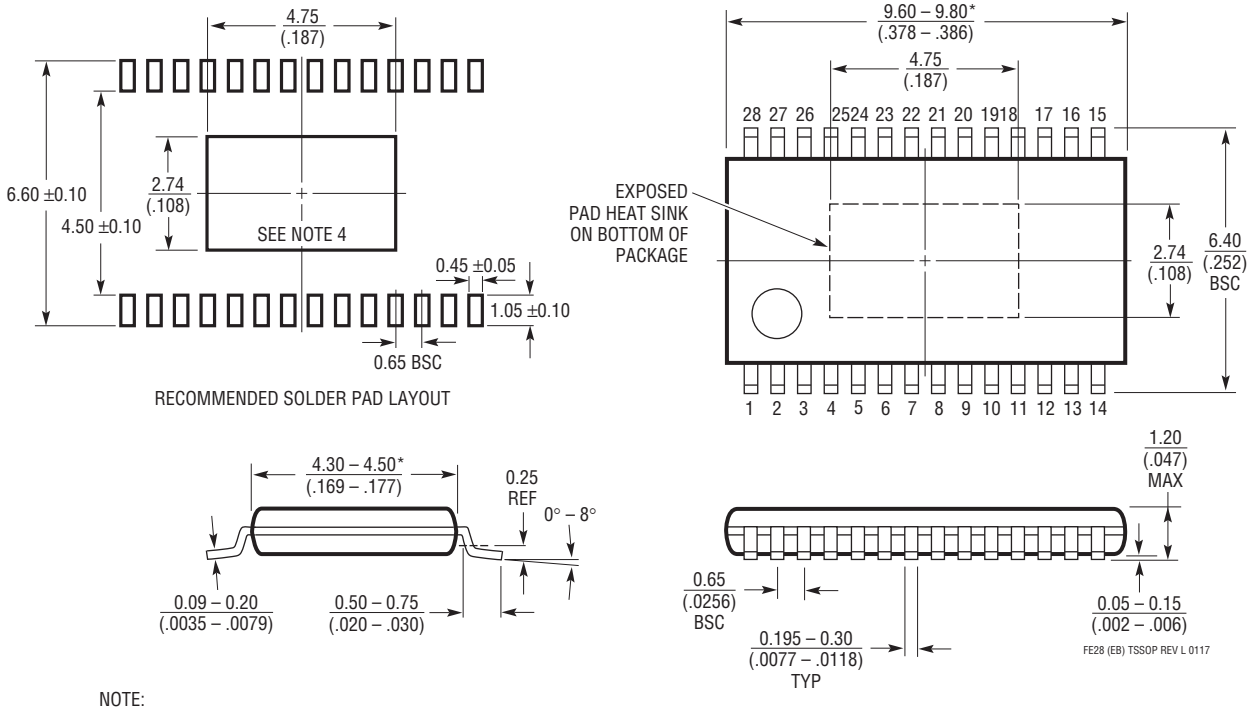
Low Voltage, High Current Output, 4V to 60V Input to 3.3V, 20A



PACKAGE DESCRIPTION

Please refer to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB

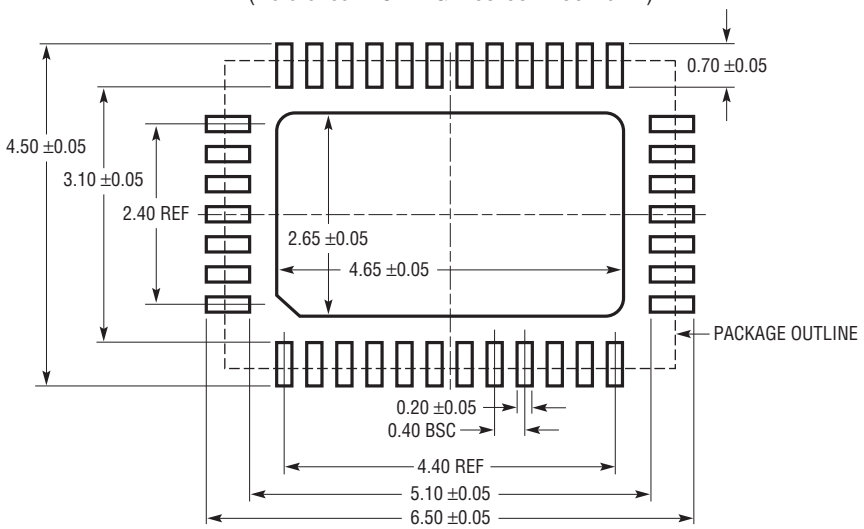


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

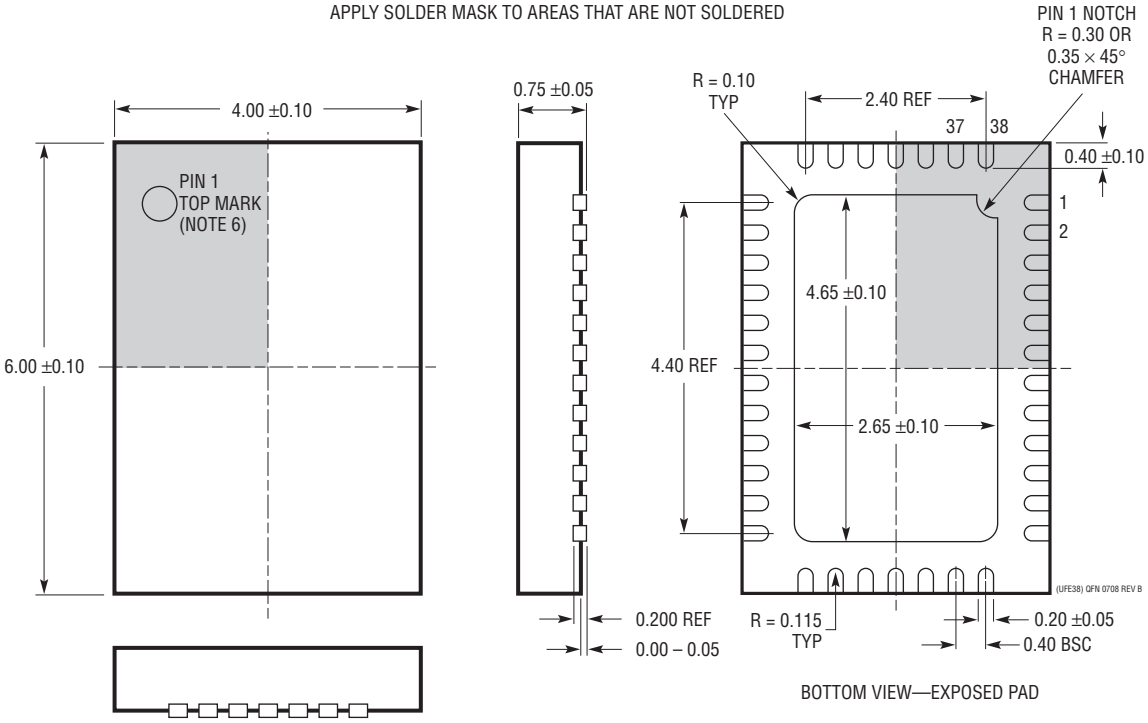
PACKAGE DESCRIPTION

Please refer to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html for the most recent package drawings.

UFE Package
38-Lead Plastic QFN (4mm × 6mm)
(Reference LTC DWG # 05-08-1750 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

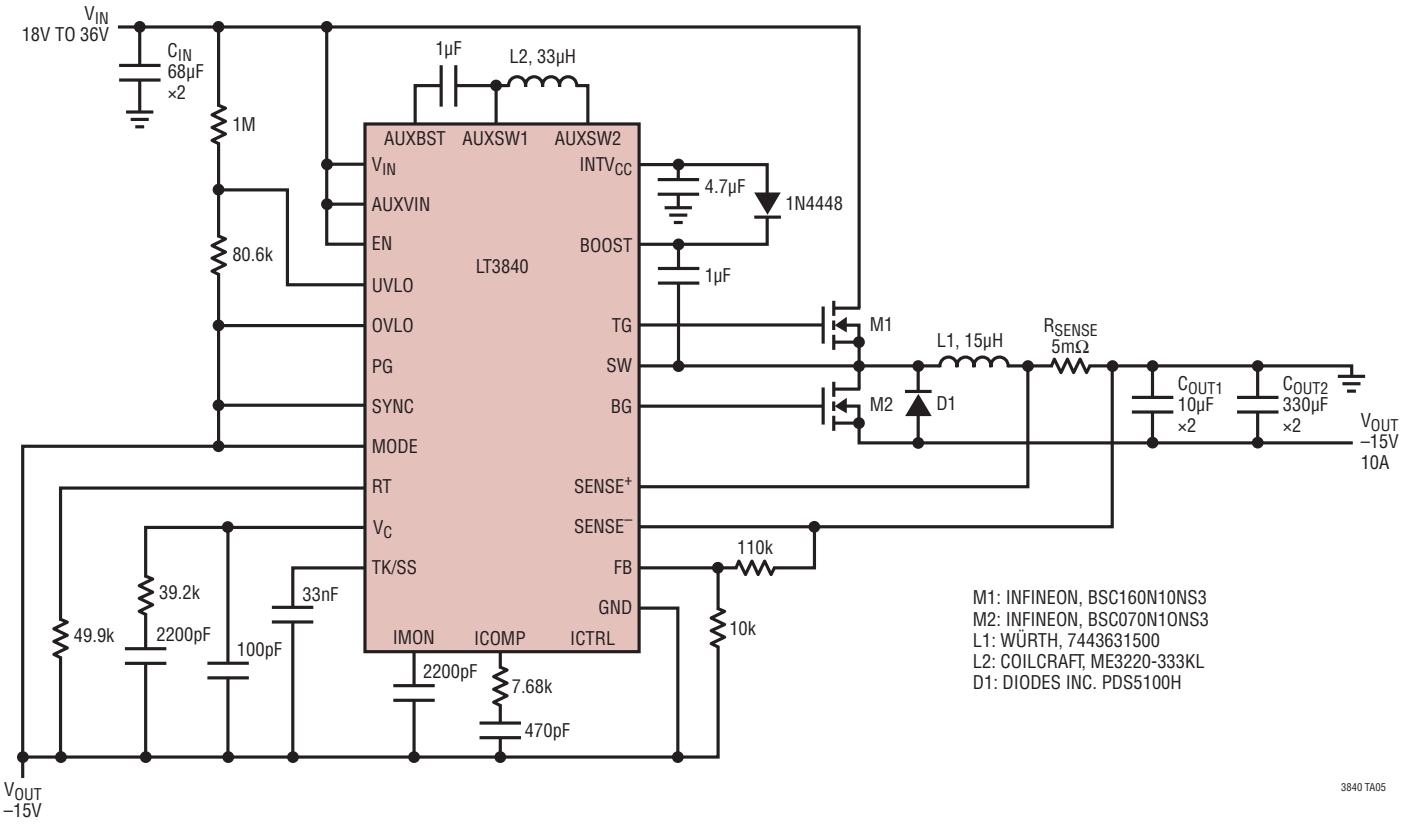
Rev B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/14	Changed PG hysteresis	4
		Modified schematic	20
B	10/23	Replaced FE package POD with the correct package variation	21
		Updated hyperlink to POD database	21, 22

TYPICAL APPLICATION

Inverting Application, 24V Input to –15V, 10A



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Synchronizable Fixed Frequency 100kHz to 600kHz, 4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16 Package
LT3844	60V, Low I_Q, Single Output Step-Down DC/DC Controller	Synchronizable Fixed Frequency 50kHz to 600kHz, 4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16 Package
LTC3864	60V, Low I_Q, Step-Down DC/DC Controller 100% Duty Cycle Capability	Selectable Fixed Frequency 200kHz to 600kHz, 3.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E Package
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3890/ LTC3890-1/ LTC3890-2	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3859A	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	All Outputs Remain in Regulation Through Cold Crank, 2.5V ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 27µA
LT8705	30V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	Synchronizable Fixed Frequency 100kHz to 400kHz, 2.8V ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 30V, Four Regulation Loops