NVIDIA Jetson Nano System-on-Module

Maxwell GPU + Arm Cortex-A57 + 4GB LPDDR4 + 16GB eMMC

Data Sheet

Document History

DA-09366-001_v1.2

Version	Date	Description of Change
v0.1	January 2019	Initial Release
v0.8	October 2019	Updated: > Operating Requirements: corrected Module Power to reflect power for module only (previous stated range included module + IO) > Temperature Range for clarity, included maximum operating temperature and updated note to reflect module temperature is based on T_j.
v1.0	February 2020	Updated: > GPIO Pins: corrected pin number listing for GPIO01 > High-Definition Multimedia Interface (HDMI) and DisplayPort (DP) Interfaces reference to YUV output support > Gigabit Ethernet – Corrected Realtek Gigabit Ethernet Controller part number > Operating and Absolute Maximum Ratings – Added Mounting Force to Absolute Maximum Ratings table. > Package Drawing and Dimensions Added: > Environmental and Mechanical Screening
v1.1	May 2022	Updated: > PMIC_BBAT Pin Description > GPIO Pins: updated GPIO8 (pin 208) description; Fan tachometer only > SD/SDIO pin descriptions to include 3.3V support; deprecated GPIO8 SD Card Detect support > SPI master timing diagram and parameters > UART – UART1_CTS (pin 209) updated PoR > Package Drawing and Dimensions Added: > Module dimensions table
v1.2	January 19, 2023	Updated > CARRIER_PWR_ON to SYS_RESET* in the Absolute Maximum Ratings table > CUDA 10.2 to CUDA 11.4+ > Open Drain Pin Type DC Characteristics table Added: > Storage and Handling table Removed not supported features: > Color Decompression

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Chapter 1. Overview

Description	Operation/Performance
Maxwell GPU ◊	
128-core GPU | End-to-end lossless compression | Tile Caching | OpenGL® 4.6 | OpenGL ES 3.2 | Vulkan™ 1.1◊ | CUDA 11.4+ | OpenGL ES Shader Performance (up to): 512 GFLOPS (FP16)	
Operating Frequency (up to):	921MHz
CPU Cluster	
Arm® Cortex® -A57 MPCore (Quad-Core) Processor with NEON Technology | L1 Cache: 48KB L1 instruction cache (I-cache) per core; 32KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB	
Operating Frequency per Core (up to):	1.43GHz
Memory Subsystem	
Dual Channel | System MMU | Memory Type: 4ch x 16-bit LPDDR4 | Maximum Capacity: 4GiB	
Maximum Operating Frequency (up to)	1600MHz
Peak Memory Bandwidth	25.6GB/s
HD Video	
Decode Supported Standards: H.265, H.264, VP9, VP8, AV1, MPEG-2 (see Multi-Standard Video Decoder section for detailed description)	
Encode Supported Standards: H.265, H.264, VP8, AV1, JPEG (see Multi-Standard Video Encoder section for detailed description)	
Display Controller Subsystem	
Two independent display controllers support DSI, HDMI, DP, eDP: > MIPI-DSI (1.5Gbps/lane): Single x2 lane | Maximum Resolution: 1920x960 at 60Hz (up to 24bpp) > HDMI 2.0a/b (up to 6Gbps) | DP 1.2a (HBR2 5.4 Gbps) | eDP 1.4 (HBR2 5.4Gbps) | Maximum Resolution (DP/eDP/HDMI): 3840 x 2160 at 60Hz (up to 24bpp)	
Clocks	
System clock: 38.4MHz | Sleep clock: 32.768kHz | Dynamic clock scaling and clock source selection	
Boot Sources	
eMMC and USB (recovery mode)	
Audio Subsystem	

Description	Operation/Performance
Industry-standard High-Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI® interface	
Networking	
10/100/1000 BASE-T Ethernet | Media Access Controller (MAC)	
Imaging	
Dedicated RAW to YUV processing engines process up to 1400Mpix/s (up to 24MP sensor) | MIPI CSI 2.0 up to 1.5Gbps (per lane) | Support for x4 and x2 configurations (up to four active streams)	
Storage	
eMMC 5.1 Flash Storage | Bus Width: 8-bit | Maximum Bus Frequency: 200MHz (HS400) | Storage Capacity: 16GB	
Peripheral Interfaces	
USB: xHCI host controller with integrated PHY (up to) 1x USB 3.0, 3x USB 2.0 | USB 3.0 device controller with integrated PHY | EHCI controller with embedded hub for USB 2.0	
PCIe: Up to GEN4 | 3 x1 (or 1 x2 + 1 x1) + 1 x4 | x1 and x2 (supports Root Port only), x4 (supports Root Port or Endpoint modes)	
UART: 3 x UART **SPI:** 2 x SPI **I2C:** 4 x I2C **I2S:** 2 x I2S, RJM, LJM, PCM, TDM (multi-slot mode) **GPIO:** multiple dedicated GPIOs **SD/MMC:** 1 x SD/MMC controller (supporting SDIO 4.0, SD HOST 4.0) **PCIe:** 1 x1/2/4 controller	
Mechanical	
Module Size: 69.6 mm x 45 mm | PCB: 8L HDI | 260 pin SO-DIMM Connector	
Operating Requirements	
Temp. Range (TJ)*: -25°C – 97°C | Supported Power Input: 5V | Module Power: 5 – 10W	

Notes:

- Refer to the software release feature list for current software support; all features may not be available for a particular OS.
- ◊ Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.
- * See the *Jetson Nano Thermal Design Guide* for details

Chapter 2. Functional Description

The NVIDIA® Jetson Nano is designed for use in power-limited environments and provides industry-leading compute capabilities, 64-bit operating capability, and integrated advanced multi-function audio, video, and image processing pipelines into a 260-pin SO-DIMM. The Maxwell GPU architecture implemented several architectural enhancements designed to extract maximum performance per watt consumed. Core components of the Jetson Nano series module include:

- NVIDIA® Tegra® X1 series SoC
  - NVIDIA Maxwell GPU
  - Arm® quad-core Cortex®-A57 CPU Complex
- 4GB LPDDR4 memory
- 16GB eMMC 5.1 storage
- Gigabit Ethernet (10/100/1000 Mbps)
- PMIC, regulators, power and voltage monitors
- 260-pin keyed connector (exposes both high-speed and low-speed industry standard I/O)
- On-chip temperature sensors

2.1 Maxwell GPU

The Graphics Processing Cluster (GPC) is a dedicated hardware block for rasterization, shading, texturing, and compute; most of the GPU's core graphics functions are performed inside the GPC. Within the GPC there are multiple Streaming Multiprocessor (SM) units and a Raster Engine. Each SM includes a Polymorph Engine and Texture Units; raster operations remain aligned with L2 cache slices and memory controllers.

The Maxwell GPU architecture introduced an all-new design for the SM, redesigned all unit and crossbar structures, optimized data flows, and significantly improved power management. The SM scheduler architecture and algorithms were rewritten to be more intelligent and avoid unnecessary stalls, while further reducing the energy per instruction required for scheduling. The organization of the SM also changed; each Maxwell SM (called SMM) is now partitioned into four separate processing blocks, each with its own instruction buffer, scheduler and 32 CUDA cores.

The SMM CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the Polymorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output. The SMM geometry and pixel processing performance make it highly

suitable for rendering advanced user interfaces and complex gaming applications; the power efficiency of the Maxwell GPU enables this performance on devices with power-limited environments.

Features:

- End-to-end lossless compression
- Tile Caching
- Support for OpenGL 4.6, OpenGL ES 3.2, Vulkan 1.1, DirectX 12, CUDA 11.4+ (FP16)
- Adaptive Scalable Texture Compression (ATSC) LDR profile supported
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power-of-2 and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute Instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

GPU frequency and voltage are actively managed by Tegra Power and Thermal Management Software and influenced by workload. Frequency may be throttled at higher temperatures (above a specified threshold) resulting in a behavior that reduces the GPU operating frequency. Observed chip-to-chip variance is due to NVIDIA ability to maximize performance (DVFS) on a per-chip basis, within the available power budget.

2.2 CPU Complex

The CPU complex is a high-performance Multi-Core SMP cluster of four Arm Cortex-A57 CPUs with 2MB of L2 cache (shared by all cores). Features include:

- Superscalar, variable-length, out-of-order pipeline.
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer RAMs, a return stack, and an indirect predictor.
- 48-entry fully-associative L1 instruction TLB with native support for 4KB, 64KB, and 1MB page sizes.
- 32-entry fully-associative L1 data TLB with native support for 4KB, 64KB, and 1MB pages sizes.
- 4-way set-associative unified 1024-entry Level 2 (L2) TLB in each processor.
- 48Kbyte I-cache and 32Kbyte D-cache for each core.

- Full implementation of Armv8 architecture instruction set.
- Embedded Trace Microcell (ETM) based on the ETMv4 architecture.
- Performance Monitor Unit (PMU) based on the PMUv3 architecture.
- Cross Trigger Interface (CTI) for multiprocessor debugging.
- Cryptographic Engine for crypto function support.
- Interface to an external Generic Interrupt Controller (vGIC-400).
- Power management with multiple power domains.

CPU frequency and voltage are actively managed by Tegra Power and Thermal Management Software and influenced by workload. Frequency may be throttled at higher temperatures (above a specified threshold) resulting in a behavior that reduces the CPU operating frequency. Observed chip-to-chip variance is due to NVIDIA ability to maximize performance (DVFS) on a per-chip basis, within the available power budget.

2.2.1 Snoop Control Unit and L2 Cache

The CPU cluster includes an integrated snoop control unit (SCU) that maintains coherency between the CPUs within the cluster and a tightly coupled L2 cache that is shared between the CPUs within the cluster. The L2 cache also provides a 128-bit AXI master interface to access DRAM. L2 cache features include:

- 2MB L2
- Fixed line length of 64 bytes
- 16-way set-associative cache structure
- Duplicate copies of the L1 data cache directories for coherency support
- Hardware pre-fetch support
- ECC support

2.2.2 Performance Monitoring

The performance monitoring unit (part of MPCore non-CPU logic) provides six counters, each of which can count any of the events in the processor. The unit gathers various statistics on the operation of the processor and memory system during runtime, based on Arm PMUv3 architecture.

2.3 High-Definition Audio-Video Subsystem

The audio-video subsystem off-loads audio and video processing activities from the CPU subsystem resulting in faster, fully concurrent, highly efficient operation.

2.3.1 Multi-Standard Video Decoder

The video decoder accelerates video decode, supporting low resolution content, Standard Definition (SD), High Definition (HD) and UltraHD (2160p, or 4k video) profiles. The video decoder is designed to be extremely power efficient without sacrificing performance.

The video decoder communicates with the memory controller through the video DMA which supports a variety of memory format output options. For low power operations, the video decoder can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques.

Video standards supported:

- H.265: Main10, Main
- WEBM VP9 and VP8
- H.264: Baseline (no FMO/ASO support), Main, High, Stereo SEI (half-res)
- VC-1: Simple, Main, Advanced
- MPEG-4: Simple (with B frames, interlaced; no DP and RVLC)
- H.263: Profile 0
- DiVX: 4/5/6
- XviD Home Theater
- MPEG-2: MP

2.3.2 Multi-Standard Video Encoder

The multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high-quality video encoding operations for applications such as video recording and video conferencing. The encode processor is designed to be extremely power-efficient without sacrificing performance.

Video standards supported:

- H.265 Main Profile: I-frames and P-frames (No B-frames)
- H.264 Baseline/Main/High Profiles: IDR/I/P/B-frame support, MVC
- VP8
- MPEG4 (ME only)
- MPEG2 (ME only)
- VC1 (ME only): No B frame, no interlaced

2.3.3 JPEG Processing Block

The JPEG processing block is responsible for JPEG (de)compression calculations (based on JPEG still image standard), image scaling, decoding (YUV420, YUV422H/V, YUV444, YUV400) and color space conversion (RGB to YUV; decode only).

Input (encode) formats:

- Pixel width: 8bpc

- Subsample format: YUV420
- Resolution up to 16K x 16K
- Pixel pack format
  - Semi-planar/planar for 420

Output (decode) formats:

- Pixel width 8bpc
- Resolution up to 16K x 16K
- Pixel pack format
  - Semi-planar/planar for YUV420
  - YUY2/planar for 422H/422V
  - Planar for YUV444
  - Interleave for RGBA

2.3.4 Video Image Compositor (VIC)

The Video Image Compositor implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features:

- High-quality Deinterlacing
- Inverse Teleciné
- Temporal Noise Reduction
  - High-quality video playback
  - Reduces camera sensor noise
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation

2.4 Image Signal Processor (ISP)

The ISP module takes data from the VI/CSI module or memory in raw Bayer format and processes it to YUV output. The imaging subsystem supports raw (Bayer) image sensors up to 24 million

pixels. Advanced image processing is used to convert input to YUV data and remove artifacts introduced by high megapixel CMOS sensors and optics with up to 30-degree CRA.

Features:

- Flexible post-processing architecture for supporting custom computer vision and computational imaging operations
- Bayer domain hardware noise reduction
- Per-channel black-level compensation
- High-order lens-shading compensation
- 3 x 3 color transform
- Bad pixel correction
- Programmable coefficients for de-mosaic with color artifact reduction

  Color Artifact Reduction: a two-level (horizontal and vertical) low-pass filtering scheme that is used to reduce/remove any color artifacts that may result from Bayer signal processing and the effects of sampling an image.
- Enhanced down scaling quality
- Edge Enhancement
- Color and gamma correction
- Programmable transfer function curve
- Color-space conversion (RGB to YUV)
- Image statistics gathering (per-channel)
  - Two 256-bin image histograms
  - Up to 4,096 local region averages
  - AC flicker detection (50Hz and 60Hz)
  - Focus metric block

2.5 Display Controller Complex

The Display Controller Complex integrates two independent display controllers. Each display controller is capable of interfacing to an external display device and can drive the same or different display contents at different resolutions and refresh rates. Each controller supports a cursor and three windows (Window A, B, and C); controller A supports two additional simple windows (Window D, T). The display controller reads rendered graphics or video frame buffers in memory, blends them and sends them to the display.

Features:

- Two heads. Each can be mapped to one of:
  - 1x DSI, 1x eDP/DP (Limited Functionality: No Audio)
  - 1x HDMI/DP (Full Functionality)
- 90, 180, 270-degree image transformation uses both horizontal and vertical flips (controller A only)
- Byte-swapping options on 16-bit and 32-bit boundary for all color depths

- NVIDIA Pixel Rendering Intensity and Saturation Management™ (PRISM)
- 256 x 256 cursor size
- Scaling and tiling in hardware for lower power operation
- Full color alpha-blending
- Captive panels
  - Secure window (Win T) for TrustZone
  - Supports cursor and up to four windows (Win A, B, C, and D)
  - 1x 2-lane MIPI DSI
  - Supports MIPI D-PHY rates up to 1.5Gbps
  - 4-lane eDP with AUX channel
  - Independent resolution and pixel clock
  - Supports display rotation and scaling in hardware
- External displays
  - Supports cursor and three windows (Window A, B, and C)
  - 1x HDMI (2.0) or DisplayPort (HBR2) interface
  - Supports display scaling in hardware

2.6 Memory

The Jetson Nano integrates 4GB of LPDDR4 over a four-channel x 16-bit interface. Memory frequency options are 204MHz and 1600MHz; maximum frequency of 1600MHz has a theoretical peak memory bandwidth of 25.6GB/s.

The Memory Controller (MC) maximizes memory utilization while providing minimum latency access for critical CPU requests. An arbiter is used to prioritize requests, optimizing memory access efficiency and utilization and minimizing system power consumption. The MC provides access to main memory for all internal devices. It provides an abstract view of memory to its clients via standardized interfaces, allowing the clients to ignore details of the memory hierarchy. It optimizes access to shared memory resources, balancing latency and efficiency to provide best system performance, based on programmable parameters.

Features:

- TrustZone (TZ) Secure and OS-protection regions
- System Memory Management Unit
- Dual CKE signals for dynamic power down per device
- Dynamic Entry/Exit from Self -Refresh and Power Down states

The MC can sustain high utilization over a very diverse mix of requests. For example, the MC is prioritized for bandwidth (BW) over latency for all multimedia blocks (the multimedia blocks have been architected to prefetch and pipeline their operations to increase latency tolerance); this enables the MC to optimize performance by coalescing, reordering, and grouping requests to minimize memory power. DRAM also has modes for saving power when it is either not being used, or during periods of specific types of use.

Chapter 3. Power and System Management

The Jetson Nano module operates from a single power source (VDD_IN) with all internal module voltages and I/O voltages generated from this input. This enables the on-board power management controller to implement a tiered structure of power and clock gating in a complex environment that optimizes power consumption based on workload:

- **Power Management Controller (PMC) and Real Time Clock (RTC):** These blocks reside in an Always On (not power gated) partition. The PMC provides an interface to an external power manager IC or PMU. It primarily controls voltage transitions for the SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC, USB attach) which can wake the system from a deep-sleep state. The RTC maintains the ability to wake the system based on either a timer event or an external trigger (e.g., key press).
- **Power Gating:** The SoC aggressively employs power-gating (controlled by PMC) to power-off modules which are idle. CPU cores are on a separate power rail to allow complete removal of power and eliminate leakage. Each CPU can be power gated independently. Software provides context save/restore to/from DRAM.
- **Clock Gating:** Used to reduce dynamic power in a variety of power states.
- **Dynamic Voltage and Frequency Scaling (DVFS):** Raises voltages and clock frequencies when demand requires, lowers them when less is sufficient, and removes them when none is needed. DVFS is used to change the voltage and frequencies in the following power domains: CPU, CORE, and GPU.

Table 3-1: Power and System Control Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
251 252 253 254 255 256 257 258 259	VDD_IN	Input	5.0V		Power: Main DC input, supplies PMIC and other regulators

Pin	Name	Direction	Type	PoR	Description
260					
235	PMIC_BBAT	Bidirectional	1.65V-5.5V		Power: PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC).
240	SLEEP/WAKE*	Input	CMOS – 5.0V	PU	Sleep / Wake. Configured as GPIO for optional use to place system in sleep mode or wake system from sleep.
214	FORCE_RECOVERY*	Input	CMOS – 1.8V	PU	Force Recovery: strap pin
237	POWER_EN	Input	CMOS – 5.0V		Module on/off: high = on, low = off.
233	SHUTDOWN_REQ*	Output	CMOS – 5.0V	z	Shutdown Request: used by the module to request a shutdown from the carrier board (POWER_EN low). 100kΩ pull-up to VDD_IN (5V) on the module.
239	SYS_RESET*	Bidirectional	Open Drain, 1.8V	1	Module Reset. Reset to the module when driven low by the carrier board. When module power sequence is complete used as carrier board supply enable. Used to ensure proper power on/off sequencing between module and carrier board supplies. 4.7kΩ pull-up to 1.8V on the module.
178	MOD_SLEEP*	Output	CMOS – 1.8V		Indicates the module sleep status. Low is in sleep mode, high is normal operation. This pin is controlled by system software and should not be modified.

3.1 Power Rails

VDD_IN must be supplied by the carrier board that the Jetson Nano is designed to connect to. It must meet the required electrical specifications detailed in Section 5. All Jetson Nano interfaces are referenced to on-module voltage rails; no I/O voltage is required to be supplied to the module. See the *Jetson Nano Product Design Guide* for details of connecting to each of the interfaces.

3.2 PMIC_BBAT

An optional back up battery can be attached to the PMIC_BBAT module input. It is used to maintain the RTC voltage when VDD_IN is not present. This pin is connected directly to the onboard PMIC. When a backup cell is connected to the PMIC, the RTC will retain its contents and can be configured to charge the backup cell. RTC accuracy is 2 seconds/day under typical room temperature conditions (only).

The following backup cells may be attached to the PMIC_BBAT pin:

- Super Capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)

- Rechargeable Lithium Manganese cells

A backup cell **MUST** provide a voltage in the range 2.5V to 3.5V. The backup cell is charged with a constant current, constant voltage charger that can be configured between 2.5V and 3.5V (constant voltage) output and 50µA to 800µA (constant current).

Table 3-2: PMIC_BBAT Pin Descriptions

Pin	Name	Description	Direction	Pin Type
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power. Constant current of 2.0µA for 2.5V; 2.3µA for 3.3V typical; 4.2µA maximum.	Bidir	1.65V-5.5V

3.3 Power Domains/Islands

Power domains and power islands are used to optimize power consumption for various low-power use cases and limiting leakage current. The RTC domain is always on, CORE/CPU/GPU domains can be turned on and off. The CPU, CORE, and GPU power domains also contain power-gated islands which are used to power individual modules (as needed) within each domain. Clock-gating is additionally applied during powered-on but idle periods to further reduce unnecessary power consumption. Clock-gating can be applied to both power-gated and non-power-gated islands (NPG).

Table 3-3: Power Domains

Power Domain	Power Island in Domain	Modules in Power Island
RTC (VDD_RTC)	N/A	PMC (Power Management Controller)
		RTC (Real Time Clock)
CORE (VDD_SOC)	NPG (Non-Power-Gated)	AHB, APB Bus, AVP, Memory Controller (MC/EMC), USB 2.0, SDMMC
	VE, VE2	ISPs (image signal processing) A and B, VI (video input), CSI (Camera Serial Interface)
	NVENC	Video Encode
	NVDEC	Video Decode
	NVJPG	JPG accelerator and additional Video Decode
	PCX	PCIe
	SOR	HDMI, DSI, DP
	IRAM	IRAM
	DISP-A, DISP-B	Display Controllers A and B

Power Domain	Power Island in Domain	Modules in Power Island
	XUSBA, XUSBB, XUSBC	USB 3.0
	VIC	VIC (Video Image Compositor)
	ADSP	APE (Audio Processing Engine)
	DFD	Debug logic
GPU (VDD_GPU)	GPU	3D, FE, PD, PE, RAST, SM, ROP
CPU (VDD_CPU)	CPU 0	CPU 0
	CPU 1	CPU 1
	CPU 2	CPU 2
	CPU 3	CPU 3
	Non-CPU	L2 Cache for Main CPU complex
	TOP	Top level logic

3.4 Power Management Controller (PMC)

The PMC power management features enable both high-speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the SoC as it transitions to/from different low-power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC, USB attach) which can wake the system from deep sleep state. The PMC enables aggressive power-gating capabilities on idle modules and integrates specific logic to maintain defined states and control power domains during sleep and deep sleep modes.

3.4.1 Resets

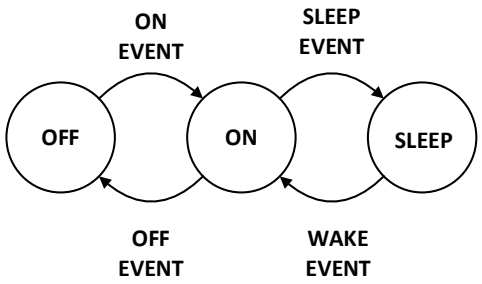
The PMC receives the primary reset event (from SYS_RESET*) and generates various resets for: PMC, RTC, and CAR. From the PMC provided reset, the Clock and Reset (CAR) controller generates resets for most of the blocks in the module. In addition to reset events, the PMC receives other events (e.g., thermal, WatchDog Timer (WDT), software, wake) which also result in variants of system reset.

The RTC block includes an embedded real-time clock and can wake the system based on either a timer event or an external trigger (e.g., key press).

3.4.2 System Power States and Transitions

The Jetson module operates in three main power modes: OFF, ON, and SLEEP. The module transitions between these states are based on various events from hardware or software. The figure below shows the transitions between these states.

Figure 3-1: Power State Diagram



3.4.2.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state the Jetson module is fully functional and operates normally. An ON event has to occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_EN pin. This must occur with VDD_IN connected to a power rail, and POWER_EN is asserted (at a logic1). The POWER_EN control is the carrier board indication to the Jetson module that the VDD_VIN power is good. The Carrier board should assert this high only when VDD_IN has reached its required voltage level and is stable. This prevents the Jetson module from powering up until the VDD_IN power is stable.

Note: The Jetson Nano module does include an Auto-Power-On option; a system input that enables the module to power on if asserted. For more information on available signals and broader system usage, see the *Jetson Nano Product Design Guide.*

3.4.2.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state, through an OFF event. OFF Events are listed in the table below.

Table 3-4: OFF State Events

Event	Details	Preconditions
HW Shutdown	Set POWER_EN pin to zero for at least 100µS, the internal PMIC will start shutdown sequence.	In ON State
SW Shutdown	Software initiated shutdown	ON state, Software operational
Thermal Shutdown	If the internal temperature of the Jetson module reaches an unsafe temperature, the hardware is designed to initiate a shutdown.	Any power state

3.4.2.3 SLEEP State

The Sleep state can only be entered from the ON state. This state allows the Jetson module to quickly resume to an operational state without performing a full boot sequence. In this state the Jetson module operates in low power with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state the output signals from Jetson module are maintained at their logic level prior to entering the state (i.e., they do not change to a 0V level).

The SLEEP state can only be entered directly by software. For example, operating within an OS, with no operations active for a certain time can trigger the OS to initiate a transition to the SLEEP state.

To Exit the SLEEP state a WAKE event must occur. WAKE events can occur from within the Jetson module or from external devices through various pins on the Jetson Nano connector. A full list of Wake enabled pins is available in the pinmux.

Table 3-5: SLEEP State Events

Event	Details
RTC WAKE up	Timers within the Jetson module can be programmed, on SLEEP entry. When these expire, they create a WAKE event to exit the SLEEP state.
Thermal Condition	If the Jetson module internal temperature exceeds programmed hot and cold limits the system is forced to wake up, so it can report and take appropriate action (shut down for example).
USB VBUS detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate.

3.5 Thermal and Power Monitoring

The Jetson Nano is designed to operate under various workloads and environmental conditions. It has been designed so that an active or passive heat sinking solution can be attached. The module contains various methods through hardware and software to limit the internal temperature to within operating limits. See the *Jetson Nano Thermal Design Guide* for more details.

3.6 Power Sequencing

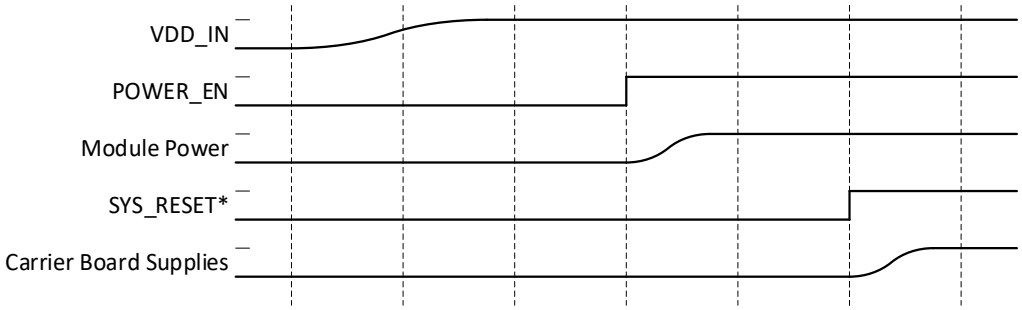
The Jetson Nano module is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the SYS_RESET* signal (when deasserted) is used to indicate when the carrier board can power on. The following sections provide an overview of the power sequencing steps between the carrier board and Jetson Nano module. Refer to the *Jetson Nano Product Design Guide* for system level details on the application of power, power sequencing, and monitoring. The Jetson Nano module and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

3.6.1 Power Up

During power up, the carrier board must wait until the signal SYS_RESET* is deasserted from the Jetson module before enabling its power; the Jetson module will deassert the SYS_RESET* signal to enable the complete system to boot.

Note: I/O pins cannot be high (>0.5V) before SYS_RESET* goes high. When SYS_RESET* is low, the maximum voltage applied to any I/O pin is 0.5V. For more information, refer to the Jetson Nano Product Design Guide.

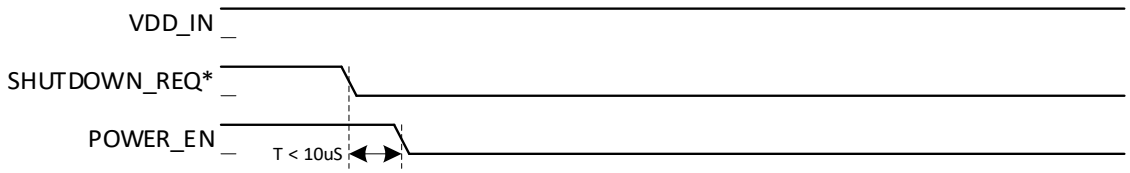
Figure 3-2: Power-up Sequence (No Power Button – Auto-Power-On Enabled)



3.6.2 Power Down

In a shutdown event the Jetson module asserts SHUTDOWN_REQ*. The SHUTDOWN_REQ* must be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss. The Jetson module starts the power off sequence when POWER_EN is deasserted; SYS_RESET* is asserted by the Jetson module, allowing the carrier board to put any components into a known state and power down.

Figure 3-3: Power Down Sequence (Initiated by SHUTDOWN_REQ* Assertion)



Chapter 4. Pin Descriptions

The primary interface to Jetson Nano is via a 260-pin SO-DIMM connector. Connector exposes power, ground, high-speed and low-speed industry standard I/O connections. See the *NVIDIA Jetson Nano Product Design Guide* for details on integrating the module and mating connector into product designs.

The I/O pins on the SO-DIMM are comprised of both Single Function I/O (SFIO) and Multi-Purpose digital I/O (MPIO) pins. Each MPIO can be configured to act as a GPIO, or it can be assigned for use by a particular I/O controller. Though each MPIO has up to five functions (GPIO function and up to four SFIO functions), a given MPIO can only act as a single function at a given point in time. The functions for each pin on the Jetson module are fixed to a single SFIO function or as a GPIO. The different MPIO pins share a similar structure, but there are several varieties of such pins. The varieties are designed to minimize the number of on-board components (such as level shifters or pull-up resistors) required in Jetson Nano designs.

MPIO pin types:

- ST (standard) pins are the most common pins on the chip. They are used for typical General Purpose I/O.
- DD (dual-driver) pins are similar to the ST pins. A DD pin can tolerate its I/O pin being pulled up to 3.3V (regardless of supply voltage) if the pin's output-driver is set to open-drain mode. There are special power-sequencing considerations when using this functionality.

Note: The output of DD pins cannot be pulled High during deep-power-down (DPD).

- CZ (controlled output impedance) pins are optimized for use in applications requiring tightly controlled output impedance. They are similar to ST pins except for changes in the drive strength circuitry and in the weak pull-ups/-downs. CZ pins are included on the VDDIO_SDMMC3 (Module SDMMC pins) power rail; also includes a CZ_COMP pin. Circuitry within the Jetson module continually matches the output impedance of the CZ pins to the on-board pull-up/-down resistors attached to the CZ_COMP pins.
- LV_CZ (low voltage-controlled impedance) pins are similar to CZ pins but are optimized for use with a 1.2V supply voltage (and signaling level). They support a 1.8V supply voltage (and signaling level) as a secondary mode. The Jetson nano uses LV_CZ pins for SPI interfaces operating at 1.8V.

- DP_AUX pin is used as an Auxiliary control channel for the DisplayPort which needs differential signaling. Because the same I/O block is used for DisplayPort and HDMI to ensure the control path to the display interface is minimized, the DP_AUX pins can operate in open-drain mode so that HDMI's control path (i.e., DDC interface which needs I2C) can also be used in the same pin.

Each MPIO pin consists of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either Schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pins are partitioned into multiple "pin control groups" with controls being configured for the group. During normal operation, these per-pin controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the *Tegra X1 (SoC) Technical Reference Manual* for more information on modifying pin controls.

4.1 MPIO Power-on Reset Behavior

Each MPIO pin has a deterministic power-on reset (PoR) state. The particular reset state for each pin is chosen to minimize the need of on-board components like pull-up resistors in a Jetson Nano-based system. For example, the on-chip weak pull-ups are enabled during PoR for pins which are usually used to drive active-low chip selects.

4.2 MPIO Deep Sleep Behavior

Deep Sleep is an ultra-low-power standby state in which the Jetson Nano maintains much of its I/O state while most of the chip is powered off. The following lists offer a simplified description of the deep sleep entry and exit concentrating on those aspects which relate to the MPIO pins. During deep sleep most of the pins are put in a state called Deep Power Down (DPD). The sequence for entering to DPD is same across pins. Specific variations are there in some pins in terms of type of features that are available in DPD.

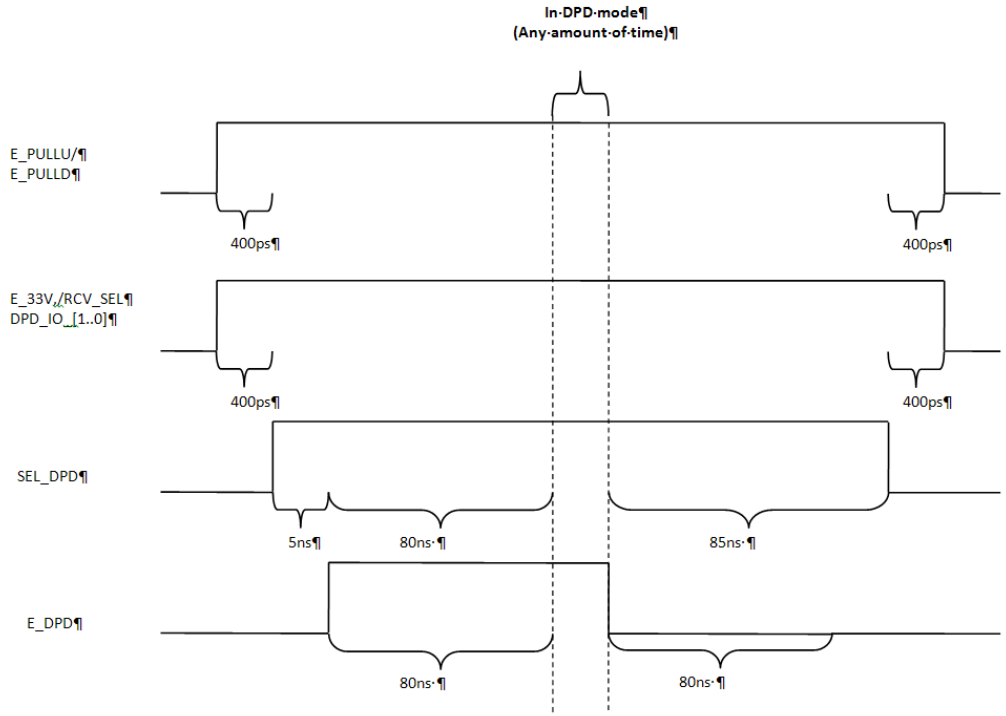
Note: The output of DD pins cannot be pulled High during deep-power-down (DPD). OD pins do NOT retain their output during DPD. OD pins should NOT be configured as GPIOs in a platform where they are expected to hold a value during DPD.

ALL MPIO pins **do NOT** have identical behavior during deep sleep. They differ with regard to:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a "GPIO wake event" OR
  - Enabled for some other purpose (e.g., a "clock request" pin)

- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Pins that do not enter deep sleep
  - Some of the pins whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pins that are associated with PMC logic do not enter deep sleep, pins that are associated with JTAG do not enter into deep sleep any time.

Figure 4-1: DPD Wait Times



4.3 GPIO Pins

The Jetson Nano has multiple dedicated GPIOs. Each GPIO can be individually configurable as an Output, Input, or Interrupt source with level/edge controls. The pins listed in the following table are dedicated GPIOs; some with alternate SFIO functionality. Many other pins not included in this list are capable of being configured as GPIOs instead of the SFIO functionality the pin name suggests (e.g., UART, SPI, I^2S, etc.). All pins that can support GPIO functionality have this exposed in the Pinmux.

Table 4-1: Dedicated GPIO Pin Descriptions

Pin	Name	Direction	Type	PoR	Alternate Function
87	GPIO00	Bidirectional	Open-Drain [DD]	0	USB VBUS Enable (USB_VBUS_EN0)
118	GPIO01	Bidirectional	CMOS – 1.8V [ST]	pd	Camera MCLK #2 (CLK)
124	GPIO02	Bidirectional	CMOS – 1.8V [ST]	pd	
126	GPIO03	Bidirectional	CMOS – 1.8V [ST]	pd	
127	GPIO04	Bidirectional	CMOS – 1.8V [ST]	pd	
128	GPIO05	Bidirectional	CMOS – 1.8V [ST]	pd	
130	GPIO06	Bidirectional	CMOS – 1.8V [ST]	pd	
206	GPIO07	Bidirectional	CMOS – 1.8V [ST]	pd	Pulse Width Modulation Signal
208	GPIO08	Bidirectional	CMOS – 1.8V [ST]	pd	Fan Tachometer
211	GPIO09	Bidirectional	CMOS – 1.8V [ST]	pd	Audio Clock (AUD_MCLK)
212	GPIO10	Bidirectional	CMOS – 1.8V [ST]	pd	
216	GPIO11	Bidirectional	CMOS – 1.8V [ST]	pd	Camera MCLK #3
218	GPIO12	Bidirectional	CMOS – 1.8V [ST]	pd	
228	GPIO13	Bidirectional	CMOS – 1.8V [ST]	pd	Pulse Width Modulation Signal
230	GPIO14	Bidirectional	CMOS – 1.8V [ST]	pd	Pulse Width Modulation Signal
114	CAM0_PWDN	Bidirectional	CMOS – 1.8V [ST]	pd	
120	CAM1_PWDN	Bidirectional	CMOS – 1.8V [ST]	pd	

Chapter 5. Interface Descriptions

The following sections outline the interfaces available on the Jetson Nano module and details the module pins used to interact with and control each interface. See the *Tegra X1 Series SoC Technical Reference Manual* for complete functional descriptions, programming guidelines and register listings for each of these blocks.

5.1 USB

Standard	Notes
Universal Serial Bus Specification Revision 3.0	Refer to specification for related interface timing details.
Universal Serial Bus Specification Revision 2.0	USB Battery Charging Specification, version 1.0; including Data Contact Detect protocol Modes: Host and Device Speeds: Low, Full, and High Refer to specification for related interface timing details.
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	Refer to specification for related interface timing details.

An xHCI/Device controller (named XUSB) supports the xHCI programming model for scheduling transactions and interface managements as a host that natively supports USB 3.0, USB 2.0, and USB 1.1 transactions with its USB 3.0 and USB 2.0 interfaces. The XUSB controller supports USB 2.0 L1 and L2 (suspend) link power management and USB 3.0 U1, U2, and U3 (suspend) link power managements. The XUSB controller supports remote wakeup, wake on connect, wake on disconnect, and wake on overcurrent in all power states, including sleep mode.

5.1.1 USB 2.0 Port

Each USB 2.0 port operates in USB 2.0 High Speed mode when connecting directly to a USB 2.0 peripheral and operates in USB 1.1 Full- and Low-Speed modes when connecting directly to a USB 1.1 peripheral. All USB 2.0 ports operating in High-Speed mode share one High-Speed Bus Instance, which means 480 Mb/s theoretical bandwidth is distributed across these ports. All USB 2.0 ports operating in Full- or Low-Speed modes share one Full/Low-Speed Bus Instance, which means 12 Mb/s theoretical bandwidth is distributed across these ports.

5.1.2 USB 3.0 Port

The USB 3.0 port only operates in USB 3.0 Super Speed mode (5 Gb/s theoretical bandwidth).

Table 5-1: USB 2.0 Pin Descriptions

Pin	Name	Direction	Type	Description
87	GPIO0	Input	USB VBUS, 5V	USB 0 VBUS Detect (USB_VBUS_EN0). Do not feed 5V directly into this pin; see the *Jetson Nano Product Design Guide* for complete details.
109 111	USB0_D_N USB0_D_P	Bidirectional	USB PHY	USB 2.0 Port 0 Data
115 117	USB1_D_N USB1_D_P	Bidirectional	USB PHY	USB 2.0 Port 1 Data
121 123	USB2_D_N USB2_D_P	Bidirectional	USB PHY	USB 2.0 Port 2 Data

Table 5-2: USB 3.0 Pin Descriptions

Pin	Name	Direction	Type	Description
163 161	USBSS_RX_P USBSS_RX_N	Input	USB SS PHY	USB 3.0 SS Receive
168 166	USBSS_TX_P USBSS_TX_N	Output	USB SS PHY	USB 3.0 SS Transmit

5.2 PCI Express (PCIe)

Standard	Notes
PCI Express Base Specification Revision 2.0	Jetson Nano meets the timing requirements for the Gen2 (5.0 GT/s) data rates. Refer to specification for complete interface timing details. Although NVIDIA validates that the Jetson Nano design complies with the PCIe specification, PCIe software support may be limited.

The Jetson module integrates a single PCIe Gen2 controller supporting:

- Connections to a single (x1/2/4) endpoint
- Upstream and downstream AXI interfaces that serve as the control path from the Jetson Nano to the external PCIe device.
- Gen1 (2.5 GT/s/lane) and Gen2 (5.0 GT/s/lane) speeds.

Note: Upstream Type 1 Vendor Defined Messages (VDM) should be sent by the Endpoint Port (EP) if the Root Port (RP) also belongs to same vendor/partner; otherwise, the VDM is silently discarded.

See the *Jetson Nano Product Design Guide* for supported USB 3.0/PCIe configuration and connection examples.

Table 5-3: PCIe Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
179	PCIE_WAKE*	Input	Open Drain 3.3V	z	PCI Express Wake. This signal is used as the PCI Express defined WAKE# signal. When asserted by a PCI Express device, it is a request that system power be restored. No interrupt or other consequences result from the assertion of this signal. On module 100kΩ pull-up to 3.3V
160 162	PCIE0_CLK_N PCIE0_CLK_P	Output	PCIe PHY	0 0	PCIe Reference Clock.
180	PCIE0_CLKREQ*	Bidirectional	Open Drain 3.3V	z	PCIe Reference Clock Request. This signal is used by a PCIe device to indicate it needs the PCIE0_CLK_N and PCIE0_CLK_P to actively drive reference clock. On module 47kΩ pull-up to 3.3V
181	PCIE0_RST*	Output	Open Drain 3.3V	0	PCIe Reset. This signal provides a reset signal to all PCIe links. It must be asserted 100 ms after the power to the PCIe slots has stabilized. On module 47kΩ pull-up to 3.3V
157 155	PCIE0_RX3_P PCIE0_RX3_N	Input	PCIe PHY		PCIe Receive (Lane 3)
151 149	PCIE0_RX2_P PCIE0_RX2_N	Input	PCIe PHY		PCIe Receive (Lane 2)
139 137	PCIE0_RX1_P PCIE0_RX1_N	Input	PCIe PHY		PCIe Receive (Lane 1)
133 131	PCIE0_RX0_P PCIE0_RX0_N	Input	PCIe PHY		PCIe Receive (Lane 0)
156 154	PCIE0_TX3_P PCIE0_TX3_N	Output	PCIe PHY		PCIe Transmit (Lane 3)
150 148	PCIE0_TX2_P PCIE0_TX2_N	Output	PCIe PHY		PCIe Transmit (Lane 2)
142 140	PCIE0_TX1_P PCIE0_TX1_N	Output	PCIe PHY		PCIe Transmit (Lane 1)
136 134	PCIE0_TX0_P PCIE0_TX0_N	Output	PCIe PHY		PCIe Transmit (Lane 0)

5.3 Display Interfaces

The Jetson Nano Display Controller Complex integrates a MIPI-DSI interface and Serial Output Resource (SOR) to collect pixels from the output of the display pipeline, format/encode them to desired format, and then streams to various output devices. The SOR consists of several individual resources which can be used to interface with different display devices such as HDMI, DP, or eDP.

5.3.1 MIPI Display Serial Interface (DSI)

The Display Serial Interface (DSI) is a serial bit-stream replacement for the parallel MIPI DPI and DBI display interface standards. DSI reduces package pin-count and I/O power consumption. DSI support enables both display controllers to connect to an external display(s) with a MIPI DSI receiver. The DSI transfers pixel data from the internal display controller to an external third-party LCD module.

Features:

- PHY Layer
  - Start / End of Transmission. Other out-of-band signaling.
  - Per DSI interface: one Clock Lane; two Data Lanes
  - Supports link configuration – 1x 2
  - Maximum link rate 1.5Gbps as per MIPI D-PHY 1.1v version
  - Maximum 10MHz LP receive rate
- Lane Management Layer with Distributor
- Protocol Layer with Packet Constructor
- Supports MIPI DSI 1.0.1v version mandatory features
- Command Mode (One-shot) with Host and/or display controller as master
- Clocks
  - Bit Clock: Serial data stream bit-rate clock
  - Byte Clock: Lane Management Layer Byte-rate clock
  - Application Clock: Protocol Layer Byte-rate clock.
- Error Detection / Correction
  - ECC generation for packet Headers
  - Checksum generation for long packets
- Error recovery
- High-Speed Transmit timer
- Low-Power Receive timer
- Turnaround Acknowledge Timeout

Table 5-4: DSI Pin Descriptions

Pin	Name	Direction	Type	Description
76 78	DSI_CLK_N DSI_CLK_P	Output	MIPI D-PHY	Differential output clock for DSI interface
82 84	DSI_D1_N DSI_D1_P	Output	MIPI D-PHY	Differential data lanes for DSI interface.
70 72	DSI_D0_N DSI_D0_P	Bidirectional	MIPI D-PHY	Differential data lanes for DSI interface. DSI lane can read data back from the panel side in low power (LP) mode.

5.3.2 HDMI and DisplayPort (DP) Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0	> 340MHz pixel clock Scrambling support Clock/4 support (1/40 bit-rate clock)

The HDMI and DP interfaces share the same set of interface pins. A new transport mode was introduced in HDMI 2.0 to enable link clock frequencies greater than 340MHz and up to 600MHz. For transfer rates above 340MHz, there are two main requirements:

- All link data, including active pixel data, guard bands, data islands, and control islands must be scrambled.
- The TMDS clock lane must toggle at CLK/4 instead of CLK. Below 340MHz, the clock lane toggles as normal (independent of the state of scrambling).

Features:

- HDMI
  - HDMI 2.0 mode (3.4Gbps < data rate <= 6Gbps)
  - HDMI 1.4 mode (data rate<=3.4Gbps)
  - Multi-channel audio from HDA controller, up to eight channels 192kHz 24-bit.
  - Vendor Specific Info-frame (VSI) packet transmission
  - 24-bit RGB pixel formats
  - Transition Minimized Differential Signaling (TMDS) functional up to 340MHz pixel clock rate
- DisplayPort
  - Display Port mode: interface is functional up to 540MHz pixel clock rate (i.e., 1.62GHz for RBR, 2.7GHz for HBR, and 5.4GHz for HBR2).
  - 8b/10b encoding support
  - External Dual Mode standard support
- Audio streaming support

Table 5-5: HDMI Pin Descriptions

Pin	Name	Direction	Type	Description
83 81	DP1_TXD3_P DP1_TXD3_N	Differential Output	AC-Coupled on Carrier Board [DP]	DP Data lane 3 or HDMI Differential Clock. AC coupling required on carrier board. For HDMI, pull-downs (with disable) also required on carrier board.
77 75 71 69 65 63	DP1_TXD2_P DP1_TXD2_N DP1_TXD1_P DP1_TXD1_N DP1_TXD0_P DP1_TXD0_N	Differential Output	AC-Coupled on Carrier Board [DP]	HDMI Differential Data lanes 2:0. AC coupling required on carrier board. For HDMI, pull-downs (with disable) also required on carrier board. HDMI: DP1_TXD2_[P,N] = HDMI Lane 0 DP1_TXD1_[P,N] = HDMI Lane 1 DP1_TXD0_[P,N] = HDMI Lane 2
96	DP1_HPD	Input	CMOS – 1.8V [ST]	HDMI Hot Plug detection. Level shifter required as this pin is not 5V tolerant.
94	HDMI_CEC	Bidirectional	Open Drain, 1.8V [DD]	Consumer Electronics Control (CEC) one-wire serial bus. NVIDIA provides low level CEC APIs (read/write). These are not supported in earlier Android releases. For additional CEC support, 3rd party libraries need to be made available.
100	DP1_AUX_P	Bidirectional	Open-Drain, 1.8V (3.3V tolerant - DDC) [DP_AUX]	DDC Serial Clock for HDMI. Level shifter required; pin is not 5V tolerant.
98	DP1_AUX_N	Bidirectional	Open-Drain, 1.8V (3.3V tolerant - DDC)	DDC Serial Data. Level shifter required; pin is not 5V tolerant.

Table 5-6: DisplayPort on DP1 Pin Descriptions

Pin	Name	Direction	Type	Description
83 81 77 75 71 69 65 63	DP1_TXD3_P DP1_TXD3_N DP1_TXD2_P DP1_TXD2_N DP1_TXD1_P DP1_TXD1_N DP1_TXD0_P DP1_TXD0_N	Differential Output	AC-Coupled on Carrier Board [DP]	DisplayPort 1 Differential Data lanes 2:0. AC coupling required on carrier board. DP1_TXD2_[P,N] = DP Lane 2 DP1_TXD1_[P,N] = DP Lane 1 DP1_TXD0_[P,N] = DP Lane 0
96	DP1_HPD	Input	CMOS – 1.8V [ST]	DisplayPort 1 Hot Plug detection. Level shifter required and must be non-inverting.
100 98	DP1_AUX_P DP1_AUX_N	Bidirectional	Open-Drain, 1.8V [DP_AUX]	DisplayPort 1 auxiliary channels. AC coupling required on carrier board.

5.3.3 Embedded DisplayPort (eDP) Interface

Standard	Notes
Embedded DisplayPort 1.4	Supported eDP 1.4 features: > Additional link rates > Enhanced framing > Power sequencing > Reduced aux timing > Reduced main voltage swing

eDP is a mixed-signal interface consisting of four differential serial output lanes and one PLL. This PLL is used to generate a high frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. Embedded DisplayPort (eDP) modes (1.6GHz for RBR, 2.16GHz, 2.43GHz, 2.7GHz for HBR, 3.42GHz, 4.32GHz and 5.4GHz for HBR2).

Note: eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

DisplayPort on DP0 is limited to display functionality only; no HDCP or audio support.

Table 5-7: eDP (or DisplayPort on DP0) Pin Descriptions

Pin	Name	Direction	Type	Description
59 57 53 51 47 45 41 39	DP0_TXD3_P DP0_TXD3_N DP0_TXD2_P DP0_TXD2_N DP0_TXD1_P DP0_TXD1_N DP0_TXD0_P DP0_TXD0_N	Differential Output	AC-Coupled on Carrier Board [DP]	DP0 Differential Data. AC coupling and pull-downs (with disable) required on carrier board. DP0_TXD3_[P,N] = DisplayPort 0 Data Lane 3 DP0_TXD2_[P,N] = DisplayPort 0 Data Lane 2 DP0_TXD1_[P,N] = DisplayPort 0 Data Lane 1 DP0_TXD0_[P,N] = DisplayPort 0 Data Lane 0
88	DP0_HPD	Input	CMOS – 1.8V [ST]	DP0 Hot Plug detection. Level shifter required as this pin is not 5V tolerant
92 90	DP0_AUX_P DP0_AUX_N	Bidirectional	AC-Coupled on Carrier Board [DP_AUX]	DP0 auxiliary channels. AC coupling required on Carrier board.

5.4 MIPI Camera Serial Interface (CSI) / VI (Video Input)

Standard
MIPI CSI 2.0 Receiver specification
MIPI D-PHY® v1.2 Physical Layer specification

The Camera Serial Interface (CSI) is based on MIPI CSI 2.0 standard specification and implements the CSI receiver which receives data from an external camera module with CSI transmitter. The Video Input (VI) block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor (ISP) execution resources.

Features:

- Supports both x4-lane and x2-lane sensor camera configurations:
  - x4 only configuration (up to three active streams)
  - x4 + x2 configurations (up to four active streams)
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b, YUV444-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - DPCM: user defined
  - User defined: JPEG8
  - Embedded: Embedded control information
- Supports single-shot mode
- Physical Interface (MIPI D-PHY) Modes of Operation
  - High Speed Mode – High-speed differential signaling up to 1.5Gbps; burst transmission for low power
  - Low Power Control – Single-ended 1.2V CMOS level; low-speed signaling for handshaking.
  - Low Power Escape – Low-speed signaling for data, used for escape command entry only.

If the two streams come from a single source, then the streams are separated using a filter indexed on different data types. In case of separation using data types, the normal data type is separated from the embedded data type.

Table 5-8: CSI Pin Descriptions

Pin	Name	Direction	Type	Description
10	CSI0_CLK_N	Input	MIPI D-PHY	CSI 0 Clock–
12	CSI0_CLK_P	Input	MIPI D-PHY	CSI 0 Clock+
4	CSI0_D0_N	Input	MIPI D-PHY	CSI 0 Data 0–
6	CSI0_D0_P	Input	MIPI D-PHY	CSI 0 Data 0+

Pin	Name	Direction	Type	Description
16	CSI0_D1_N	Input	MIPI D-PHY	CSI 0 Data 1–
18	CSI0_D1_P	Input	MIPI D-PHY	CSI 0 Data 1+
3	CSI1_D0_N	Input	MIPI D-PHY	CSI 1 Data 0–
5	CSI1_D0_P	Input	MIPI D-PHY	CSI 1 Data 0+
15	CSI1_D1_N	Input	MIPI D-PHY	CSI 1 Data 1–
17	CSI1_D1_P	Input	MIPI D-PHY	CSI 1 Data 1+
28	CSI2_CLK_N	Input	MIPI D-PHY	CSI 2 Clock–
30	CSI2_CLK_P	Input	MIPI D-PHY	CSI 2 Clock+
22	CSI2_D0_N	Input	MIPI D-PHY	CSI 2 Data 0–
24	CSI2_D0_P	Input	MIPI D-PHY	CSI 2 Data 0+
34	CSI2_D1_N	Input	MIPI D-PHY	CSI 2 Data 1–
36	CSI2_D1_P	Input	MIPI D-PHY	CSI 2 Data 1+
27	CSI3_CLK_N	Input	MIPI D-PHY	CSI 3 Clock–
29	CSI3_CLK_P	Input	MIPI D-PHY	CSI 3 Clock+
21	CSI3_D0_N	Input	MIPI D-PHY	CSI 3 Data 0–
23	CSI3_D0_P	Input	MIPI D-PHY	CSI 3 Data 0+
33	CSI3_D1_N	Input	MIPI D-PHY	CSI 3 Data 1–
35	CSI3_D1_P	Input	MIPI D-PHY	CSI 3 Data 1+
52	CSI4_CLK_N	Input	MIPI D-PHY	CSI 4 Clock–
54	CSI4_CLK_P	Input	MIPI D-PHY	CSI 4 Clock+
46	CSI4_D0_N	Input	MIPI D-PHY	CSI 4 Data 0–
48	CSI4_D0_P	Input	MIPI D-PHY	CSI 4 Data 0+
58	CSI4_D1_N	Input	MIPI D-PHY	CSI 4 Data 1–
60	CSI4_D1_P	Input	MIPI D-PHY	CSI 4 Data 1+
40	CSI4_D2_N	Input	MIPI D-PHY	CSI 4 Data 2–
42	CSI4_D2_P	Input	MIPI D-PHY	CSI 4 Data 2+
64	CSI4_D3_N	Input	MIPI D-PHY	CSI 4 Data 3–
66	CSI4_D3_P	Input	MIPI D-PHY	CSI 4 Data 3+

Table 5-9: Camera Clock and Control Pin Descriptions

Pin	Name	I/O	Pin Type	PoR	Description
213	CAM_I2C_SCL	Bidirectional	Open Drain – 3.3V [DD]	z	Camera I2C Clock
215	CAM_I2C_SDA	Bidirectional	Open Drain – 3.3V [DD]	z	Camera I2C Data
116	CAM0_MCLK	Output	CMOS – 1.8V [ST]	PD	Camera 1 Reference Clock
114	CAM0_PWDN	Output	CMOS – 1.8V [ST]	PD	Camera 1 Powerdown or GPIO
122	CAM1_MCLK	Output	CMOS – 1.8V [ST]	PD	Camera 2 Reference Clock
120	CAM1_PWDN	Output	CMOS – 1.8V [ST]	PD	Camera 2 Powerdown or GPIO

5.5 SD / SDIO

Standard	Notes
SD Specifications Part A2 SD Host Controller Standard Specification Version 4.00	
SD Specifications Part 1 Physical Layer Specification Version 4.00	
SD Specifications Part E1 SDIO Specification Version 4.00	Support for SD 4.0 Specification without UHS-II
Embedded Multimedia Card (eMMC), Electrical Standard 5.1	

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is used to support the on-module eMMC and a single SDIO interface made available for use with SDIO peripherals; it supports Default and High-Speed modes.

The SDMMC controller has a direct memory interface and is capable of initiating data transfers between memory and external device. The SDMMC controller supports both the SD and eMMC bus protocol and has an APB slave interface to access configuration registers. Interface is intended for supporting various compatible peripherals with an SD/MMC interface.

Table 5-10: SD/SDIO Controller I/O Capabilities

Controller	Bus Width	Supported Voltages (V)	I/O bus Clock (MHz)	Max Bandwidth (MBps)	Notes
SD/SDIO Card	4	1.8 / 3.3	208	104	Available at connector for SDIO or SD Card use
eMMC	8	1.8	200	400	On-module eMMC

Table 5-11: SD/SDIO Pin Descriptions

Pin	Name	I/O	Pin Type	PoR	Description
229	SDMMC_CLK	Output	CMOS – 1.8V / 3.3V [CZ]	PD	SDIO/MMC Clock
227	SDMMC_CMD	Bidirectional	CMOS – 1.8V / 3.3V [CZ]	PU	SDIO/MMC Command
225 223 221 219	SDMMC_DAT3 SDMMC_DAT2 SDMMC_DAT1 SDMMC_DAT0	Bidirectional	CMOS – 1.8V / 3.3V [CZ]	PU	SDIO/MMC Data bus
Note:	Pin voltage is determined by LDO on module setting.				

5.6 Inter-IC Sound (I^2S)

Standard
Inter-IC Sound (I^2S) specification

The I^2S controller transports streaming audio data between system memory and an audio codec. The I^2S controller supports I^2S format, Left-justified Mode format, Right-justified Mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I^2S) bus specification.

The I^2S and PCM (master and slave modes) interfaces support clock rates up to 24.5760MHz.

The I^2S controller supports point-to-point serial interfaces for the I^2S digital audio streams. I^2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, and those with digital TV sound may be directly connected to the I^2S controller. The controller also supports the Pulse-Code-Modulation and telephony mode of data-transfer. Pulse-Code-Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. The Telephony mode is used to transmit and receive data to and from an external mono CODEC in a slot-based scheme of time-division multiplexing (TDM). The I^2S controller supports bidirectional audio streams and can operate in half-duplex or full-duplex mode.

Features:

- Basic I^2S modes to be supported (I^2S, RJM, LJM and DSP) in both Master and Slave modes.
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both master and slave modes.
- NW-mode with independent slot-selection for both Tx and Rx
- TDM mode with flexibility in number of slots and slot(s) selection.
- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream.

Table 5-12: Audio Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
211	GPIO09	Output	CMOS – 1.8V [ST]	PD	Audio Codec Master Clock (AUD_MCLK)
195	I2S0_DIN	Input	CMOS – 1.8V [CZ]	PD	I²S Audio Port 0 Data In
193	I2S0_DOUT	Output	CMOS – 1.8V [CZ]	PD	I²S Audio Port 0 Data Out
197	I2S0_FS	Bidirectional	CMOS – 1.8V [CZ]	PD	I²S Audio Port 0 Frame Select (Left/Right Clock)
199	I2S0_SCLK	Bidirectional	CMOS – 1.8V [CZ]	PD	I²S Audio Port 0 Clock
222	I2S1_DIN	Input	CMOS – 1.8V [ST]	PD	I²S Audio Port 1 Data In
220	I2S1_DOUT	Output	CMOS – 1.8V [ST]	PD	I²S Audio Port 1 Data Out
224	I2S1_FS	Bidirectional	CMOS – 1.8V [ST]	PD	I²S Audio Port 1 Frame Select (Left/Right Clock)
226	I2S1_SCLK	Bidirectional	CMOS – 1.8V [ST]	PD	I²S Audio Port 1 Clock

5.7 Miscellaneous Interfaces

5.7.1 Inter-Chip Communication (I2C)

Standard
NXP inter-IC-bus (I²C) specification

This general purpose I²C controller allows system expansion for I²C -based devices as defined in the NXP inter-IC-bus (I²C) specification. The I²C bus supports serial device communications to multiple devices; the I²C controller handles clock source negotiation, speed negotiation for standard and fast devices, 7-bit slave address support according to the I²C protocol and supports master and slave mode of operation.

The I²C controller supports the following operating modes: Master – Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s); Slave – Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s).

Table 5-13: I2C Pin Descriptions

Pin	Name	I/O	Pin Type	PoR	Description
185 187	I2C0_SCL I2C0_SDA	Bidirectional	Open Drain – 3.3V [DD]	z z	Only 3.3V devices supported without level shifter. I²C 0 Clock/Data pins. On module 2.2kΩ pull-up to 3.3V.
189 191	I2C1_SCL I2C1_SDA	Bidirectional	Open Drain – 3.3V [DD]	z z	Only 3.3V devices supported without level shifter. I²C 1 Clock/Data pins. On module 2.2kΩ pull-up to 3.3V.

Pin	Name	I/O	Pin Type	PoR	Description
232 234	I2C2_SCL I2C2_SDA	Bidirectional	Open Drain – 1.8V [DD]	z z	Only 1.8V devices supported without level shifter. I²C 2 Clock/Data pins. On module 2.2kΩ pull-up to 1.8V.
213 215	CAM_I2C_SCL CAM_I2C_SDA	Bidirectional	Open Drain – 3.3V [DD]	z z	Only 3.3V devices supported without level shifter. Camera I²C Clock/Data pins. On module 4.7kΩ pull-up to 3.3V.

5.7.2 Serial Peripheral Interface (SPI)

The SPI controllers operate up to 65Mbps in master mode and 45Mbps in slave mode. It allows a duplex, synchronous, serial communication between the controller and external peripheral devices. It consists of four signals, SS_N (Chip select), SCK (clock), MOSI (Master data out and Slave data in) and MISO (Slave data out and master data in). The data is transferred on MOSI or MISO based on the data transfer direction on every SCK edge. The receiver always receives the data on the other edge of SCK.

Features:

- Independent Rx FIFO and Tx FIFO.
- Software controlled bit-length supports packet sizes of 1 to 32 bits.
- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size).
- SS_N can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries.
- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO).
- Simultaneous receive and transmit supported.
- Supports Master mode. Slave mode has not been validated.

Table 5-14: SPI Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
95	SPI0_CS0*	Bidirectional	CMOS – 1.8V [LV-CZ]	PU	SPI 0 Chip Select 0
97	SPI0_CS1*	Bidirectional	CMOS – 1.8V [LV-CZ]	PU	SPI 0 Chip Select 1
93	SPI0_MISO	Bidirectional	CMOS – 1.8V [LV-CZ]	PD	SPI 0 Master In / Slave Out
89	SPI0_MOSI	Bidirectional	CMOS – 1.8V [LV-CZ]	PD	SPI 0 Master Out / Slave In
91	SPI0_SCK	Bidirectional	CMOS – 1.8V [LV-CZ]	PD	SPI 0 Clock
110	SPI1_CS0*	Bidirectional	CMOS – 1.8V [CZ]	PU	SPI 1 Chip Select 0
112	SPI1_CS1*	Bidirectional	CMOS – 1.8V [CZ]	PU	SPI 1 Chip Select 1
108	SPI1_MISO	Bidirectional	CMOS – 1.8V [CZ]	PD	SPI 1 Master In / Slave Out
104	SPI1_MOSI	Bidirectional	CMOS – 1.8V [CZ]	PD	SPI 1 Master Out / Slave In
106	SPI1_SCK	Bidirectional	CMOS – 1.8V [CZ]	PD	SPI 1 Clock

Figure 5-1: SPI Master Timing Diagram

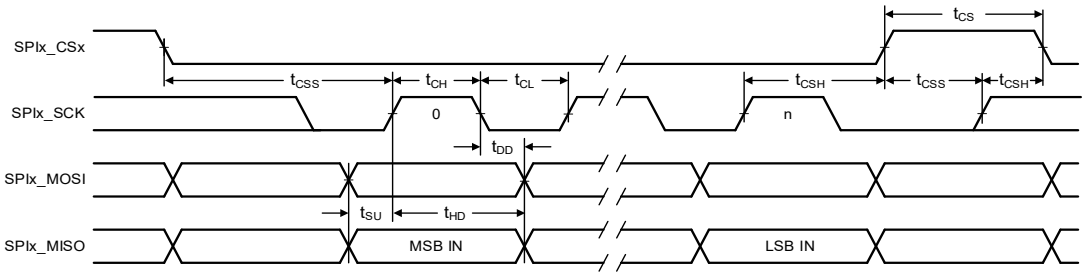


Table 5-15: SPI Master Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Fsck	SPIx_SCK clock frequency		65	MHz
Psck	SPIx_SCK period	1/Fsck		ns
t_{CH}	SPIx_SCK high time	50%Psck -10%	50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%	50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1		V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1		V/ns
t_{SU}	SPIx_MISO setup to SPIx_SCK rising edge	2		ns
t_{HD}	SPIx_MISO hold from SPIx_SCK rising edge	3		ns
t_{DD}	SPIx_MOSI delay from SPIx_SCK falling edge	0	4	ns
t_{CSS}	SPIx_CSx setup time	2		ns
t_{CSH}	SPIx_CSx hold time	3		ns
t_{CS}	SPIx_CSx high time	10		ns
Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.				

Figure 5-2: SPI Slave Timing Diagram

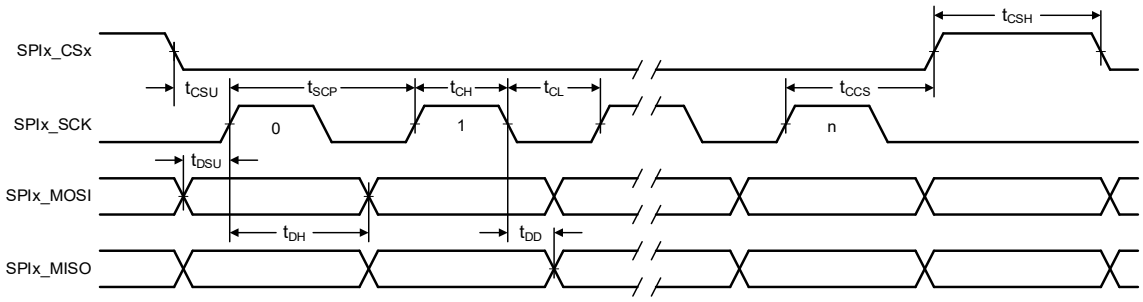


Table 5-16: SPI Slave Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{DD}+ t_{MSU}[1])$		ns
t_{CH}	SPIx_SCK high time	$t_{DD} + t_{MSU}[1]$		ns
t_{CL}	SPIx_SCK low time	$t_{DD} + t_{MSU}[1]$		ns
t_{CSU}	SPIx_CSx setup time	1		t_{SCP}
t_{CSH}	SPIx_CSx high time	1		t_{SCP}
t_{CCS}	SPIx_SCK rising edge to SPIx_CSx rising edge	1	1	t_{SCP}
t_{DSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1	1	ns
t_{DH}	SPIx_MOSI hold from SPIx_SCK rising edge[2]	2	11	ns

1. t_{MSU} is the setup time required by the external master.
2. Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

5.7.3 UART

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Note: The UART receiver input has low baud rate tolerance in 1-stop bit mode. External devices must use 2 stop bits.

In 1-stop bit mode, the Tegra UART receiver can lose sync between Tegra receiver and the external transmitter resulting in data errors/corruption. In 2-stop bit mode, the extra stop bit allows the Tegra UART receiver logic to align properly with the UART transmitter.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200MHz, baud rate of 12.5Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both Tx and Rx
- 8-bit x 36 deep Tx FIFO
- 11-bit x 36 deep Rx FIFO. Three bits of 11 bits per entry log the Rx errors in FIFO mode (break, framing, and parity errors as bits 10, 9, 8 of FIFO entry)

- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 5-17: UART Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
99	UART0_TXD	Output	CMOS – 1.8V [ST]	PD	UART 0 Transmit
101	UART0_RXD	Input	CMOS – 1.8V [ST]	PU	UART 0 Receive
103	UART0_RTS*	Output	CMOS – 1.8V [ST]	PD	UART 0 Request to Send
105	UART0_CTS*	Input	CMOS – 1.8V [ST]	PD	UART 0 Clear to Send
203	UART1_TXD	Output	CMOS – 1.8V [ST]	PD	UART 1 Transmit
205	UART1_RXD	Input	CMOS – 1.8V [ST]	PD	UART 1 Receive
207	UART1_RTS*	Output	CMOS – 1.8V [ST]	PD	UART 1 Request to Send
209	UART1_CTS*	Input	CMOS – 1.8V [ST]	PD	UART 1 Clear to Send
236	UART2_TXD	Output	CMOS – 1.8V [ST]	PD	UART 2 Transmit
238	UART2_RXD	Input	CMOS – 1.8V [ST]	PD	UART 2 Receive

5.7.4 Gigabit Ethernet

The Jetson Nano integrates a Realtek RTL81119ICG Gigabit Ethernet controller. The on-module Ethernet controller supports:

- 10/100/1000 Mbps Gigabit Ethernet
- IEEE 802.3u Media Access Controller (MAC)

Table 5-18: Gigabit Ethernet Pin Descriptions

Pin	Name	Direction	Type	Description
194	GBE_LED_ACT	Output		Activity LED (yellow) enable
188	GBE_LED_LINK	Output		Link LED (green) enable. Link LED only illuminates if link established is 1000. 100/10 will not cause the Link LED to light up.
184 186	GBE_MDI0_N GBE_MDI0_P	Bidirectional	MDI	GbE Transformer Data 0
190 192	GBE_MDI1_N GBE_MDI1_P	Bidirectional	MDI	GbE Transformer Data 1

Pin	Name	Direction	Type	Description
196 198	GBE_MDI2_N GBE_MDI2_P	Bidirectional	MDI	GbE Transformer Data 2
202 204	GBE_MDI3_N GBE_MDI3_P	Bidirectional	MDI	GbE Transformer Data 3

5.7.5 Fan

The Jetson Nano includes PWM and Tachometer functionality to enable fan control as part of a thermal solution. The Pulse Width Modulator (PWM) controller is a frequency divider with a varying pulse width. The PWM runs off a device clock programmed in the Clock and Reset controller and can be any frequency up to the device clock maximum speed of 48MHz. The PWFM gets divided by 256 before being subdivided based on a programmable value.

Table 5-19: Fan Pin Descriptions

Pin	Name	Direction	Type	PoR	Description
230	GPIO14	Output	CMOS – 1.8V [ST]	PD	Fan PWM
208	GPIO08	Input	CMOS – 1.8V [ST]	PD	Fan Tachometer

5.7.6 Debug

A debug interface is supported via JTAG on-module test points or serial interface over UART1. The JTAG interface can be used for SCAN testing or communicating with integrated CPU**.** See the *NVIDIA Jetson Nano Product Design Guide* for more information**.**

Table 5-20: Debug Pin Descriptions

Pin	Name	I/O	Pin Type	PoR	Description
-	JTAG_RTCK	Output	CMOS – 1.8V [JT_RST]	0	Return Test Clock
-	JTAG_TCK	Input	CMOS – 1.8V [JT_RST]	z	Test Clock
-	JTAG_TDI	Input	CMOS – 1.8V [JT_RST]	PU	Test Data In
-	JTAG_TDO	Output	CMOS – 1.8V [ST]	z	Test Data Out
-	JTAG_TMS	Input	CMOS – 1.8V [JT_RST]	PU	Test Mode Select
-	JTAG_GP0	Input	CMOS – 1.8V [JT_RST]	PD	Test Reset
236	UART2_TXD	Output	CMOS – 1.8V [ST]	PD	Debug UART Transmit
238	UART2_RXD	Input	CMOS – 1.8V [ST]	PD	Debug UART Receive

Chapter 6. Electrical, Mechanical, and Thermal Characteristics

6.1 Operating and Absolute Maximum Ratings

The parameters listed in following table are specific to a temperature range and operating voltage. Operating the Jetson Nano module beyond these parameters is not recommended. Exceeding these conditions for extended periods may adversely affect device reliability.

> ⚠ **Warning:** Exceeding the listed conditions may damage and/or affect long-term reliability of the part. The Jetson Orin Nano 8GB module should never be subjected to conditions extending beyond the ratings listed below

Table 6-1: Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_{DC}	VDD_IN	4.75	5.0	5.25	V
	PMIC_BBAT	1.65	-	5.5	V

Absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, no guarantee is made and device reliability may be affected. It is not recommended to operate the Jetson Nano module under these conditions.

Table 6-2: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VDD_{MAX}	VDD_IN	-0.5	5.5	V	
	PMIC_BBAT	-0.3	6.0	V	
IDD_{MAX}	VDD_IN Imax	-	5	A	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	VDD + 0.5V when SYS_RESET* is high and associated I/O rail powered. I/O pins

Symbol	Parameter	Minimum	Maximum	Unit	Notes
					cannot be high (>0.5V) before SYS_RESET* goes high. When SYS_RESET* is low, the maximum voltage applied to any I/O pin is 0.5V
	DD pins configured as open drain	-0.5	3.63	V	The pin's output-driver must be set to open-drain mode
T_{OP}	Operating Temperature	-25	97	°C	See the *Jetson Nano Thermal Design Guide* for details.
T_{STG}	Storage Temperature (ambient)	-40	80	°C	
M_{MAX}	Mounting Force		4.0	kgf	kilogram-force (kgf). Maximum force applied to PCB. See the *Jetson Nano Thermal Design Guide* for additional details on mounting a thermal solution.

6.2 Storage and Handling

Table 6-3: Typical Handling and Storage Environment

Parameter	Description
Storage temperature (ambient)[1]	18°C to 30°C
Storage humidity	30% to 70% RH
Storage life[2]	5 years from NVIDIA shipment date to customers

Notes:

- Transportation is a limited range of time that is covered by AEC grade 3 specs (-40°C to 85°C). Longer term storage at hubs, distribution points, and warehousing where climate controls are in place should follow conditions mentioned above.
- Duration based on product being packed and stored in a controlled environment without power on.

6.3 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 6-4: CMOS Pin Type DC Characteristics

Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	-	V

Table 6-5: Open Drain Pin Type DC Characteristics

Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.2 x VDD	V
V_{IH}	Input High Voltage	0.8 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
	I2C[1,0] Output Low Voltage (I_{OL} = 2mA) (see note)	-	0.3 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.7 x VDD	-	V
Note: I2C[1,0]_[SCL, SDA] pins pull-up to 3.3V through on module 2.2kΩ resistor. I2C2_[SCL, SDA] pins pull-up to 1.8V through on module 2.2kΩ resistor.				

6.4 Environmental and Mechanical Screening

Module performance was assessed against a series of industry standard tests designed to evaluate robustness and estimate the failure rate of an electronic assembly in the environment in which it will be used. Mean Time Between Failures (MTBF) calculations are produced in the design phase to predict a product's future reliability in the field.

Table 6-6: Jetson Nano Reliability Report

Test	Reference Standards / Test Conditions
Temperature Humidity Biased	JESD22-A101 85°C / 85% RH, 168 hours, Power ON
Temperature Cycling	JESD22-A104, IPC9701 -40°C to 105°C, 250 cycles, non-operational
Humidity Steady State	NVIDIA Standard 45°C 90% RH 336hrs, operational
Mechanical Shock – 140G	JESD22-B110 140G, half sine, 1 shock/orientation, 6 orientations total, non-operational

Test	Reference Standards / Test Conditions
Mechanical Shock – 50G	IEC600068-2-27 50G, half sine,1 shock/orientation, 6 orientations total, operational
Connector Insertion Cycling	EIA-364 30 cycles
Sine Vibration – 3G	IEC60068-2-6 3G, 10-500 Hz, 1 sweep/axis, 3 axes total, non-operational
Random Vibration – 2G	IEC60068-2-64 10-500 Hz, 2 Grms,1 hour/axis, non-operational
Random Vibration – 1G	IEC60068-2-64 10-500 Hz, 1 Grms,1 hour/axis, operational
Hard Boot	NVIDIA Standard Power ON/OFF, ON for 150 sec OFF for 30 sec 1000 cycles at 25°C, 1000 cycles at -40°C
Operational Low Temp	NVIDIA Standard -5°C, 24 hours, operational
Operational High Temp	NVIDIA Standard 40°C, 90%RH, 168 hours, operational
MTBF / Failure Rate: 3,371K Hours	Telcordia SR-332, ISSUE 3 Parts Count (Method I) Controlled Environment (GB), T = 35°C, CL = 90%
MTBF / Failure Rate: 1,836K Hours	Telcordia SR-332, ISSUE 3 Parts Count (Method I) Uncontrolled Environment (GF), T = 35°C, CL = 90%
MTBF / Failure Rate: 957K Hours	Telcordia SR-332, ISSUE 3 Parts Count (Method I) Uncontrolled Environment (GM), T = 35°C, CL = 90%

6.5 Pinout

Signal Name	Pin # Top Odd	Pin # Bottom Even	Signal Name
GND	1	2	GND
CSI1_D0_N	3	4	CSI0_D0_N
CSI1_D0_P	5	6	CSI0_D0_P
GND	7	8	GND
RSVD	9	10	CSI0_CLK_N
RSVD	11	12	CSI0_CLK_P
GND	13	14	GND
CSI1_D1_N	15	16	CSI0_D1_N
CSI1_D1_P	17	18	CSI0_D1_P
GND	19	20	GND
CSI3_D0_N	21	22	CSI2_D0_N
CSI3_D0_P	23	24	CSI2_D0_P
GND	25	26	GND
CSI3_CLK_N	27	28	CSI2_CLK_N
CSI3_CLK_P	29	30	CSI2_CLK_P
GND	31	32	GND
CSI3_D1_N	33	34	CSI2_D1_N
CSI3_D1_P	35	36	CSI2_D1_P
GND	37	38	GND
DP0_TXD0_N	39	40	CSI4_D2_N
DP0_TXD0_P	41	42	CSI4_D2_P
GND	43	44	GND
DP0_TXD1_N	45	46	CSI4_D0_N
DP0_TXD1_P	47	48	CSI4_D0_P
GND	49	50	GND
DP0_TXD2_N	51	52	CSI4_CLK_N
DP0_TXD2_P	53	54	CSI4_CLK_P
GND	55	56	GND
DP0_TXD3_N	57	58	CSI4_D1_N
DP0_TXD3_P	59	60	CSI4_D1_P
GND	61	62	GND
DP1_TXD0_N	63	64	CSI4_D3_N
DP1_TXD0_P	65	66	CSI4_D3_P
GND	67	68	GND
DP1_TXD1_N	69	70	DSI_D0_N

Signal Name	Pin # Top Odd	Pin # Bottom Even	Signal Name
PCIE0_RX0_P	133	134	PCIE0_TX0_N
GND	135	136	PCIE0_TX0_P
PCIE0_RX1_N	137	138	GND
PCIE0_RX1_P	139	140	PCIE0_TX1_N
GND	141	142	PCIE0_TX1_P
RSVD	143	144	GND
KEY	KEY	KEY	KEY
RSVD	145	146	GND
GND	147	148	PCIE0_TX2_N
PCIE0_RX2_N	149	150	PCIE0_TX2_P
PCIE0_RX2_P	151	152	GND
GND	153	154	PCIE0_TX3_N
PCIE0_RX3_N	155	156	PCIE0_TX3_P
PCIE0_RX3_P	157	158	GND
GND	159	160	PCIE0_CLK_N
USBSS_RX_N	161	162	PCIE0_CLK_P
USBSS_RX_P	163	164	GND
GND	165	166	USBSS_TX_N
RSVD	167	168	USBSS_TX_P
RSVD	169	170	GND
GND	171	172	RSVD
RSVD	173	174	RSVD
RSVD	175	176	GND
GND	177	178	MOD_SLEEP*
PCIE_WAKE*	179	180	PCIE0_CLKREQ*
PCIE0_RST*	181	182	RSVD
RSVD	183	184	GBE_MDI0_N
I2C0_SCL	185	186	GBE_MDI0_P
I2C0_SDA	187	188	GBE_LED_LINK
I2C1_SCL	189	190	GBE_MDI1_N
I2C1_SDA	191	192	GBE_MDI1_P
I2S0_DOUT	193	194	GBE_LED_ACT
I2S0_DIN	195	196	GBE_MDI2_N
I2S0_FS	197	198	GBE_MDI2_P
I2S0_SCLK	199	200	GND

Signal Name	Pin # Top Odd	Pin # Bottom Even	Signal Name
DP1_TXD1_P	71	72	DSI_D0_P
GND	73	74	GND
DP1_TXD2_N	75	76	DSI_CLK_N
DP1_TXD2_P	77	78	DSI_CLK_P
GND	79	80	GND
DP1_TXD3_N	81	82	DSI_D1_N
DP1_TXD3_P	83	84	DSI_D1_P
GND	85	86	GND
GPIO0	87	88	DP0_HPD
SPI0_MOSI	89	90	DP0_AUX_N
SPI0_SCK	91	92	DP0_AUX_P
SPI0_MISO	93	94	HDMI_CEC
SPI0_CS0*	95	96	DP1_HPD
SPI0_CS1*	97	98	DP1_AUX_N
UART0_TXD	99	100	DP1_AUX_P
UART0_RXD	101	102	GND
UART0_RTS*	103	104	SPI1_MOSI
UART0_CTS*	105	106	SPI1_SCK
GND	107	108	SPI1_MISO
USB0_D_N	109	110	SPI1_CS0*
USB0_D_P	111	112	SPI1_CS1*
GND	113	114	CAM0_PWDN
USB1_D_N	115	116	CAM0_MCLK
USB1_D_P	117	118	GPIO01
GND	119	120	CAM1_PWDN
USB2_D_N	121	122	CAM1_MCLK
USB2_D_P	123	124	GPIO02
GND	125	126	GPIO03
GPIO04	127	128	GPIO05
GND	129	130	GPIO06
PCIE0_RX0_N	131	132	GND

Signal Name	Pin # Top Odd	Pin # Bottom Even	Signal Name
GND	201	202	GBE_MDI3_N
UART1_TXD	203	204	GBE_MDI3_P
UART1_RXD	205	206	GPIO07
UART1_RTS*	207	208	GPIO08
UART1_CTS*	209	210	CLK_32K_OUT
GPIO09	211	212	GPIO10
CAM_I2C_SCL	213	214	FORCE_RECOVERY*
CAM_I2C_SDA	215	216	GPIO11
GND	217	218	GPIO12
SDMMC_DAT0	219	220	I2S1_DOUT
SDMMC_DAT1	221	222	I2S1_DIN
SDMMC_DAT2	223	224	I2S1_FS
SDMMC_DAT3	225	226	I2S1_SCLK
SDMMC_CMD	227	228	GPIO13
SDMMC_CLK	229	230	GPIO14
GND	231	232	I2C2_SCL
SHUTDOWN_REQ*	233	234	I2C2_SDA
PMIC_BBAT	235	236	UART2_TXD
POWER_EN	237	238	UART2_RXD
SYS_RESET*	239	240	SLEEP/WAKE*
GND	241	242	GND
GND	243	244	GND
GND	245	246	GND
GND	247	248	GND
GND	249	250	GND
VDD_IN	251	252	VDD_IN
VDD_IN	253	254	VDD_IN
VDD_IN	255	256	VDD_IN
VDD_IN	257	258	VDD_IN
VDD_IN	259	260	VDD_IN

6.6 Package Drawing and Dimensions

Table 6-7: Module Dimensions

Description	Minimum	Typical	Maximum	Unit
Connector to opposite side	-	-	45	mm
Side (perpendicular to connector) to opposite side	-	-	69.6	mm
SoC height	1.36	1.51	1.66	mm

Figure 6-1: Module Top and Side View with Cover Outline

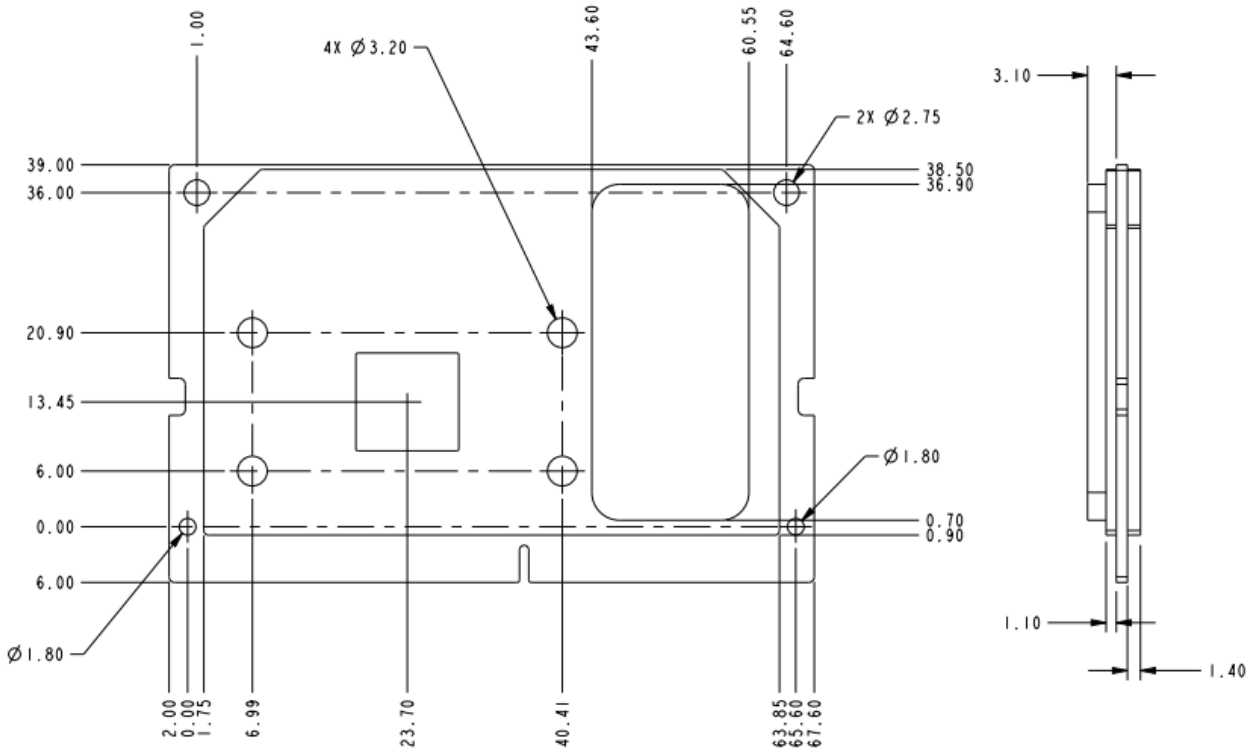


Figure 6-2: Module Bottom with Cover Outline

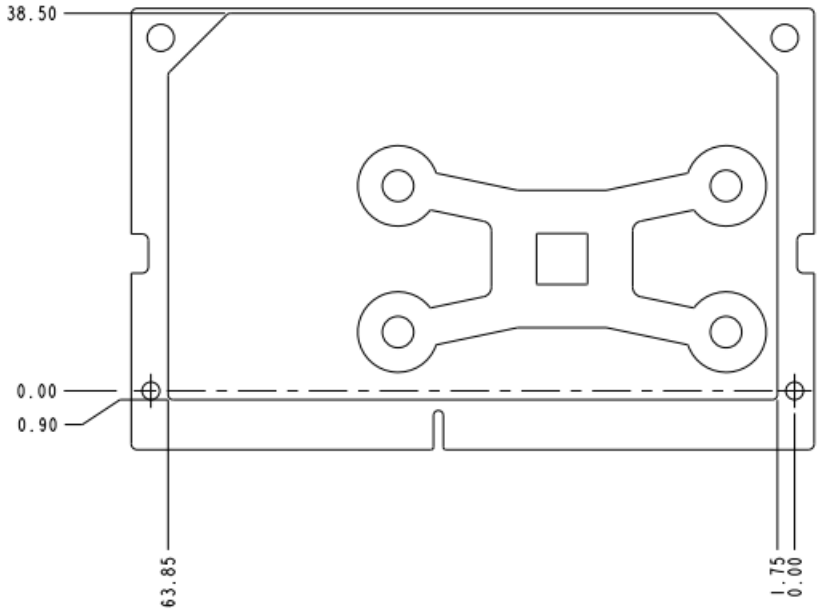


Figure 6-3: Module Top Showing DRAM Placement and Side View

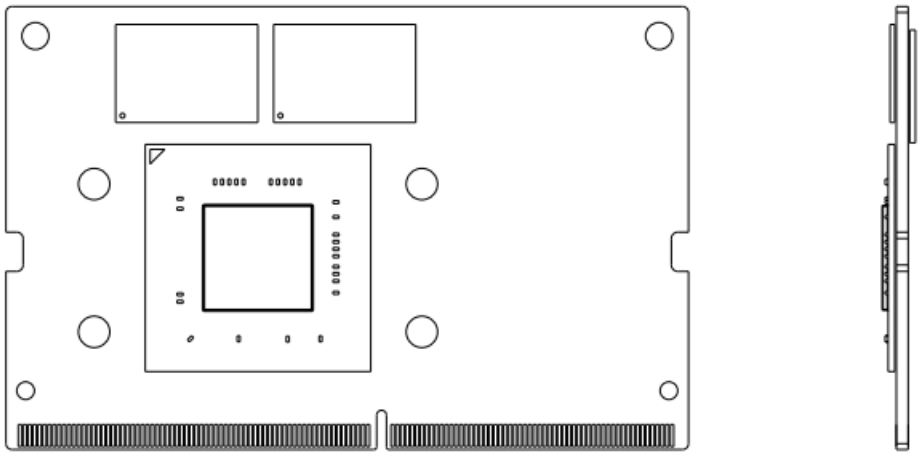
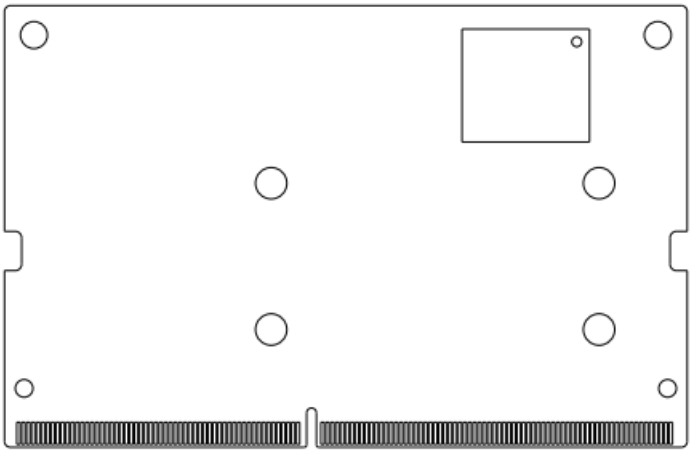


Figure 6-4: Module Bottom Showing EMMC Placement



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