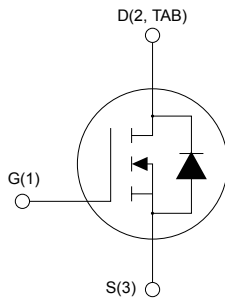
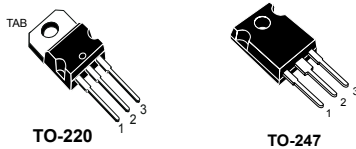


## N-channel 650 V, 198 mΩ typ., 15 A MDmesh M5 Power MOSFETs in a TO-220 and TO-247 packages

### Features



AM01475v1\_noZen

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP18N65M5	650 V	220 mΩ	15 A
STW18N65M5			

- Higher  $V_{DSS}$  rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low  $R_{DS(on)}$
- 100% avalanche tested

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.



#### Product status links

[STP18N65M5](#)

[STW18N65M5](#)

#### Product summary

Order code	STP18N65M5
Marking	18N65M5
Package	TO-220
Packing	Tube
Order code	STW18N65M5
Marking	18N65M5
Package	TO-247
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9.4	
$I_{DM}^{(1)}$	Drain current (pulsed)	60	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Maximum operating junction temperature	150	$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 15\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220FP	TO-247	
$R_{thJC}$	Thermal resistance, junction-to-case	1.14		$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	50	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	210	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$	-	-	$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 7.5\text{ A}$	-	198	220	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1240	-	pF
$C_{oss}$	Output capacitance		-	32	-	pF
$C_{rss}$	Reverse transfer capacitance		-	3.2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	99	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	30	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 7.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 15. Test circuit for gate charge behavior)	-	31	-	nC
$Q_{gs}$	Gate-source charge		-	8	-	nC
$Q_{gd}$	Gate-drain charge		-	14	-	nC

- $C_{o(tr)}$  is an equivalent capacitance that provides the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.
- $C_{o(er)}$  is an equivalent capacitance that provides the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 9.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	36	-	ns
$t_{r(v)}$	Voltage rise time		-	7	-	ns
$t_{f(i)}$	Current fall time	(see the Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	9	-	ns
$t_{c(off)}$	Crossing time		-	11	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-	-	1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	290	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$	-	3.4	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	23.5	-	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 15 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,	-	352	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	4	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	24	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

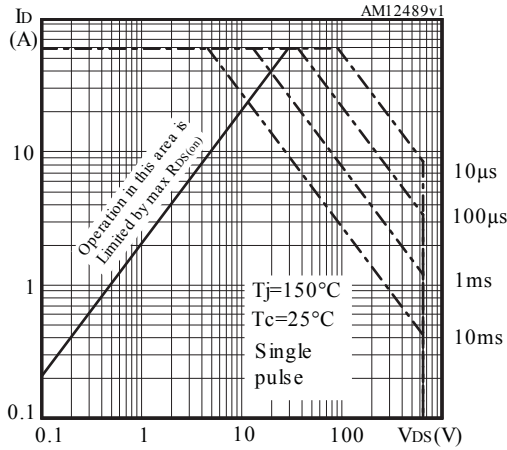


Figure 2. Normalized transient thermal impedance

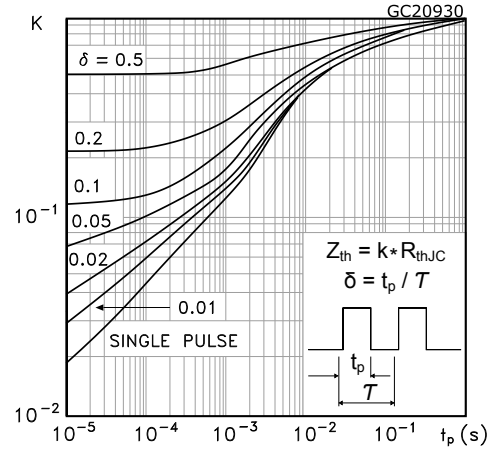


Figure 3. Typical output characteristics

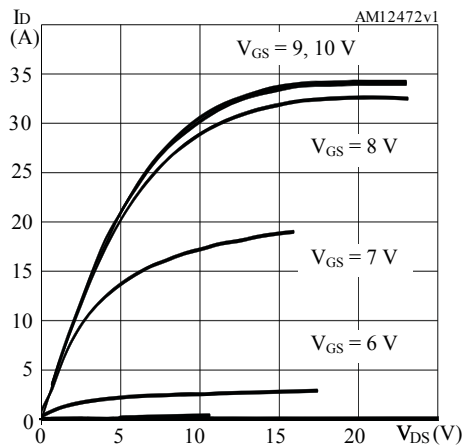


Figure 4. Typical transfer characteristics

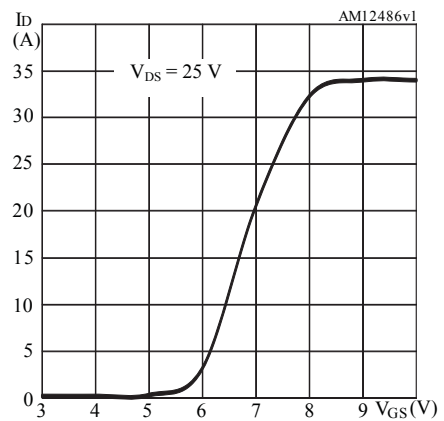


Figure 5. Typical gate charge characteristics

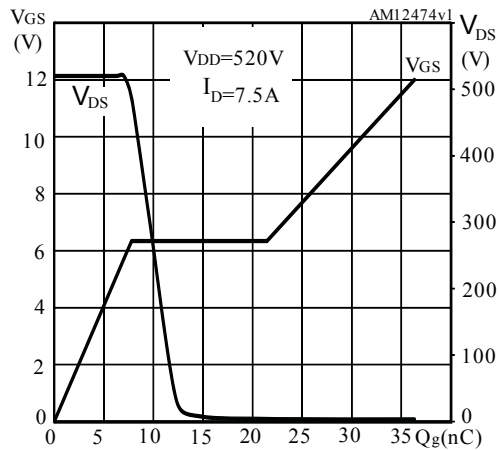


Figure 6. Typical drain-source on-resistance

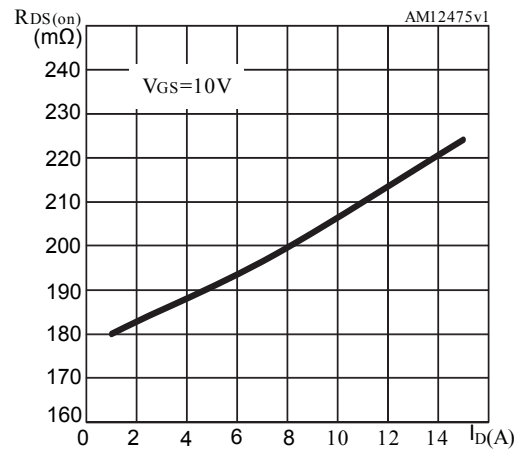


Figure 7. Typical capacitance characteristics

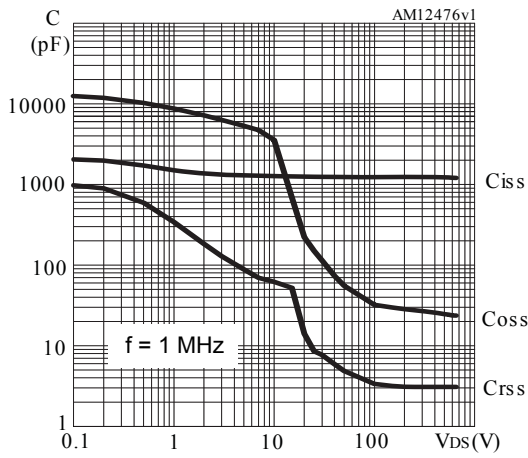


Figure 8. Typical output capacitance stored energy

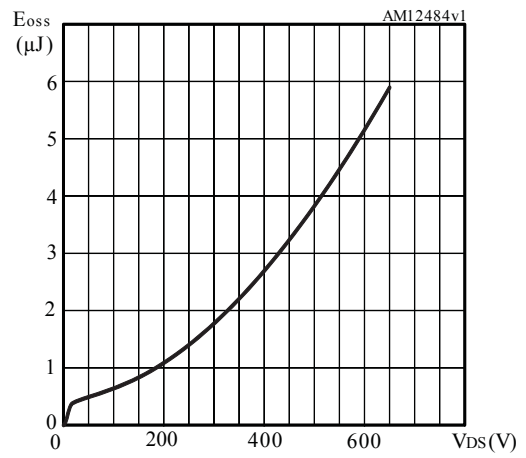


Figure 9. Normalized gate threshold vs temperature

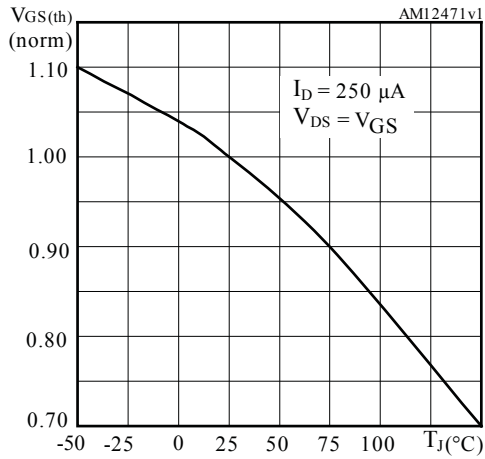


Figure 10. Normalized on-resistance vs temperature

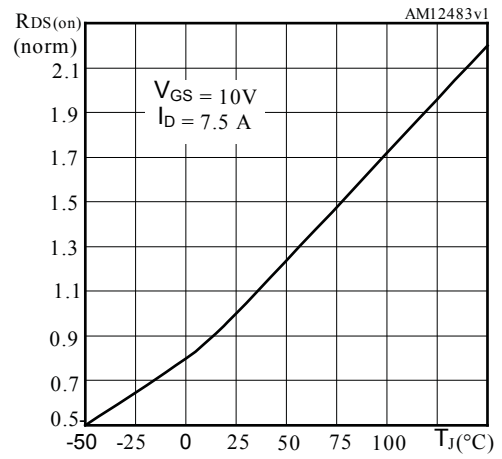


Figure 11. Typical reverse diode forward characteristics

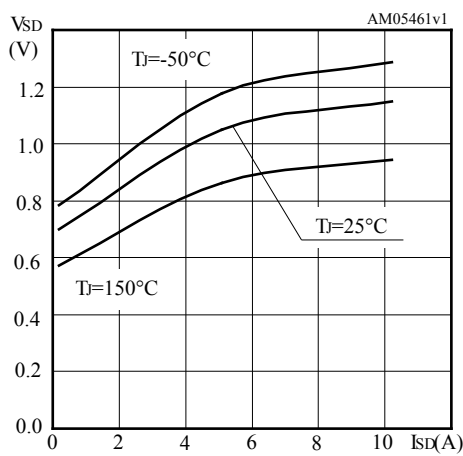


Figure 12. Normalized breakdown voltage vs temperature

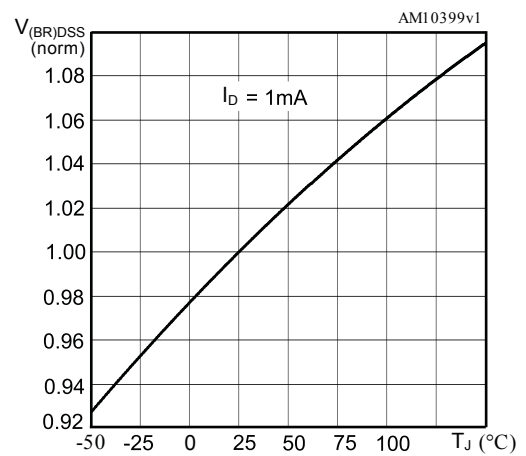
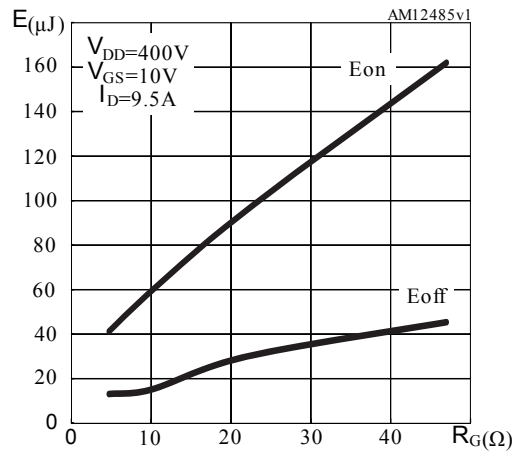
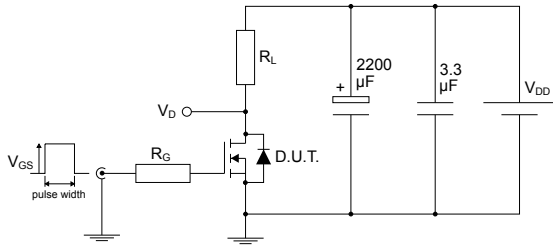


Figure 13. Typical switching energy vs gate resistance

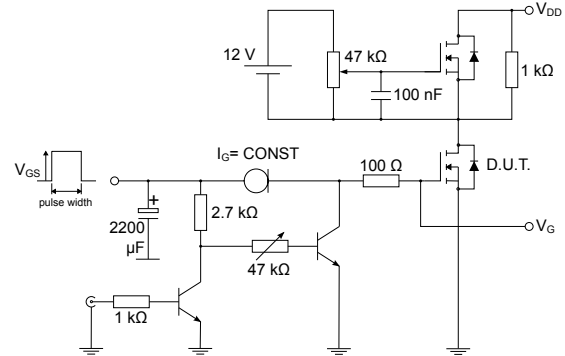


Note:  $E_{on}$  including reverse recovery of a SiC diode.

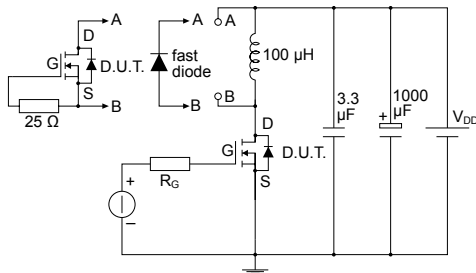
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


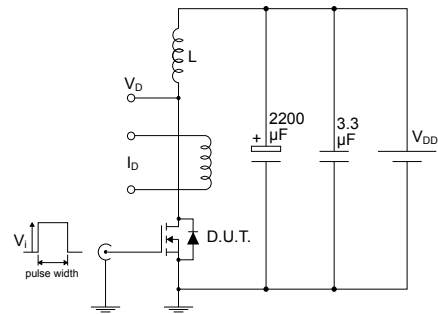
AM01468v1

**Figure 15. Test circuit for gate charge behavior**


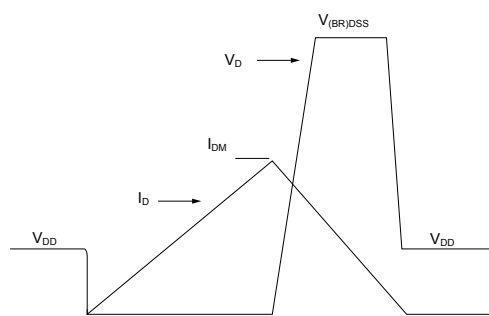
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


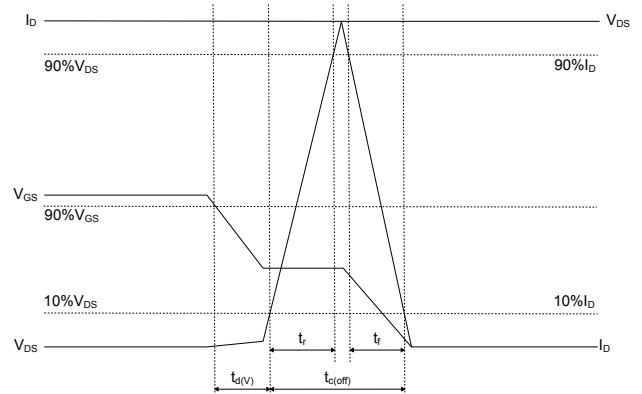
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**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


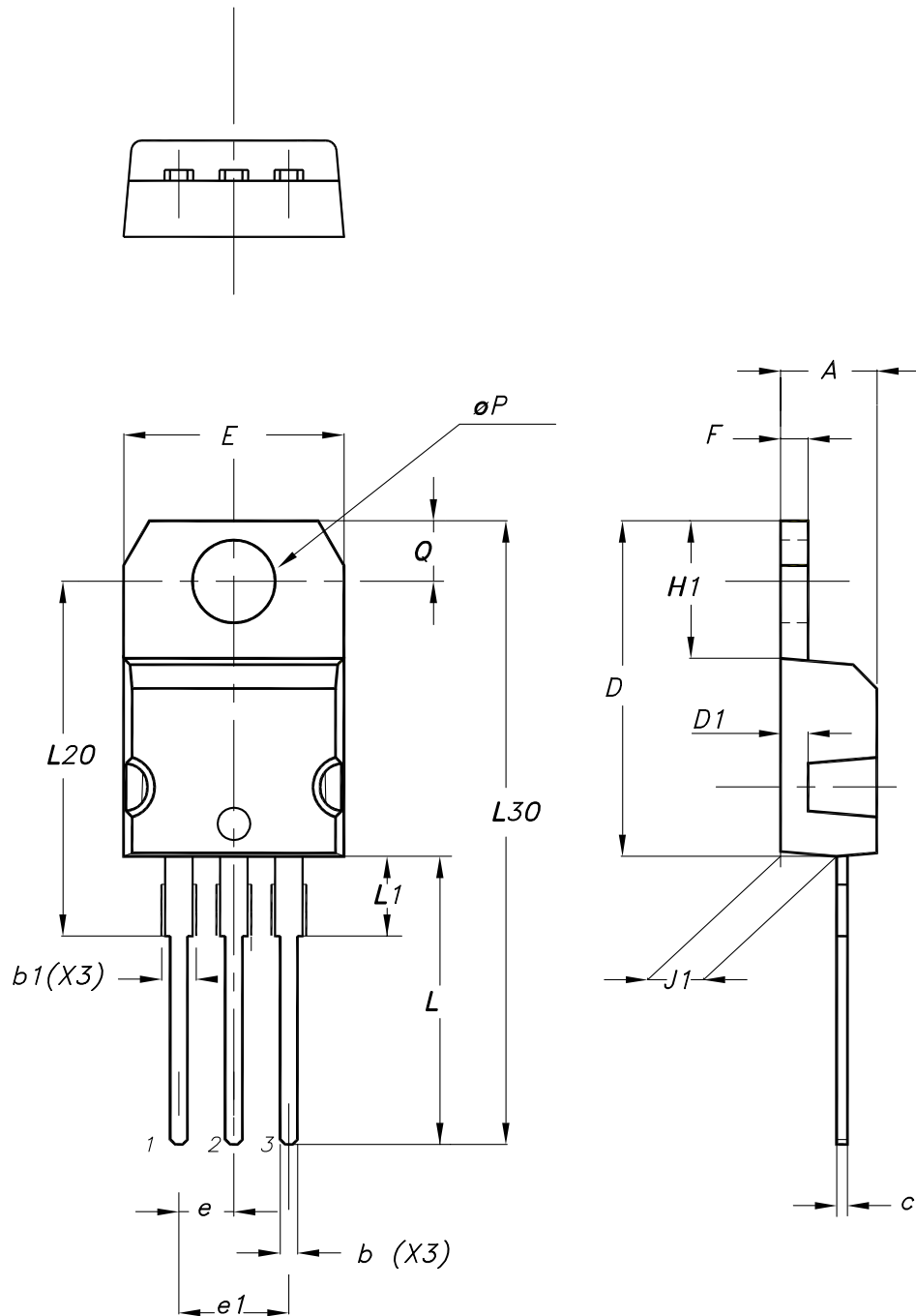
AM05540v2

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline



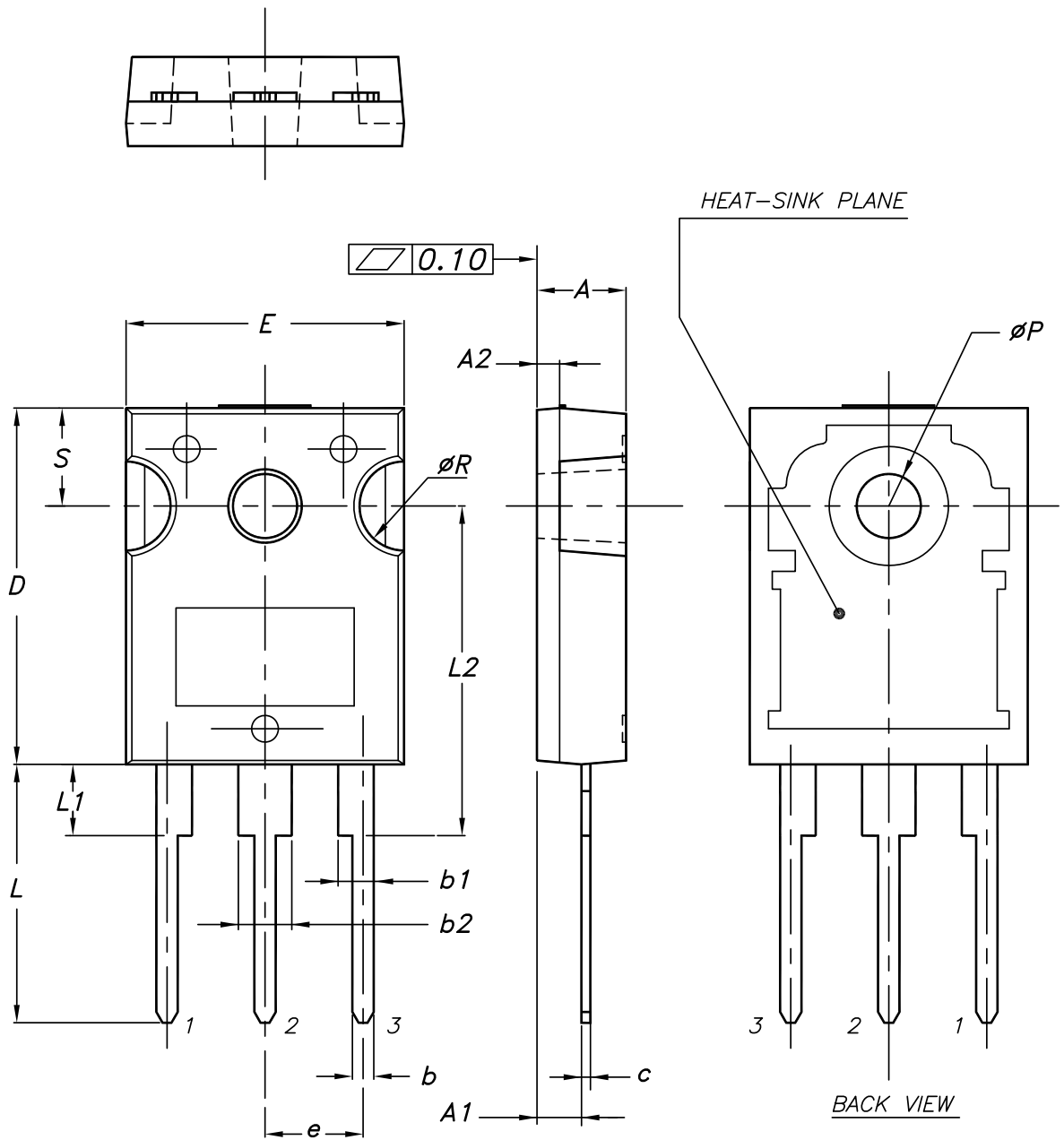
0015988\_typeA\_Rev\_24

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## 4.2 TO-247 package information

Figure 21. TO-247 package outline



0075325\_11

Table 9. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
01-Mar-2012	1	First release. Part numbers previously included in datasheet DocID022851.
11-Jul-2012	2	The part numbers STB18N65M5 and STD18N65M5 have been moved to a separate datasheet. The part numbers STI18N65M5 and STW18N65M5 in I <sup>2</sup> PAK and TO-247 packages have been added. Document status promoted from preliminary data to production data. Added <i>Section 2.1: Electrical characteristics (curves)</i> .
19-Jul-2012	3	Updated <i>Figure 8: Output characteristics</i> , <i>Figure 11: Static drainsource on-resistance</i> and <i>Figure 14: Normalized gate threshold voltage vs temperature</i> .
27-Nov-2025	4	Removed order code STF18N65M5 and STI18N65M5. Updated <a href="#">Section 4: Package information</a> . Minor text changes.



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## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	<b>Electrical characteristics (curves)</b> .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package information</b> .....	<b>9</b>
<b>4.1</b>	<b>TO-220 type A package information</b> .....	<b>9</b>
<b>4.2</b>	<b>TO-247 package information</b> .....	<b>11</b>
	<b>Revision history</b> .....	<b>13</b>



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