Primary Side PWM Controller for Low Power Offline SMPS

NCP1362



SOIC−8
CASE 751−07

The NCP1362 is a highly integrated primary side quasi−resonant flyback controller capable of controlling rugged and high−performance off−line power supplies.

Due to a Novel Method this new controller saves the secondary feedback circuitry for Constant Voltage and Constant Current regulation, achieving excellent line and load regulation without traditional opto coupler and TL431 voltage reference.

The NCP1362 operates in valley lockout quasi−resonant peak current mode control mode at high load to provide high efficiency. When the power on the secondary side starts to diminish, the controller automatically adjusts the duty−cycle then at lower load the controller enters in pulse frequency modulation at fixed peak current with a valley switching detection. This technique allows keeping the output regulation with tiny dummy load. Valley lockout at the first 4 valleys prevent valley jumping operation and then a valley switching at lower load provides high efficiency.

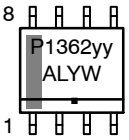
Features

- Constant Voltage Primary−Side Regulation < ±5%
- Constant Current Primary−Side Regulation < ±5%
- LFF and BO Feature on a Dedicated Pin:
  - BO Detection
  - LFF for CC Regulation Improvement
- Quasi−Resonant with Valley Switching Operation
- Optimized Light Load Efficiency and Stand−by Performance
- Maximum Frequency Clamp (No Clamp, 80, 110 and 140 kHz)
- Cycle by Cycle Peak Current Limit
- Output Voltage Under Voltage and Over Voltage Protection (UVP or OVP)
- Secondary Diode or Winding Short−Circuit Protection
- Wide Operation V_{CC} Range (up to 28 V)
- Low Start−up Current
- CS & V_S/ZCD Pin Short and Open Protection
- Internal Temperature Shutdown
- Internal and Fixed Frequency Jittering for Better EMI Signature
- Dual Frozen Peak Current to Both Optimize Light Load Efficiency (10% Load) and Stand−by Performance (No−load)
- Fault Input for Severe Fault Conditions, NTC Compatible for OTP
- These are Pb−Free Devices

Applications

- Low Power ac−dc Adapters for Routers and Set−Top Box
- Low Power ac−dc Adapters for Chargers

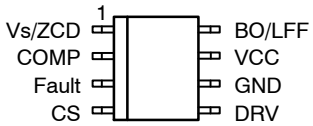
MARKING DIAGRAM



IC (Pb−Free)

P1362yy	= Specific Device Code (See page 29)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

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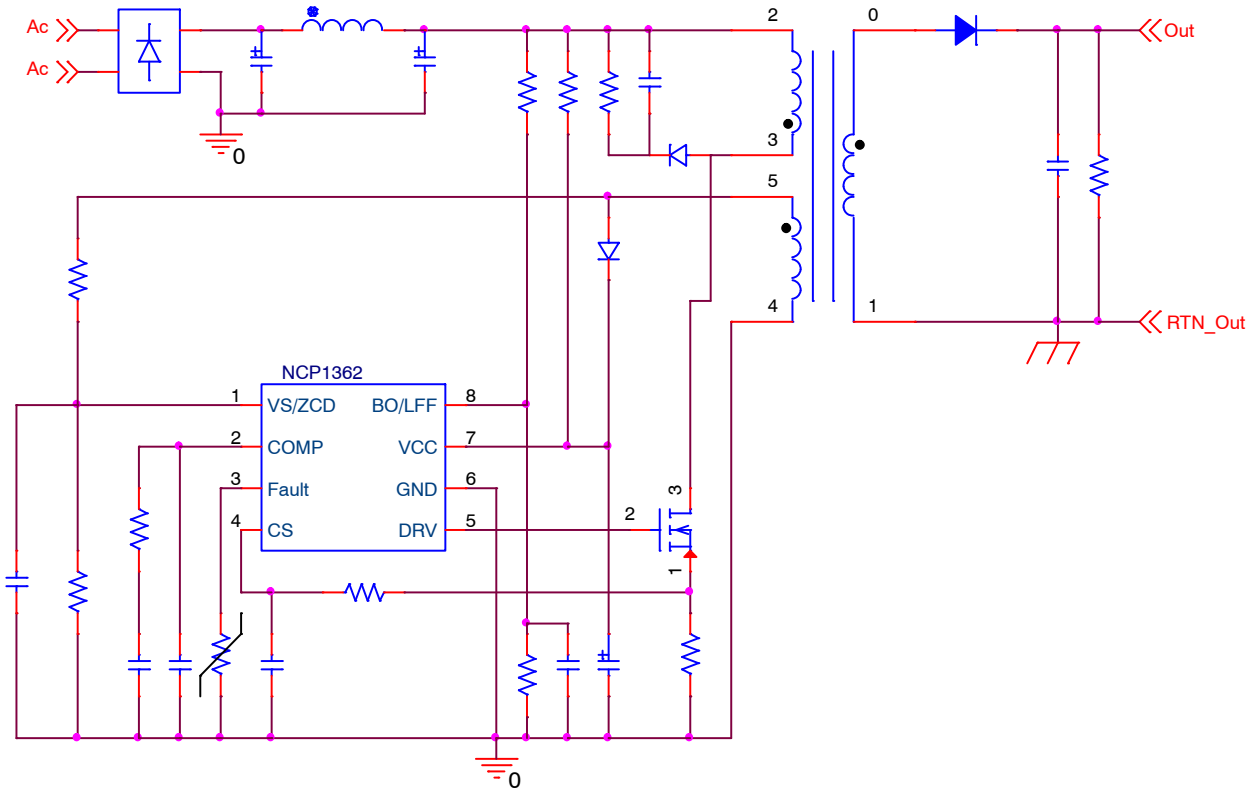


Figure 1. NCP1362 Typical Application Schematic for AC Input Voltage

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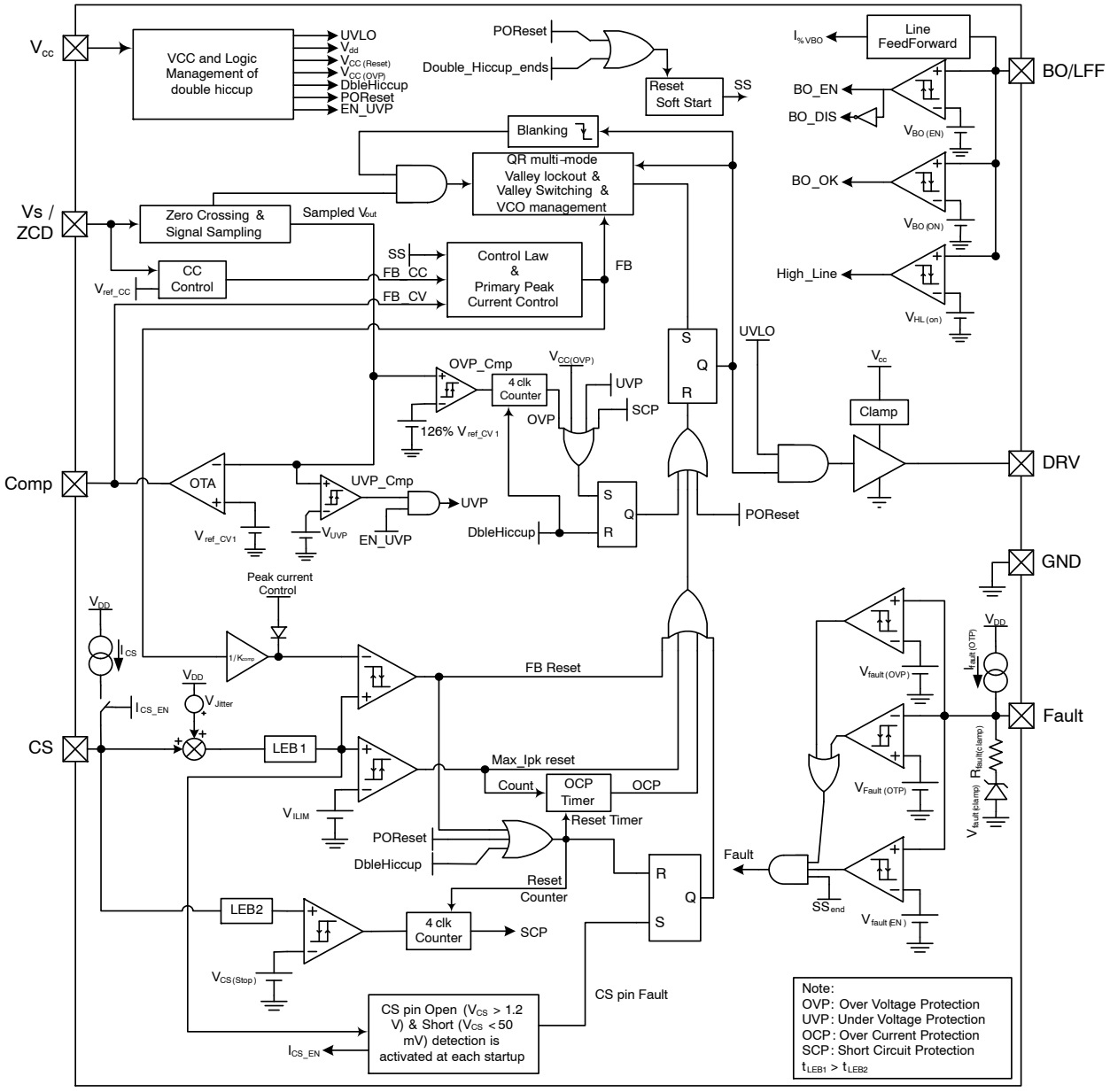


Figure 2. Functional Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Function
1	V_s/ZCD	Connected to the auxiliary winding; this pin senses the voltage output for the primary regulation and detects the core reset event for the Quasi−Resonant mode of operation.
2	Comp	This is the error amplifier output. The network connected between this pin and the ground adjusts the regulation loop bandwidth.
3	Fault	The controller enters in fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pullup current allows direct interface with an NTC thermistor. Fault detection triggers a latch.
4	CS	This pin monitors the primary peak current.
5	DRV	The driver's output to an external MOSFET gate.
6	GND	Ground reference.
7	V_{CC}	This pin is connected to an external auxiliary voltage and supplies the controller.
8	BO/LFF	Detects too low input voltage conditions (Brown−Out). Also voltage pin level is used for building Line FeedForward compensation for improving Constant Current regulation tolerance.

Table 2. MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, V_{CC} pin, continuous voltage Maximum current for V_{CC} pin	−0.3 to 28 Internally limited	V mA
$\Delta V_{CC}/\Delta t$	Maximum slew rate on V_{CC} pin during start−up phase	+0.4	V/μs
E_{as}	Single Pulse Avalanche Rating	120	mJ
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins DRV and VCC) Current range for low power pins (except pins DRV and VCC)	−0.3, 5.5 −2, +5	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 2) −300, +500	V mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air, 2.0 oz Printed Circuit Copper Clad	190	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	Human Body Model ESD Capability per JEDEC JESD22−A114F	2	kV
	Machine Model ESD Capability (All pins except DRV) per JEDEC JESD22−A115C	200	V
	Charged−Device Model ESD Capability per JEDEC JESD22−C101E	500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
2. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.

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Table 3. ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION AND V_{CC} MANAGEMENT						
V_{CC} Level at which Driving Pulses are Authorized	V_{CC} increasing	$V_{CC(on)}$	16.5	18	19.5	V
V_{CC} Level at which Driving Pulses are Stopped	V_{CC} decreasing	$V_{CC(off)}$	6.0	6.5	7.0	V
Internal Latch/Logic Reset Level		$V_{CC(reset)}$	–	6.25	–	V
Internal Autorecovery Reset Level	(Note 4)	$V_{CC(reset_auto)}$	0.6	–	–	V
Hysteresis above $V_{CC(off)}$ for Fast Hiccup in Latch Mode		$V_{CC(latch_hyst)}$	–	0.2	–	V
Hysteresis below $V_{CC(off)}$ before Latch Reset		$V_{CC(reset_hyst)}$	0.15	0.30	0.50	V
Over Voltage Protection	Over Voltage threshold	$V_{CC(OVP)}$	24	26	28	V
Start−up Supply Current, Controller Disabled or Latched	V_{CC} < $V_{CC(on)}$ & V_{CC} increasing from 0 V	$I_{CC(start)}$	–	4.3	7.0	μA
Internal IC Consumption, Steady State	F_{SW} = 65 kHz C_L = 1 nF	$I_{CC(steady)}$	–	1.6	2.3	mA
Internal IC Consumption in Minimum Frequency Clamp	VCO mode, F_{SW} = $f_{VCO(min)}$, V_{Comp} = GND $f_{VCO(min)}$ = 1 kHz $f_{VCO(min)}$ = 200 Hz C_L = 1 nF	$I_{CC(VCO)}$	 – –	 325 210	 430 370	μA
Internal IC Consumption in Fault Mode (after a fault when V_{CC} decreasing to $V_{CC(off)}$)	Autorecovery mode	$I_{CC(auto)}$	–	2.0	2.2	mA
Internal IC Consumption in Fault Mode (after a fault when V_{CC} decreasing to $V_{CC(off)}$)	Latch mode	$I_{CC(latch)}$	–	1.0	1.2	mA
CURRENT COMPARATOR						
Current Sense Voltage Threshold	V_{Comp} = $V_{Comp(max)}$, V_{CS} increasing	V_{ILIM}	0.76	0.8	0.84	V
Cycle by Cycle Leading Edge Blanking Duration		t_{LEB1}	250	320	380	ns
Cycle by Cycle Current Sense Propagation Delay	V_{CS} > (V_{ILIM} + 100 mV) to DRV turn−off	t_{ILIM}	–	50	110	ns
Timer Delay before Detecting an Overload Condition	When CS pin ≥ V_{ILIM} (Note 3)	T_{OCP}	50	70	90	ms
Threshold for Immediate Fault Protection Activation		$V_{CS(stop)}$	1.10	1.20	1.30	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{LEB2}	–	120	–	ns
Maximum Peak Current Level at which VCO Takes Over or Frozen Peak Current	V_{CS} increasing 0.6 V < V_{Comp} < 1.9 V (other possible options on demand)	$V_{CS(VCO)}$	–	250	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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4. Guaranteed by Design.
5. See the details about this parameter in the chapter Primary Side Regulation: Constant Voltage Operation on page 17

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(V_{CC} = 12 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
CURRENT COMPARATOR						
Minimum Peak Current Level	V_{CS} increasing V_{Comp} < 0.2 V (other possible options on demand)	$V_{CS(STB)}$	–	65	–	mV
REGULATION BLOCK						
Internal Voltage Reference for Constant Current Regulation	T_J = 25°C −40°C < T_J < 125°C	V_{ref_CC}	0.98 0.97	1.00 1.00	1.02 1.03	V
Internal Voltage Reference for Constant Voltage Regulation (Note 5)	T_J = 25°C −40°C < T_J < 125°C	V_{ref_CV1}	2.450 2.425	2.500 2.500	2.550 2.575	V
Error Amplifier Current Capability		I_{EA}	–	±40	–	μA
Error Amplifier Gain		G_{EA}	150	200	250	μS
Error Amplifier Output Voltage	Internal offset on Comp pin	$V_{Comp(max)}$ $V_{Comp(min)}$ $V_{Comp(offset)}$	– – –	4.9 0 1.1	– – –	V
Internal Current Setpoint Division Ratio		K_{Comp}	–	4	–	–
Valley Thresholds Transition from 1st to 2nd Valley Transition from 2nd to 3rd Valley Transition from 3rd to 4th Valley Transition from 4th Valley to VCO Transition from VCO to 4th Valley Transition from 4th to 3rd Valley Transition from 3rd to 2nd Valley Transition from 2nd to 1st Valley	 V_{Comp} decreasing V_{Comp} decreasing V_{Comp} decreasing V_{Comp} decreasing V_{Comp} increasing V_{Comp} increasing V_{Comp} increasing V_{Comp} increasing	 V_{H2D} V_{H3D} V_{H4D} V_{HVCOD} V_{HVCOI} V_{H4I} V_{H3I} V_{H2I}	 – – – – – – – –	 2.50 2.30 2.10 1.90 2.50 2.70 2.90 3.10	 – – – – – – – –	V
Minimal Difference between any Two Valleys	V_{Comp} increasing or V_{Comp} decreasing	ΔV_H	176	–	–	mV
Internal Dead Time Generation for VCO Mode	Entering in VCO when V_{Comp} is decreasing and crosses V_{HVCOD}	$T_{DT(start)}$	–	1.15	–	μs
Internal Dead Time Generation for VCO Mode	Leaving VCO mode when V_{Comp} is increasing and crosses V_{HVCOI}	$T_{DT(ends)}$	–	650	–	ns
Internal Dead Time Generation for VCO Mode	When in VCO mode – 1−kHz option V_{Comp} = 1.8 V V_{Comp} = 1.4 V V_{Comp} = 0.9 V V_{Comp} < 0.2 V	T_{DT}	 – – – –	 1.6 11 110 1000	 – – – –	μs
Minimum Switching Frequency in VCO Mode	V_{Comp} = GND Option 1 Option 2 (other possible options on demand)	$f_{VCO(MIN)}$	 0.8 0.16	 1.0 0.200	 1.2 0.24	kHz
Maximum Switching Frequency	 Option 1 Option 2 Option 3 Option 4	f_{MAX}	 – 72 99 127	 No Clamp 80 110 140	 – 88 121 153	kHz

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4. Guaranteed by Design.
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(V_{CC} = 12 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
REGULATION BLOCK						
Maximum On Time		$T_{on(max)}$	32	36	40	μs
DEMAGNETIZATION INPUT – ZERO VOLTAGE DETECTION CIRCUIT and VOLTAGE SENSE						
V_{ZCD} Threshold Voltage	V_{ZCD} decreasing	$V_{ZCD(TH)}$	25	45	70	mV
V_{ZCD} Hysteresis	V_{ZCD} increasing	$V_{ZCD(HYS)}$	15	30	45	mV
Threshold Voltage for Output Short Circuit or Aux. Winding Short Circuit Detection	After t_{BLANK_ZCD} if $V_{ZCD} < V_{ZCD(short)}$	$V_{ZCD(short)}$	30	50	75	mV
Delay after On−time that the V_S/ZCD is still Pulled to Ground	When V_{Comp} > 1.7 V When V_{Comp} < 1.7 V	t_{short_ZCD}	– –	0.750 0.350	– –	μs
Blanking Delay after On−time (V_S/ZCD Pin is Disconnected from the Internal Circuitry)	When V_{Comp} > 1.7 V When V_{Comp} < 1.7 V	t_{BLANK_ZCD}	– –	1.450 0.750	– –	μs
Timeout after Last Demagnetization Transition		t_{out}	4.0	4.5	5.0	μs
Input Leakage Current	V_{CC} > $V_{CC(on)}$ V_{ZCD} = 4 V, DRV is low	I_{ZCD}	–	–	0.1	μA
Delay from Valley Detection to DRV Low		t_{ZCD_delay}	–	290	–	ns
DRIVE OUTPUT – GATE DRIVE						
Drive resistance	DRV Sink – V_{CC} = 8 V DRV Source – V_{CC} = 8 V	R_{SNK} R_{SRC}	– –	8 10	– –	Ω
Rise time	C_{DRV} = 1 nF, from 10% to 90%	t_r	–	45	85	ns
Fall time	C_{DRV} = 1 nF, from 90% to 10%	t_f	–	30	65	ns
DRV Low voltage	V_{CC} = $V_{CC(off)}$ + 0.2 V, C_{DRV} = 220 pF, R_{DRV} = 33 kΩ	$V_{DRV(low)}$	6.0	–	–	V
DRV High voltage	V_{CC} = $V_{CC(OVP)}$ − 0.2 V, C_{DRV} = 220 pF, R_{DRV} = 33 kΩ	$V_{DRV(high)}$	–	12.0	13.0	V
SOFT START						
Internal Fixed Soft Start Duration	Current Sense peak current rising from $V_{CS(VCO)}$ to V_{ILIM}	t_{SS}	3	4	5	ms
JITTERING						
Frequency of the Jittering CS Pin Source Current	Option 1 (other possible options on demand)	f_{jitter}	1.2	1.5	1.8	kHz
Peak Jitter Voltage Added to PWM Comparator	Option 1 (other possible options on demand)	$V_{jittter}$	–	60	–	mV
BROWN−OUT & LINE FEED FORWARD						
Brown−out Function is Disabled below this Level (before the 1st DRV pulse only)		$V_{BO(en)}$	80	100	120	mV
Pull−down Current Source on BO Pin for Open Detection		I_{BO}	–	300	–	nA

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(V_{CC} = 12 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
BROWN−OUT & LINE FEED FORWARD						
Brown−out Level at which the Controller Starts Pulsing		$V_{BO(on)}$	0.75	0.80	0.85	V
Brown−out Level at which the Controller Stops Pulsing		$V_{BO(off)}$	0.65	0.70	0.75	V
Brown−out Filter Time		t_{BO}	–	50	–	μs
Line Feed Forward Compensation Gain		K_{LFF}	16	20	24	μA/V
FAULT PROTECTION						
Controller Thermal Shutdown	Device switching (F_{SW} ~ 65 kHz) – T_j rising	$T_{SHTDN(on)}$	–	150	–	°C
Thermal Shutdown Hysteresis	Device switching (F_{SW} ~ 65 kHz) – T_j falling	$T_{SHTDN(off)}$	–	120	–	°C
Fault Level Detection for OVP	Internal sampled V_{out} increasing $V_{OVP} = V_{ref_CV1}$ + 26%	V_{OVP}	2.95	3.15	3.35	V
Fault Level Detection for UVP → Double Hiccup Autorecovery (UVP detection is disabled during T_{EN_UVP})	Internal sampled V_{out} decreasing	V_{UVP}	1.40	1.50	1.60	V
Blanking Time for UVP Detection	Starting after the Soft start	T_{EN_UVP}	–	36	–	ms
Pull−up Current Source on CS Pin for Open or Short Circuit Detection	When $V_{CS} > V_{CS_min}$	I_{CS}	–	60	–	μA
CS Pin Open Detection	CS pin open	$V_{CS(open)}$	–	1.2	–	V
CS Pin Short Detection		V_{CS_min}	–	50	75	mV
CS pin Short Detection Timer	(Note 4)	T_{CS_short}	–	3	–	μs
Fault Pin is Disabled below this Level (before the 1st DRV pulse only)		$V_{Fault(EN)}$	80	100	120	mV
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	$V_{Fault(OVP)}$	2.79	3.00	3.21	V
Overtemperature Protection (OTP) Threshold	V_{Fault} decreasing	$V_{Fault(OTP)}$	0.38	0.40	0.42	V
OTP Pull−up Current Source	V_{Fault} = 0 V T_j = 25°C T_j = 110°C	 $I_{Fault(OTP)}$ $I_{Fault(OTP_110)}$	 42.5 42.9	 45.0 45.0	 47.5 46.5	μA
Fault Input Clamp Voltage	I_{Fault} = 0 mA (V_{Fault} = open)	$V_{Fault(clamp)0}$	1.10	1.35	1.60	V
Fault Input Clamp Voltage	I_{Fault} = 1 mA	$V_{Fault(clamp)1}$	2.2	2.7	3.2	V
Fault Filter Time		$t_{Fault(filter)}$	–	2	–	μs
Number of Drive Cycle before Latch Confirmation	$V_{Comp} = V_{Comp(max)}$, $V_{CS} > V_{CS(stop)}$ or Internal rebuilded $V_{out} > V_{OVP}$ or 0.40 V < V_{Fault} < 3.00 V or $V_{ZCD(short)}$	$t_{latch(count)}$	–	4	–	–

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TYPICAL CHARACTERISTICS

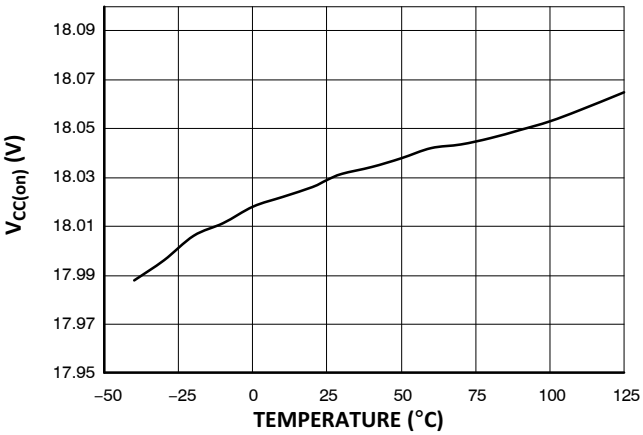


Figure 3. $V_{CC(on)}$ vs. Junction Temperature

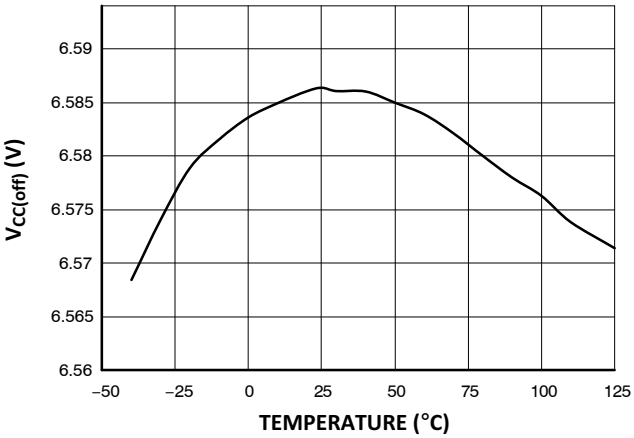


Figure 4. $V_{CC(off)}$ vs. Junction Temperature

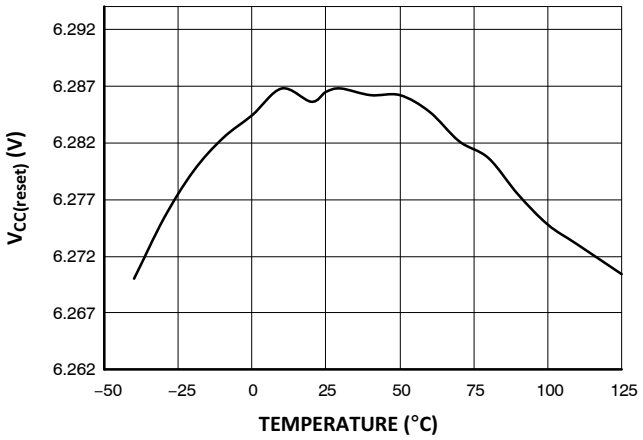


Figure 5. $V_{CC(reset)}$ vs. Junction Temperature

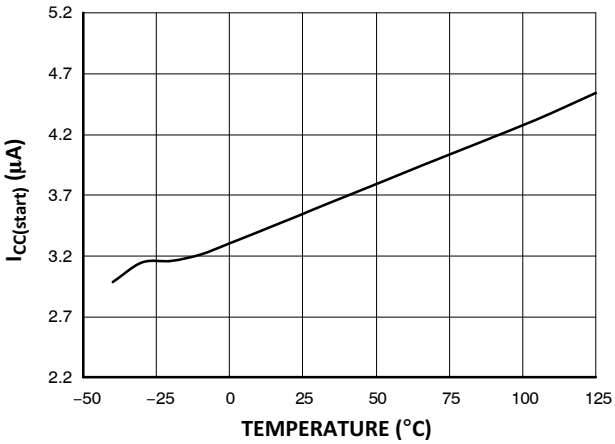


Figure 6. $I_{CC(start)}$ vs. Junction Temperature

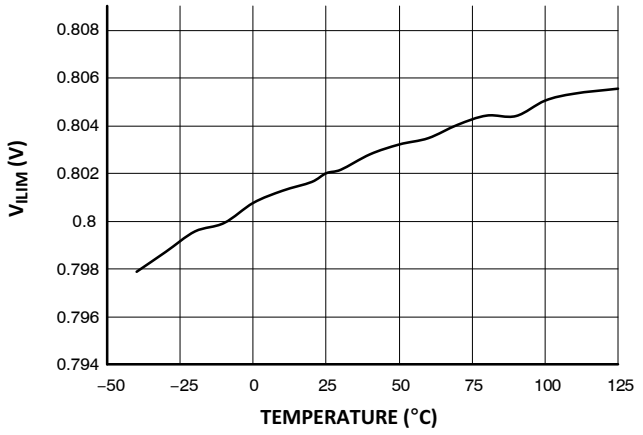


Figure 7. V_{ILIM} vs. Junction Temperature

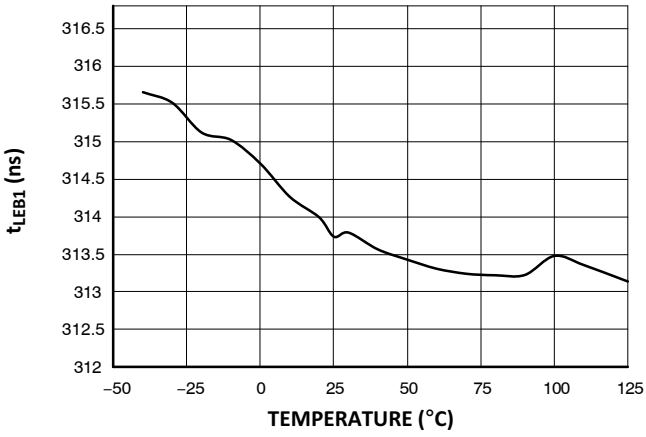


Figure 8. t_{LEB1} vs. Junction Temperature

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TYPICAL CHARACTERISTICS (CONTINUED)

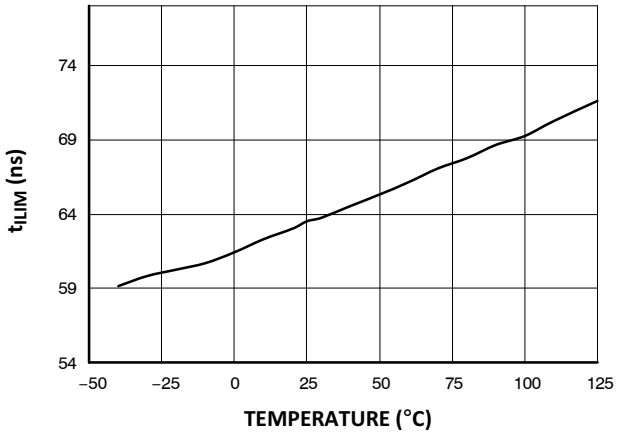


Figure 9. t_{ILIM} vs. Junction Temperature

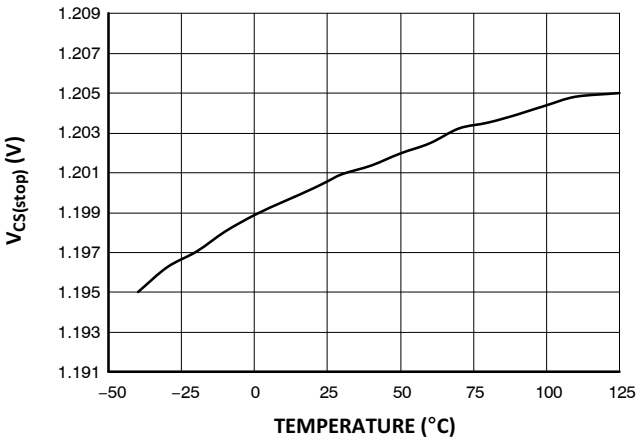


Figure 10. $V_{CS(stop)}$ vs. Junction Temperature

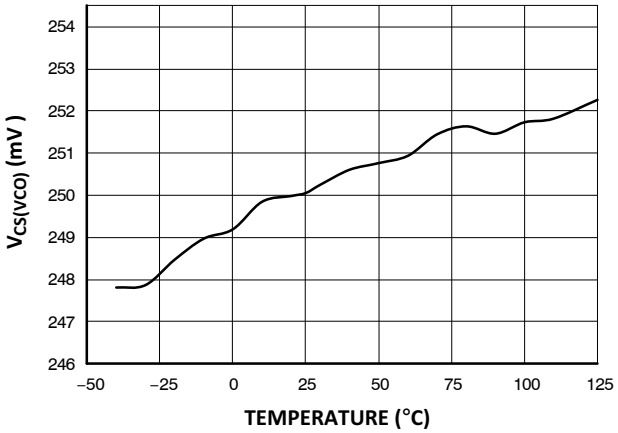


Figure 11. $V_{CC(VCO)}$ vs. Junction Temperature

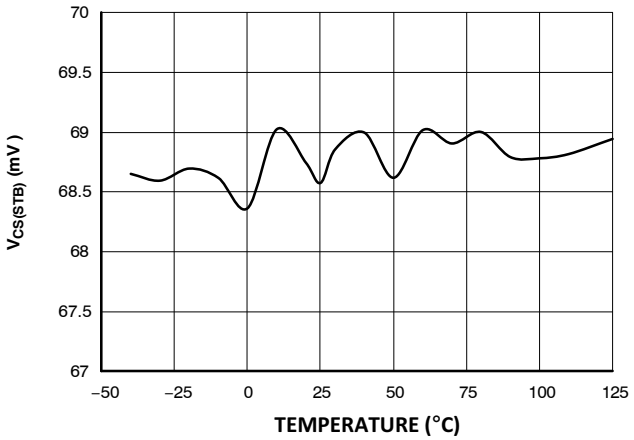


Figure 12. $V_{CS(STB)}$ vs. Junction Temperature

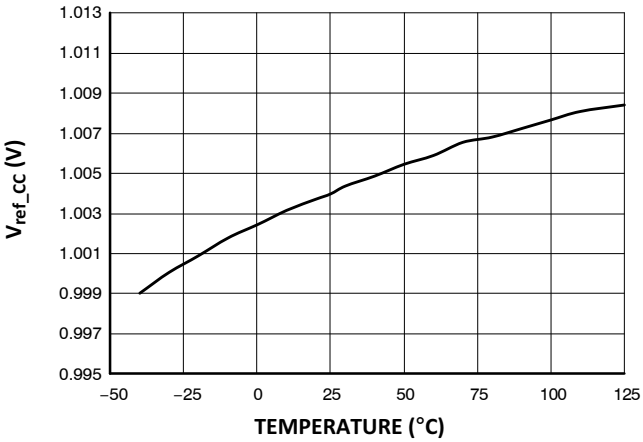


Figure 13. $V_{ref\ CC}$ vs. Junction Temperature

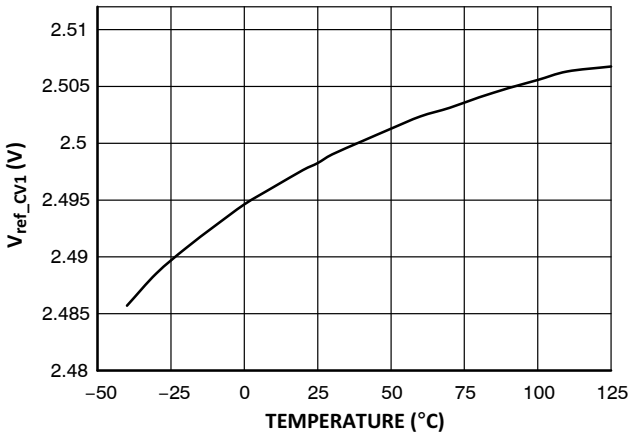


Figure 14. $V_{ref\ CV1}$ vs. Junction Temperature

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TYPICAL CHARACTERISTICS (CONTINUED)

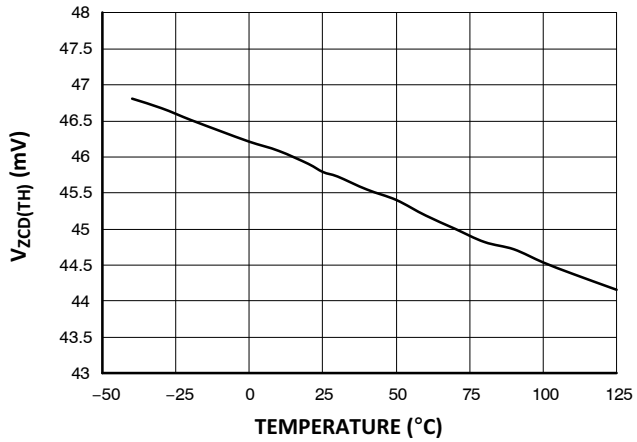


Figure 15. $V_{ZCD(TH)}$ vs. Junction Temperature

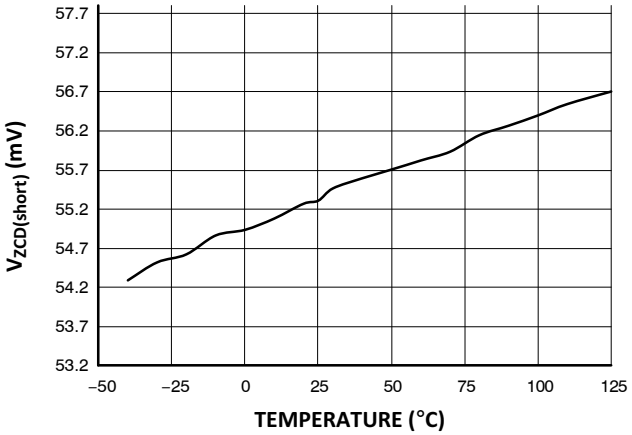


Figure 16. $V_{ZCD(short)}$ vs. Junction Temperature

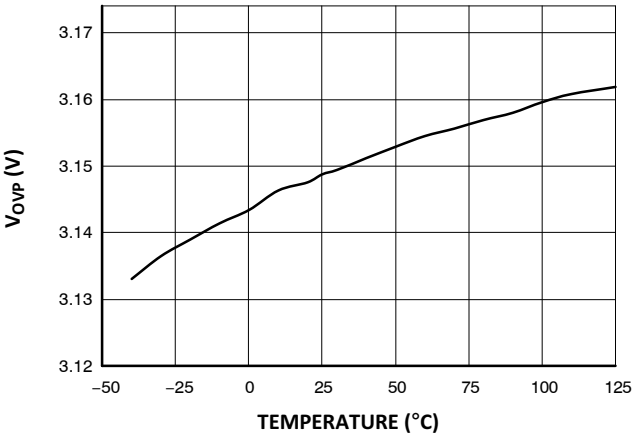


Figure 17. V_{OVP} vs. Junction Temperature

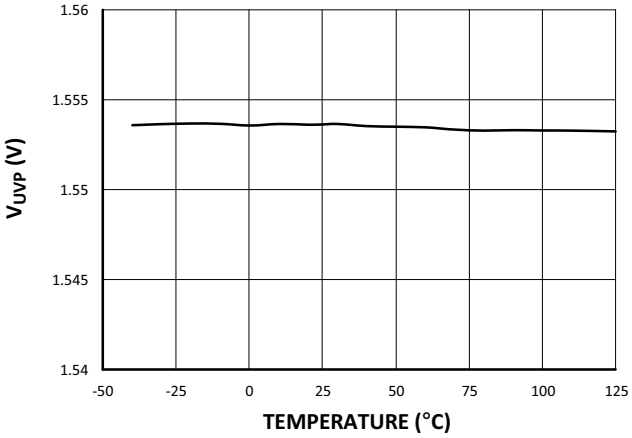


Figure 18. V_{UVP} vs. Junction Temperature

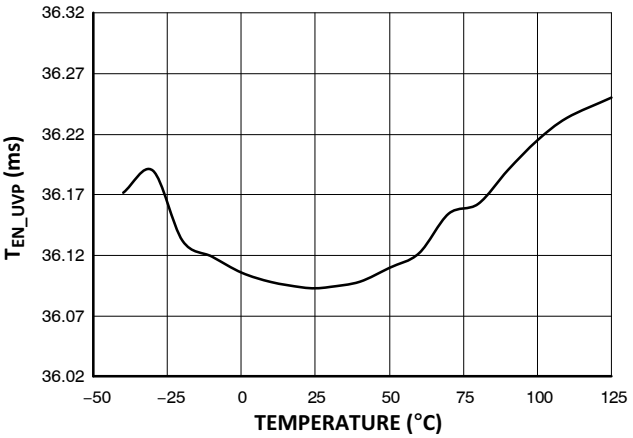


Figure 19. $T_{EN\ UVP}$ vs. Junction Temperature

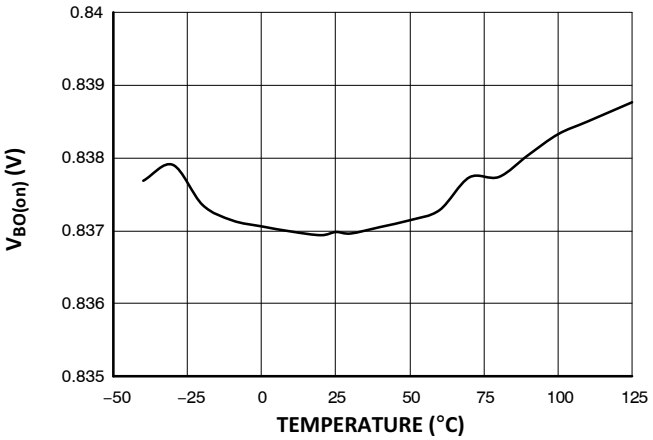


Figure 20. $V_{BO(on)}$ vs. Junction Temperature

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TYPICAL CHARACTERISTICS (CONTINUED)

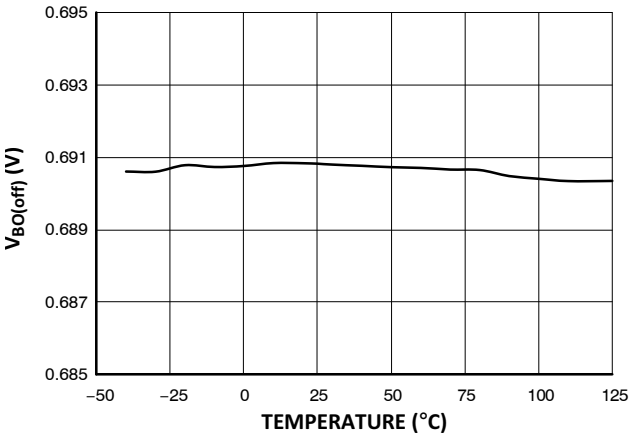


Figure 21. $V_{BO(off)}$ vs. Junction Temperature

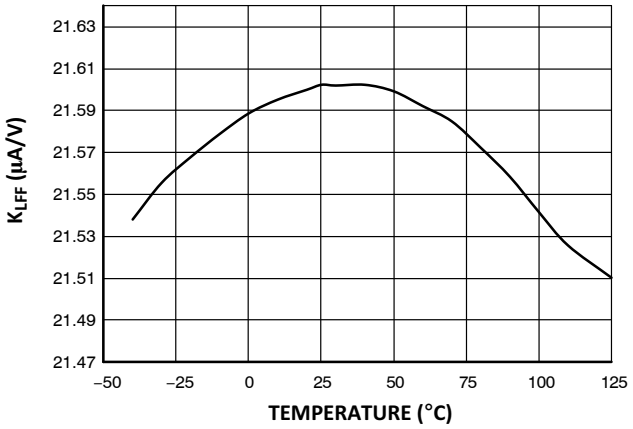


Figure 22. K_{LFF} vs. Junction Temperature

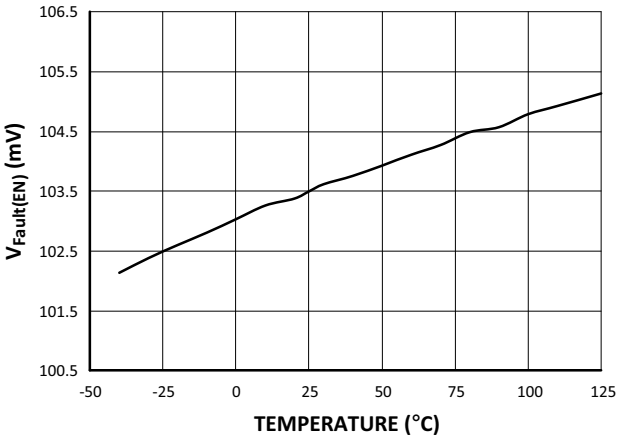


Figure 23. $V_{Fault(EN)}$ vs. Junction Temperature

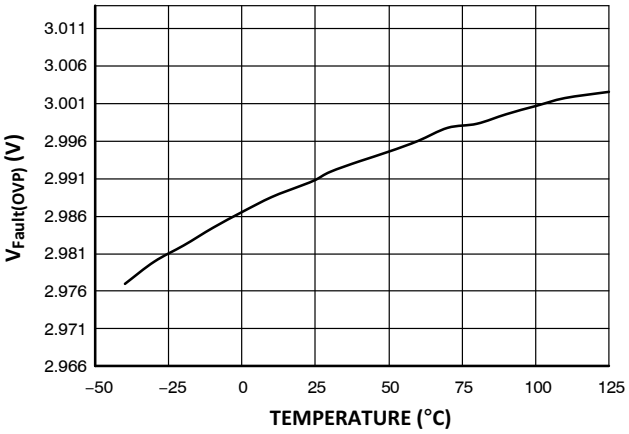


Figure 24. $V_{Fault(OVP)}$ vs. Junction Temperature

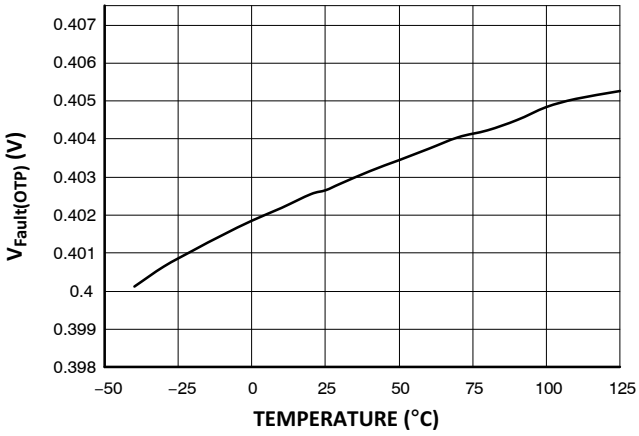


Figure 25. $V_{Fault(OTP)}$ vs. Junction Temperature

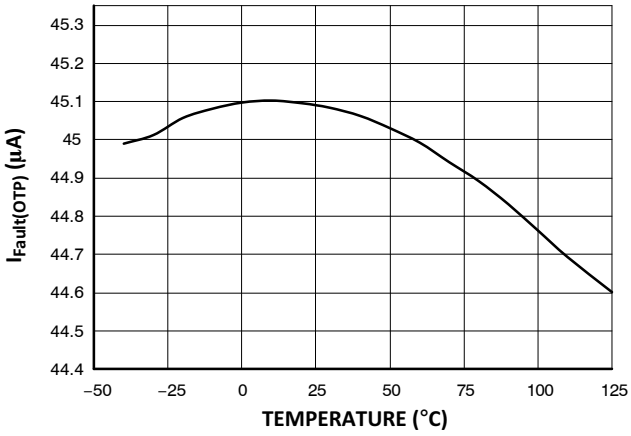


Figure 26. $I_{Fault(OTP)}$ vs. Junction Temperature

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Table 4. FAULT MODES

Event	Timer Protection	Next Device Status	Release to Normal Operation Mode
Overcurrent $V_{CS} > V_{ILIM}$	OCP Timer	Double Hiccup	– Resume to normal operation: if 4 pulses from FB Reset & then Reset timer – Resume operation after Double Hiccup
Winding Short $V_{CS} > V_{CS(stop)}$	4 Consecutive Pulses with $V_{CS} > V_{CS(stop)}$	Double Hiccup	Resume operation after Double Hiccup
CS Pin Fault: Short & Open	Before Start−up Immediate	Double Hiccup	Resume operation after Double Hiccup
ZCD Short $V_{ZCD} < V_{ZCD(short)}$ after t_{BLANK_ZCD} time	4 Consecutive Pulses	Double Hiccup	Resume operation after Double Hiccup
Low Supply $V_{CC} < V_{CC(off)}$	10−μs Timer	Simple Hiccup	Resume operation after Simple Hiccup
High Supply $V_{CC} > V_{CC(ovp)}$	10−μs Timer	Double Hiccup	Resume operation after Double Hiccup
Internal V_{out} OVP: $V_{out} > 126\%\ V_{ref_CV1}$	4 Consecutive Pulses	Double Hiccup	Resume operation after Double Hiccup
Internal V_{out} UVP: $V_{out} < 60\%\ V_{ref_CV1}$, when V_{out} is Decreasing Only	4 Consecutive Pulses	Double Hiccup	Resume operation after Double Hiccup
Internal TSD	10−μs Timer	Double Hiccup	Resume operation after Double Hiccup & $T < (T_{SHTDN(off)})$

NOTE: Latching off protection available upon request.

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APPLICATION INFORMATION

The NCP1362 is a flyback power supply controller providing a means to implement primary side constant−current regulation and secondary side constant−voltage regulation. NCP1362 implements a current−mode architecture operating in quasi−resonant mode. The controller prevents valley−jumping instability and steadily locks out in a selected valley as the power demand goes down. As long as the controller is able to detect a valley, the new cycle or the following drive remains in a valley. Thanks to a dedicated valley detection circuitry operating at any line and load conditions, the power supply efficiency will always be optimized. In order to prevent any high switching frequency two frequency clamp options are available.

- *Quasi−Resonance Current−mode Operation:* implementing quasi−resonance operation in peak current−mode control optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to a proprietary circuitry, the controller locks−out in a selected valley and remains locked until the input voltage significantly changes. Only the four first valleys could be locked out. When the load current diminishes, valley switching mode of operation is kept but without valley lock−out. Valley−switching operation across the entire input/output conditions brings efficiency improvement and lets the designer build higher−density converters.
- *Frequency Clamp:* As the frequency is not fixed and dependent on the line, load and transformer specifications, it is important to prevent switching frequency runaway for applications requiring maximum switching frequencies up to 90 kHz or 130 kHz. Three frequency clamp options at 80 kHz, 110 kHz or 140 kHz are available for this purpose. In case frequency clamp is not needed, a specific version of the NCP1362 exists in which the clamp is deactivated.
- *Primary Side Constant Current Regulation:* NCP1362 controls and regulates the output current at a constant level regardless of the input and output voltage conditions. This function offers tight over power protection by estimating and limiting the maximum output current from the primary side, without any particular sensor.

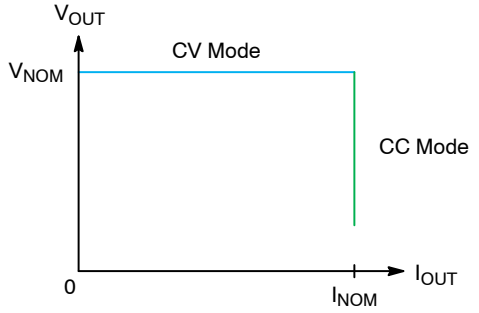


Figure 27. Constant−Voltage & Constant−Current Mode

- *Soft−Start:* 4−ms internal fixed soft start guarantees a peak current starting from zero to its nominal value with smooth transition in order to prevent any overstress on the power components at each startup.
- *Cycle−by−Cycle Peak Current Limit:* If the max peak current reaches the V_{ILIM} level, the over current protection timer is enabled and starts counting. If the overload lasts T_{OCP} delay, then the fault is detected and the controller stops immediately driving the power MOSFET. The controller enters in a double hiccup mode before autorecovering with a new startup cycle.
- *V_{CC} Over Voltage Protection:* If the V_{CC} voltage reaches the $V_{CC(OVP)}$ threshold the controller enters in fault mode. Thus it stops driving pulse on DRV pin. The part enters in double hiccup mode before resuming operation.
- *Winding Short−Circuit Protection:* An additional comparator senses the CS signal and stops the controller if V_{CS} reaches V_{ILIM} + 50% (after a reduced LEB: t_{LEB2}). Short circuit protection is enabled only if 4 consecutive pulses reach SCP level. This small counter prevents any false triggering of short circuit protection during surge test for instance. This fault is detected and operations will be resumed like in a case of *V_{CC} Over Voltage Protection*.
- *V_{out} Over Voltage Protection:* if the internally−built output voltage becomes higher than V_{OVP} level (V_{ref_CV1} + 26%) a fault is detected. This fault is detected and operations are resumed like in the *V_{CC} Over Voltage Protection* case.
- *V_{out} Under Voltage Protection:* After each circuit power on sequence, V_{out} UVP detection is enabled only after the startup timer T_{EN_UVP}. This timer ensures that the power supply is able to fuel the output capacitor before checking the output voltage in on target. After this startup blanking time, UVP detection is enabled and monitors the Output voltage level. When the power supply is running in constant−current mode and when the output voltage falls below V_{UVP} level, the controller stops sending drive pulses and enters a double hiccup mode before resuming operations.
- *V_S/ZCD Pin Short Protection:* at the beginning of each off−time period, the V_S/ZCD pin is tested to check whether it is shorted or left open. In case a fault is detected, the controller enters in a double hiccup mode before resuming operations.
- *EMI Jittering:* a low−frequency triangular voltage waveform is added to the CS pin. This helps spreading out energy in conducted noise analysis. Jittering is disabled in frequency foldback mode.
- *Frequency Foldback:* In frequency foldback mode, the system reduces the switching frequency by adding some dead−time after the 4th valley is detected.

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The controller will still run in valley switching mode even when the FF is enabled.

- *Temperature Shutdown:* if the junction temperature reaches the T_{SHTDN} level, the controller stop driving the power MOSFET until the junction temperature decreases to $T_{SHTDN(off)}$, then the operation is resumed after a double hiccup mode.
- *Brown−Out Detection:* BO pin monitors bulk voltage level via resistive divider and thus assures that the application is working only for designed bulk voltages. When BO pin is grounded before start−up ($V_{BO} < V_{BO(en)}$), Brown−Out, Line FeedForward and dynamic frequency clamp are disabled.
- *Line FeedForward:* By monitoring the voltage available on BO pin it is possible to create a line feedforward compensation in order to improve the constant current accuracy.
- *Fault Input:* the NCP1362 includes a dedicated fault input. It can be used to sense an overvoltage condition and latch off the controller by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. The controller is also disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault (by the means of an NTC). If this pin is grounded before start−up, then its associated feature are disabled.

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DETAILED APPLICATION INFORMATION

Start−up Sequence

The NCP1362 start−up voltage is made purposely high to permit large energy storage in a small V_{CC} capacitor value. This helps operate with a small start−up current which, together with a small V_{CC} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low (see $I_{CC(start)}$). The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage to further reduce the power dissipation.

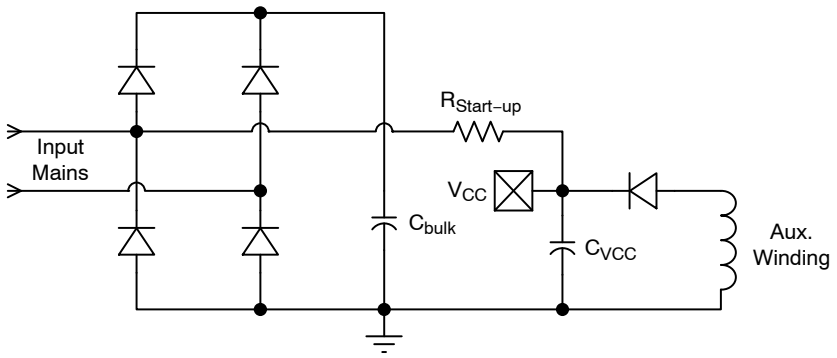


Figure 28. The Startup Resistor can be Connected to the Input Mains for Further Power Dissipation Reduction

The first step starts with the calculation of the needed V_{CC} capacitor which will supply the controller when it operates until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 ms and 20 ms. If we consider we need at least an energy reservoir for a t_1 time of 10 ms, the V_{CC} capacitor must be larger than:

$$C_{V_{CC}} \geq \frac{I_{CC} \times t_1}{V_{CC(on)} - V_{CC(off)}} \geq \frac{1.6\ m \times 10\ m}{18 - 6.5} \geq 1.4\ \mu F \quad \text{(eq. 1)}$$

Let us select a 1.5 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for the time t_1. The V_{CC} capacitor being known, we can now evaluate the charging current we need to bring the V_{CC} voltage from 0 V to the $V_{CC(on)}$ of the IC. This current has to be selected to ensure a start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{V_{CC(on)} \times C_{Vcc}}{t_{start-up}} \geq \frac{18 \times 1.5\ \mu}{2.5} \geq 11\ \mu A \quad \text{(eq. 2)}$$

If we account for the $I_{CC(start)}$ = 7.0 μA (maximum) that will flow inside the controller, then the total charging current delivered by the start−up resistor must be 18 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the $V_{CC(on)}$ of the controller:

$$I_{CVcc,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 18 μA, then the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{85\sqrt{2}}{\pi} - 18}{18\ \mu} \leq 1.13\ M\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{CC} capacitor. Thus, a decrease in charging current and an increase of the start−up resistor can be experimentally tested, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 1.2−MΩ resistor as suggested by Eq. 4, the dissipated power at high line amounts to:

$$P_{R_{start-up,max}} \approx \frac{V_{ac,peak}^2}{4 \times R_{start-up}} \approx \frac{\left(230 \times \sqrt{2}\right)^2}{4 \times 1.1\ M} \approx 24\ mW \quad \text{(eq. 5)}$$

Primary Side Regulation: Constant Current Operation

Figure 29 portrays idealized primary and secondary transformer currents of a flyback converter operating in Discontinuous Conduction Mode (DCM).

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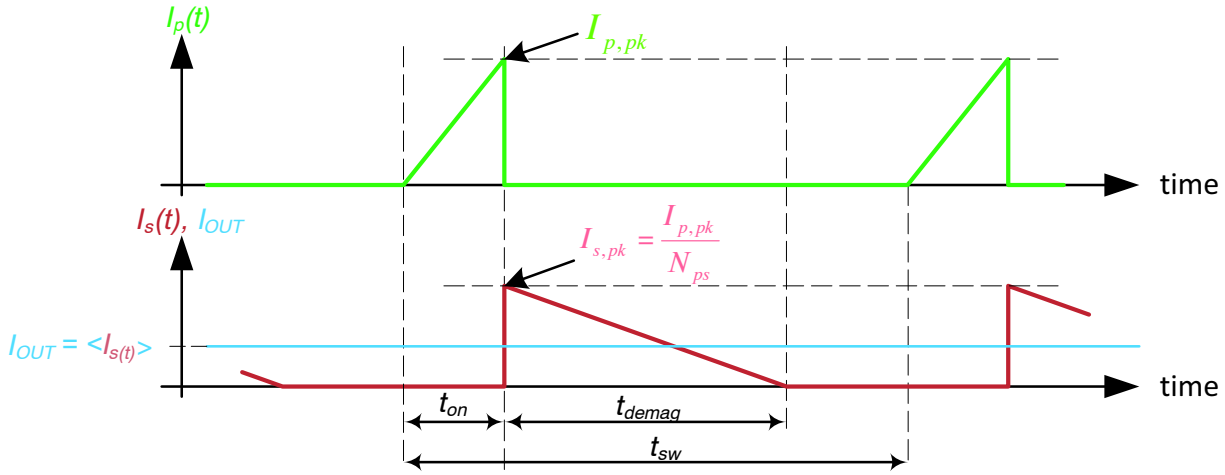


Figure 29. Primary and Secondary Transformer Current Waveforms

When the primary power MOSFET is turned on, the primary current is illustrated by the green curve of Figure 29. When the power MOSFET is turned off the primary side current drops to zero and the current into the secondary winding immediately rises to its peak value equal to the primary peak current divided by the primary to secondary turns ratio. This is an ideal situation in which the leakage inductance action is neglected.

The output current delivered to the load is equal to the average value of the secondary winding current, thus we can write:

$$I_{out} = \langle i_{sec}(t) \rangle = \frac{I_{p,pk}}{2N_{ps}} \times \frac{t_{demag}}{t_{sw}} \qquad \text{(eq. 6)}$$

Where:

- t_{SW} is the switching period
- t_{demag} is the demagnetizing time of the transformer
- N_{PS} is the secondary to primary turns ratio, where N_P & N_S are respectively the transformer primary and secondary turns:

$$N_{ps} = \frac{N_s}{N_p} \qquad \text{(eq. 7)}$$

- $I_{p,pk}$ is the magnetizing peak current sensed across the sense resistor on CS pin:

$$I_{p,pk} = \frac{V_{CS}}{R_{sense}} \qquad \text{(eq. 8)}$$

Internal constant current regulation block is building the constant current feedback information as follow:

$$V_{FB_CC} = V_{ref_CC} \times \frac{t_{SW}}{t_{demag}} \qquad \text{(eq. 9)}$$

As the controller monitors the primary peak current via the sense resistor and due to the internal current setpoint divider (K_{comp}) between the CS pin and the internal feedback information, the output current could be written as follow:

$$I_{out} = \frac{V_{ref_CC}}{8N_{ps} \times R_{sense}} \qquad \text{(eq. 10)}$$

The output current value is set by choosing the sense resistor value:

$$R_{sense} = \frac{V_{ref_CC}}{8N_{ps} \times I_{out}} \qquad \text{(eq. 11)}$$

Primary Side Regulation: Constant Voltage Operation

In primary side constant voltage regulation, the output voltage is sensed via the auxiliary winding. During the on−time period, the energy is stored in the transformer gap. During the off−time this energy stored in the transformer is delivered to the secondary and auxiliary windings.

As illustrated by Figure 30, when the transformer energy is delivered to the secondary, the auxiliary voltage sums the output voltage scaled by the auxiliary and secondary turns ratios and the secondary forward diode voltage. This secondary forward diode voltage could be split in two elements: the first part is the forward voltage of the diode (V_f), and the second is related to the dynamic resistance of the diode multiplied by secondary current ($R_D \times I_S(t)$). Where this second term will be dependant of the load and line conditions.

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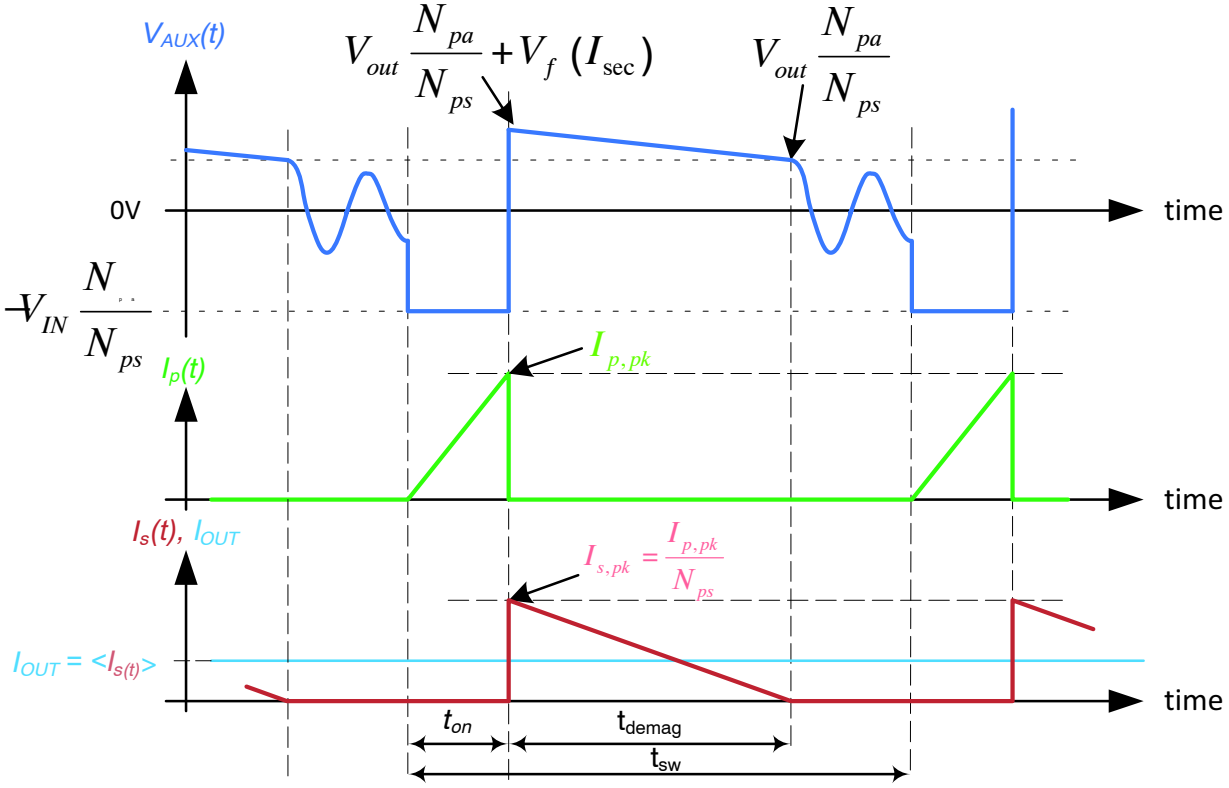


Figure 30. Typical Idealized Waveforms of a Flyback Transformer in DCM

To reach an accurate primary−side constant−voltage regulation, the controller detects the end of the demagnetization time and precisely samples output voltage level seen on the auxiliary winding. As this moment coincides with the secondary−side current equal to zero, the diode forward voltage drop becomes independent from the loading conditions.

Thus when the secondary current $I_s(t)$ reaches zero ampere, the auxiliary is sensed:

$$V_{aux} = V_{out} \times \frac{N_{pa}}{N_{ps}} \qquad \text{(eq. 12)}$$

Where: N_{pa} is the auxiliary to primary turns ratio, where N_p & N_a are respectively the primary and auxiliary turns:

$$N_{pa} = \frac{N_a}{N_p} \qquad \text{(eq. 13)}$$

Figure 32 illustrates how the constant voltage feedback has been built. The auxiliary winding voltage must be scaled down via the resistor divider to V_{ref_CV1} level before building the constant voltage feedback error.

$$V_{ref_CV1} = \frac{R_{s2}}{R_{s1} + R_{s2}} \times V_{aux} \qquad \text{(eq. 14)}$$

By inserting Eg. 12 into Eq. 14 we obtain the following equation:

$$V_{ref_CV1} = \frac{R_{s2}}{R_{s1} + R_{s2}} \times \frac{N_{pa}}{N_{ps}} \times V_{out} \qquad \text{(eq. 15)}$$

Please note that the controller regulates the output volage through the ZCD voltage when the voltage value in a knee is 2.7 V (see the Figure 31). Therefore, the value 2.7 V should be used as V_{ref_CV1} parameter instead of 2.5 V stated in Table 3. Electrical characteristics. Also, all voltage drops between secondary winding and measured output voltage needs to be considered and add to the output voltage value. It's recommended to verify the actual output voltage value in the real application and tune up the ZCD divider.

$$V_{OUT} = 2.7\ V \times \frac{N_{ps}}{N_{pa}} \times \frac{R_{s1} + R_{s2}}{R_{s2}} - V_{f(0)} \qquad \text{(eq. 16)}$$

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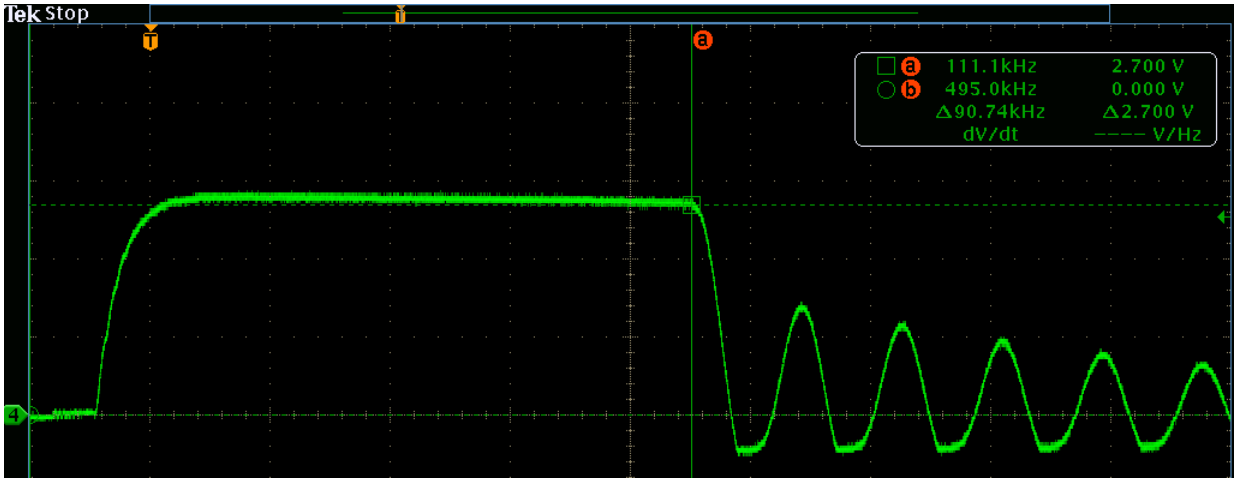


Figure 31. ZCD Voltage Waveform during Constant Voltage Regulation

Once the sampled V_{out} is applied to the negative input terminal of the operational transconductance amplifier (OTA) and compared to the internal voltage reference an adequate voltage feedback is built. The OTA output being pinned out, it is possible to compensate the converter and adjust step load response to what the project requires.

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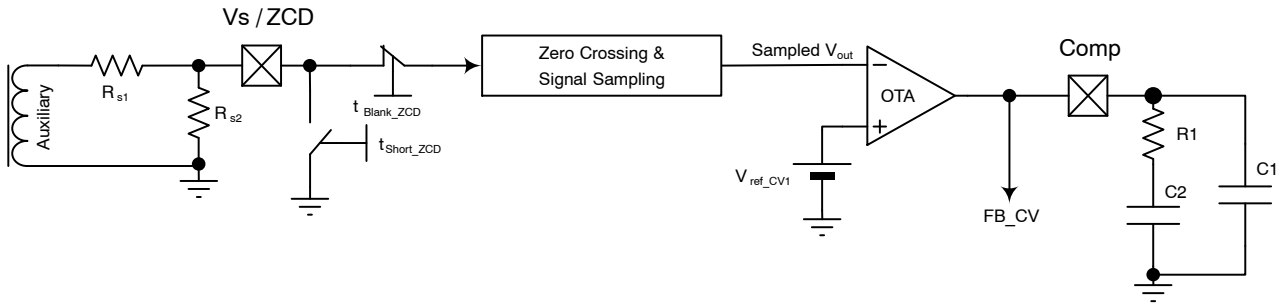


Figure 32. Constant Voltage Feedback Arrangement

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When the power MOSFET is released at the end of the on time, because of the transformer leakage inductance and the drain lumped capacitance some voltage ringing appears on the drain node. These voltage ringings are also visible on the auxiliary winding and could cheat the controller detection circuits. To avoid false detection operations, two protecting circuits have been implemented on the V_S/*ZCD* pin (see Figure 33):

1. An internal switch grounds the V_S/*ZCD* pin during t_{on} + t_{short_ZCD} in order to protect the pin from negative voltage.
2. In order to prevent any misdetection from the zero crossing block an internal switch disconnects V_S/*ZCD* pin until t_{blank_ZCD} time ends.

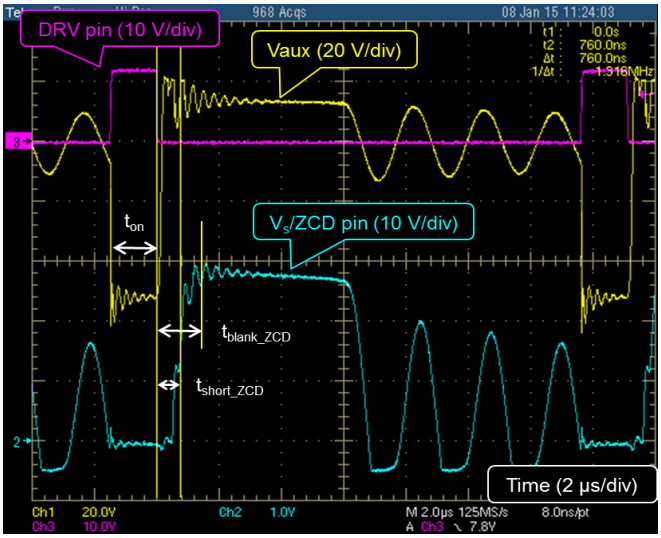


Figure 33. V_S/ZCD Pin Waveforms

Constant−Current and Constant−Voltage Overall Regulation

As already presented in the two previous paragraphs, the controller integrates two different feedback loops: the first one deals with the constant−current regulation scheme while the second one builds the constant−voltage regulation. One of the two feedback paths sets the primary peak current into the transformer. During startup phase, however, the peak current is controlled by the softstart.

Zero Current Detection

The NCP1362 integrates a quasi−resonant (QR) flyback controller. The power switch turn−off of a QR converter is determined by the peak current whose value depends on the feedback loop. The switch restart event is determined by the transformer demagnetization end. The demagnetization end is detected by monitoring the transformer auxiliary winding voltage. Turning on the power switch once the transformer is demagnetized (or reset) reduces turn−on switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lumped capacitance, eventually settling at the input voltage value. A QR controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce turn−on switching losses and electromagnetic interference (EMI).

As sketched by Figure 34, a valley is detected once the ZCD pin voltage falls below the QR flyback demagnetization threshold, $V_{ZCD(TH)}$, typically 45 mV. The controller will switch once the valley is detected or increment the valley counter depending on FB voltage.

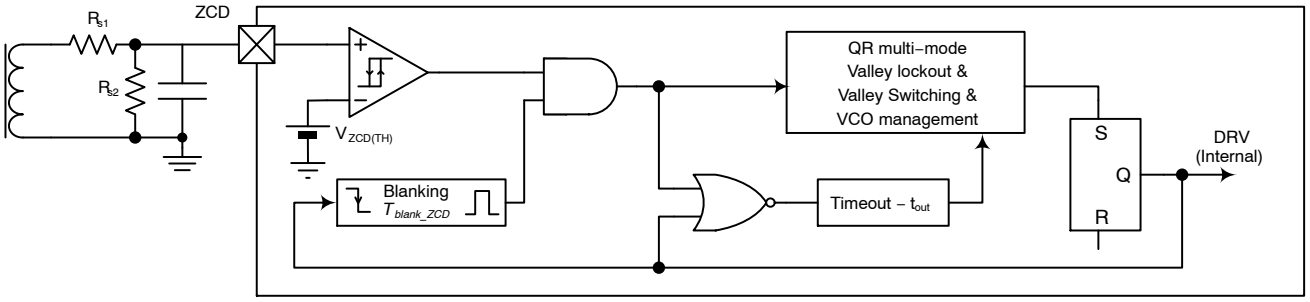


Figure 34. Valley Lockout Detection Circuitry Internal Schematic

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Timeout

The ZCD block actually detects falling edges of the auxiliary winding voltage applied to the ZCD pin. At start−up or during other transient phases, the ZCD comparator may be unable to detect such an event. Also, in the case of extremely damped oscillations, the system may not succeed in detecting all the valleys required by valley lockout operation (VLO, see next section). In this condition, the NCP1362 ensures continued operation by incorporating a maximum timeout period that resets itself when a demagnetization phase is properly detected. In case the ringing signal is too weak or heavily damped, the timeout signal supersedes the ZCD signal for the valley counter. Figure 34 shows the timeout period generator circuit schematic. The timeout duration, t_{out}, is set to 4.5 μs (typ.).

In VLO operation, the timeout occurrences are counted instead of valleys when the drain−source voltage oscillations are too damped to be detected. For instance, assume the circuit must turn on at the third valley and the ZCD ringing only enables the detection of:

- *Valleys #1 to #2:* the circuit generates a DRV pulse t_{out} (steady−state timeout delay) after valley #2 detection.
- *Valley #1:* the timeout delay must run twice so that the circuit generates a DRV pulse 9 μs ($2 \times t_{out}$ typ.) after valley #1 detection.

Valley LockOut (VLO) and Frequency Foldback (FF)

The operating frequency of a traditional Quasi−Resonant (QR) flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when associated with a valley−switching circuit, instabilities can arise because of the discrete frequency jumps. The controller tends to hesitate between two valleys and audible noise can be generated

To avoid this issue, the NCP1362 incorporates a proprietary valley lockout circuitry which prevents so−called valley jumping. Once a valley is selected, the controller stays locked in this valley until the input level or output power changes significantly. This technique extends QR operation over a wider output power range while maintaining good efficiency and naturally limiting the maximum operating frequency.

The operating valley (from 1st to 4th valley) is determined by the internal feedback level (Internal FB node on Figure 2). As FB voltage level decreases or increases, the valley comparators toggle one after another to select the proper valley.

The decimal counter increases each time a valley is detected. The activation of an “n” valley comparator blanks the “n−1” or “n+1” valley comparator output depending if V_{FB} decreases or increases, respectively. Figure 35 shows a typical frequency characteristic obtained at low line in a 10−W charger.

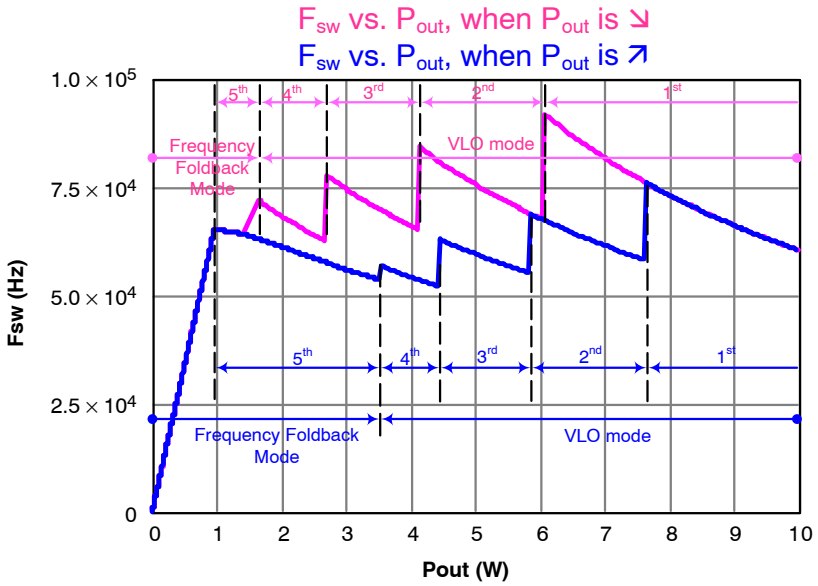


Figure 35. Typical Switching Frequency vs. Output Power Relationship in a 10−W Adapter

When an “n” valley is asserted by the valley selection circuitry, the controller locks in this valley until the FB voltage decreases to the lower threshold (“n+1” valley activates) or increases to the “n valley threshold” + 600 mV (“n−1” valley activates). The regulation loop adjusts the peak current to deliver the necessary output power at the valley operating point. Each valley selection comparator features a 600−mV hysteresis that helps stabilize operation despite the FB voltage swing produced by the regulation loop.

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Table 5. VALLEY FB THRESHOLD ON CONSTANT VOLTAGE REGULATION

FB Falling		FB Rising	
1st to 2nd Valley	2.5 V	FF Mode to 4th	2.5 V
2nd to 3rd Valley	2.3 V	4th to 3rd Valley	2.7 V
3rd to 4th Valley	2.1 V	3rd to 2nd Valley	2.9 V
4th to FF Mode	1.9 V	2nd to 1st Valley	3.1 V

Frequency Foldback (FF)

As the output current decreases (FB voltage decreases), the valleys are incremented from 1 to 4. In case the fourth valley is reached, the FB voltage further decreases below 1.9 V and the controller enters the frequency foldback mode (FF). The current setpoint being internally forced to remain above $V_{CS(VCO)}$ (setpoint corresponding to V_{Comp}), the controller regulates the power delivery by modulating the switching frequency. When an output current increase causes FB to exceed the 2.5−V FF upper threshold (600−mV hysteresis), the circuit recovers VLO operation.

In frequency foldback mode, the system reduces the switching frequency by adding some dead−time after the 4th valley is detected. However, in order to keep the high efficiency benefit inherent to the QR operation, the controller turns on again with the next valley after the dead time has ended. As a result, the controller will still run in valley switching mode even when the FF is enabled. This dead−time increases when the FB voltage decays. There is no discontinuity when the system transitions from VLO to FF and the frequency smoothly reduces as FB goes below 1.9 V.

The dead−time is selected to generate a 1.15−μs dead−time when V_{Comp} is decreasing and crossing V_{HVCOD} (1.9 V typ.). At this moment, it can linearly go down to the minimal frequency limit. The generated dead−time is 650 ns when V_{Comp} is increasing and crossing V_{HVCOI} (2.5 V typ.).

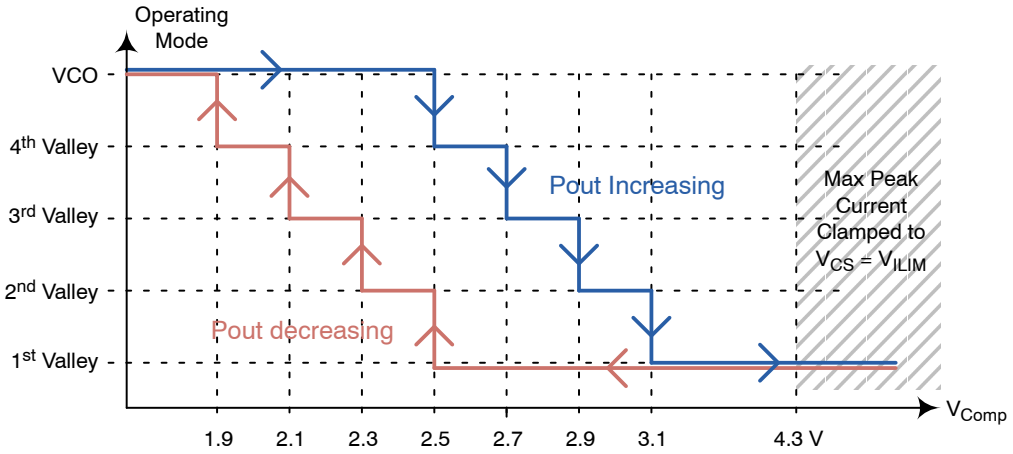


Figure 36. Valley Lockout Threshold

Stand−by Mode

An high frozen peak current is necessary to have good efficiency at 10% of the load. On the other hand, the standby performance will not be optimized. Indeed, in no load condition, the switching frequency has to be high enough to have a good transient response and then keep the output voltage within the limits. If we set a minimum switching frequency, the only parameter that can be adjusted to deliver less power is the primary peak current as shown in Eq. 17.

$$P_{out} = \frac{1}{2} \times I_{p,pk}^{2} \times f_{SW} \times \eta \qquad \text{(eq. 17)}$$

The NCP1362 implements a peak control mode when the load is closed to 0. From frozen peak current in FF mode (250 mV here), the maximum voltage threshold on CS pin is reduced to 65 mV when the Comp voltage crossed 0.260 V. If the 65−mV threshold is reached in 200 ns for instance due to small primary inductance, the minimum ON time will be defined by the 320−ns leading edge blanking duration and the propagation delay (50 ns) so 370 ns typically.

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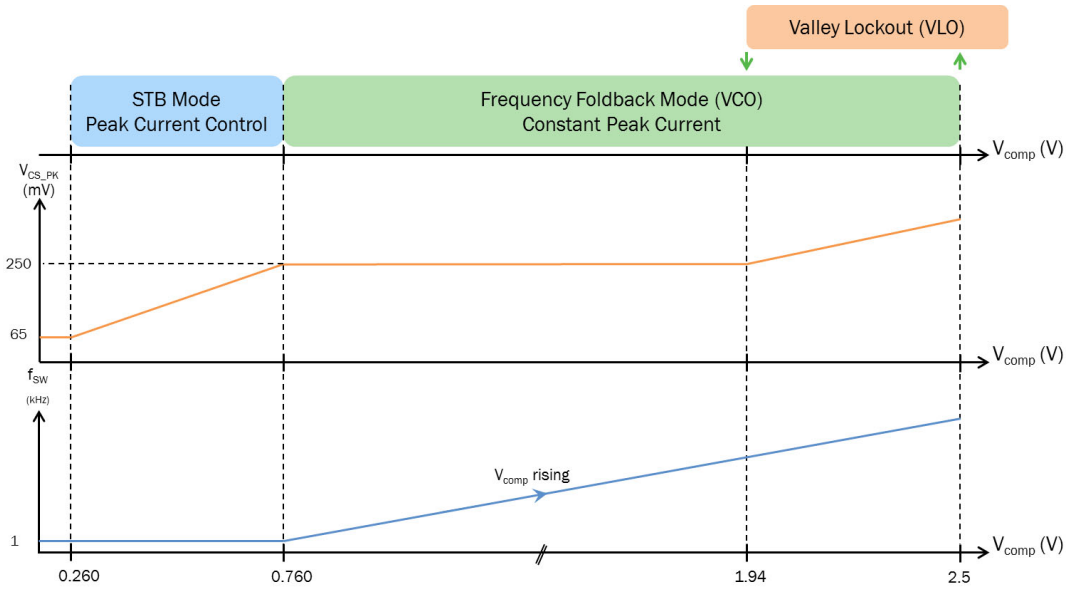


Figure 37. Frequency Foldback and Standby Mode Behavior with 1−kHz Minimum Frequency Clamp, $V_{CS(VCO)}$ = 250 mV and $V_{CS(STB)}$ = 65 mV

Current Setpoint

As explained in this operating description, the current setpoint is affected by several functions. Figure 38 summarizes these interactions. As shown by this figure, the current setpoint is the output of the control law divided by K_{comp} (4 typ.). This current setpoint is clamped by the soft−start slope as long as the peak current requested by the FB_CV or FB_CC level are higher. The softstart clamp is starting from the frozen peak current ($V_{CS(VCO)}$) to V_{ILIM} (0.8 V typ.) within 4 ms (t_{ss}).

However, this internal FB value is also limited by the following functions:

- A minimum setpoint is forced that equals $V_{CS(VCO)}$ (250 mV, typ.) when 0.760 V < V_{comp} < 1.9 V
- A second minimum setpoint is forced that equals $V_{CS(STB)}$ (65 mV, typ.) when V_{comp} < 0.260 V
- The peak current is linearly reduced between this two previous frozen peak current ($V_{CS(VCO)}$ & $V_{CS(STB)}$)
- In addition, a second OCP comparator ensures that in any case the current setpoint is limited to V_{ILIM}. This ensures the MOSFET current setpoint remains limited to V_{ILIM} in a fault condition.

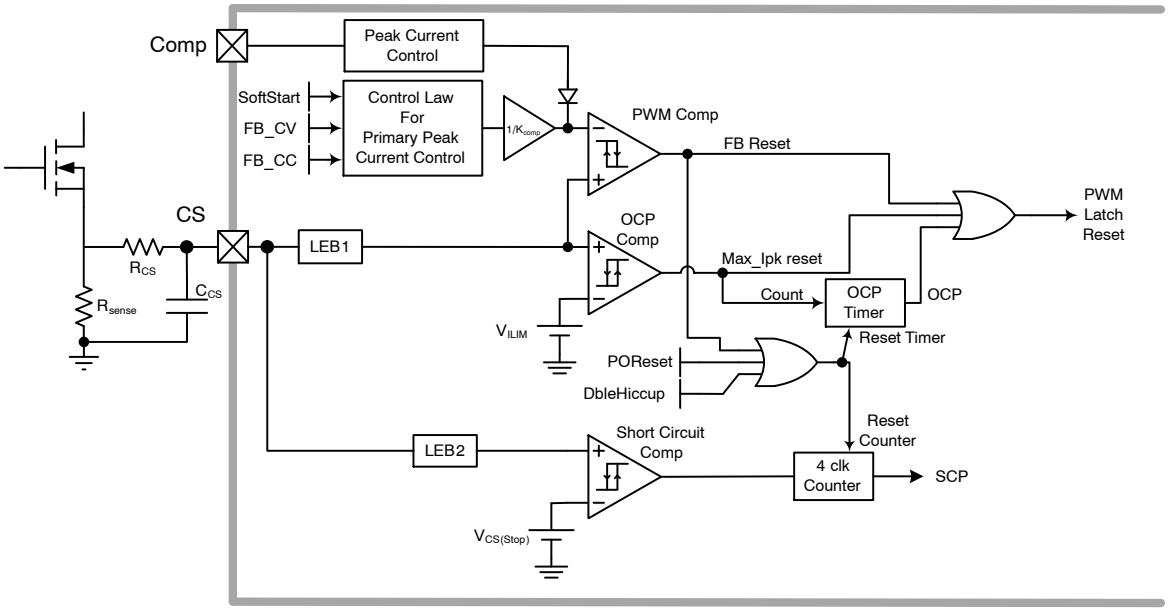


Figure 38. Current Setpoint

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A 2nd Over−Current Comparator for Abnormal Overcurrent Fault Detection

A severe fault like a winding short−circuit can cause the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{ILIM}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the power switch current can abnormally increase, possibly causing system damages. The NCP1362 protects against this dangerous mode by adding an additional comparator for abnormal overcurrent fault detection or short−circuit condition. The current sense signal is blanked with a shorter LEB duration, t_{LEB2}, typically 120 ns, before applying it to the short−circuit comparator. The voltage threshold of this extra comparator, $V_{CS(stop)}$, is typically 1.2 V, set 50% higher than V_{ILIM}. This is to avoid interference with normal operation. Four consecutive abnormal overcurrent faults cause the controller to enter in auto−recovery mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the fault overcurrent comparator or after double hiccup sequence or if the power supply is unplugged with a new startup sequence after the initial power on reset.

Jittering Capability

In order to help meet the EMI requirements, the NCP1362 features the jittering capability to average the spectrum rays over the frequency range. The function consists of adding a voltage ripple to the peak current information in order to change the operation frequency. The peak−to−peak amplitude of the ripple waveform is 60 mV at 1.5 kHz.

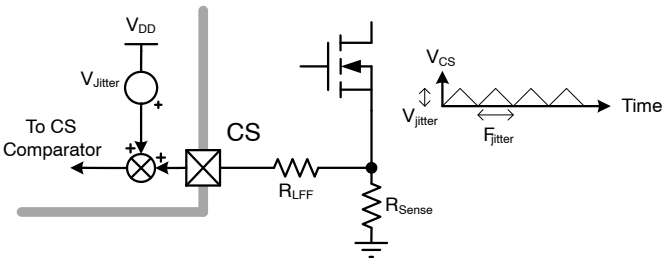


Figure 39. Frequency Jittering

Fault Mode and Protection

- *CS Pin:* at each startup, a 60−µA (I_{CS}) current source pulls up the CS pin to disable the controller if the pin is left open or grounded. Then the controller enters in a double hiccup mode.
- *V_S/ZCD Pin:* after sending the first drive pulse the controller checks the correct wiring of V_S/ZCD pin: after the ZCD blanking time, if there is an open or short conditions, the controller enters in double hiccup mode.

Brown−out Function

The Brown−out circuitry offers a way to protect the application from operation under too low input voltage. The controller allows the output pulses, only if the input voltage is above $V_{BO(on)}$ level. An extra comparator detects if the BO pin is grounded for disabling the BO feature. The internal circuitry, depicted by Figure 40, offers a way to observe the bulk voltage.

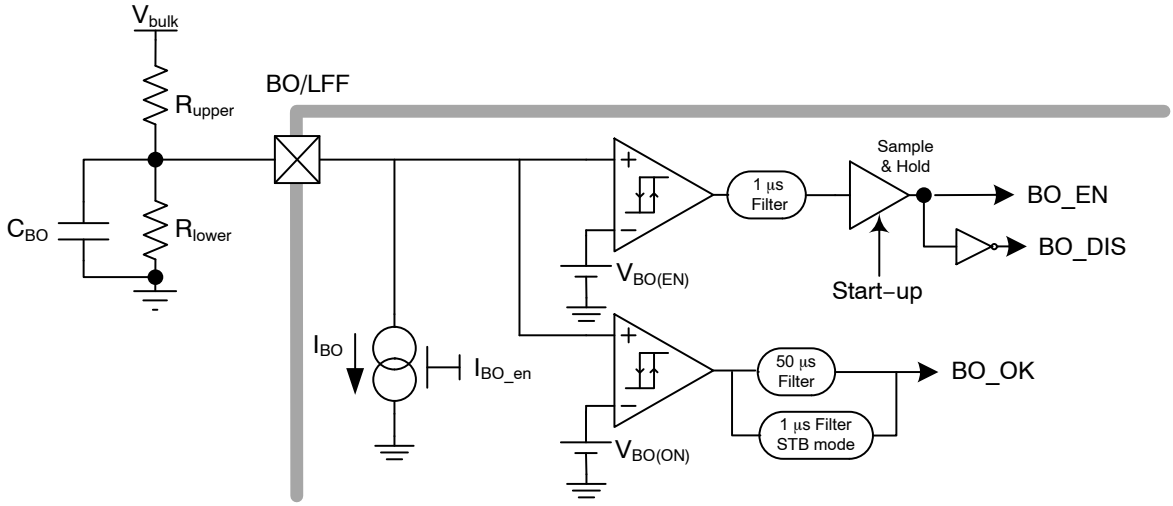


Figure 40. Internal Brown−out Configuration

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The following figures illustrate the behavior of the Brown−out pin:

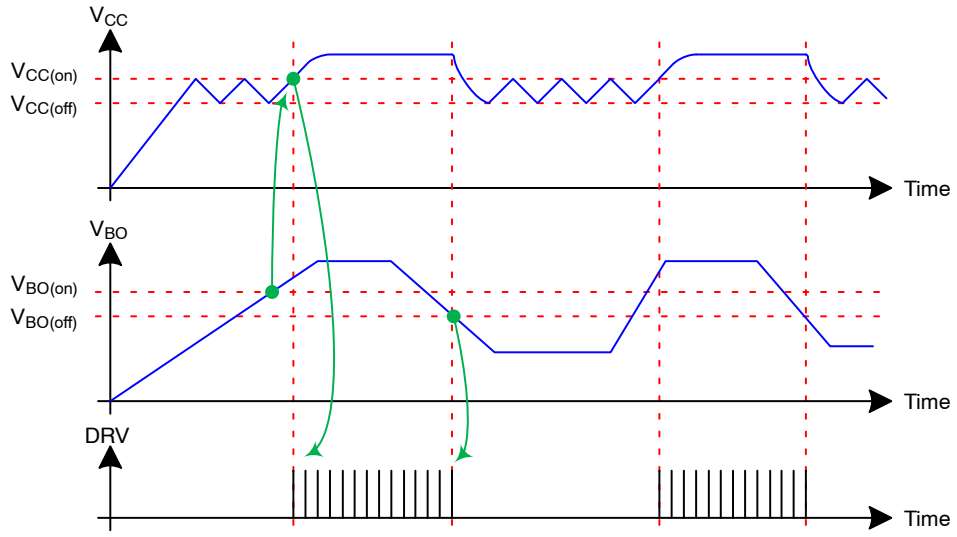


Figure 41. Brown−out Input Functionality − $V_{CC} < V_{CC(on)}$

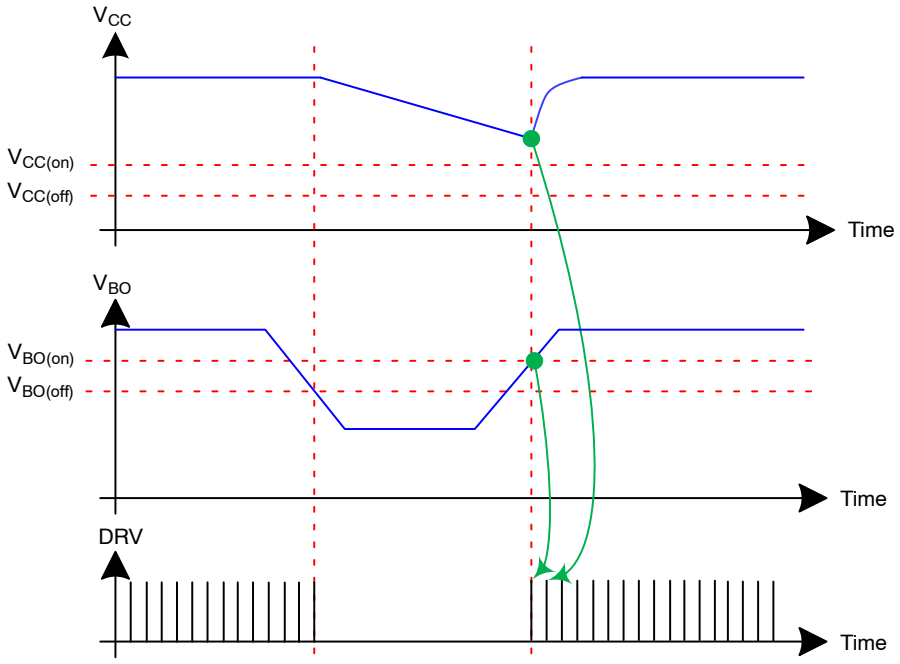


Figure 42. Brown−out Input Functionality − $V_{CC} > V_{CC(on)}$

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Calculation of the resistors divider:

$$R_{lower} = R_{upper} \times \frac{V_{BO(on)}}{V_{bulk} - V_{BO(on)}} \quad \text{(eq. 18)}$$

If the power supply must start pulsing at V_{in} = 80 V rms (V_{bulk} = 113 V) with a selected R_{upper} = 10 MΩ:

$$R_{lower} = 10\ M \times \frac{0.8}{113 - 0.8} = 71.2\ k\Omega \quad \text{(eq. 19)}$$

With a selected 71.5−kΩ normalized ±1% resistor for R_{lower}, it is now possible to calculate all the bulk levels versus the internal voltage references of the BO pin.

Table 6. EXAMPLE OF BROWN−OUT LEVELS WITH R_{lower} = 71.5 kΩ & R_{upper} = 10 MΩ

Parameters	BO Pin Level (V)	Bulk Level (V)	V_{in} Level (V rms)
$V_{BO(en)}$	0.1	14.0	10
$V_{BO(on)}$	0.8	112.7	79.7
$V_{BO(off)}$	0.7	98.6	69.7

These resistances have to be adjusted after measurements according to the bulk capacitor ripple and also the capacitor connected on the BO pin.

There is the possibility for the customer to disable the BO protection if this function is not needed. To implement this feature, the BO pin voltage is checked when V_{CC} crosses $V_{CC(on)}$ threshold. If the BO voltage is still below $V_{BO(EN)}$ after the $V_{CC(on)}$, the BO function is disabled.

Line Feed Forward

Sensing input line voltage via BO pin allows to generate a current to CS pin directly proportional to the input line level in order to compensate the over current on CS pin due to the propagation delay. The resistor in series with the CS pin adjusts the compensation level.

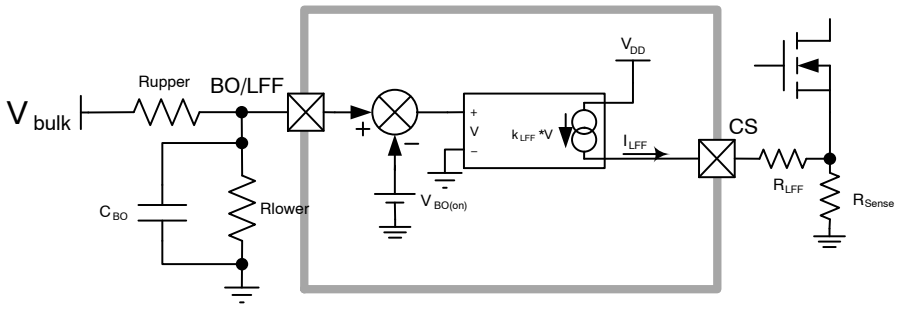


Figure 43. Internal Line Feed Forward Configuration

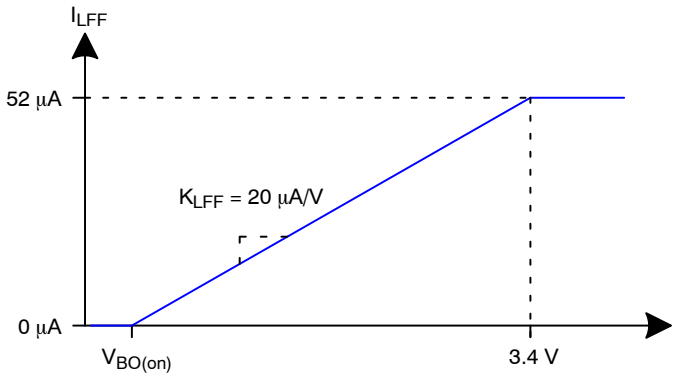


Figure 44. Transfer Function of the Line Feed Forward

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Calculation of the resistor (R_{LFF}) for compensating the overpower.

Let's assume the power supply needs to have a compensation of 45 mV (V_{LFF}) at 265 V rms (V_{in}).

First, it is needed to calculate what is the BO level corresponding to the line voltage (here 265 V rms) of the desired compensation level:

$$V_{BO_LFF} = V_{bulk} \times \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 20)}$$

Then, the resistor value to be inserted between the CS resistor and CS pin could be calculated, as illustrated here after:

$$R_{LFF} = \frac{V_{LFF}}{K_{LFF} \times \left(V_{BO_LFF} - V_{BO(on)}\right)} \quad \text{(eq. 21)}$$

Numerical application yields:

$$V_{BO_LFF} = 265\sqrt{2} \times \frac{71.5\ k}{71.5\ k + 10\ M} = 2.66\ V \quad \text{(eq. 22)}$$

$$R_{LFF} = \frac{45\ mV}{20\ \frac{\mu A}{V} \times (2.66\ V - 0.8\ V)} = 1.2\ k\Omega \quad \text{(eq. 23)}$$

The offset voltage can affect the standby power performance by reducing the peak current setpoint in light−load conditions. For this reason, it is desirable to cancel its action as soon as the VCO mode occurs. A typical curve variation is shown in Figure 45. At low power, below the VCO mode starting point, the LFF current is linearly absorbed and no offset is created through the CS pin when the Comp pin voltage is below 1.6 V. When feedback increases again and reaches the 1.6−V threshold, OPP starts to build up and reaches its full value at 1.9 V.

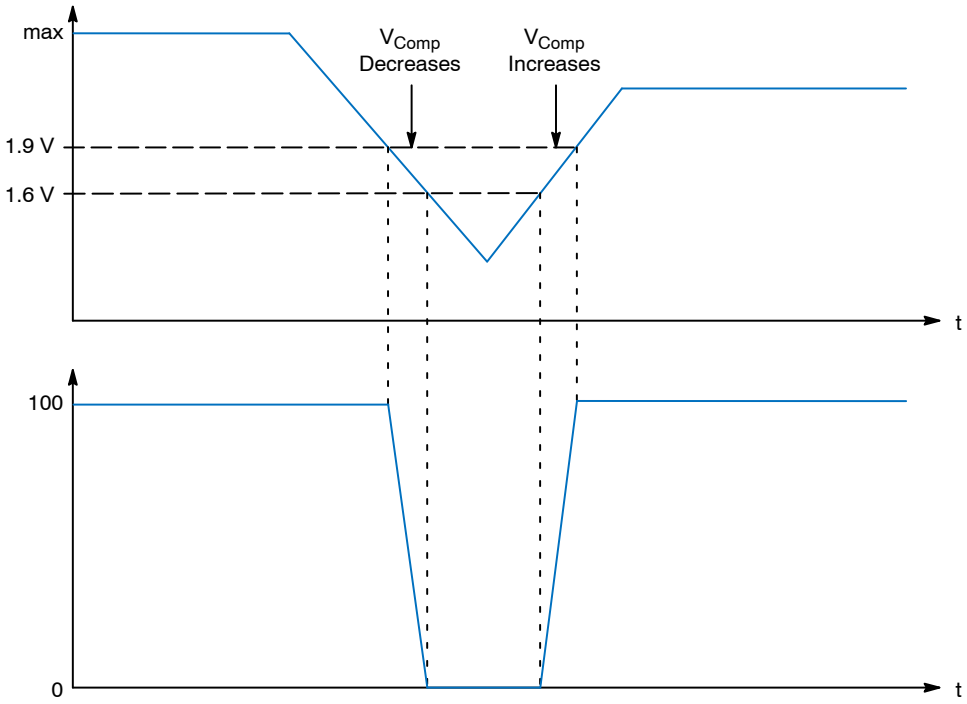


Figure 45. The LFF Current is Applied when the Comp Voltage Exceeds 1.6 V. It is 0 below it

Fault Input

The NCP1362 includes a dedicated fault input accessible via the Fault pin. Figure 46 shows the architecture of the Fault input. The controller can be latched by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 3.0 V. An active clamp prevents the Fault pin voltage from reaching the $V_{Fault(OVP)}$ if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp.

$$\frac{V_{Fault(OVP)} - V_{Fault(clamp)}}{R_{Fault(clamp)}} = \frac{3\ V - 1.35\ V}{1.35\ k\Omega}, \quad \text{(eq. 24)}$$

i.e. approximately 1.2 mA.

This function is typically used to detect a V_{CC} or auxiliary winding overvoltage by means of a Zener diode generally in series with a small resistor (see Figure 46).

Neglecting the resistor voltage drop, the OVP threshold is then:

$$V_{AUX(OVP)} = V_Z + V_{Fault(OVP)} \quad \text{(eq. 25)}$$

where V_Z is the Zener diode voltage.

The controller can also be latched off if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP)}$, typically 0.4 V. This capability is normally used for detecting an overtemperature fault by means of an NTC

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thermistor. A pull up current source $I_{Fault(OTP)}$, (typically 45 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP)}$.

The circuit detects an overtemperature situation when:

$$R_{NTC} \times I_{Fault(OVP)} = V_{Fault(OVP)} \quad \text{(eq. 26)}$$

Hence, the OTP protection trips when

$$R_{NTC} = \frac{V_{Fault(OVP)}}{I_{Fault(OTP)}} \quad \text{(eq. 27)}$$

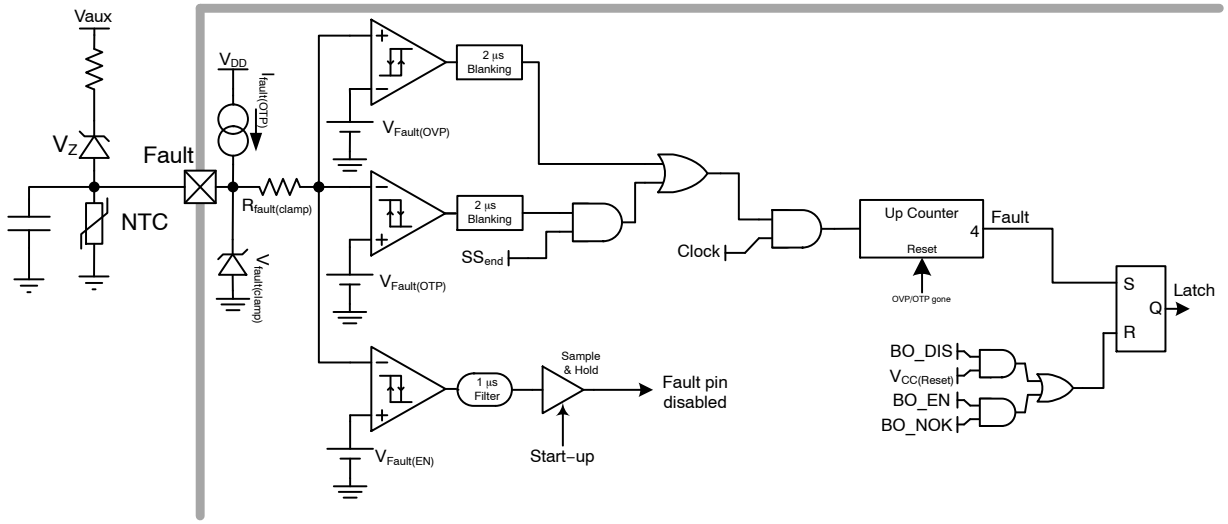


Figure 46. Fault Detection Schematic

As a matter of fact, the controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Upper and lower fault detector have blanking delays to prevent noise from triggering them. Both OVP and OTP comparator output are validated only if its high−state duration lasts a minimum of 2 μs. Below this value, the event is ignored. Then, a counter ensures that OVP/OTP events occurred for 4 successive drive clock pulses before actually latching the part.

When the part is latched−off, the drive is immediately turned off and V_{CC} goes in endless hiccup mode. The power supply needs to be un−plugged to reset the part as a result of a BO_NOK (BO fault condition) if Brown−Out feature is enabled otherwise $V_{CC(Reset)}$.

There is the possibility for the customer to disable the fault pin protection if this function is not needed or to reduce the IC consumption in stand−by mode. To implement this feature, the fault pin voltage is checked when V_{CC} crosses $V_{CC(on)}$ threshold. If the voltage is still below $V_{Fault(EN)}$ after the $V_{CC(on)}$, the fault pin is disabled.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{Fault(OTP)}$. This current source is enabled once V_{CC} reaches $V_{CC(on)}$. A bypass capacitor is usually connected between the Fault and GND pins. It will take some time for V_{Fault} to reach its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during soft−start.

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of controller die of the IC. The controller is disabled if its junction temperature exceeds the thermal shutdown threshold (T_{SHDN}). A continuous V_{CC} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below T_{SHDN} reduced by the thermal shutdown hysteresis ($T_{SHDN(off)}$). The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$. A new power up sequences commences at the next $V_{CC(on)}$ once all the faults are removed.

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Table 7. ORDERING TABLE OPTION

OPN # NCP1362_ _	Minimum Switching Frequency in VCO Mode (kHz)		Maximum Switching Frequency (kHz)				Jittering Frequency	
	0.2	1	No	80	110	140	Enable	Disable
NCP1362AADR2G		x	x				x	
NCP1362ABDR2G		x			x		x	

Table 8. ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
NCP1362AADR2G	P1362AA	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1362ABDR2G	P1362AB		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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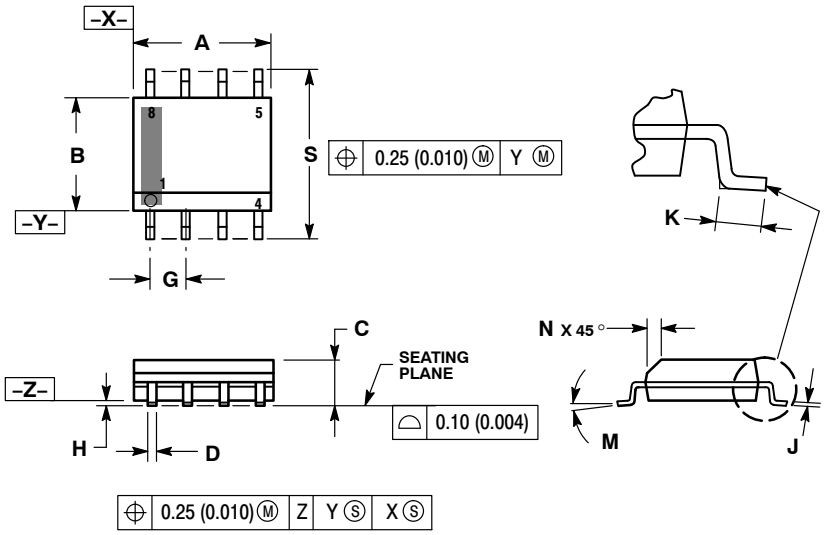
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

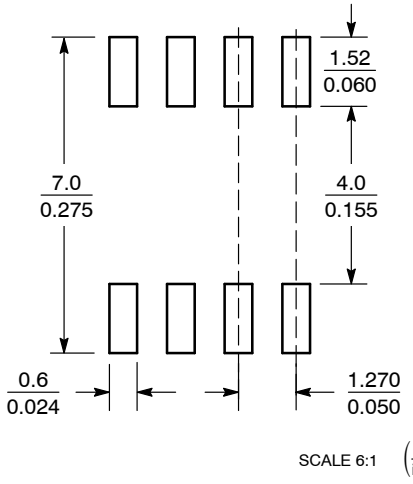
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

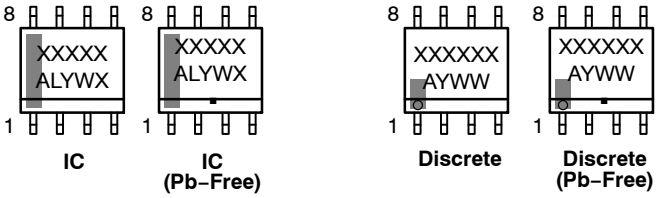
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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