Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_A = +25°C
-30V	7.5mΩ @ V_{GS} = -10V	-36A
	10mΩ @ V_{GS} = -4.5V	-31A

Description

This new generation 30V P-Channel Enhancement Mode MOSFET is designed to minimize $R_{DS(ON)}$, yet maintain superior switching performance. This device is ideal for use in notebook battery power management and loadswitch.

Applications

- Notebook Battery Power Management
- DC-DC Converters
- Loadswitch

Features

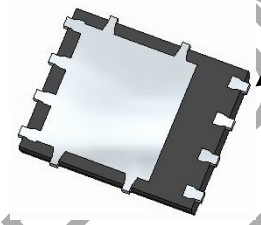
- Thermally Efficient Package – Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- ESD HBM Protected up to 1kV
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **An Automotive-Compliant Part is Available Under Separate Datasheet (DMP3010LPSQ)**

Mechanical Data

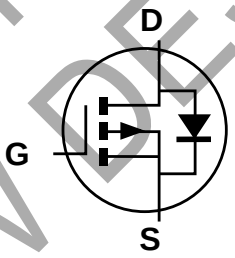
- Case: PowerDI® 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

PowerDI5060-8

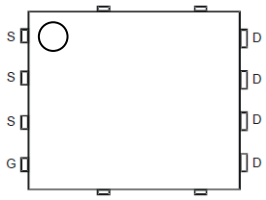
Top View



Bottom View



Internal Schematic



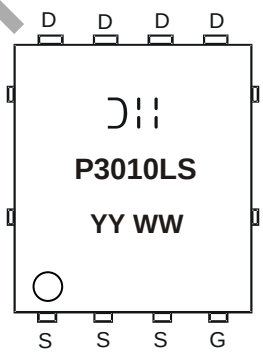
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DMP3010LPS-13	Standard	PowerDI5060-8	2,500/Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



DH = Manufacturer's Marking
P3010LS = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 17 = 2017)
WW = Week (01 to 53)

PowerDI is a registered trademark of Diodes Incorporated.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 7) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-36 -29	A
Continuous Drain Current (Note 7) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-31 -25	A
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-14.5 -11.5	A
Pulsed Drain Current (Notes 6 & 9)			I_{DM}	-100	A
Avalanche Current (Notes 10 & 11)			I_{AS}	-17.5	A
Avalanche Energy (Notes 10 & 11) L = 1mH			E_{AS}	153	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	1.26	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 5)	$R_{\theta JA}$	97	°C/W
Power Dissipation (Note 6)	P_D	2.18	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{\theta JA}$	55	°C/W
Power Dissipation (Note 7)	P_D	14.37	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 7)	$R_{\theta JA}$	8.7	°C/W
Power Dissipation (Notes 7 & 8)	P_D	58.7	W
Thermal Resistance, Junction to Case @T_C = +25°C (Notes 7 & 8)	$R_{\theta JC}$	2.13	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	µA	V_{DS} = -30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.1	-1.6	-2.1	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	5.7	7.5	mΩ	V_{GS} = -10V, I_D = -10A
		—	7.2	10		V_{GS} = -4.5V, I_D = -10A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	30	—	S	V_{DS} = -15V, I_D = -10A
Diode Forward Voltage	V_{SD}	—	-0.65	-1.0	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	6,234	—	pF	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	1,500	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	774	—	pF	
Gate Resistance	R_g	—	1.28	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -10V)	Q_g	—	126.2	—	nC	V_{DS} = -15V, I_D = -10A
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	59.2	—	nC	V_{DS} = -15V, V_{GS} = -4.5V, I_D = -10A
Gate-Source Charge	Q_{gs}	—	16.1	—	nC	
Gate-Drain Charge	Q_{gd}	—	15.7	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	11.4	—	ns	V_{DS} = -15V, V_{GEN} = -10V, R_G = 6Ω, I_D = -1A
Turn-On Rise Time	t_R	—	9.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	260.7	—	ns	
Turn-Off Fall Time	t_F	—	99.3	—	ns	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Device mounted on FR-4 PCB with infinite heatsink.
8. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
9. Repetitive rating, pulse width limited by junction temperature, 10s pulse, duty cycle = 1%.
10. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
11. Short duration pulse test used to minimize self-heating effect.
12. Guaranteed by design. Not subject to product testing.

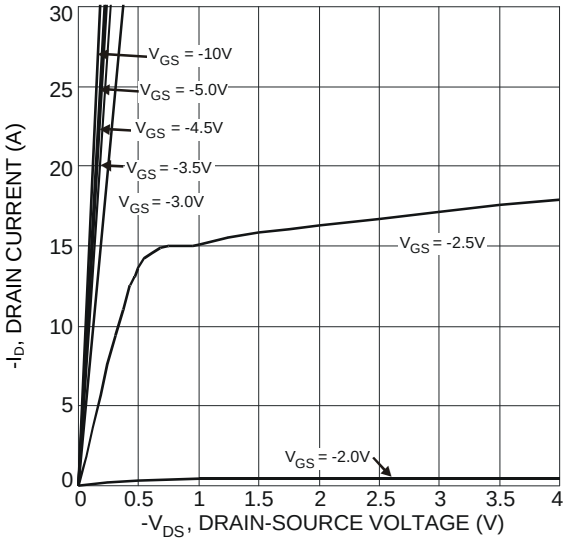


Fig. 1 Typical Output Characteristic

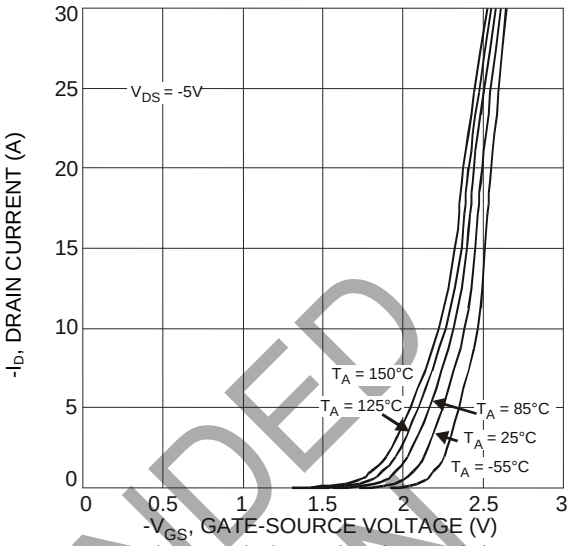


Fig. 2 Typical Transfer Characteristic

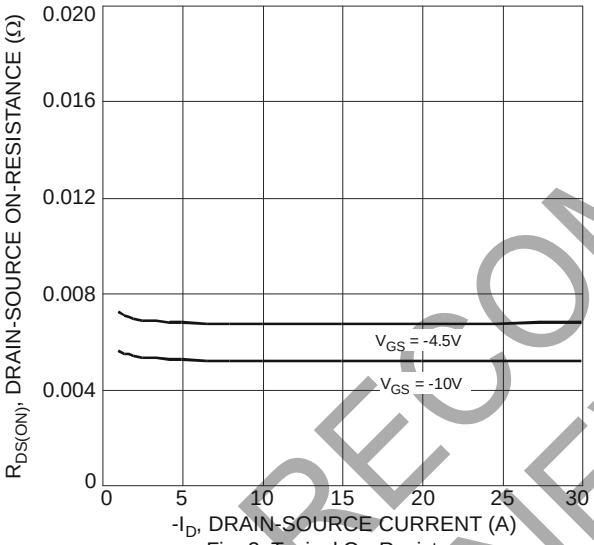


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

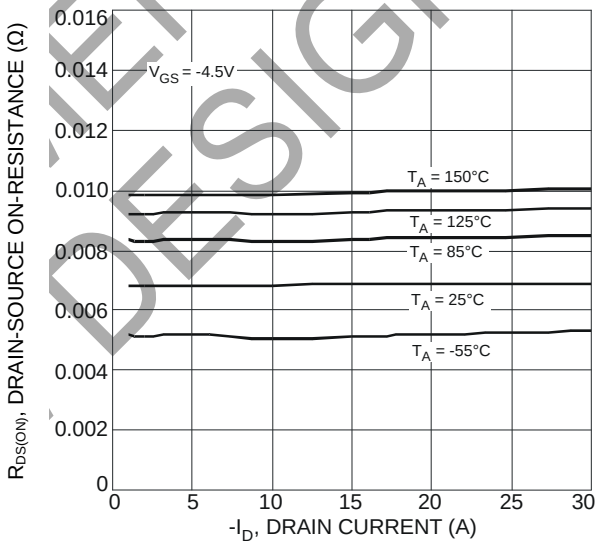


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

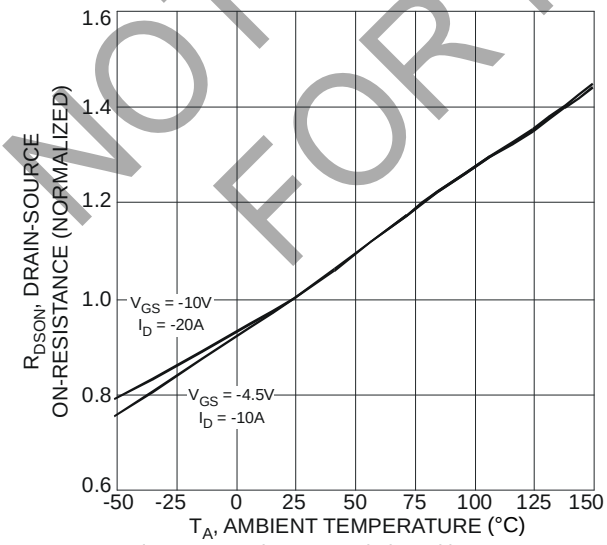


Fig. 5 On-Resistance Variation with Temperature

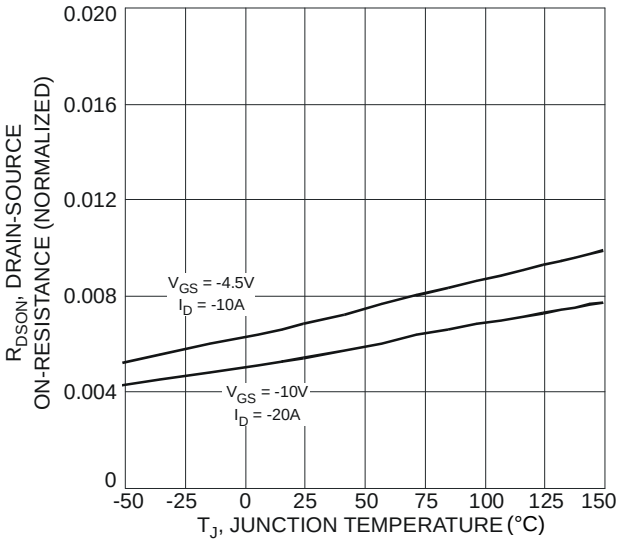


Fig. 6 On-Resistance Variation with Temperature

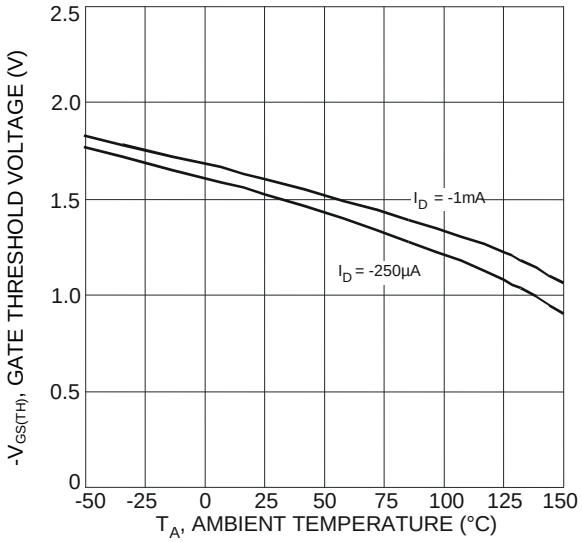


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

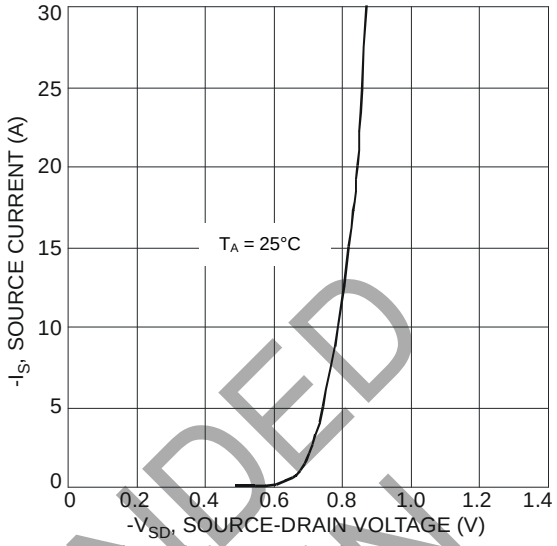


Fig. 8 Diode Forward Voltage vs. Current

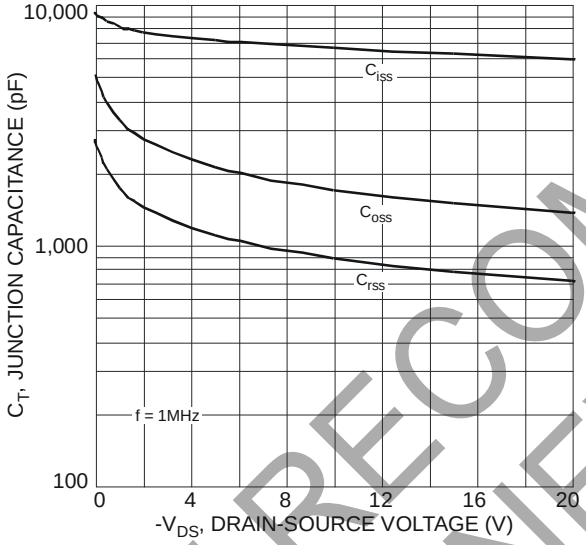


Fig. 9 Typical Total Capacitance

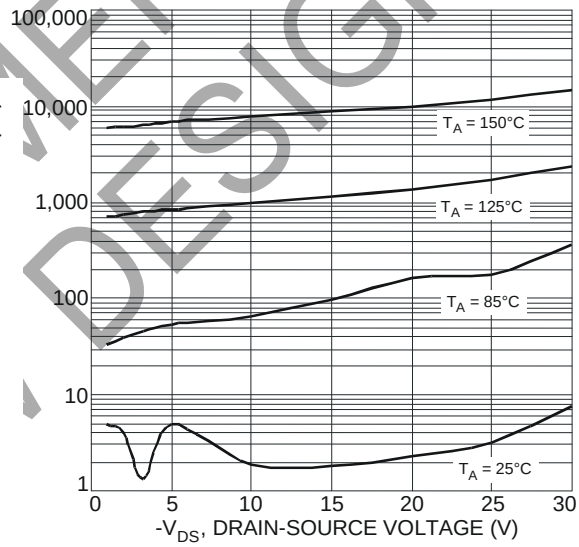


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

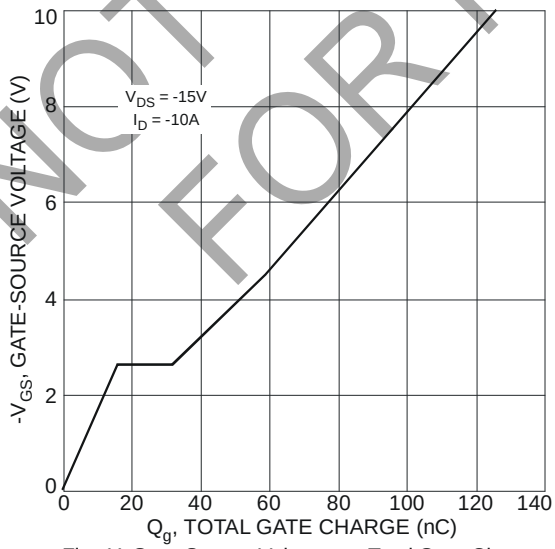


Fig. 11 Gate-Source Voltage vs. Total Gate Charge

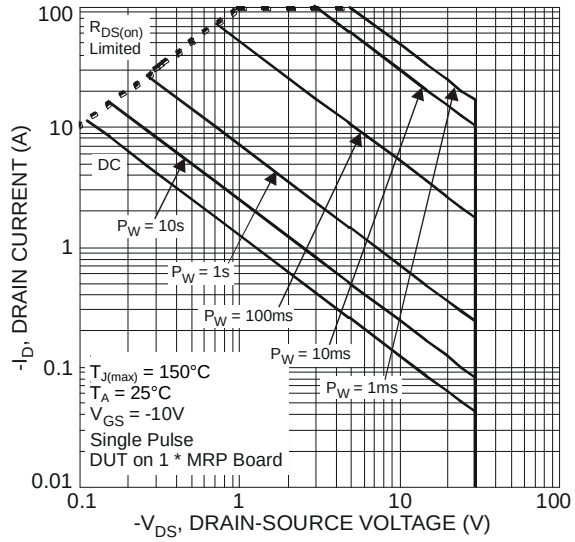


Fig. 12 SOA, Safe Operation Area

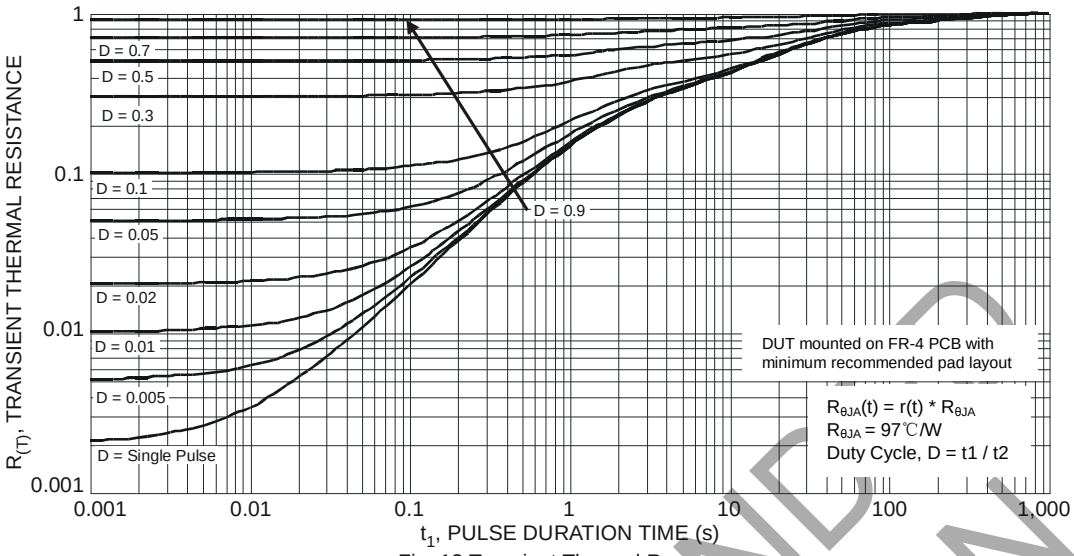
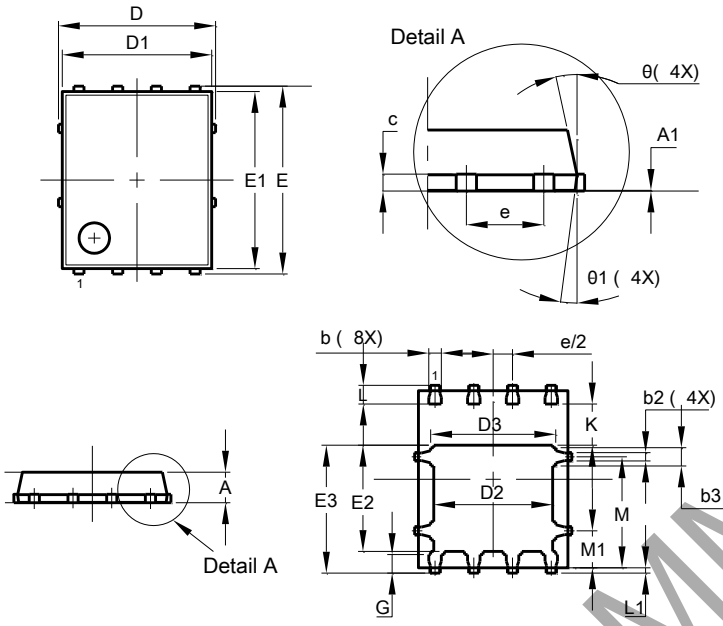


Fig. 13 Transient Thermal Response

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

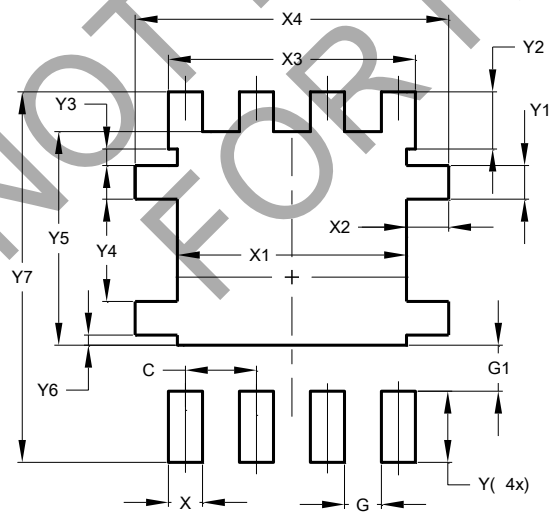


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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