STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME **Over Voltage Protection Controller with Internal FET**

MODEL NAME **BD6044GUL**

BLOCK DIAGRAM See Figure 1

PACKAGE DIMENSIONS See Figure 2

FEATURES

- ●Overvoltage Protection up to 36V
- ●Internal Low Ron (125mΩ) FET
- ●Over voltage Lockout (OVLO)
- ●Under voltage Lockout(UVLO)
- ●Internal 2msec Startup Delay
- ●Over Current Protect
- ●Thermal Shut Down
- ●Small package: VCSP50L1(1.6mm x 1.6mm, height=0.55mm)

※This product is not especially designed to be protected from radioactivity.

● Absolute maximum ratings (Ta=25℃)

Contents	Symbol	Rating	Unit	Conditions
Input supply voltage 1	Vmax1	-0.3～36	V	IN1, IN2, IN3, IN4
Input supply voltage 2	Vmax2	-0.3～7	V	other
Power dissipation	Pd	725	mW	
Operating temperature range	Topr	-35～+85	℃	
Storage temperature range	Tstr	-55～+150	℃	

※1 When using more than at Ta=25℃, it is reduced 5.8 mW per 1℃.
ROHM specification board 50mm × 58mm mounting.

● Recommended operating range (Ta=-35～+85℃)

Parameter	Symbol	Range	Unit	Usage
Input voltage range	V_{in}	2.2～34	V	

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● Electrical Characteristics

(Unless otherwise noted, Ta = 25°C, IN=5V)

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
● ELECTRICAL						
Input Voltage Range	VIN	-	-	34	V	
Supply Quiescent Current 1	ICC1	-	45	90	μA	IN=5V, EN=L
Supply Quiescent Current 2	ICC2	-	60	120	μA	IN=5V, EN=H
Under Voltage Lockout	UVLO	2.53	2.65	2.77	V	IN=decreasing
Under Voltage Lockout Hysteresis	UVLOh	50	100	150	mV	IN=increasing
Over Voltage Lockout	OVLO	6.2	6.4	6.6	V	IN=increasing
Over Voltage Lockout Hysteresis	OVLOh	50	100	150	mV	IN=decreasing
Current limit	ILM	1.2	2	3	A	
Vin vs. Vout Res.	RON	-	125	150	mΩ	
FLGB Output Low Voltage	FLGBVO	-	-	400	mV	SINK=1mA
FLGB Leakage Current	FLGBleak	-	-	1	μA	
EN input voltage (H)	ENH	1.45	-	-	V	
EN input voltage (L)	ENL	-	-	0.5	V	
EN input current	ENC	12	25	50	μA	EN=1.5V
● TIMINGS (FLGB pull up resistance 100kΩ)						
Start Up Delay	Ton	-	2	4	msec	
Output Turn Off Time	Toff	-	2	10	μsec	
Alert Delay	Tovp	-	1.5	10	μsec	

* This product is not especially designed to be protected from radioactivity.

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● Block Diagram

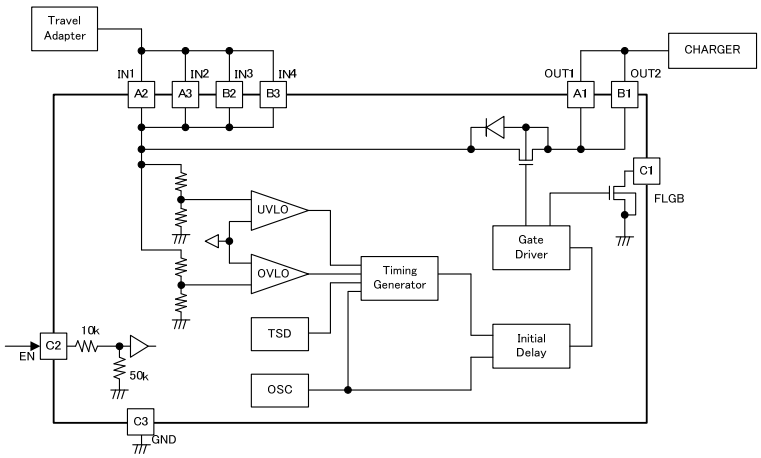


Figure1. Block Diagram

● PIN number/PIN name

Pin number	Pin name
A2	IN1
A3	IN2
B2	IN3
B3	IN4
A1	OUT1
B1	OUT2
C3	GND
C1	FLGB
C2	EN

● PIN DESCRIPTIONS

PIN	NAME	FUNCTION
A2, A3 B2, B3	IN1, 2, 3, 4	Input voltage Pin. A 1μF low ESR capacitor, or larger must be connected between this pin and GND
A1, B1	OUT1, 2	Output Voltage Pin
C1	FLGB	Active-low open drain output to signal if the adapter voltage is correct
C3	GND	Ground Pin
C2	EN	Enable input Drive EN high to turn off OUT (Hi-z output)

● Package Dimensions (VCSP50L1)

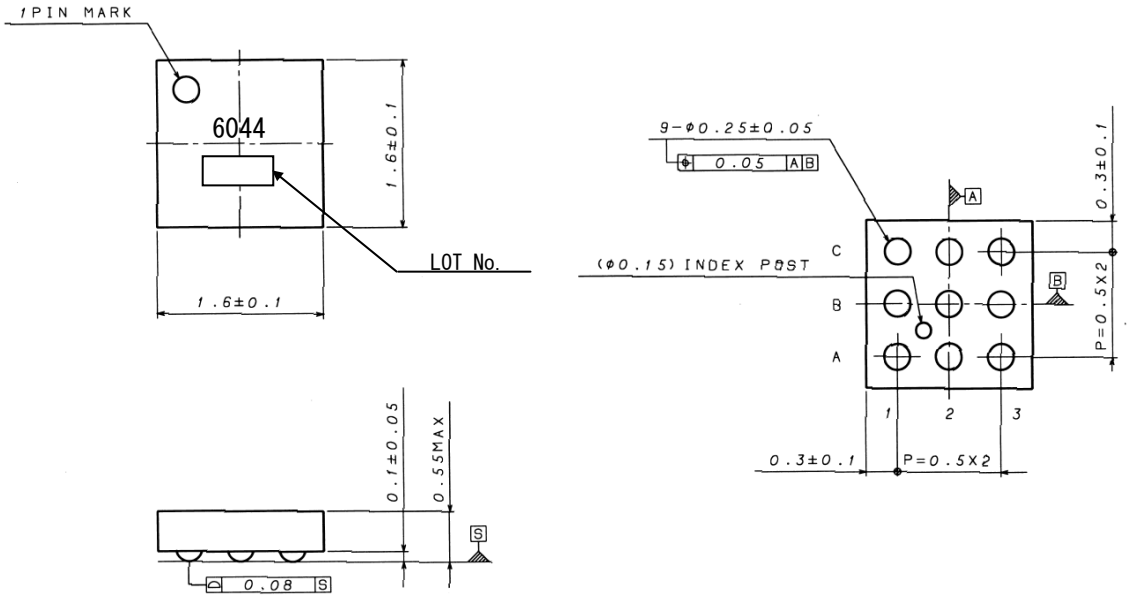


Figure2. Package

●Use-related Cautions

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(1) Absolute maximum ratings
If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range
This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector
There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines
In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage
Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation
When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields
Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board
When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins
Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern
When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors
When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)
When the junction temperature reaches the defined value, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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