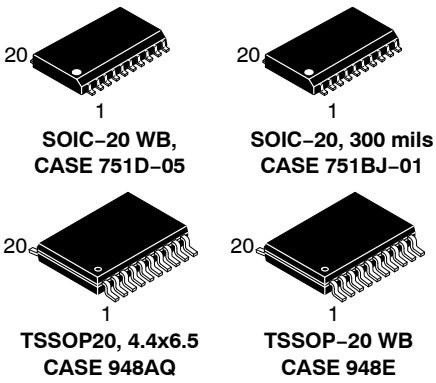
# Octal 3-STATE Transceiver

# MM74HC245A




SOIC−20 WB, CASE 751D−05

SOIC−20, 300 mils CASE 751BJ−01

TSSOP20, 4.4x6.5 CASE 948AQ

TSSOP−20 WB CASE 948E

### General Description

The MM74HC245A 3−STATE bidirectional buffer utilizes advanced silicon−gate CMOS technology, and is intended for two−way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device has an active LOW enable input G and a direction control input, DIR. When DIR is HIGH, data flows from the A inputs to the B outputs. When DIR is LOW, data flows from the B inputs to the A outputs. The MM74HC245A transfers true data from one bus to the other.

This device can drive up to 15 LS−TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to VCC and ground.

### Features

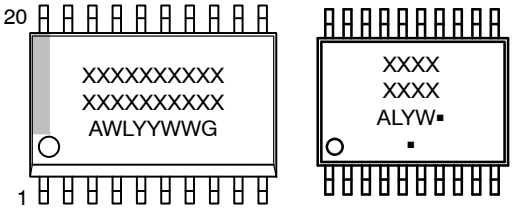
- Typical Propagation Delay: 13 ns
- Wide Power Supply Range: 2 V to 6 V
- Low Quiescent Current: 160 μA Maximum (74HC)
- 3−STATE Outputs for Connection to Bus Oriented Systems
- High Output Current: 6 mA (Minimum)
- Same as the 645
- These are Pb−Free Devices

### TRUTH TABLE

| Control Inputs | | |
|---|---|---|
| $\overline{G}$ | DIR | Operation |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

NOTE: H = HIGH Level
L = LOW Level
X = Irrelevant

### MARKING DIAGRAM

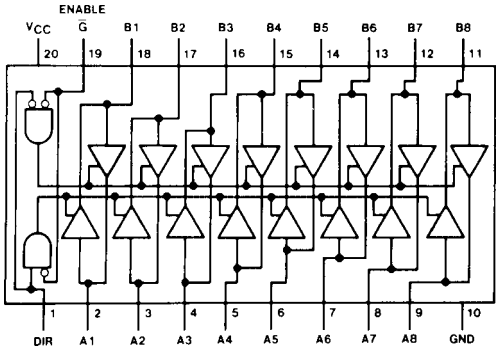



XXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ▪ = Pb−Free Package

(Note: Microdot may be in either location)

### CONNECTION DIAGRAM

Pin Assignment for SOIC and TSSOP




(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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## Logic Diagram

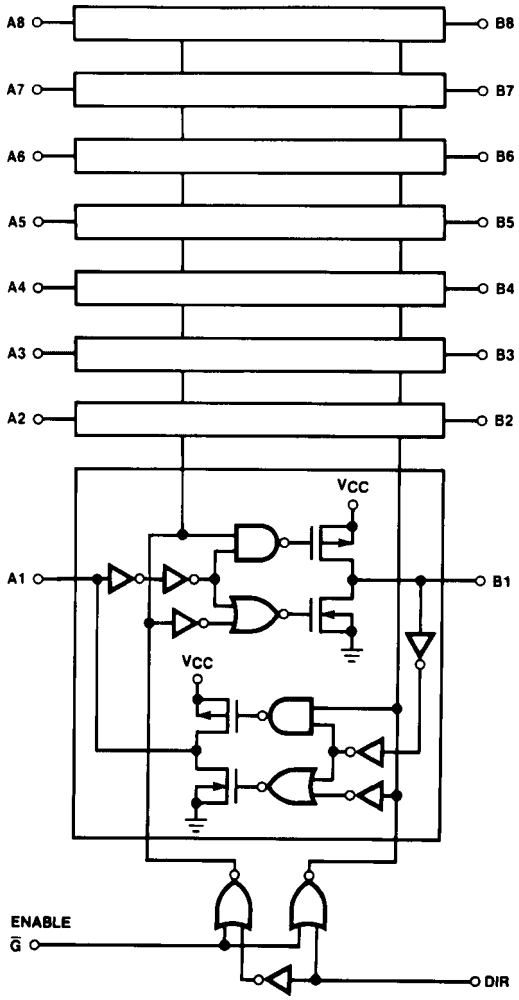



**Figure 1. Logic Diagram**

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +6.5 | V |
| $V_{IN}$ | DC Input Voltage DIR and $\overline{G}$ pins | −0.5 to $V_{CC}$ +0.5 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input/Output Voltage | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{CD}$ | Clamp Diode Current | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per pin | ±35 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current, per pin | ±70 | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | °C |
| $P_D$ | Power Dissipation SOIC<br>TSSOP | 1302<br>833 | mW |
| $T_L$ | Lead Temperature (Soldering 10 seconds) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.



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## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2 | 6 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise/Fall Times | $V_{CC}$ = 2.0 V | − | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | − | 500 | |
| | | $V_{CC}$ = 6.0 V | − | 400 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 2)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | $T_A$ = −40°C to 85°C | $T_A$ = −55°C to 125°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0 | − | 1.50 | 1.50 | 1.50 | V |
| | | | 4.5 | − | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | − | 4.20 | 4.20 | 4.20 | |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0 | − | 0.50 | 0.50 | 0.50 | V |
| | | | 4.5 | − | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | − | 1.80 | 1.80 | 1.80 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\lvert I_{OUT}\rvert \le$ 20 μA | 2.0 | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\lvert I_{OUT}\rvert \le$ 6.0 mA | 4.5 | 4.20 | 3.98 | 3.84 | 3.70 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\lvert I_{OUT}\rvert \le$ 7.8 mA | 6.0 | 5.70 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\lvert I_{OUT}\rvert \le$ 20 μA | 2.0 | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\lvert I_{OUT}\rvert \le$ 6.0 mA | 4.5 | 0.20 | 0.26 | 0.33 | 0.40 | |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\lvert I_{OUT}\rvert \le$ 7.8 mA | 6.0 | 0.20 | 0.26 | 0.33 | 0.40 | |
| $I_{IN}$ | Input Leakage Current ($\overline{G}$ and DIR) | $V_{IN}$ = $V_{CC}$ or GND | 6.0 | − | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum 3−STATE Output Leakage Current | $V_{OUT}$ = $V_{CC}$ or GND Enable $\overline{G}$ = $V_{IH}$ | 6.0 | − | ±0.5 | ±5.0 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 μA | 6.0 | − | 8.0 | 80 | 160 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of 5 V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0 V values should be used.



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## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5 V, $T_A$ = 25°C, $t_r$ = $t_f$ = 6 ns)

| Symbol | Parameter | Conditions | Typ. | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L$ = 45 pF | 12 | 17 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Output Enable Time | $R_L$ = 1 kΩ, $C_L$ = 45 pF | 24 | 35 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Output Disable Time | $R_L$ = 1 kΩ, $C_L$ = 5 pF | 18 | 25 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.0 V to 6.0 V, $C_L$ = 50 pF, $t_r$ = $t_f$ = 6 ns, unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | $T_A$ = −40°C to 85°C | $T_A$ = −55°C to 125°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L$ = 50 pF | 2.0 | 31 | 90 | 113 | 135 | ns |
| | | $C_L$ = 150 pF | | 41 | 96 | 116 | 128 | |
| | | $C_L$ = 50 pF | 4.5 | 13 | 18 | 23 | 27 | |
| | | $C_L$ = 150 pF | | 17 | 22 | 28 | 33 | |
| | | $C_L$ = 50 pF | 6.0 | 11 | 15 | 19 | 23 | |
| | | $C_L$ = 150 pF | | 14 | 19 | 23 | 28 | |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time | $R_L$ = 1 kΩ | | | | | | ns |
| | | $C_L$ = 50 pF | 2.0 | 71 | 190 | 240 | 285 | |
| | | $C_L$ = 150 pF | | 81 | 240 | 300 | 360 | |
| | | $C_L$ = 50 pF | 4.5 | 26 | 38 | 48 | 57 | |
| | | $C_L$ = 150 pF | | 31 | 48 | 60 | 72 | |
| | | $C_L$ = 50 pF | 6.0 | 21 | 32 | 41 | 48 | |
| | | $C_L$ = 150 pF | | 25 | 41 | 51 | 61 | |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Output Disable Time | $R_L$ = 1 kΩ, $C_L$ = 50 pF | 2.0 | 39 | 135 | 169 | 203 | ns |
| | | | 4.5 | 20 | 27 | 34 | 41 | |
| | | | 6.0 | 18 | 23 | 29 | 34 | |
| $t_{TLH}$, $t_{THL}$ | Output Rise and Fall Time | $C_L$ = 50 pF | 2.0 | 20 | 60 | 75 | 90 | ns |
| | | | 4.5 | 6 | 12 | 15 | 18 | |
| | | | 6.0 | 5 | 10 | 13 | 15 | |
| $C_{PD}$ | Power Dissipation Capacitance (Note 3) | $\overline{G}$ = $V_{IL}$ | | 50 | – | – | – | pF |
| | | $\overline{G}$ = $V_{IH}$ | | 5 | | | | |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |
| $C_{IN/OUT}$ | Maximum Input/Output Capacitance, A or B | | | 15 | 20 | 20 | 20 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



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## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| MM74HC245AWM | HC245A | SOIC−20 WB<br>(Pb−Free) | 38 Units / Tube |
| MM74HC245AWMX | HC245A | SOIC−20<br>(Pb−Free) | 1000 / Tape & Reel |
| MM74HC245AMTC | HC<br>245A | TSSOP−20 WB<br>(Pb−Free) | 75 Units / Tube |
| MM74HC245AMTCX | HC<br>245A | TSSOP−20<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

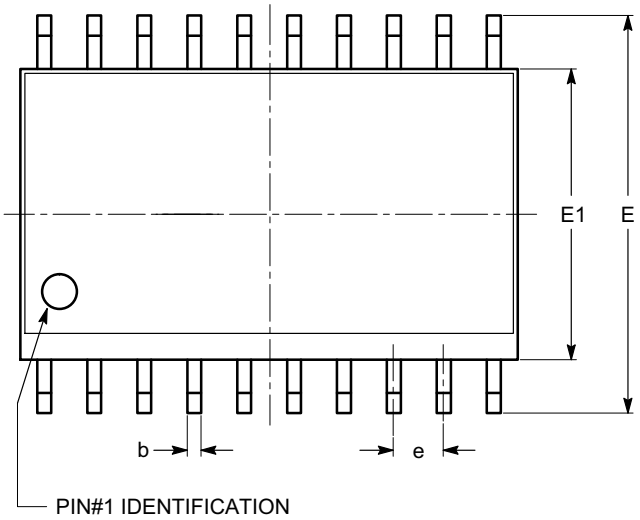


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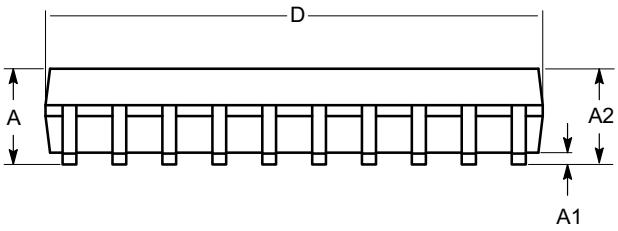
**SOIC−20, 300 mils**
CASE 751BJ
ISSUE O

DATE 19 DEC 2008

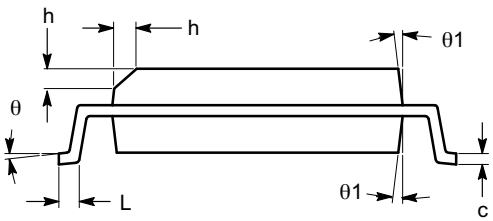



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.36 | 2.49 | 2.64 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.27 | 0.33 |
| D | 12.60 | 12.80 | 13.00 |
| E | 10.01 | 10.30 | 10.64 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.75 |
| L | 0.40 | 0.81 | 1.27 |
| θ | 0° | | 8° |
| θ1 | 5° | | 15° |




**SIDE VIEW**




**END VIEW**

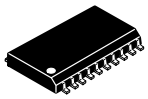
**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

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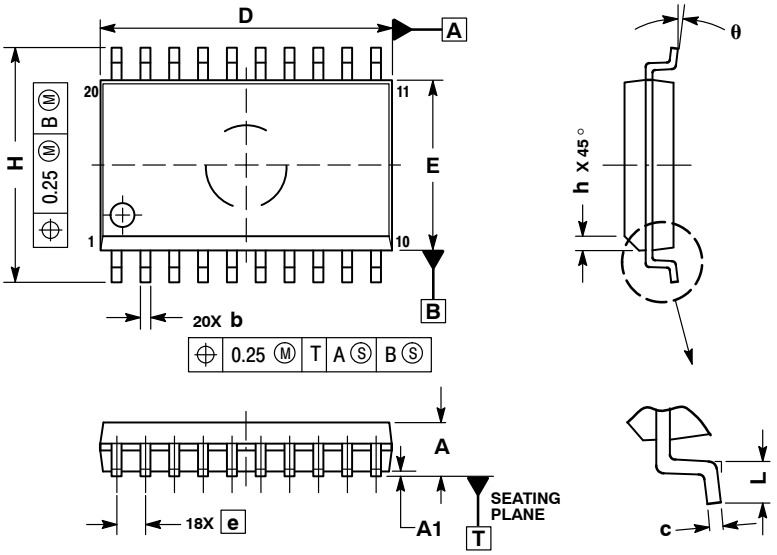
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**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015

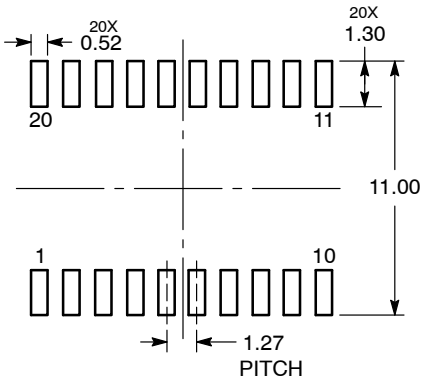
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

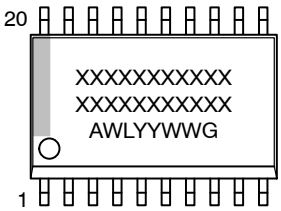
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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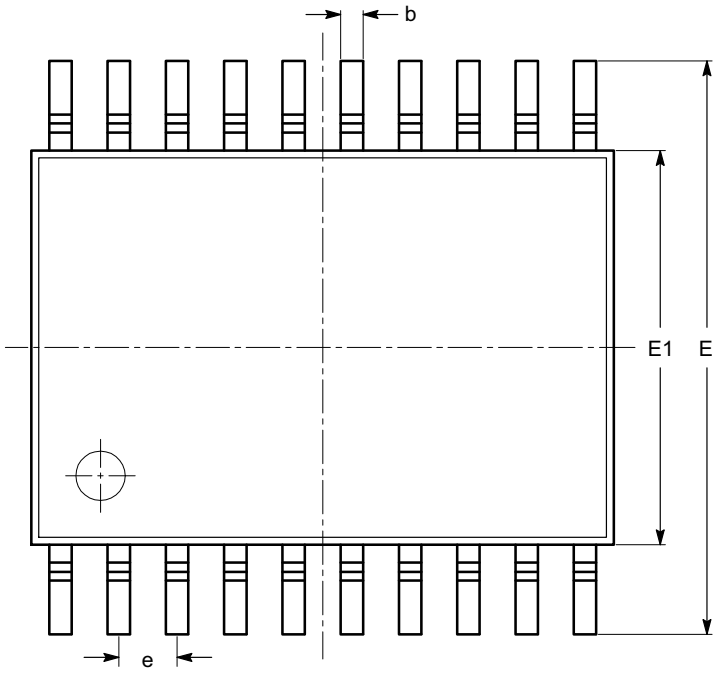
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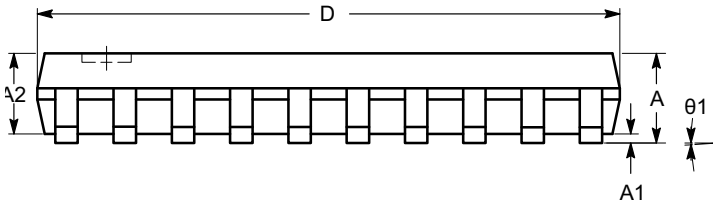
**TSSOP20, 4.4x6.5**
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

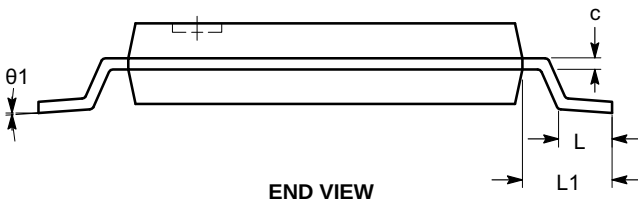



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 BSC | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| θ | 0° | | 8° |




SIDE VIEW




END VIEW

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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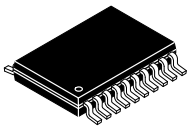
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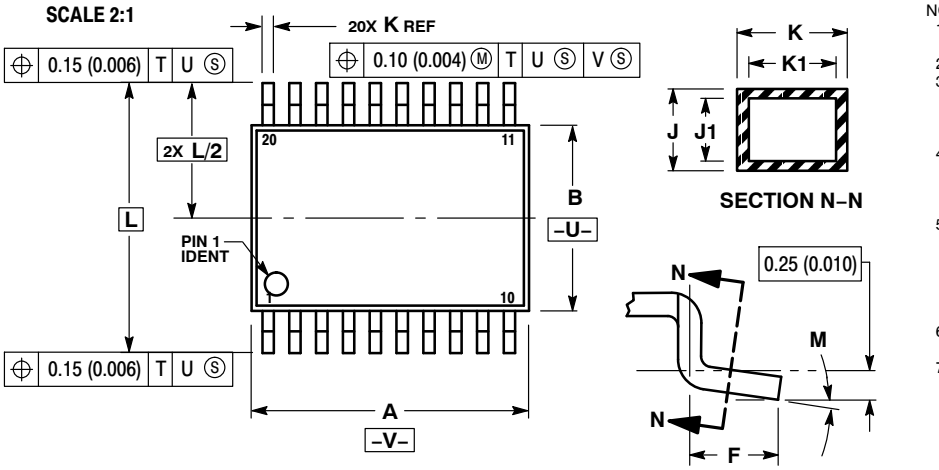
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**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016



SCALE 2:1



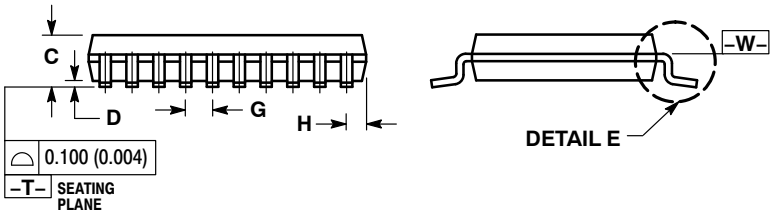




SECTION N−N




DETAIL E



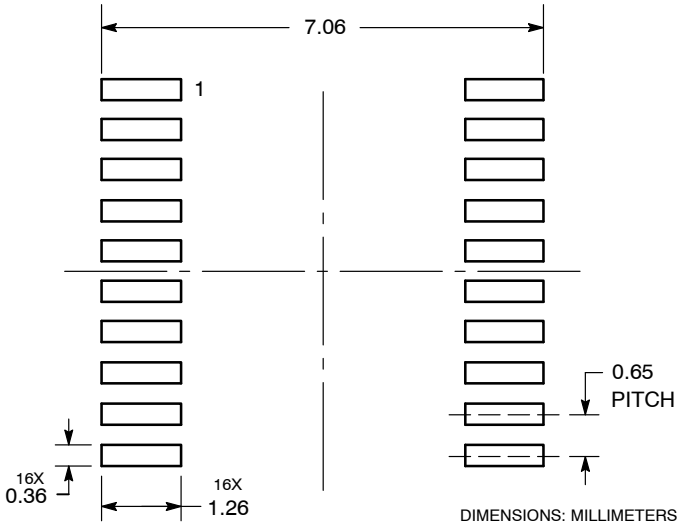




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

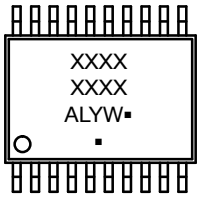
## RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSSOP−20 WB** | **PAGE 1 OF 1** |

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