CY7C1318CV18, CY7C1320CV18

18-Mbit DDR II SRAM 2-Word Burst Architecture

Features

- 18-Mbit density (1 M × 18, 512 K × 36)
- 267-MHz clock for high bandwidth
- 2-word burst for reducing address bus frequency
- Double data rate (DDR) interfaces (data transferred at 534 MHz) at 267 MHz
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Two input clocks for output data (C and $\overline{C}$) to minimize clock skew and flight time mismatches
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high speed systems
- Synchronous internally self-timed writes
- DDR II operates with 1.5 cycle read latency when delay lock loop (DLL) is enabled
- Operates similar to a DDR I device with one cycle read latency in DLL Off mode
- 1.8 V core power supply with high-speed transceiver logic (HSTL) inputs and outputs
- Variable drive HSTL output buffers
- Expanded HSTL output voltage (1.4 V – V_{DD})
- Available in 165-ball fine pitch ball grid array (FPBGA) package (13 × 15 × 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- DLL for accurate data placement

Configurations

CY7C1318CV18 – 1M × 18

CY7C1320CV18 – 512K × 36

Functional Description

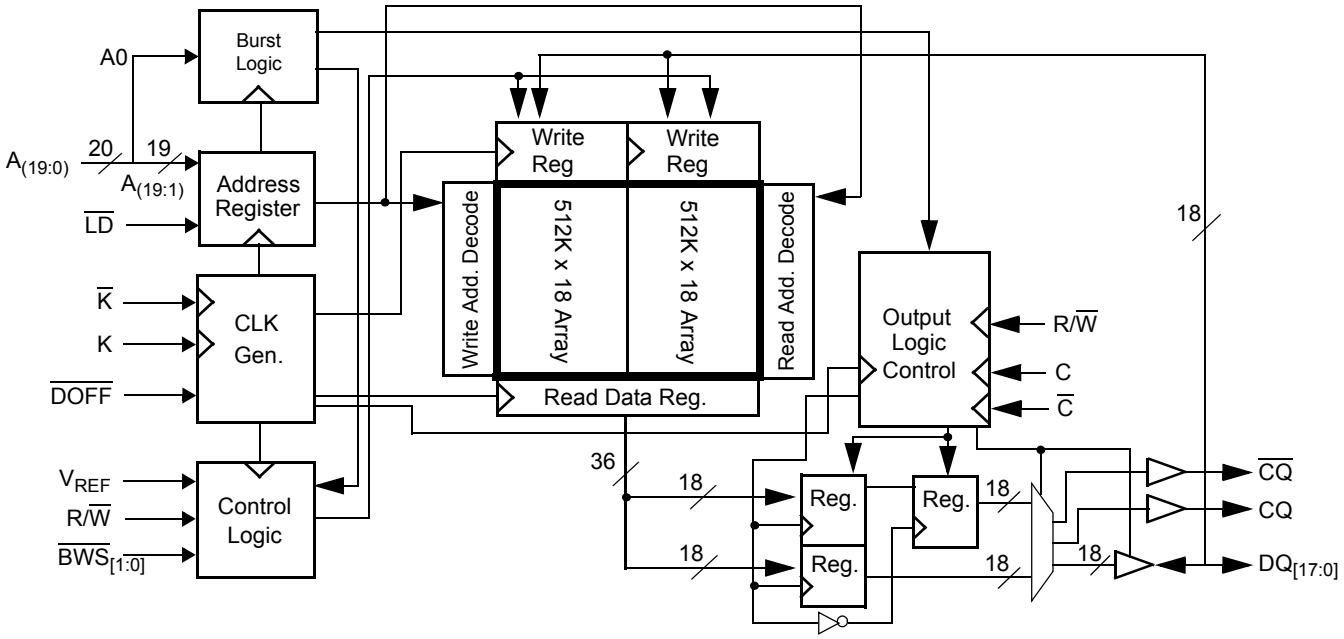
The CY7C1318CV18, and CY7C1320CV18 are 1.8 V synchronous pipelined SRAMs equipped with DDR II architecture. The DDR II consists of an SRAM core with advanced synchronous peripheral circuitry and a one-bit burst counter. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and $\overline{K}$. Read data is driven on the rising edges of C and $\overline{C}$ if provided, or on the rising edge of K and $\overline{K}$ if C/$\overline{C}$ are not provided. For CY7C1318CV18 and CY7C1320CV18, the burst counter takes in the least significant bit of the external address and bursts two 18-bit words (in the case of CY7C1318CV18) of two 36-bit words (in the case of CY7C1320CV18) sequentially into or out of the device.

Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs (Q, sharing the same physical pins as the data inputs, D) are tightly matched to the two output echo clocks CQ/$\overline{CQ}$, eliminating the need to capture data separately from each individual DDR SRAM in the system design. Output data clocks (C/$\overline{C}$) enable maximum system clocking and data synchronization flexibility.

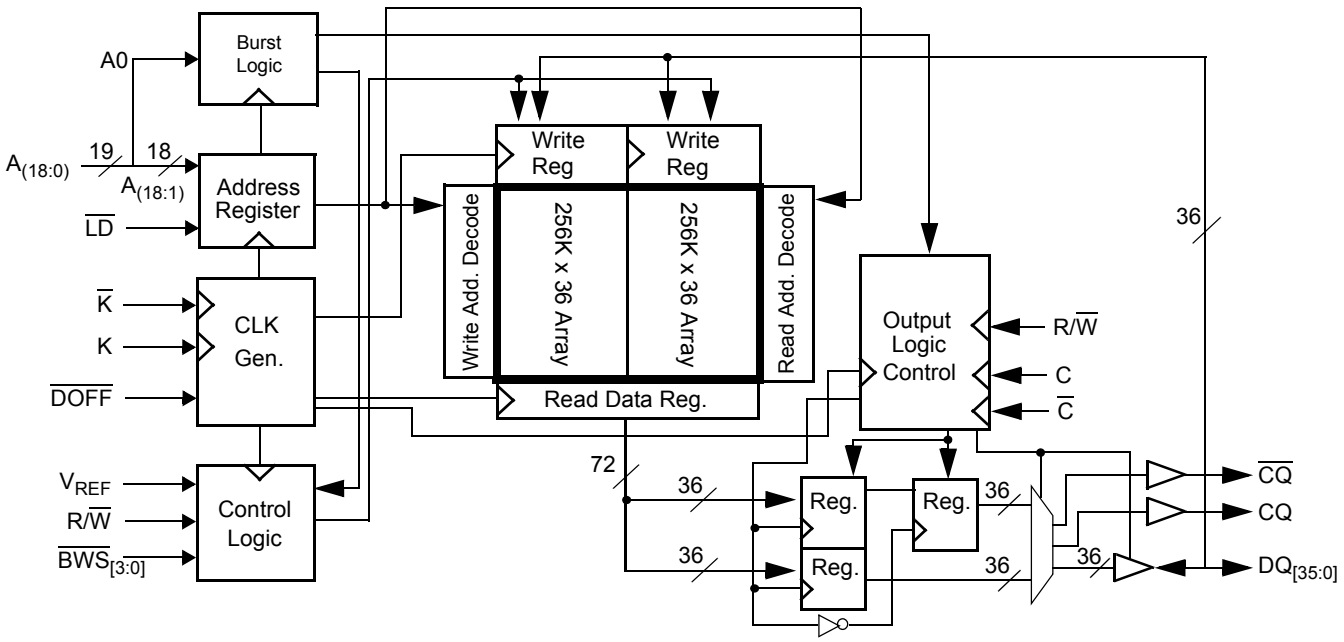
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ (or K or $\overline{K}$ in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

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Logic Block Diagram (CY7C1318CV18)



Logic Block Diagram (CY7C1320CV18)



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Contents

Selection Guide **4**
Pin Configuration **5**
165-ball FBGA (13 × 15 × 1.4 mm) Pinout 5
Pin Definitions **6**
Functional Overview **8**
Read Operations 8
Write Operations 8
Byte Write Operations 8
Single Clock Mode 8
DDR Operation 8
Depth Expansion 8
Programmable Impedance 9
Echo Clocks 9
DLL 9
Application Example **9**
Truth Table **10**
Burst Address Table **10**
Write Cycle Descriptions **10**
Write Cycle Descriptions **11**
IEEE 1149.1 Serial Boundary Scan (JTAG) **12**
Disabling the JTAG Feature 12
Test Access Port—Test Clock 12
Test Mode Select (TMS) 12
Test Data-In (TDI) 12
Test Data-Out (TDO) 12
Performing a TAP Reset 12
TAP Registers 12
TAP Instruction Set 12
TAP Controller State Diagram **14**
TAP Controller Block Diagram **15**
TAP Electrical Characteristics **15**
TAP AC Switching Characteristics **16**
TAP Timing and Test Conditions **16**
Identification Register Definitions **17**
Scan Register Sizes **17**
Instruction Codes **17**
Boundary Scan Order **18**
Power Up Sequence in DDR II SRAM **19**
Power Up Sequence 19
DLL Constraints 19
Maximum Ratings **20**
Operating Range **20**
Neutron Soft Error Immunity **20**
Electrical Characteristics **20**
DC Electrical Characteristics 20
AC Electrical Characteristics 21
Capacitance **21**
Thermal Resistance **21**
Switching Characteristics **22**
Switching Waveforms **24**
Ordering Information **25**
Ordering Code Definitions 25
Package Diagram **26**
Acronyms **27**
Document Conventions **27**
Units of Measure 27
Document History Page **28**
Sales, Solutions, and Legal Information **29**
Worldwide Sales and Design Support 29
Products 29
PSoC Solutions 29

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Selection Guide

Description		267 MHz	250 MHz	200 MHz	167 MHz	Unit
Maximum operating frequency		267	250	200	167	MHz
Maximum operating current	×18	805	730	600	510	mA
	×36	855	775	635	540	

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Pin Configuration

The pin configuration for CY7C1318CV18 and CY7C1320CV18 follow.[1]

165-ball FBGA (13 × 15 × 1.4 mm) Pinout

CY7C1318CV18 (1M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	NC/36M	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	A0	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

CY7C1320CV18 (512K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	NC/36M	R/$\overline{W}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{LD}$	A	NC/72M	CQ
B	NC	DQ27	DQ18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	A	A0	A	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	A	A	A	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	A	A	C	A	A	NC	DQ9	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Note
1. NC/36M, NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.

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Pin Definitions

Pin Name	I/O	Pin Description
$DQ_{[x:0]}$	Input Output-Synchronous	**Data Input Output Signals**. Inputs are sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during read operations or K and $\overline{K}$ when in single clock mode. When read access is deselected, $Q_{[x:0]}$ are automatically tristated. CY7C1318CV18 – $DQ_{[17:0]}$ CY7C1320CV18 – $DQ_{[35:0]}$
$\overline{LD}$	Input-Synchronous	**Synchronous Load**. This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	**Byte Write Select (BWS) 0, 1, 2, and 3** – **Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the Write operations. Bytes not written remain unaltered. CY7C1318CV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$. CY7C1320CV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the BWS pins are sampled on the same edge as the data. Deselecting a BWS ignores the corresponding byte of data and it is not written into the device.
A, A0	Input-Synchronous	**Address Inputs**. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 1M x 18 (2 arrays each of 512K x 18) for CY7C1318CV18, and 512K x 36 (2 arrays each of 256K x 36) for CY7C1320CV18. CY7C1318CV18 – A0 is the input to the burst counter. These are incremented internally in a linear fashion. 20 address inputs are needed to access the entire memory array. CY7C1320CV18 – A0 is the input to the burst counter. These are incremented internally in a linear fashion. 19 address inputs are needed to access the entire memory array. All the address inputs are ignored when the appropriate port is deselected.
R/$\overline{W}$	Input-Synchronous	**Synchronous Read/Write Input**. When $\overline{LD}$ is LOW, this input designates the access type (read when R/$\overline{W}$ is HIGH, write when R/$\overline{W}$ is LOW) for the loaded address. R/$\overline{W}$ must meet the setup and hold times around the edge of K.
C	Input Clock	**Positive Input Clock for Output Data.** C is used in conjunction with $\overline{C}$ to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See "Application Example" on page 9 for more information.
$\overline{C}$	Input Clock	**Negative Input Clock for Output Data**. $\overline{C}$ is used in conjunction with C to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See "Application Example" on page 9 for more information.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous data being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Output Clock	**CQ Referenced with Respect to C**. This is a free running clock and is synchronized to the input clock for output data (C) of the DDR II. In single clock mode, CQ is generated with respect to K. The timing for the echo clocks is shown in "Switching Characteristics" on page 22.
$\overline{CQ}$	Output Clock	**$\overline{CQ}$ Referenced with Respect to $\overline{C}$**. This is a free running clock and is synchronized to the input clock for output data ($\overline{C}$) of the DDR II. In single clock mode, $\overline{CQ}$ is generated with respect to $\overline{K}$. The timing for the echo clocks is shown in "Switching Characteristics" on page 22.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

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Pin Definitions (continued)

Pin Name	I/O	Pin Description
$\overline{DOFF}$	Input	**DLL Turn Off** – **Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timing in the DLL turned off operation is different from that listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in DDR I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR I timing.
TDO	Output	**Test Data Out (TDO) for JTAG**.
TCK	Input	**Test Clock (TCK) Pin for JTAG**.
TDI	Input	**Test Data In (TDI) Pin for JTAG**.
TMS	Input	**Test Mode Select (TMS) Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/36M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/72M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

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Functional Overview

The CY7C1318CV18, and CY7C1320CV18 are synchronous pipelined Burst SRAMs equipped with a DDR interface, which operates with a read latency of one and half cycles when DOFF pin is tied HIGH. When DOFF pin is set LOW or connected to V_{SS} the device behaves in DDR I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and K) and all output timing is referenced to the rising edge of the output clocks (C/C, or K/K when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the rising edge of the input clocks (K and K). All synchronous data outputs ($Q_{[x:0]}$) pass through output registers controlled by the rising edge of the output clocks (C/C, or K/K when in single-clock mode).

All synchronous control (R/W, LD, $BWS_{[0:X]}$) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1318CV18 is described in the following sections. The same basic descriptions apply to CY7C1320CV18.

Read Operations

The CY7C1318CV18 is organized internally as two arrays of 512K x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting R/W HIGH and LD LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the read address register and the least significant bit of the address is presented to the burst counter. The burst counter increments the address in a linear fashion. Following the next K clock rise, the corresponding 18-bit word of data from this address location is driven onto $Q_{[17:0]}$, using C as the output timing reference. On the subsequent rising edge of C the next 18-bit data word from the address location generated by the burst counter is driven onto $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the output clock (C or C, or K and K when in single clock mode, 200 MHz and 250 MHz device). To maintain the internal logic, each read access must be allowed to complete. Read accesses can be initiated on every rising edge of the positive input clock (K).

The CY7C1318CV18 first completes the pending read transactions, when read access is deselected. Synchronous internal circuitry automatically tristates the output following the next rising edge of the positive output clock (C). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting R/W LOW and LD LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register and the least significant bit of the address is presented to the burst counter. The burst counter increments the address in a linear fashion. On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the 18-bit write data register, provided $BWS_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock (K) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $BWS_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses can be initiated on every rising edge of the positive input clock (K). This pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and K).

When Write access is deselected, the device ignores all inputs after the pending write operations are completed.

Byte Write Operations

Byte write operations are supported by the CY7C1318CV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by BWS_0 and BWS_1, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read/modify/write operations to a byte write operation.

Single Clock Mode

The CY7C1318CV18 can be used with a single clock that controls both the input and output registers. In this mode the device recognizes only a single pair of input clocks (K and K) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/K and C/C clocks. All timing parameters remain the same in this mode. To use this mode of operation, tie C and C HIGH at power on. This function is a strap option and not alterable during device operation.

DDR Operation

The CY7C1318CV18 enables high-performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. The CY7C1318CV18 requires a single No Operation (NOP) cycle when transitioning from a read to a write cycle. At higher frequencies, some applications may require a second NOP cycle to avoid contention.

If a read occurs after a write cycle, address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the read(s), the stored data from the earlier write is written into the SRAM array. This is called a posted write.

If a read is performed on the same address on which a write is performed in the previous cycle, the SRAM reads out the most current data. The SRAM does this by bypassing the memory array and reading the data from the registers.

Depth Expansion

Depth expansion requires replicating the LD control signal for each bank. All other control signals can be common between banks as appropriate.

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Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5 V. The output impedance is adjusted every 1024 cycles at power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the DDR II to simplify data capture on high speed systems. Two echo clocks are generated by the DDR II. CQ is referenced with respect to C and $\overline{CQ}$ is referenced with respect to $\overline{C}$. These are free running clocks and are synchronized to the output clock of the DDR II. In the single clock mode, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$. The timing for the echo clocks is shown in "Switching Characteristics" on page 22.

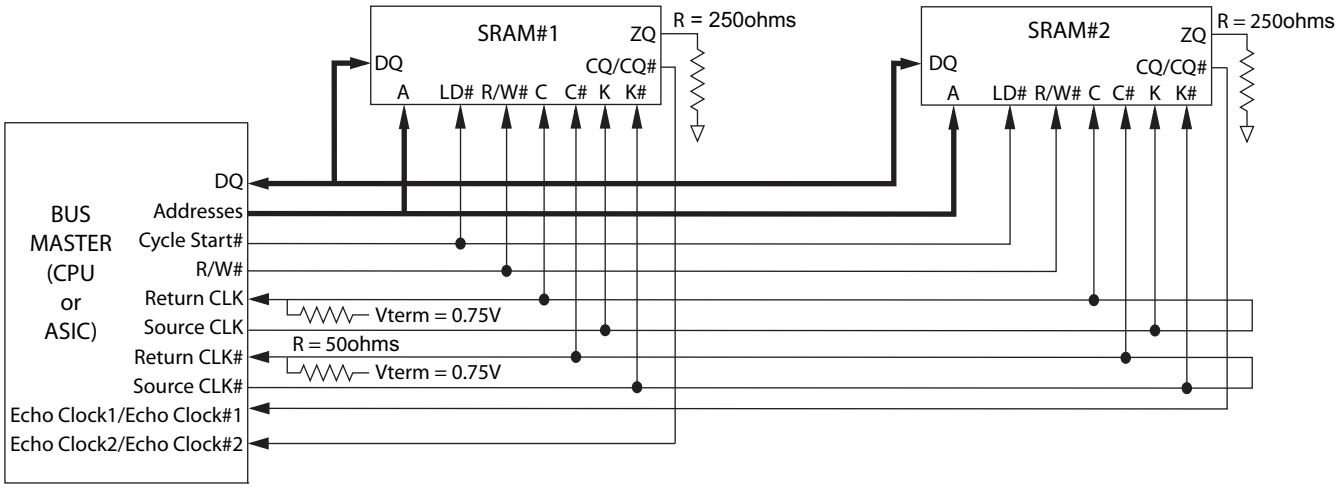
DLL

These chips use a delay lock loop (DLL) that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the $\overline{DOFF}$ is tied HIGH, the DLL is locked after 1024 cycles of stable clock. The DLL can also be reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the DLL to lock it to the desired frequency. The DLL automatically locks 1024 clock cycles after a stable clock is presented. The DLL may be disabled by applying ground to the $\overline{DOFF}$ pin. When the DLL is turned off, the device behaves in DDR I mode (with one cycle latency and a longer access time). For information refer to the application note *DLL Considerations in QDRII™/DDRII*.

Application Example

Figure 1 shows two DDR II used in an application.

Figure 1. Application Example



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Truth Table

The truth table for the CY7C1318CV18, and CY7C1320CV18 follows.[2, 3, 4, 5, 6, 7]

Operation	K	$\overline{LD}$	R/$\overline{W}$	DQ	DQ
Write cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{K}$ rising edges.	L–H	L	L	D(A1) at K(t + 1) ↑	D(A2) at $\overline{K}$(t + 1) ↑
Read cycle: Load address; wait one and a half cycle; read data on consecutive $\overline{C}$ and C rising edges.	L–H	L	H	Q(A1) at $\overline{C}$(t + 1)↑	Q(A2) at C(t + 2) ↑
NOP: No operation	L–H	H	X	High Z	High Z
Standby: Clock stopped	Stopped	X	X	Previous State	Previous State

Burst Address Table

(CY7C1318CV18, CY7C1320CV18)

First Address (External)	Second Address (Internal)
X..X0	X..X1
X..X1	X..X0

Write Cycle Descriptions

The write cycle description table for CY7C1318CV18 follows. [2, 8]

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence : Both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L–H	During the data portion of a write sequence : Both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence : Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence : Only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence : Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence : Only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes
2. X = “Don’t Care,” H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device powers up deselected with the outputs in a tristate condition.
4. On CY7C1318CV18 and CY7C1320CV18, “A1” represents address location latched by the devices when transaction was initiated and “A2” represents the addresses sequence in the burst.
5. “t” represents the cycle at which a read/write operation is started. t + 1 and t + 2 are the first and second clock cycles succeeding the “t” clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
7. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

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Write Cycle Descriptions

The write cycle description table for CY7C1320CV18 follows.[9, 10]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

Notes

9. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
10. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

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IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8 V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the "TAP Controller State Diagram" on page 14. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see "Instruction Codes" on page 17). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in "TAP Controller Block Diagram" on page 15. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The "Boundary Scan Order" on page 18 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in "Identification Register Definitions" on page 17.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in "Instruction Codes" on page 17. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

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IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRISTATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

The boundary scan register has a special bit located at bit #47. When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

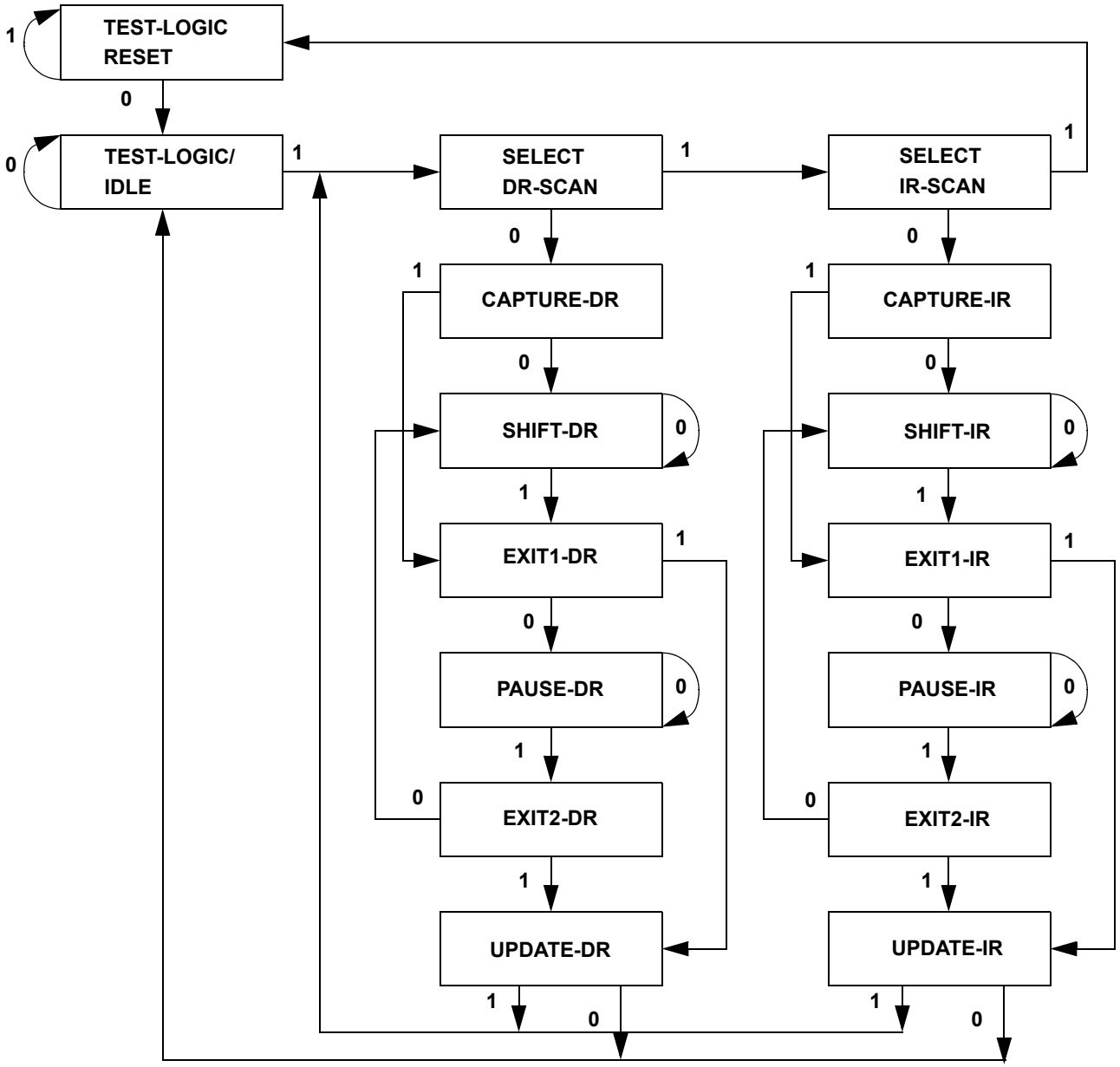
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

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TAP Controller State Diagram

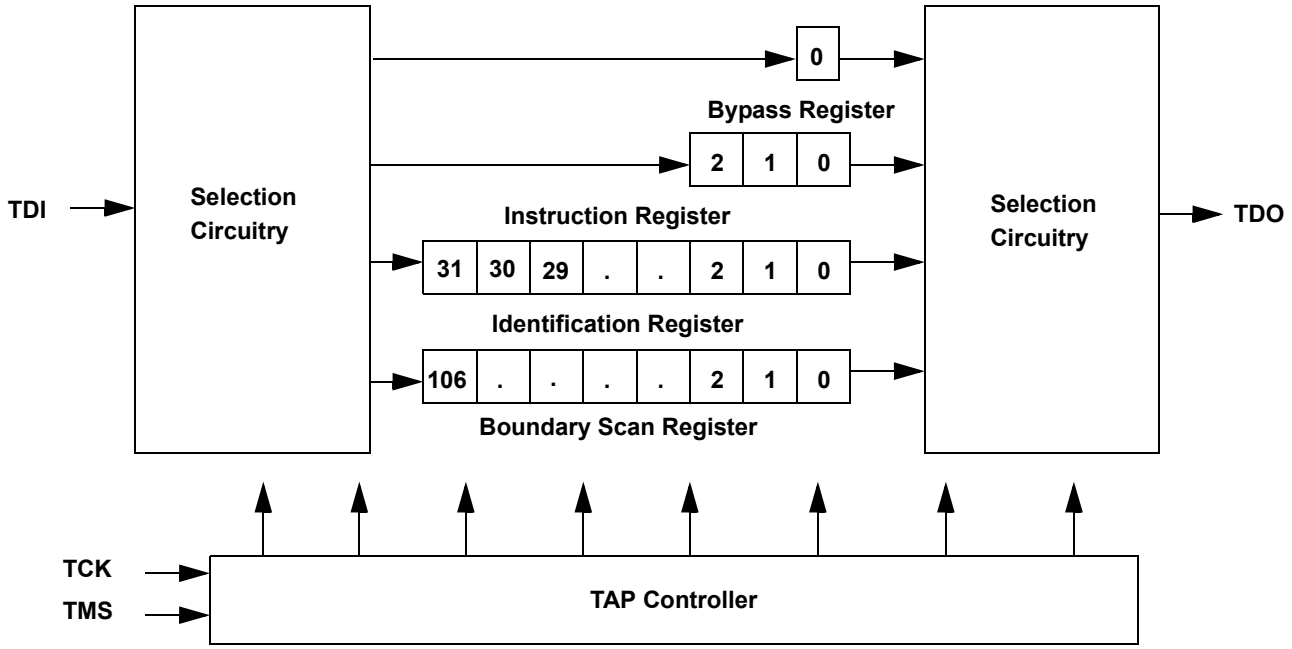
The state diagram for the TAP controller follows.[11]



Note
11. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

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TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range[12, 13, 14]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –2.0 mA	1.4	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	1.6	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2.0 mA	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	–	0.2	V
V_{IH}	Input HIGH voltage		0.65 V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		–0.3	0.35 V_{DD}	V
I_X	Input and output load current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
12. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
13. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -1.5$ V (Pulse width less than $t_{CYC}/2$).
14. All Voltage referenced to Ground.

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TAP AC Switching Characteristics

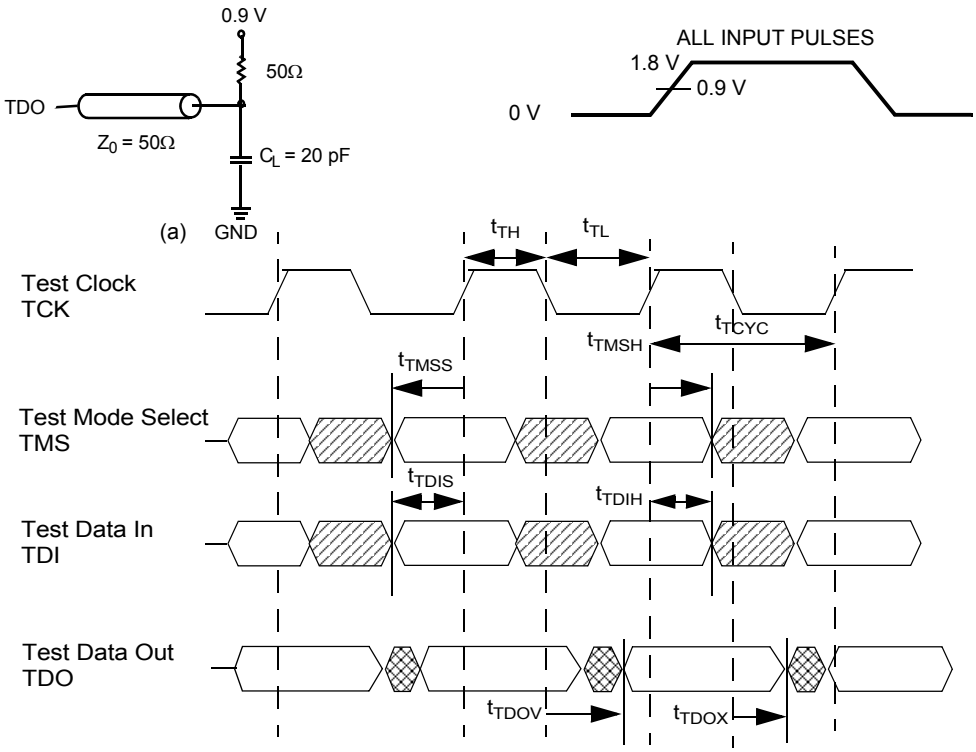
Over the Operating Range[15, 16]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH	20	–	ns
t_{TL}	TCK clock LOW	20	–	ns
Setup Times				
t_{TMSS}	TMS setup to TCK clock rise	5	–	ns
t_{TDIS}	TDI setup to TCK clock rise	5	–	ns
t_{CS}	Capture setup to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns

TAP Timing and Test Conditions

Figure 2 shows the TAP timing and test conditions.[16]

Figure 2. TAP Timing and Test Conditions



Notes

15. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
16. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

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Identification Register Definitions

Instruction Field	Value		Description
	CY7C1318CV18	CY7C1320CV18	
Revision number (31:29)	000	000	Version number.
Cypress device ID (28:12)	11010100010010101	11010100010100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID register presence (0)	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

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Boundary Scan Order

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
0	6R	28	10G	56	6A	84	2J
1	6P	29	9G	57	5B	85	3K
2	6N	30	11F	58	5A	86	3J
3	7P	31	11G	59	4A	87	2K
4	7N	32	9F	60	5C	88	1K
5	7R	33	10F	61	4B	89	2L
6	8R	34	11E	62	3A	90	3L
7	8P	35	10E	63	1H	91	1M
8	9R	36	10D	64	1A	92	1L
9	11P	37	9E	65	2B	93	3N
10	10P	38	10C	66	3B	94	3M
11	10N	39	11D	67	1C	95	1N
12	9P	40	9C	68	1B	96	2M
13	10M	41	9D	69	3D	97	3P
14	11N	42	11B	70	3C	98	2N
15	9M	43	11C	71	1D	99	2P
16	9N	44	9B	72	2C	100	1P
17	11L	45	10B	73	3E	101	3R
18	11M	46	11A	74	2D	102	4R
19	9L	47	Internal	75	2E	103	4P
20	10L	48	9A	76	1E	104	5P
21	11K	49	8B	77	2F	105	5N
22	10K	50	7C	78	3F	106	5R
23	9J	51	6C	79	1G		
24	9K	52	8A	80	1F		
25	10J	53	7A	81	3G		
26	11J	54	7B	82	2G		
27	11H	55	6B	83	1J		

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Power Up Sequence in DDR II SRAM

DDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

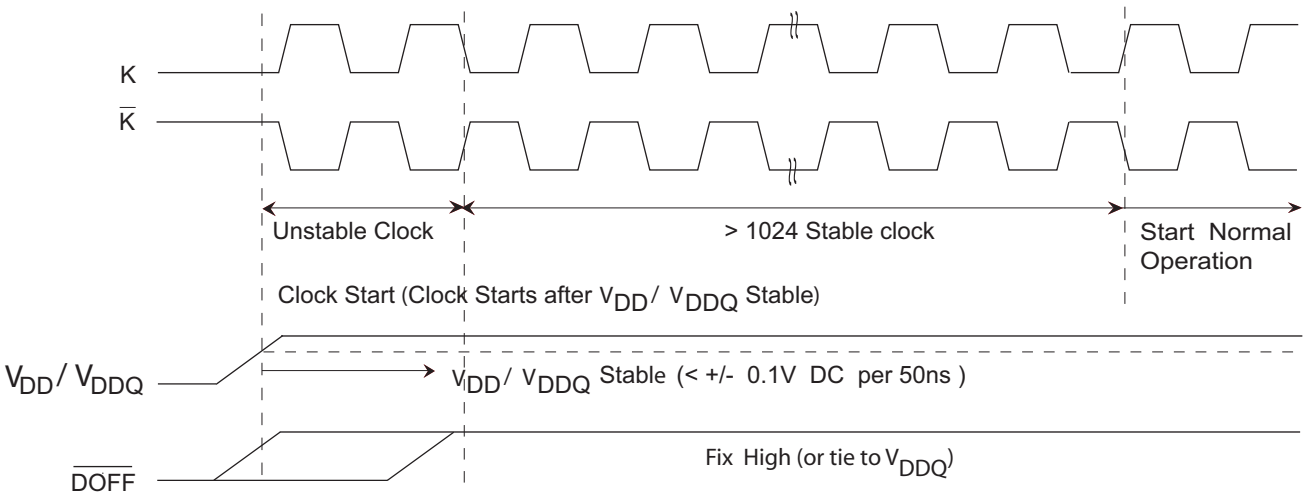
Power Up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (all other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power, and clock (K, $\overline{K}$) for 1024 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide1024 cycles stable clock to relock to the desired clock frequency.

Figure 3. Power Up Waveforms



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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .....–0.5 V to +2.9 V

Supply voltage on V_{DDQ} relative to GND..... –0.5 V to +V_{DD}

DC applied to outputs in high Z .....–0.5 V to V_{DDQ} + 0.3 V

DC input voltage[17] .....–0.5 V to V_{DD} + 0.3 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, M 3015)... > 2001 V

Latch up current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}[18]	V_{DDQ}[18]
Commercial	0 °C to +70 °C	1.8 ± 0.1 V	1.4 V to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single-bit upsets	25 °C	320	368	FIT/Mb
LMBU	Logical multi-bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/Dev

** No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

DC Electrical Characteristics

Over the Operating Range[19]

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
V_{DD}	Power supply voltage				1.7	1.8	1.9	V
V_{DDQ}	I/O supply voltage				1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH voltage	Note 20			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW voltage	Note 21			$V_{DDQ}/2 – 0.12$	–	$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH voltage	I_{OH} = –0.1 mA, nominal impedance			$V_{DDQ} – 0.2$	–	V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW voltage	I_{OL} = 0.1 mA, nominal impedance			V_{SS}	–	0.2	V
V_{IH}	Input HIGH voltage				$V_{REF} + 0.1$	–	$V_{DDQ} + 0.3$	V
V_{IL}	Input LOW voltage				–0.3	–	$V_{REF} – 0.1$	V
I_X	Input leakage current	GND ≤ V_I ≤ V_{DDQ}			–5	–	5	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled			–5	–	5	µA
V_{REF}	Input reference voltage[22]	Typical Value = 0.75 V			0.68	0.75	0.95	V
I_{DD}[23]	V_{DD} operating supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	267 MHz	(×18)	–	–	805	mA
				(×36)	–	–	855	
			250 MHz	(×18)	–	–	730	
				(×36)	–	–	775	
			200 MHz	(×18)	–	–	600	
				(×36)	–	–	635	
			167 MHz	(×18)	–	–	510	
				(×36)	–	–	540	

Notes

17. Overshoot: $V_{IH}(AC) < V_{DDQ} + 0.85$ V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > –1.5$ V (Pulse width less than $t_{CYC}/2$).
18. Power up: assumes a linear ramp from 0 V to $V_{DD}(min)$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.
19. All Voltage referenced to Ground.
20. Outputs are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
21. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
22. $V_{REF}(min)$ = 0.68 V or 0.46 V_{DDQ}, whichever is larger, $V_{REF}(max)$ = 0.95 V or 0.54 V_{DDQ}, whichever is smaller.
23. The operation current is calculated with 50% read cycle and 50% write cycle.

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Electrical Characteristics (continued)

DC Electrical Characteristics

Over the Operating Range[19]

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
I_{SB1}	Automatic power down current	Max V_{DD}, Both Ports Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ f = f_{MAX} = $1/t_{CYC}$, Inputs Static	267 MHz	(×18)	–	–	315	mA
				(×36)	–	–	330	
			250 MHz	(×18)	–	–	300	
				(×36)	–	–	320	
			200 MHz	(×18)	–	–	290	
				(×36)	–	–	300	
			167 MHz	(×18)	–	–	285	
				(×36)	–	–	295	

AC Electrical Characteristics

Over the Operating Range[24]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH voltage		V_{REF} + 0.2	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{REF} – 0.2	V

Capacitance

Tested initially and after any design or process change that may affect these parameters.

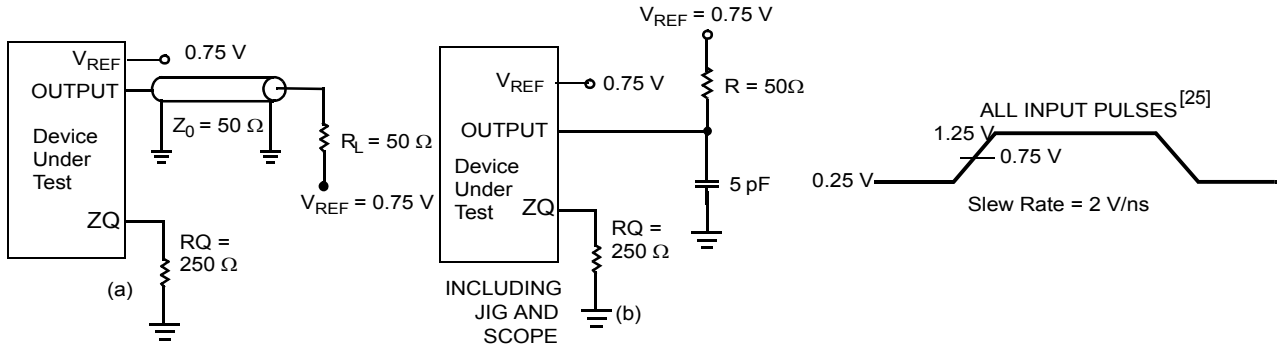
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 1.8 V, V_{DDQ} = 1.5 V	5	pF
C_{CLK}	Clock input capacitance		6	pF
C_O	Output capacitance		7	pF

Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	18.7	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		4.5	°C/W

Figure 4. AC Test Loads and Waveforms



Note

24. Overshoot: $V_{IH}(AC) < V_{DDQ}$ + 0.85 V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -1.5$ V (Pulse width less than $t_{CYC}/2$).
25. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, V_{REF} = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

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Switching Characteristics

Over the Operating Range[26, 27]

Cypress Parameter	Consortium Parameter	Description	267 MHz		250 MHz		200 MHz		167 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the first access [28]	1	–	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K clock and C clock cycle time	3.75	8.4	4.0	8.4	5.0	8.4	6.0	8.4	ns
t_{KH}	t_{KHKL}	Input clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	1.5	–	1.6	–	2.0	–	2.4	–	ns
t_{KL}	t_{KLKH}	Input clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	1.5	–	1.6	–	2.0	–	2.4	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K clock Rise to $\overline{K}$ clock rise and C to $\overline{C}$ rise (rising edge to rising edge)	1.68	–	1.8	–	2.2	–	2.7	–	ns
t_{KHCH}	t_{KHCH}	K/$\overline{K}$ clock rise to C/$\overline{C}$ clock rise (rising edge to rising edge)	0.00	1.68	0.00	1.8	0.00	2.2	0.00	2.7	ns
Setup Times											
t_{SA}	t_{AVKH}	Address setup to K clock rise	0.3	–	0.5	–	0.6	–	0.7	–	ns
t_{SC}	t_{IVKH}	Control setup to K clock rise ($\overline{LD}$, R/$\overline{W}$)	0.3	–	0.5	–	0.6	–	0.7	–	ns
t_{SCDDR}	t_{IVKH}	Double data rate control setup to clock (K/$\overline{K}$) rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.3	–	0.35	–	0.4	–	0.5	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ setup to clock (K and $\overline{K}$) rise	0.3	–	0.35	–	0.4	–	0.5	–	ns
Hold Times											
t_{HA}	t_{KHAX}	Address hold after K clock rise	0.3	–	0.5	–	0.6	–	0.7	–	ns
t_{HC}	t_{KHIX}	Control hold after K clock rise ($\overline{LD}$, R/$\overline{W}$)	0.3	–	0.5	–	0.6	–	0.7	–	ns
t_{HCDDR}	t_{KHIX}	Double data rate control hold after clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.3	–	0.35	–	0.4	–	0.5	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ hold after clock (K/$\overline{K}$) rise	0.3	–	0.35	–	0.4	–	0.5	–	ns

Notes

26. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75 V, V_{REF} = 0.75 V, RQ = 250 Ω, V_{DDQ} = 1.5 V, input pulse levels of 0.25 V to 1.25 V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.
27. When a part with a maximum frequency above 167 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
28. This part has an internal voltage regulator; t_{POWER} is the time that the power is supplied above V_{DD} minimum initially before a read or write operation can be initiated.

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Switching Characteristics (continued)

Over the Operating Range[26, 27]

Cypress Parameter	Consortium Parameter	Description	267 MHz		250 MHz		200 MHz		167 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Output Times											
t_{CO}	t_{CHQV}	C/$\overline{C}$ clock rise (or K/$\overline{K}$ in single clock mode) to data valid	–	0.45	–	0.45	–	0.45	–	0.50	ns
t_{DOH}	t_{CHQX}	Data output hold after output C/$\overline{C}$ clock rise (active to active)	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
t_{CCQO}	t_{CHCQV}	C/$\overline{C}$ clock rise to echo clock valid	–	0.45	–	0.45	–	0.45	–	0.50	ns
t_{CQOH}	t_{CHCQX}	Echo clock hold after C/$\overline{C}$ clock rise	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
t_{CQD}	t_{CQHQV}	Echo clock high to data valid	–	0.27	–	0.30	–	0.35	–	0.40	ns
t_{CQDOH}	t_{CQHQX}	Echo clock high to data invalid	–0.27	–	–0.30	–	–0.35	–	–0.40	–	ns
t_{CQH}	t_{CQHCQL}	Output clock (CQ/$\overline{CQ}$) HIGH[29]	1.43	–	1.55	–	1.95	–	2.45	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ clock rise to $\overline{CQ}$ clock rise (rising edge to rising edge)[29]	1.43	–	1.55	–	1.95	–	2.45	–	ns
t_{CHZ}	t_{CHQZ}	Clock (C/$\overline{C}$) rise to high Z (Active to high Z)[30, 31]	–	0.45	–	0.45	–	0.45	–	0.50	ns
t_{CLZ}	t_{CHQX1}	Clock (C/$\overline{C}$) rise to low Z[30, 31]	–0.45	–	–0.45	–	–0.45	–	–0.50	–	ns
DLL Timing											
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock phase jitter	–	0.20	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL lock time (K, C)	1024	–	1024	–	1024	–	1024	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K static to DLL reset	30	–	30	–	30	–	30	–	ns

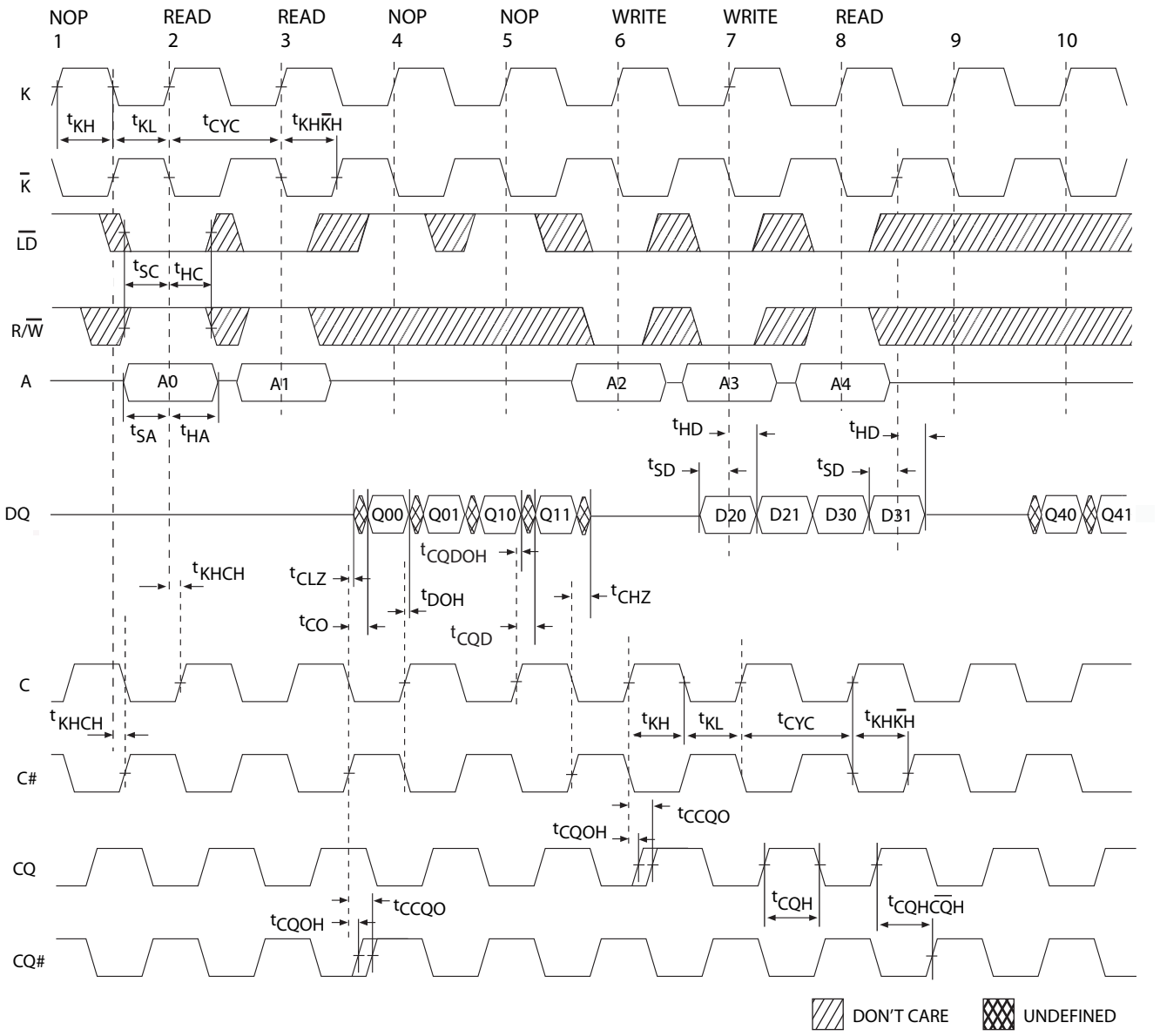
Notes

29. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
30. t_{CHZ}, t_{CLZ} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±100 mV from steady-state voltage.
31. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.

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Switching Waveforms

Figure 5. Read/Write/Deselect Sequence[32, 33, 34]



Notes
32. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
33. Outputs are disabled (high Z) one clock cycle after a NOP.
34. In this example, if address A4 = A3, then data Q40 = D30 and Q41 = D31. Write data is forwarded immediately as read results. This note applies to the whole diagram.

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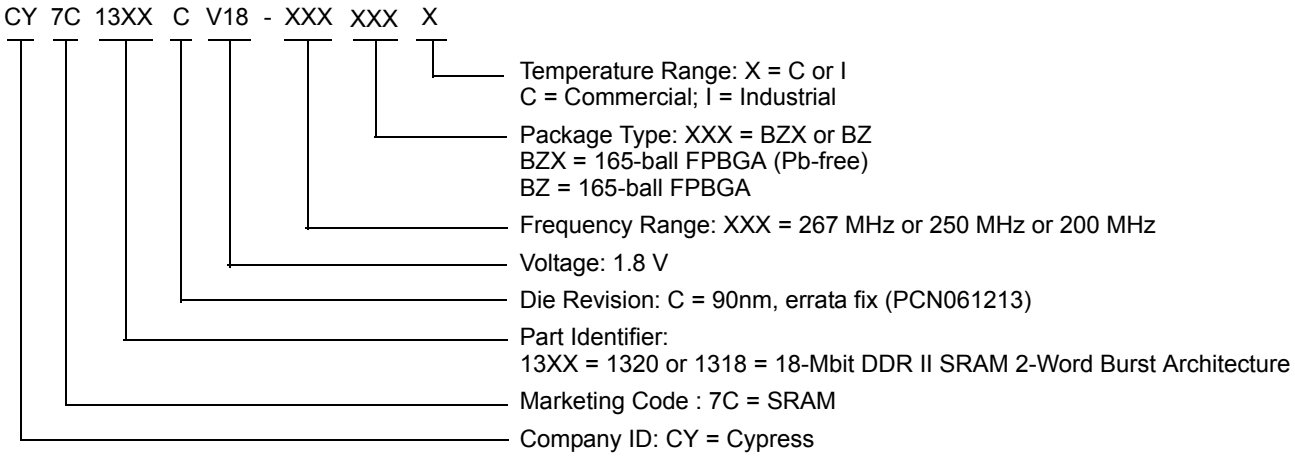
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Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.
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Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
267	CY7C1320CV18-267BZXC	51-85180	165-ball FPBGA (13 × 15 × 1.4 mm) Pb-free	Commercial
250	CY7C1318CV18-250BZXC	51-85180	165-ball FPBGA (13 × 15 × 1.4 mm) Pb-free	Commercial
	CY7C1320CV18-250BZXC			
	CY7C1318CV18-250BZI	51-85180	165-ball FPBGA (13 × 15 × 1.4 mm)	Industrial
200	CY7C1318CV18-200BZXC	51-85180	165-ball FPBGA (13 × 15 × 1.4 mm) Pb-free	Commercial
	CY7C1318CV18-200BZI	51-85180	165-ball FPBGA (13 × 15 × 1.4 mm)	Industrial

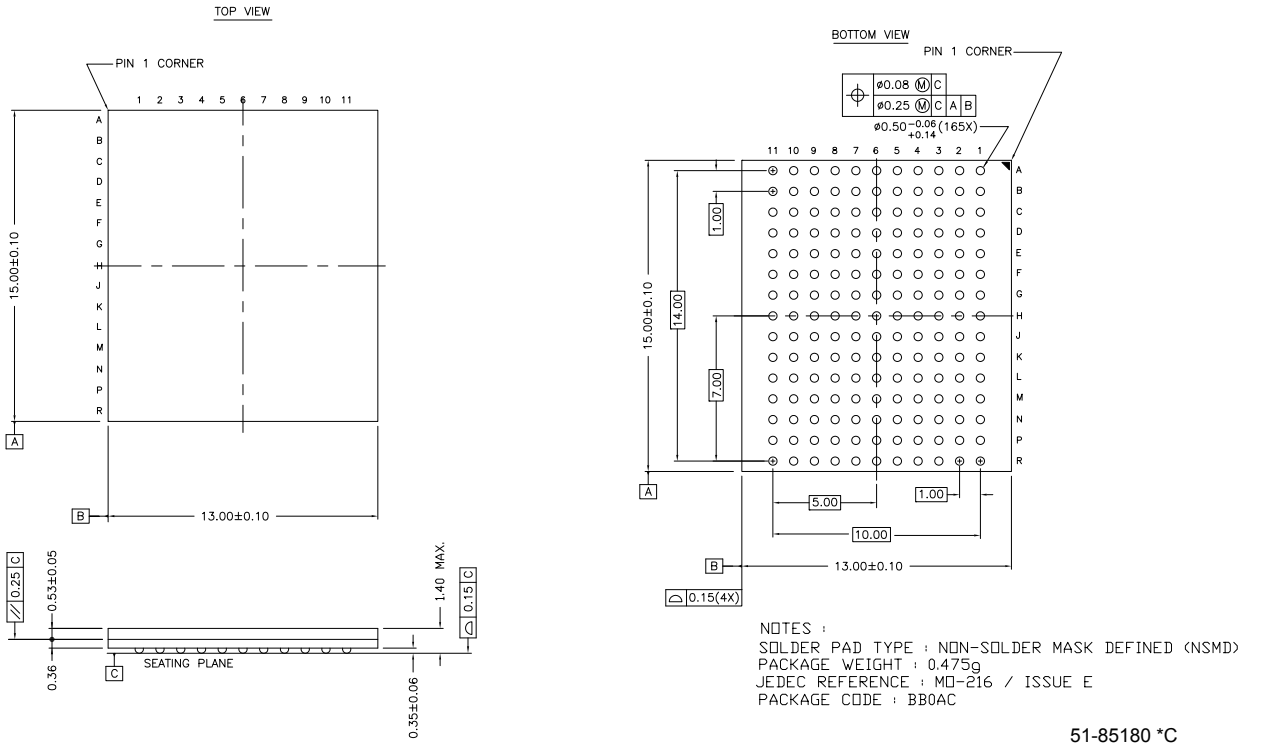
Ordering Code Definitions



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Package Diagram

Figure 6. 165-ball FBGA (13 × 15 × 1.4 mm), 51-85180



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Acronyms

Acronym	Description
DDR	double data rate
DLL	delay lock loop
FPBGA	fine-pitch ball grid array
HSTL	high-speed transceiver logic
JEDEC	Joint Electron Device Engineering Council
JTAG	joint test action group
SRAM	static random access memory
SEL	single event latch up
TDO	test data out
TCK	test clock
TDI	test data in
TMS	test mode select
TAP	test access port

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
kΩ	kilo ohms
Ω	ohms
°C	degree Celcius

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Document History Page

Document Title: CY7C1318CV18/CY7C1320CV18, 18-Mbit DDR II SRAM 2-Word Burst Architecture Document Number: 001-07160				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	433284	See ECN	NXR	New data sheet
*A	462615	See ECN	NXR	Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power-Up waveform
*B	503690	See ECN	VKN	Minor change: Moved data sheet to web
*C	1523383	See ECN	VKN/AESA	Converted from preliminary to final Updated Logic Block diagram Removed 300 MHz and 278 MHz speed bins Added 267 MHz speed bin Updated I_{DD}/I_{SB} specs Changed DLL minimum operating frequency from 80MHz to 120MHz Changed t_{CYC} max spec to 8.4ns Modified footnotes 20 and 28
*D	2507747	See ECN	VKN/PYRS	Changed Ambient Temperature with Power Applied from “–10 C to +85 C” to “–55 C to +125 C” in the “Maximum Ratings“ on page 20 Updated power up sequence waveform and its description Added footnote #19 related to I_{DD} Changed Θ_{JA} spec from 28.51 to 18.7; Changed Θ_{JC} spec from 5.91 to 4.5
*E	2518624	See ECN	NXR/PYRS	Changed JTAG ID (31:29) from 001 to 000
*F	2755838	08/25/2009	VKN/AESA	Removed x8 and x9 part number details Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.
*G	2896382	04/09/2010	NJY	Removed obsolete part numbers from Ordering Information. Updated package diagram, Sales, Solutions, and Legal Information section, and data sheet template. Removed pruned part CY7C1320CV18-200BZC.
*H	2957481	06/21/2010	VKN	Included “CY7C1318CV18-250BZI” in Ordering Information Added Ordering Code Definitions
*I	3096143	11/27/2010	NJY	Added Units of Measure. Minor edits.
*J	3160521	02/02/2011	NJY	Updated Ordering Information.

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